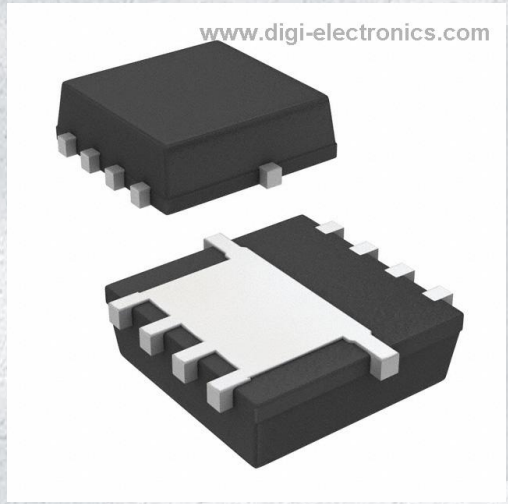
SQ7415AENW-T1_GE3 Datasheet



DiGi Electronics Part Number	SQ7415AENW-T1_GE3-DG
Manufacturer	Vishay Siliconix
Manufacturer Product Number	SQ7415AENW-T1_GE3
Description	MOSFET P-CH 60V 16A PPAK1212-8
Detailed Description	P-Channel 60 V 16A (Tc) 53W (Tc) Surface Mount PowerPAK® 1212-8

https://www.DiGi-Electronics.com

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
SQ7415AENW-T1_GE3	Vishay Siliconix
Series:	Product Status:
-	Obsolete
FET Type:	Technology:
P-Channel	MOSFET (Metal Oxide)
Drain to Source Voltage (Vdss):	Current - Continuous Drain (Id) @ 25°C:
60 V	16A (Tc)
Drive Voltage (Max Rds On, Min Rds On):	Rds On (Max) @ Id, Vgs:
4.5V, 10V	65mOhm @ 5.7A, 10V
Vgs(th) (Max) @ Id:	Gate Charge (Qg) (Max) @ Vgs:
2.5V @ 250µA	38 nC @ 10 V
Vgs (Max):	Input Capacitance (Ciss) (Max) @ Vds:
±20V	1385 pF @ 25 V
FET Feature:	Power Dissipation (Max):
-	53W (Tc)
Operating Temperature:	Mounting Type:
-55°C ~ 175°C (TJ)	Surface Mount
Supplier Device Package:	Package / Case:
PowerPAK® 1212-8	PowerPAK® 1212-8
Base Product Number:	
SQ7415	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
ECCN:	HTSUS:
EAR99	8541.29.0095

VISHAY

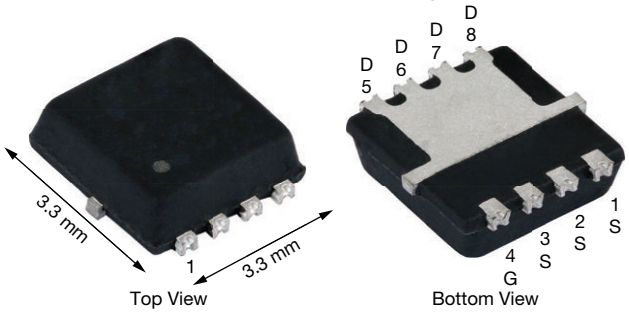
www.vishay.com

SQ7415AENW

Vishay Siliconix

Automotive P-Channel 60 V (D-S) 175 °C MOSFET

PowerPAK® 1212-8W Single



Marking code: Q021

FEATURES

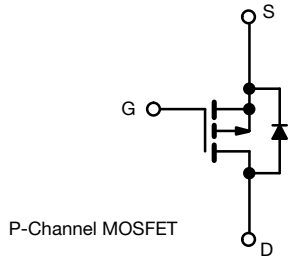
- TrenchFET® power MOSFET
- Low thermal resistance PowerPAK® 1212-8W package with 1.07 mm profile
- AEC-Q101 qualified
- Wettable flank terminals
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

AUTOMOTIVE GRADE

Pb-free

RoHS COMPLIANT

HALOGEN FREE



PRODUCT SUMMARY	
V_{DS} (V)	-60
$R_{DS(on)}$ (Ω) at V_{GS} = -10 V	0.065
$R_{DS(on)}$ (Ω) at V_{GS} = -4.5 V	0.090
I_D (A)	-16
Configuration	Single
Package	PowerPAK 1212-8W

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	-60	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current	T_C = 25 °C [a]	I_D	-16	A
	T_C = 125 °C		-11	
Continuous source current (diode conduction)[a]		I_S	-16	
Pulsed drain current [b]		I_{DM}	-64	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	-23	
Single pulse avalanche energy		E_{AS}	26	mJ
Maximum power dissipation [b]	T_C = 25 °C	P_D	53	W
	T_C = 125 °C		17	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +175	°C
Soldering recommendations (peak temperature) [d]			260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB Mount [c]	R_{thJA}	81	°C/W
Junction-to-case (drain)		R_{thJC}	2.8	

Notes

a. Package limited
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
c. When mounted on 1" square PCB (FR4 material)
d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

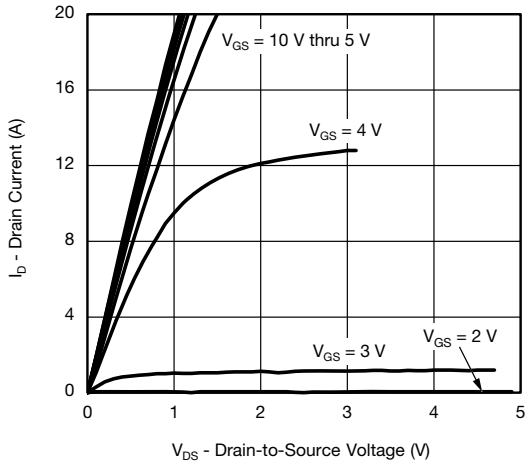
SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = -250 µA		-60	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 µA		-1.5	-2.0	-2.5	
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{GS} = 0 V	V_{DS} = -60 V	-	-	-1	µA
		V_{GS} = 0 V	V_{DS} = -60 V, T_J = 125 °C	-	-	-50	
		V_{GS} = 0 V	V_{DS} = -60 V, T_J = 175 °C	-	-	-150	
On-state drain current [a]	$I_{D(on)}$	V_{GS} = -10 V	V_{DS} ≤ -5 V	-15	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = -10 V	I_D = -5.7 A	-	0.050	0.065	Ω
		V_{GS} = -10 V	I_D = -5.7 A, T_J = 125 °C	-	-	0.112	
		V_{GS} = -10 V	I_D = -5.7 A, T_J = 175 °C	-	-	0.138	
		V_{GS} = -4.5 V	I_D = -4.4 A,	-	0.070	0.090	
Forward transconductance [b]	g_{fs}	V_{DS} = -15 V, I_D = -5.7 A		-	13	-	S
Dynamic [b]							
Input capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = -25 V, f = 1 MHz	-	1108	1385	pF
Output capacitance	C_{oss}			-	132	165	
Reverse transfer capacitance	C_{rss}			-	84	105	
Total gate charge [c]	Q_g	V_{GS} = -10 V	V_{DS} = -30 V, I_D = -5.7 A	-	25.5	38	nC
Gate-source charge [c]	Q_{gs}			-	3.6	-	
Gate-drain charge [c]	Q_{gd}			-	6.7	-	
Gate resistance	R_g	f = 1 MHz		3	6	9	Ω
Turn-on delay time [c]	$t_{d(on)}$	V_{DD} = -30 V, R_L = 30 Ω I_D ≅ -1 A, V_{GEN} = -10 V, R_g = 1 Ω		-	9	14	ns
Rise time [c]	t_r			-	9	14	
Turn-off delay time [c]	$t_{d(off)}$			-	37	56	
Fall time [c]	t_f			-	8	12	
Source-drain diode ratings and characteristics [b]							
Pulsed current [a]	I_{SM}			-	-	-64	A
Forward voltage	V_{SD}	I_F = -6 A, V_{GS} = 0 V		-	-0.85	-1.2	V

Notes

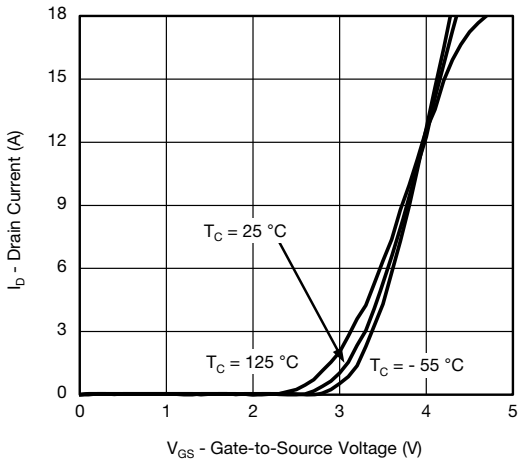
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing
c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

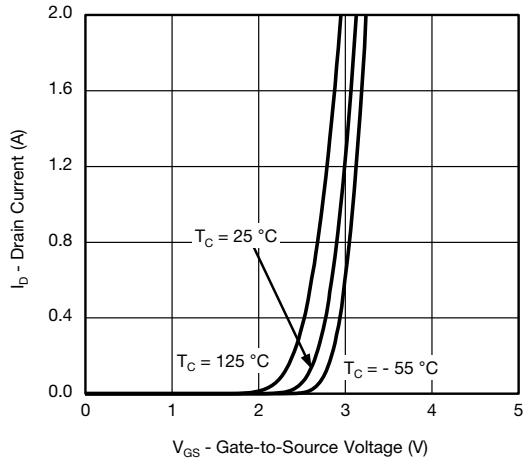
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



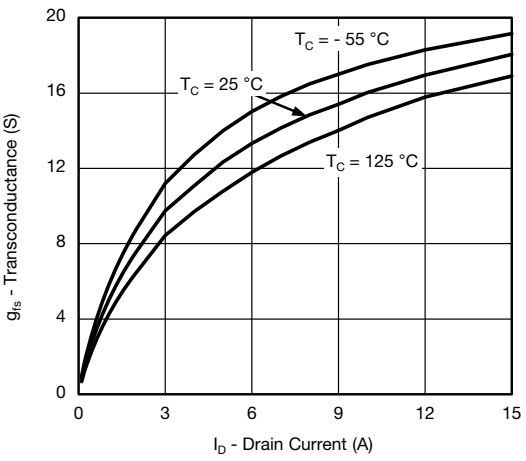
Output Characteristics



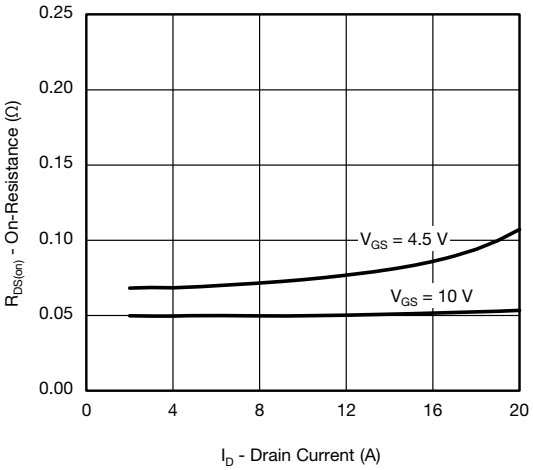
Transfer Characteristics



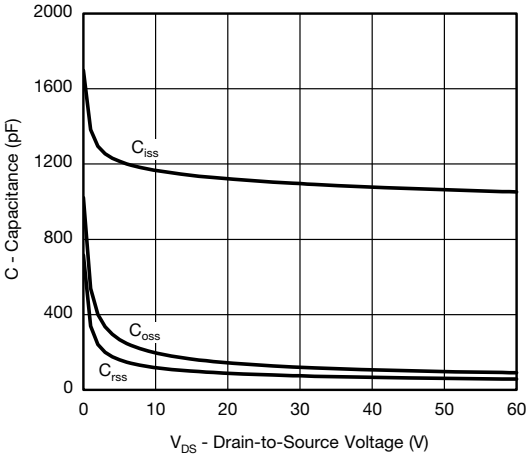
Transfer Characteristics



Transconductance

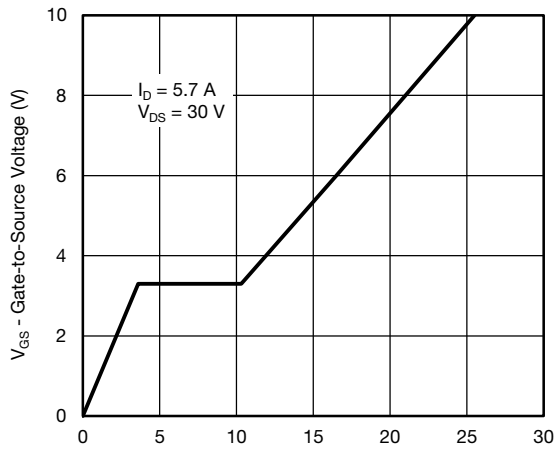


On-Resistance vs. Drain Current

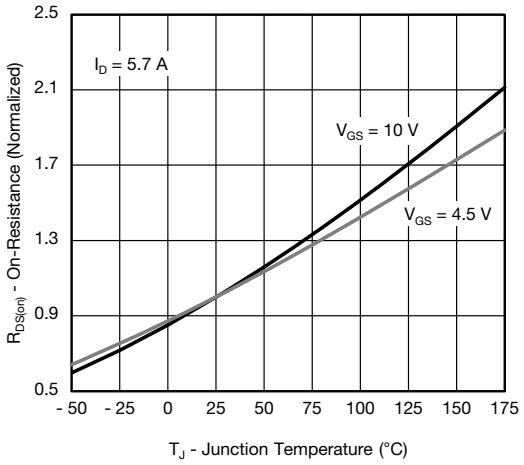


Capacitance

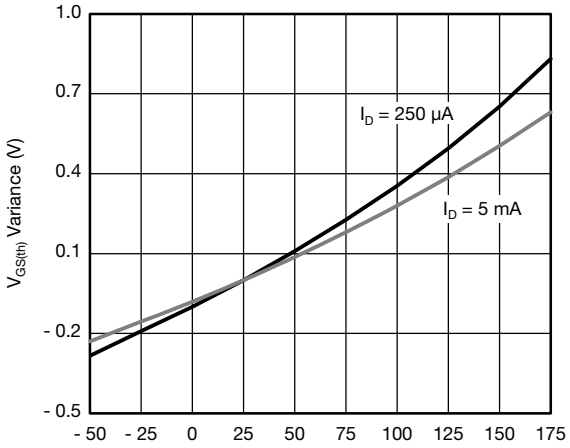
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



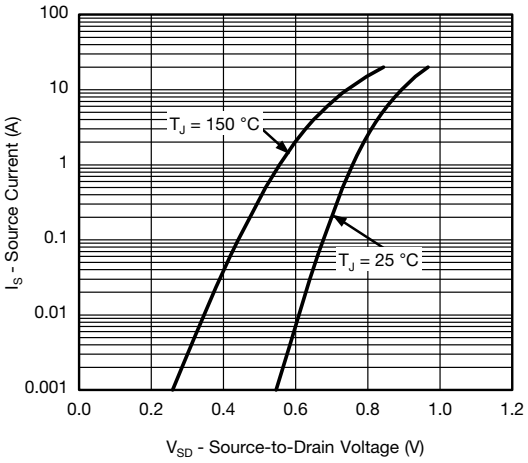
Gate Charge



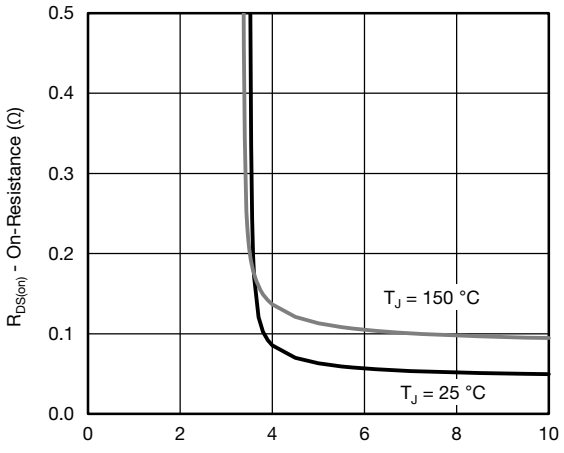
On-Resistance vs. Junction Temperature



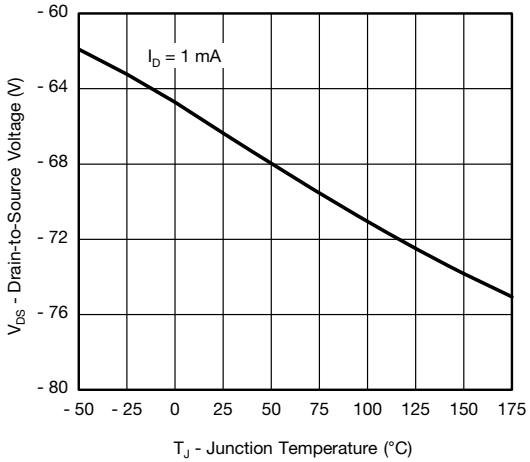
Threshold Voltage



Source Drain Diode Forward Voltage

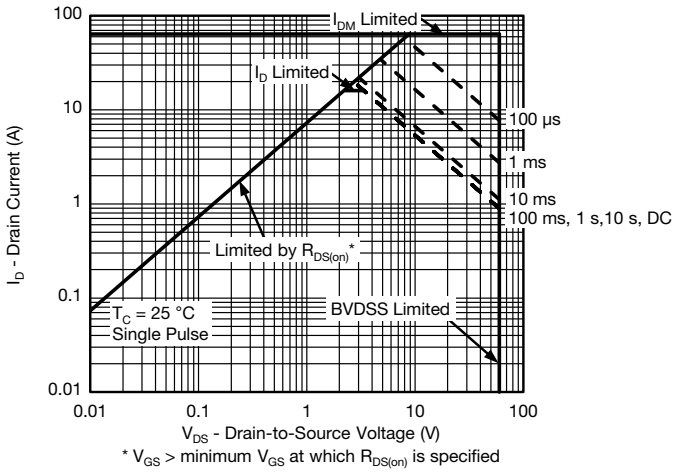


On-Resistance vs. Gate-to-Source Voltage



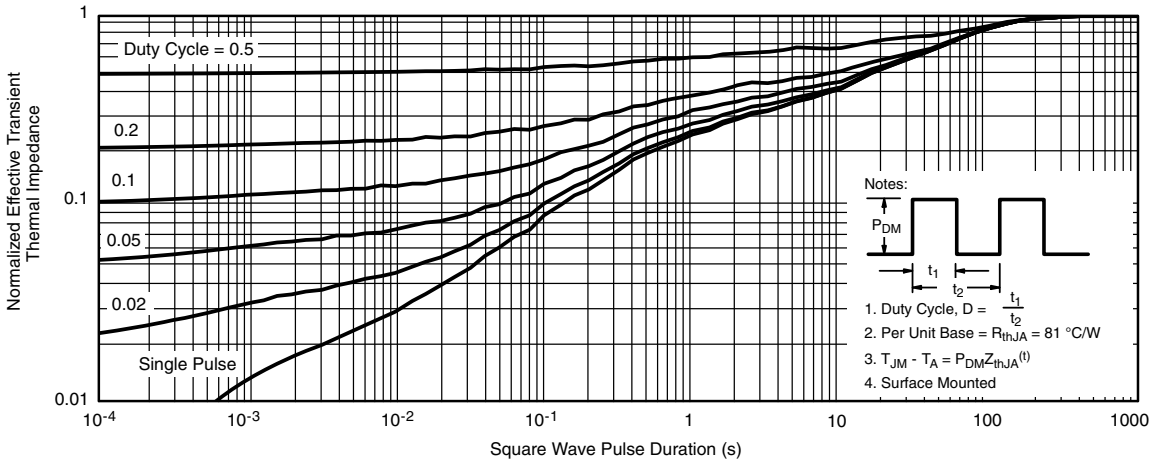
Drain Source Breakdown vs. Junction Temperature

THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)

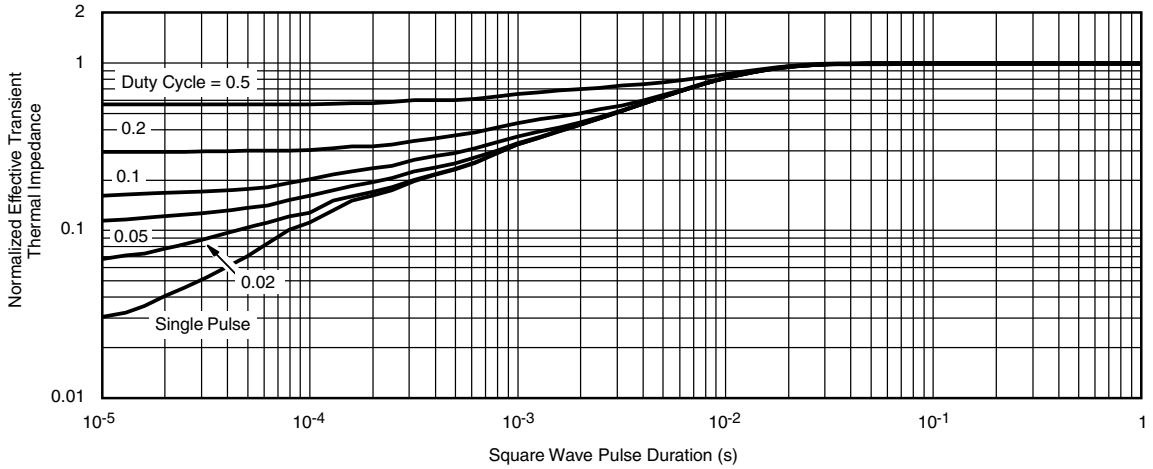


Safe Operating Area

THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

  are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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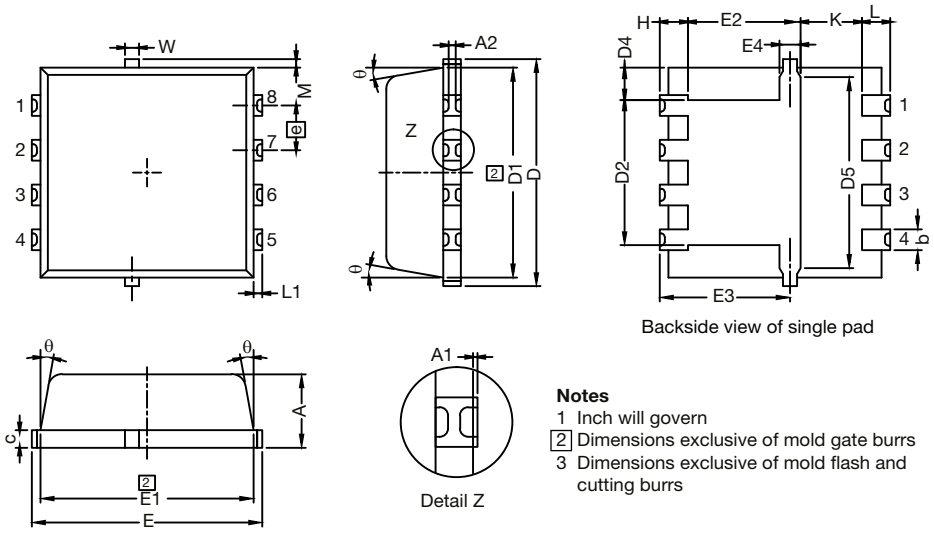
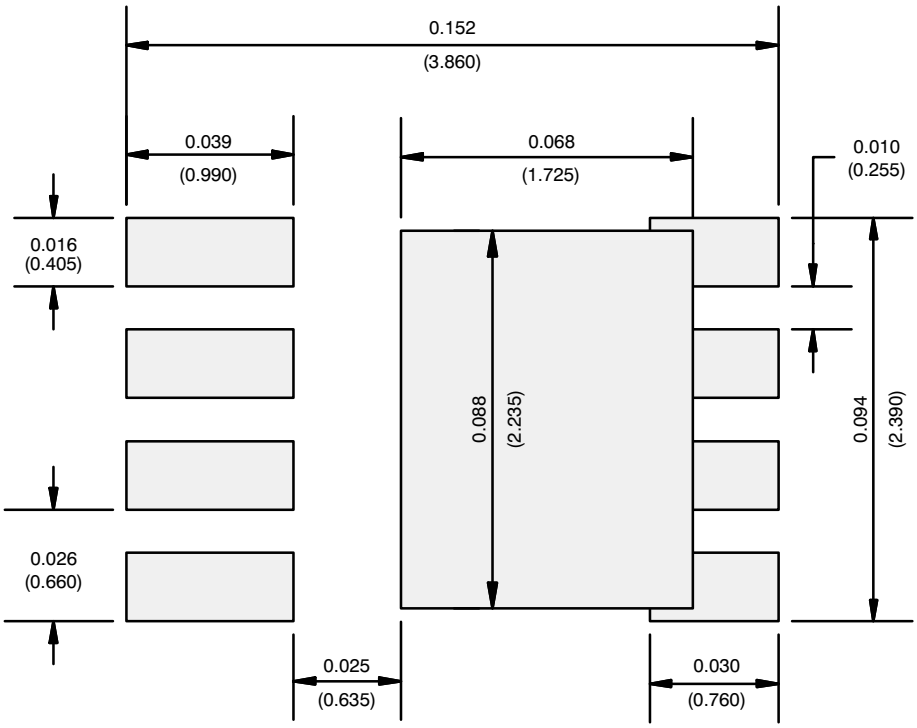
PowerPAK® 1212-8W Case Outline



Notes
1 Inch will govern
2 Dimensions exclusive of mold gate burrs
3 Dimensions exclusive of mold flash and cutting burrs

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1	0	-	0.05	0	-	0.002
A2	0	-	0.13	0	-	0.005
b	0.23	0.30	0.41	0.009	0.012	0.016
c	0.23	0.28	0.33	0.009	0.011	0.013
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
D4	0.47 typ.			0.0185 typ.		
D5	2.3 typ.			0.090 typ.		
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	1.75	1.85	1.98	0.069	0.073	0.078
E4	0.34 typ.			0.013 typ.		
e	0.65 BSC.			0.026 BSC		
K	0.86 typ.			0.034 typ.		
H	0.30	0.41	0.51	0.012	0.016	0.020
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		
ECN: C15-1530-Rev. B, 16-Nov-15 DWG: 6032						

RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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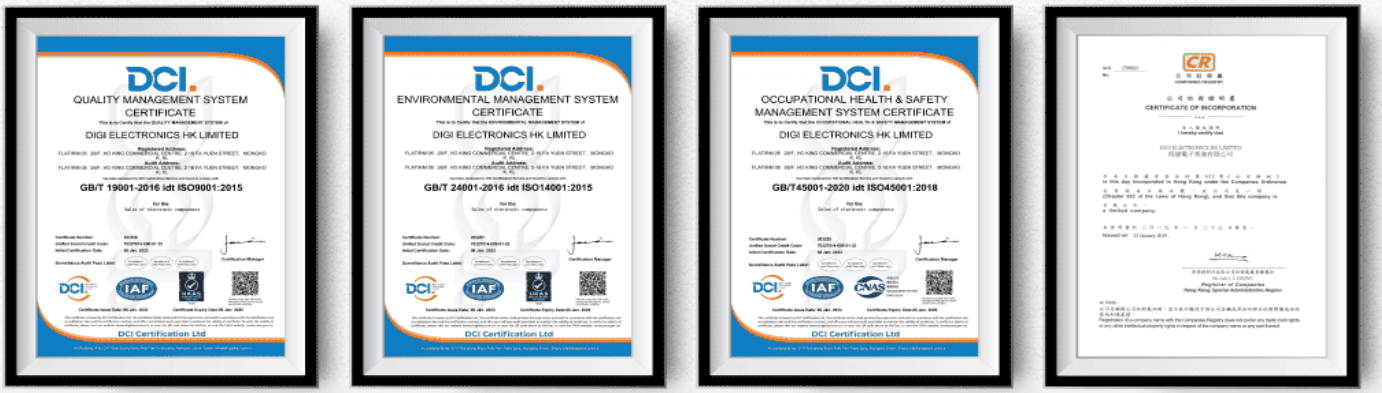

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