IHLP2020CZET4R7M11 Datasheet

DiGi Electronics Part Number	IHLP2020CZET4R7M11-DG
Manufacturer	Vishay Dale
Manufacturer Product Number	IHLP2020CZET4R7M11
Description	FIXED IND 4.7UH 4.5A 60MOHM SMD
Detailed Description	4.7 µH Shielded Molded Inductor 4.5 A 60mOhm Max Nonstandard

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
IHLP2020CZET4R7M11	Vishay Dale
Series:	Product Status:
IHLP-2020CZ-11	Obsolete
Type:	Material - Core:
Molded	-
Inductance:	Tolerance:
4.7 µH	±20%
Current Rating (Amps):	Current - Saturation (Isat):
4.5 A	5.2A
Shielding:	DC Resistance (DCR):
Shielded	60mOhm Max
Q @ Freq:	Frequency - Self Resonant:
-	22MHz
Ratings:	Operating Temperature:
-	-55°C ~ 125°C
Inductance Frequency - Test:	Features:
100 kHz	-
Mounting Type:	Package / Case:
Surface Mount	Nonstandard
Supplier Device Package:	Size / Dimension:
-	0.216" L x 0.204" W (5.49mm x 5.18mm)
Height - Seated (Max):	
0.118" (3.00mm)	

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
ECCN:	HTSUS:
EAR99	8504.50.4000

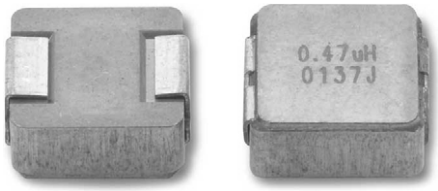
VISHAY

www.vishay.com

IHLP-2020CZ-11

Vishay Dale

IHLP® Commercial Inductors, Low DCR Series



LINKS TO ADDITIONAL RESOURCES

3D Models Calculators

FEATURES

- Shielded construction
- Lowest DCR/µH, in this package size
- Handles high transient current spikes without saturation
- Ultra low buzz noise, due to composite construction
- Excellent temperature stability for inductance and saturation
- Excellent DC/DC energy storage up to 1 MHz to 2 MHz. Filter inductor applications up to SRF (see “Standard Electrical Specifications” table)
- IHLP design; PATENT(S): www.vishay.com/patents
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- PDA / notebook / desktop / server applications
- High current POL converters
- Low profile, high current power supplies
- Battery powered devices
- DC/DC converters in distributed power systems
- DC/DC converter for field programmable gate array (FPGA)

STANDARD ELECTRICAL SPECIFICATIONS

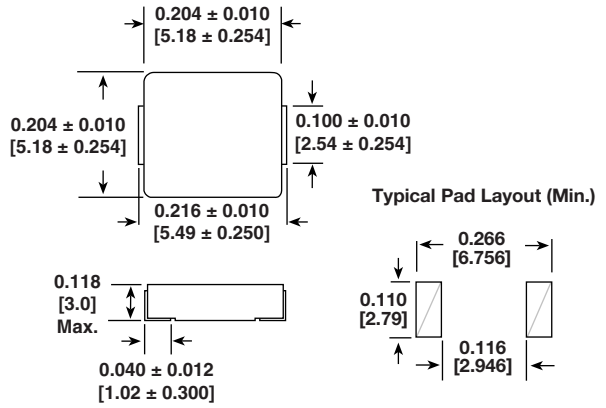
L_0 INDUCTANCE ± 20 % AT 100 kHz, 0.25 V, 0 A (µH)	DCR TYP. 25 °C (mΩ)	DCR MAX. 25 °C (mΩ)	HEAT RATING CURRENT DC TYP. (A) (1)	SATURATION CURRENT DC TYP.		SRF TYP. (MHz)
				(A) (2)	(A) (3)	
0.1	2.6	2.9	26.3	20.5	31.7	312
0.22	3.5	3.9	20.0	8.8	13.4	144
0.33	4.5	5.0	18.5	8.7	13.0	121
0.47	5.4	6.0	15.4	7.4	11.0	89
1	10.0	11.0	11.6	6.4	9.4	62
1.5	17.1	18.5	9.0	5.2	7.6	46
2.2	22.5	25.0	8.5	4.9	7.2	35
3.3	36.4	40.4	6.3	4.7	6.8	30
4.7	54.0	60.0	5.1	3.7	5.4	25
5.6	63.0	70.6	4.2	3.0	4.4	21
10	122.1	131.9	3.2	1.4	2.1	16
22	260.0	270.0	2.12	1.13	1.61	10.9

Notes

- All test data is referenced to 25 °C ambient
- Operating temperature range -55 °C to +125 °C
- The part temperature (ambient + temp. rise) should not exceed 125 °C under worst case operating conditions. Circuit design, component placement, PWB trace size and thickness, airflow and other cooling provisions all affect the part temperature. Part temperature should be verified in the end application
- Rated operating voltage (across inductor) = 40 V

(1) DC current (A) that will cause an approximate ΔT of 40 °C
(2) DC current (A) that will cause L_0 to drop approximately 20 %
(3) DC current (A) that will cause L_0 to drop approximately 30 %

DIMENSIONS in inches [millimeters]



DESCRIPTION

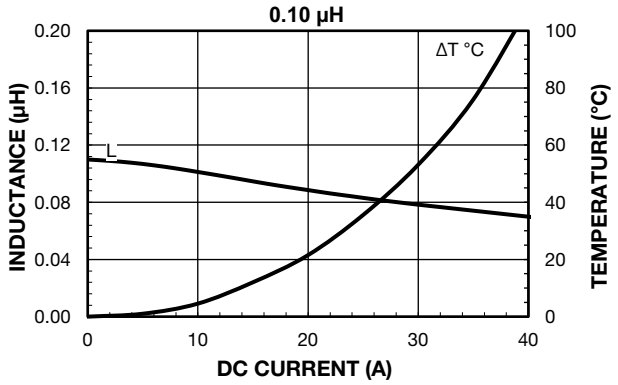
IHLP-2020CZ-11	4.7 µH	± 20 %	ER	e3
MODEL	INDUCTANCE VALUE	INDUCTANCE TOLERANCE	PACKAGE CODE	JEDEC® LEAD (Pb)-FREE STANDARD

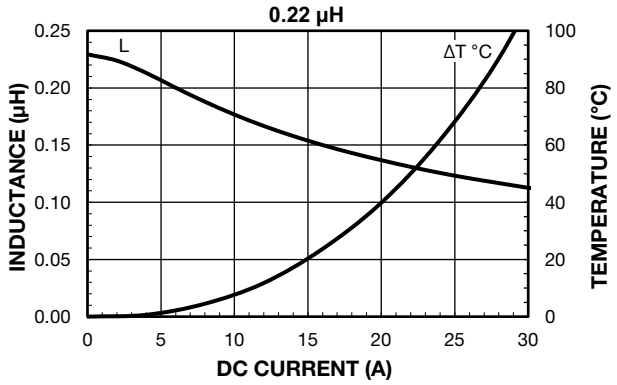
GLOBAL PART NUMBER

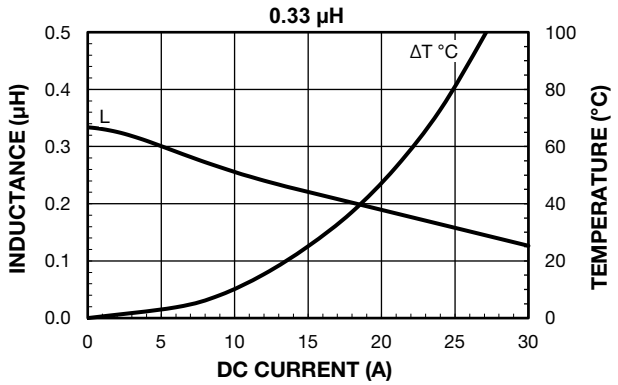
I	H	L	P	2	0	2	0	C	Z	E	R	4	R	7	M	1	1
PRODUCT FAMILY				SIZE						PACKAGE CODE		INDUCTANCE VALUE			TOL.	SERIES	

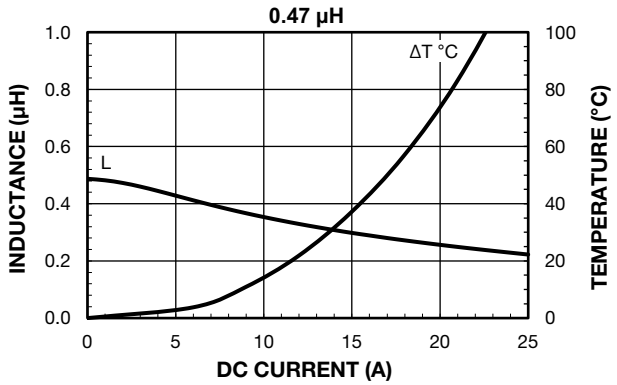
PATENT(S): www.vishay.com/patents
This Vishay product is protected by one or more United States and international patents.

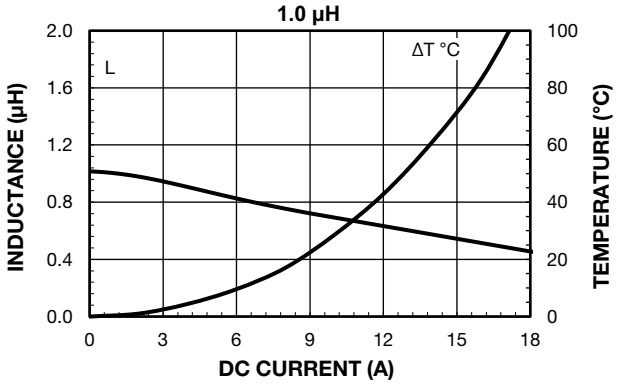
PERFORMANCE GRAPHS

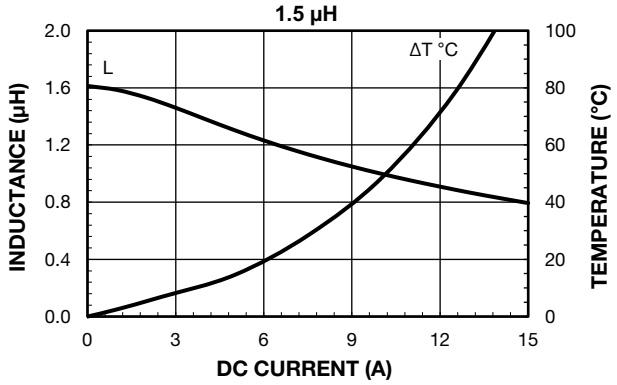


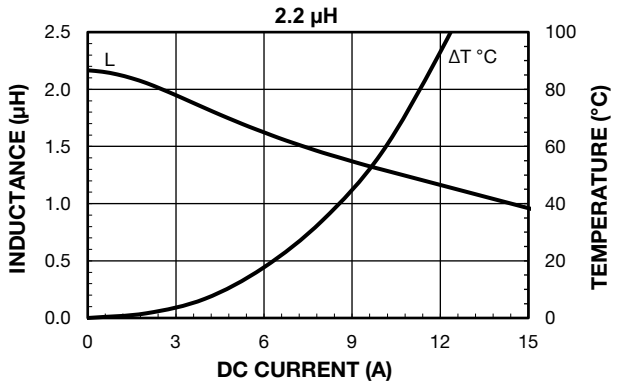


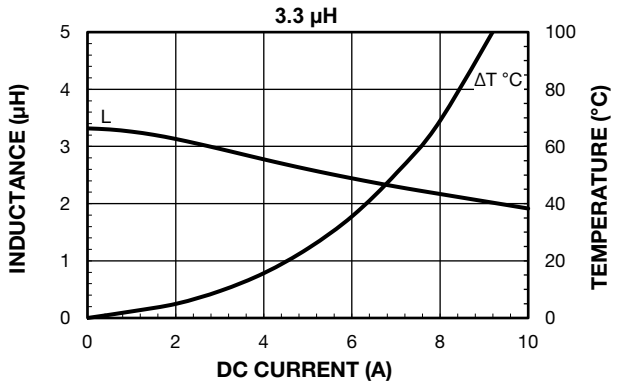












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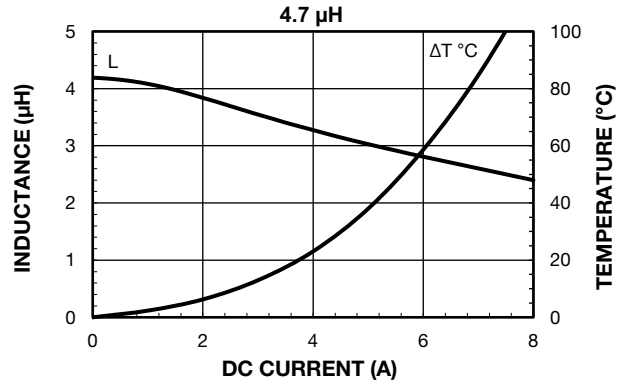
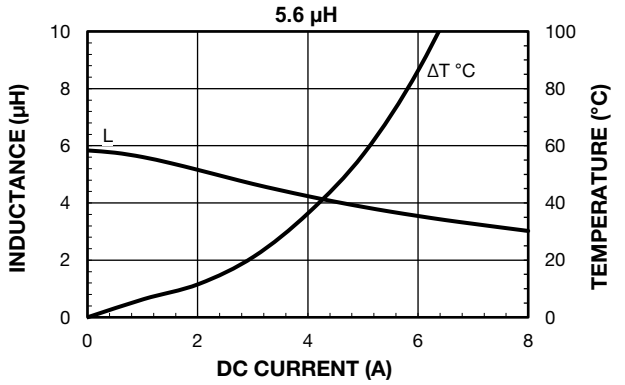
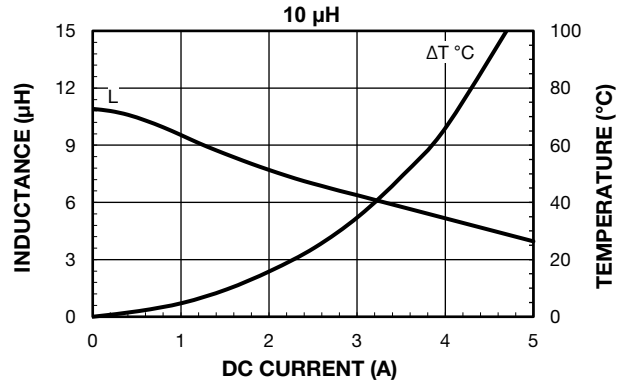
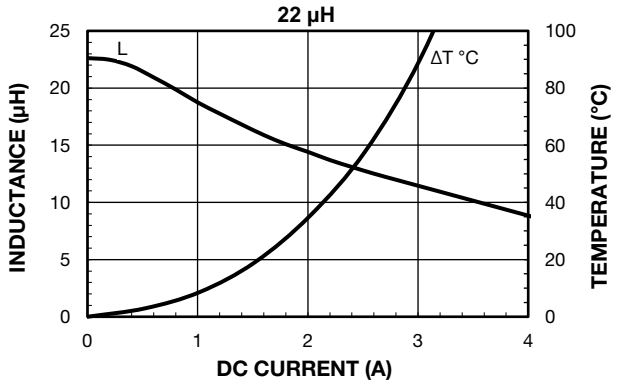
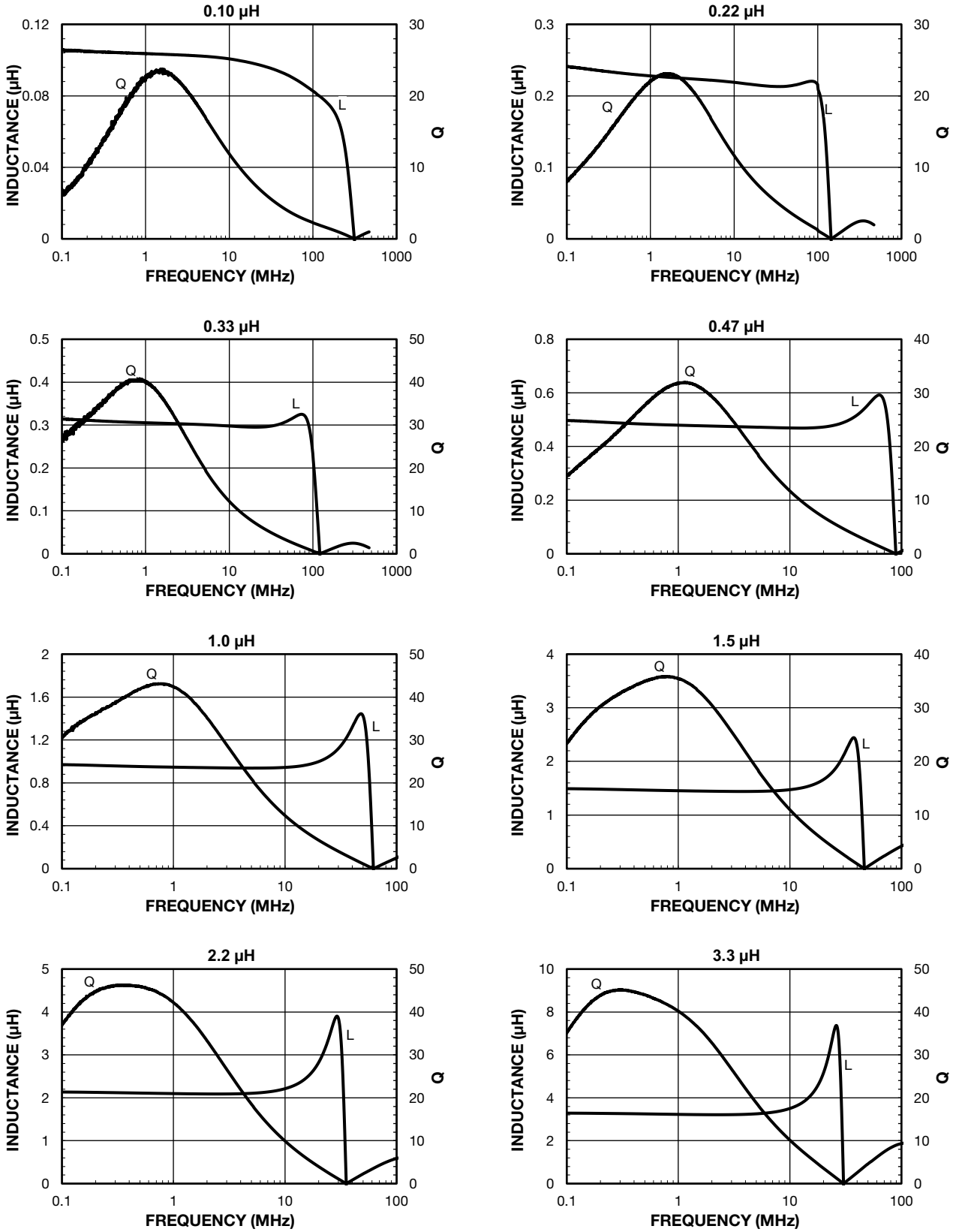








PERFORMANCE GRAPHS: INDUCTANCE AND Q VS. FREQUENCY



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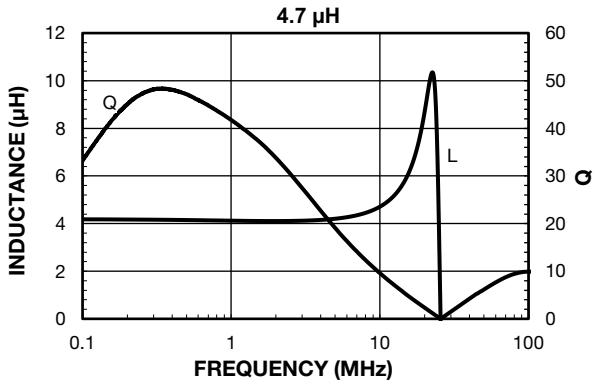

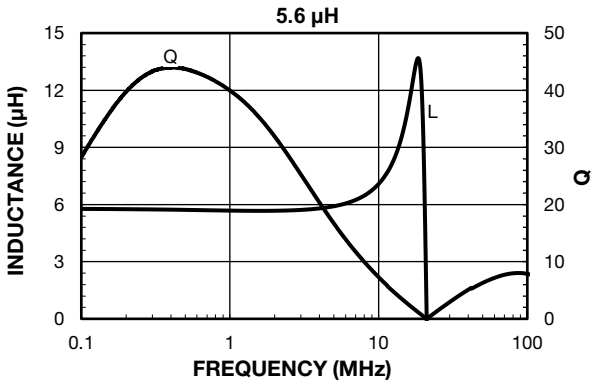

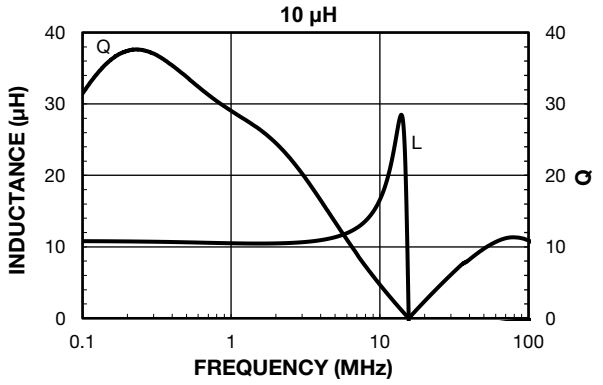

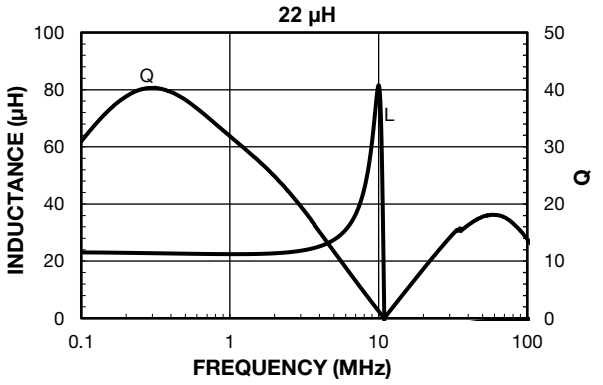

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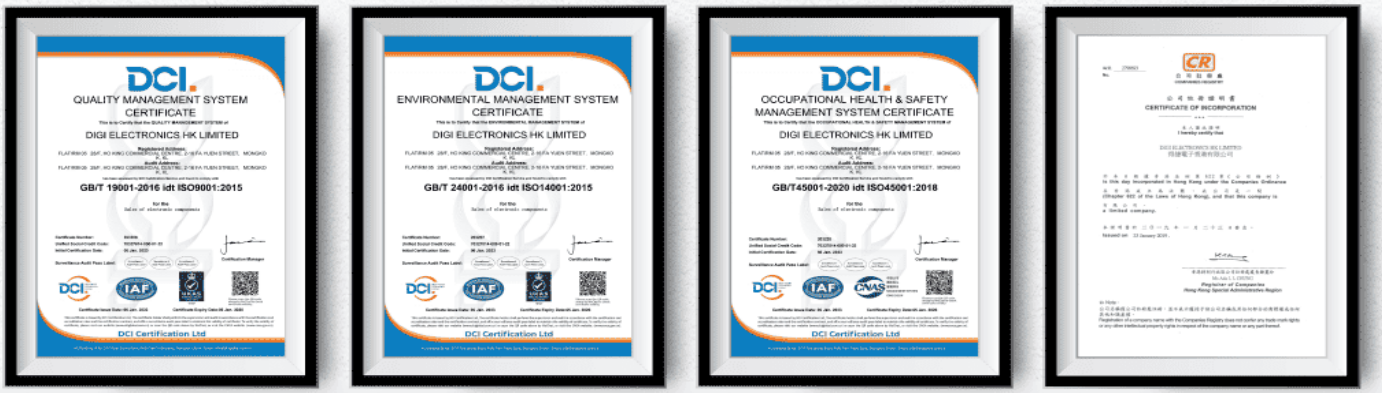

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