

XC17S200AVQ44C Datasheet

www.digi-electronics.com



XC17S200AVQ44C

<https://www.DiGi-Electronics.com>

DiGi Electronics Part Number	XC17S200AVQ44C-DG
Manufacturer	AMD
Manufacturer Product Number	XC17S200AVQ44C
Description	IC PROM SER 200000 C-TEMP 44VQFP
Detailed Description	Memory, Integrated Circuits (ICs)



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

XC17S200AVQ44C

Series:

-

DiGi-Electronics Programmable:

Not Verified

Memory Size:

2MB

Operating Temperature:

0°C ~ 70°C

Package / Case:

44-TQFP

Base Product Number:

XC17S200A

Manufacturer:

AMD

Product Status:

Obsolete

Programmable Type:

OTP

Voltage - Supply:

3V ~ 3.6V

Mounting Type:

Surface Mount

Supplier Device Package:

44-VQFP (10x10)

Environmental & Export classification

RoHS Status:

RoHS non-compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.32.0061

Moisture Sensitivity Level (MSL):

3 (168 Hours)

ECCN:

EAR99



Spartan-II/Spartan-IIe Family OTP Configuration PROMs (XC17S00A)

DS078 (v2.0) July 9, 2021

Product Specification

Features

- Configuration one-time programmable (OTP) read-only memory designed to store configuration bitstreams for Spartan™-II/Spartan-IIe FPGA devices
- Simple interface to the Spartan device
- Programmable reset polarity (active High or active Low)
- Low-power CMOS floating gate process
- 3.3V PROM
- Available in compact plastic 8-pin DIP, 8-pin VOIC, 20-pin SOIC, or 44-pin VQFP packages
- Programming support by leading programmer manufacturers
- Design support using the Xilinx Alliance and Foundation™ series software packages
- Guaranteed 20-year life data retention
- Pb-free (RoHS-compliant) packaging available

Introduction

The XC17S00A family of PROMs provide an easy-to-use, cost-effective method for storing Spartan-II/Spartan-IIe device configuration bitstreams.

When the Spartan device is in Master Serial mode, it generates a configuration clock that drives the Spartan PROM. A short access time after the rising clock edge, data appears on the PROM DATA output pin that is connected to the Spartan device D_{IN} pin. The Spartan device generates

the appropriate number of clock pulses to complete the configuration. Once configured, it disables the PROM. When a Spartan device is in Slave Serial mode, the PROM and the Spartan device must both be clocked by an incoming signal.

For device programming, either the Xilinx Alliance or the Spartan device design file into a standard HEX format which is then transferred to most commercial PROM programmers.

Spartan-II/IIe FPGA	Configuration Bits	Compatible Spartan-II/IIe PROM
XC2S15	197,696	XC17S15A
XC2S30	336,768	XC17S30A
XC2S50	559,200	XC17S50A
XC2S100	781,216	XC17S100A
XC2S150	1,040,096	XC17S150A
XC2S200	1,335,840	XC17S200A
XC2S50E	630,048	XC17S50A
XC2S100E	863,840	XC17S100A
XC2S150E ⁽¹⁾	1,134,496	XC17S200A
XC2S200E	1,442,016	XC17S200A
XC2S300E	1,875,648	XC17S300A
XC2S400E	2,693,440	XC17V04 ⁽²⁾
XC2S600E	3,961,632	XC17V04 ⁽²⁾

Notes:

1. Due to the higher configuration bit requirements of the XC2S150E device, an XC17S200A PROM is required to configure this FPGA.
2. See XC17V00 series configuration PROMs data sheet at: http://www.xilinx.com/support/documentation/data_sheets/ds073.pdf

Controlling PROMs

- Connecting the Spartan device with the PROM:
- The DATA output of the PROM drives the D_{IN} input of the lead Spartan device.
- The Master Spartan device CCLK output drives the CLK input of the PROM.
- The $\overline{\text{RESET}}/\text{OE}$ input of the PROM is connected to the $\overline{\text{INIT}}$ pin of the Spartan device and a pull-up resistor. This connection assures that the PROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a V_{CC} glitch.
- The $\overline{\text{CE}}$ input of the PROM is connected to the DONE pin of the Spartan device and a pull-up resistor. $\overline{\text{CE}}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 10 mA maximum.

FPGA Master Serial Mode Summary

The I/O and logic functions of the Configurable Logic Block (CLB) and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the Spartan device mode pins. In Master Serial mode, the Spartan device automatically loads the

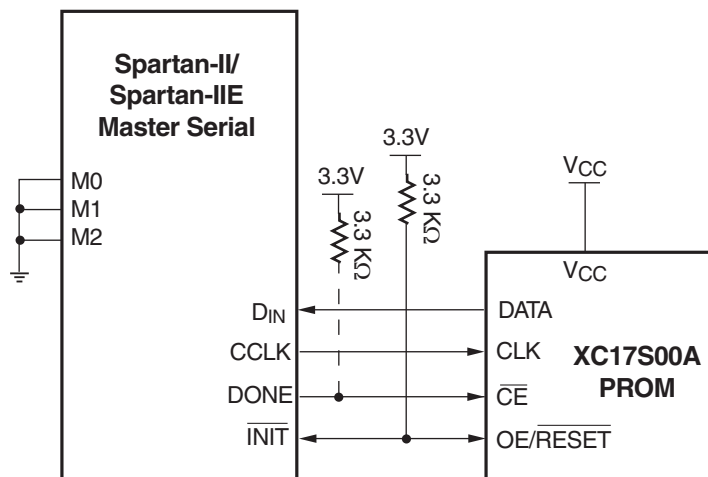
configuration program from an external memory. The XC17S00A PROM has been designed for compatibility with the Master Serial mode.

Upon power-up or reconfiguration, the Spartan device enters the Master Serial mode when the mode pins are set to Master Serial mode. Data is read from the PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial mode provides a simple configuration interface (Figure 1). Only a serial data line, two control lines, and a clock line are required to configure the Spartan device. Data from the PROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK.

If the user-programmable, dual-function D_{IN} pin on the Spartan device is used only for configuration, it must still be held at a defined level during normal operation. The Spartan-II/Spartan-IIE family takes care of this automatically with an on-chip pull-up/down resistor or keeper circuit.

The one-time-programmable XC17S00A PROM in Figure 1, page 3 supports automatic loading of configuration programs. An early DONE inhibits the PROM data output one CCLK cycle before the Spartan FPGA I/Os become active.



Notes:

1. If the DriveDone configuration option is not active, pull up DONE with a 3.3 kΩ resistor.

DS078_01_061107

Figure 1: XC17S00A PROM Connections to FPGA in Master Serial Mode

XC17S15A, XC17S30A, XC17S50A, XC17S100A, XC17S150A, XC17S200A, and XC17S300A

Absolute Maximum Ratings⁽¹⁾

Symbol	Description	Value	Units
V _{CC}	Supply voltage relative to GND	-0.5 to +4.0	V
V _{IN}	Input voltage with respect to GND	-0.5 to V _{CC} +0.5	V
V _{TS}	Voltage applied to High-Z output	-0.5 to V _{CC} +0.5	V
T _{STG}	Storage temperature (ambient)	-65 to +150	°C

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Operating Conditions⁽¹⁾

Symbol	Description	Min	Max	Units	
V _{CC}	Commercial	Supply voltage relative to GND (T _A = 0°C to +70°C)		V	
	Industrial	Supply voltage relative to GND (T _A = -40°C to +85°C)		V	
T _{VCC}	V _{CC} rise time from 0V to nominal voltage		1.0	50	ms

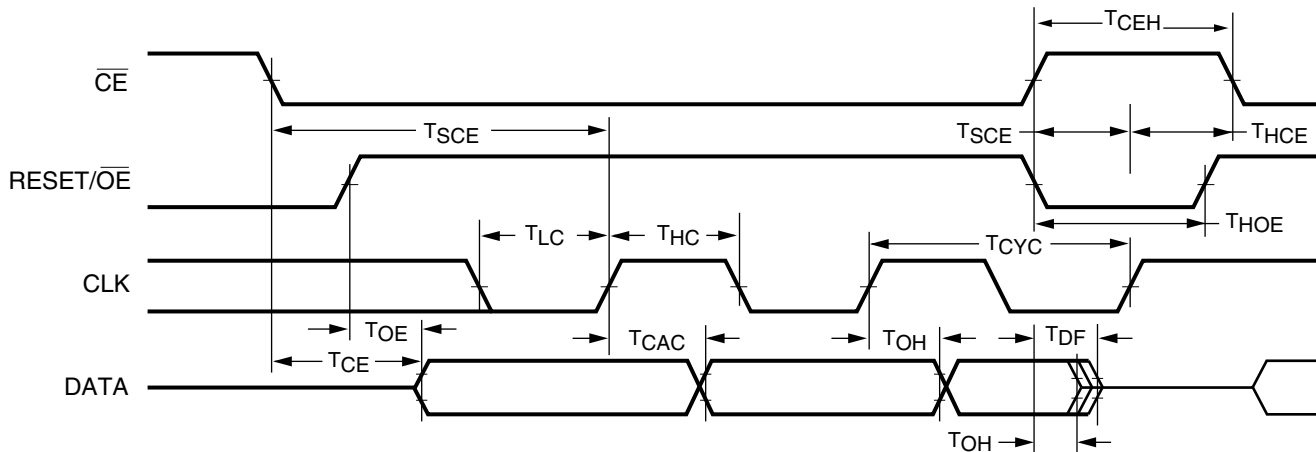
Notes:

- During normal read operation, both V_{CC} pins must be connected together.
- At power-up, the device requires the V_{CC} power supply to monotonically rise from 0V to nominal voltage within the specified V_{CC} rise time. If the power supply cannot meet this requirement, then the device may not perform a power-on-reset properly.

DC Characteristics Over Operating Condition

Symbol	Description	Min	Max	Units
V _{IH}	High-level input voltage	2.0	V _{CC}	V
V _{IL}	Low-level input voltage	0	0.8	V
V _{OH}	High-level output voltage (I _{OH} = -3 mA)	2.4	-	V
V _{OL}	Low-level output voltage (I _{OL} = +3 mA)	-	0.4	V
I _{CCA}	Supply current, active mode (at maximum frequency)	-	15	mA
I _{CCS}	Supply current, standby mode	-	1	mA
I _L	Input or output leakage current	-10	10	μA
C _{IN}	Input Capacitance (V _{IN} = GND, f = 1.0 MHz)	-	10	pF
C _{OUT}	Output Capacitance (V _{IN} = GND, f = 1.0 MHz)	-	10	pF

AC Characteristics Over Operating Condition⁽¹⁾



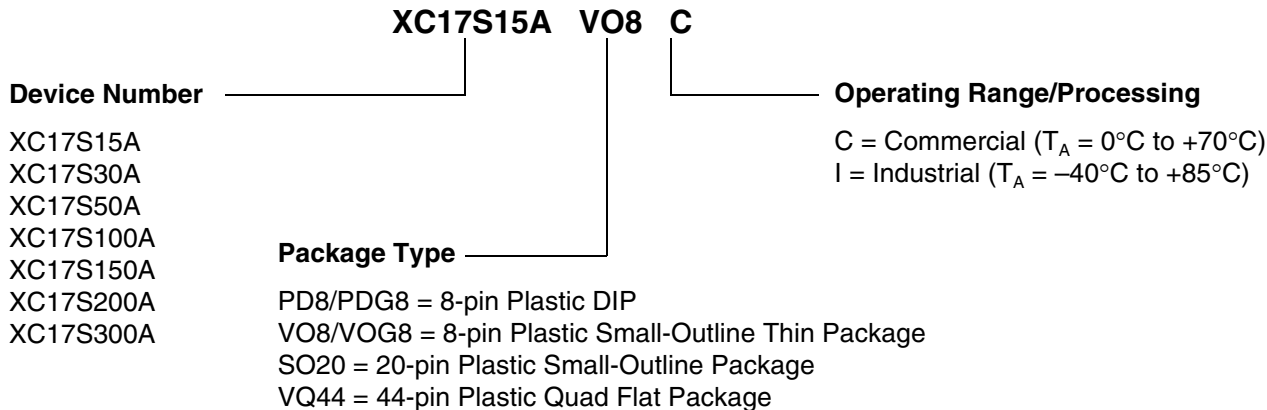
DS030_03_111502

Symbol	Description	Min	Max	Units
T_{OE}	RESET/ \overline{OE} to Data Delay	–	45	ns
T_{CE}	\overline{CE} to Data Delay	–	60	ns
T_{CAC}	CLK to Data Delay	–	80	ns
T_{OH}	Data Hold From \overline{CE} , RESET/ \overline{OE} , or CLK ⁽²⁾	0	–	ns
T_{DF}	\overline{CE} or RESET/ \overline{OE} to Data Float Delay ^(2,3)	–	50	ns
T_{CYC}	Clock Periods	100	–	ns
T_{LC}	CLK Low Time ⁽²⁾	50	–	ns
T_{HC}	CLK High Time ⁽²⁾	50	–	ns
T_{SCE}	\overline{CE} Setup Time to CLK (to guarantee proper counting)	25	–	ns
T_{HCE}	\overline{CE} Hold Time to CLK (to guarantee proper counting)	0	–	ns
T_{HOE}	RESET/ \overline{OE} Hold Time (guarantees counters are reset)	25	–	ns
T_{CEH}	CE High time (guarantees counters are reset)	20	–	ns

Notes:

1. AC test load = 50 pF
2. Guaranteed by design, not tested.
3. Float delays are measured with 5 pF AC loads. Transition is measured at ± 200 mV from steady state active levels.
4. All AC parameters are measured with $V_{IL} = 0.0V$ and $V_{IH} = 3.0V$.
5. If T_{CEH} High < 2 μs , $T_{CE} = 2 \mu s$.
6. If T_{HOE} High < 2 μs , $T_{CE} = 2 \mu s$.

Ordering Information



3.3V Valid Ordering Combinations

XC17S15APD8C	XC17S50APD8C	XC17S150APD8C
XC17S15AVO8C	XC17S50APDG8C	XC17S150AVO8C
XC17S15AVOG8C	XC17S50AVO8C	XC17S150ASO20C
XC17S15ASO20C	XC17S50AVOG8C	XC17S150APD8I
XC17S15APD8I	XC17S50ASO20C	XC17S150AVO8I
XC17S15AVO8I	XC17S50APD8I	XC17S150ASO20I
XC17S15ASO20I	XC17S50AVO8I	
	XC17S50ASO20I	
XC17S30APD8C	XC17S100APD8C	XC17S200APD8C
XC17S30AVO8C	XC17S100AVO8C	XC17S200APDG8C
XC17S30ASO20C	XC17S100AVOG8C	XC17S200AVO8C
XC17S30APD8I	XC17S100ASO20C	XC17S200AVOG8C
XC17S30AVO8I	XC17S100APD8I	XC17S200APD8I
XC17S30ASO20I	XC17S100AVO8I	XC17S200APDG8I
	XC17S100ASO20I	XC17S200AVO8I
		XC17S200AVOG8I
		XC17S200AVQ44C
		XC17S200AVQ44I
		XC17S300AVQ44C
		XC17S300AVQ44I

Notice of Disclaimer

The information disclosed to you hereunder (the "Materials") is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available "AS IS" and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx's limited warranty, please refer to Xilinx's Terms of Sale which can be viewed at www.xilinx.com/legal.htm#tos; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx's Terms of Sale which can be viewed at www.xilinx.com/legal.htm#tos.

OUR CERTIFICATE

DiGi provide top-quality products and perfect service for customer worldwide through standardization, technological innovation and continuous improvement. DiGi through third-party certification, we stricly control the quality of products and services. Welcome your RFQ to

Email: Info@DiGi-Electronics.com



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.