

# XC17S50ASO20C Datasheet



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DiGi Electronics Part Number	XC17S50ASO20C-DG
Manufacturer	<a href="#">AMD</a>
Manufacturer Product Number	XC17S50ASO20C
Description	IC PROM SER 50000 C-TEMP 20-SOIC
Detailed Description	Memory, Integrated Circuits (ICs)



Tel: +00 852-30501935

RFQ Email: [Info@DiGi-Electronics.com](mailto:Info@DiGi-Electronics.com)

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## Purchase and inquiry

Manufacturer Product Number:

XC17S50ASO20C

Series:

-

DiGi-Electronics Programmable:

Verified

Memory Size:

500kb

Operating Temperature:

0°C ~ 70°C

Package / Case:

20-SOIC (0.295", 7.50mm Width)

Base Product Number:

XC17S50A

Manufacturer:

AMD

Product Status:

Obsolete

Programmable Type:

OTP

Voltage - Supply:

3V ~ 3.6V

Mounting Type:

Surface Mount

Supplier Device Package:

20-SOIC

## Environmental & Export classification

RoHS Status:

RoHS non-compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.32.0071

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99



# Spartan-II/Spartan-IIe Family OTP Configuration PROMs (XC17S00A)

DS078 (v2.0) July 9, 2021

Product Specification

## Features

- Configuration one-time programmable (OTP) read-only memory designed to store configuration bitstreams for Spartan™-II/Spartan-IIe FPGA devices
- Simple interface to the Spartan device
- Programmable reset polarity (active High or active Low)
- Low-power CMOS floating gate process
- 3.3V PROM
- Available in compact plastic 8-pin DIP, 8-pin VOIC, 20-pin SOIC, or 44-pin VQFP packages
- Programming support by leading programmer manufacturers
- Design support using the Xilinx Alliance and Foundation™ series software packages
- Guaranteed 20-year life data retention
- Pb-free (RoHS-compliant) packaging available

## Introduction

The XC17S00A family of PROMs provide an easy-to-use, cost-effective method for storing Spartan-II/Spartan-IIe device configuration bitstreams.

When the Spartan device is in Master Serial mode, it generates a configuration clock that drives the Spartan PROM. A short access time after the rising clock edge, data appears on the PROM DATA output pin that is connected to the Spartan device D<sub>IN</sub> pin. The Spartan device generates

the appropriate number of clock pulses to complete the configuration. Once configured, it disables the PROM. When a Spartan device is in Slave Serial mode, the PROM and the Spartan device must both be clocked by an incoming signal.

For device programming, either the Xilinx Alliance or the Spartan device design file into a standard HEX format which is then transferred to most commercial PROM programmers.

Spartan-II/IIe FPGA	Configuration Bits	Compatible Spartan-II/IIe PROM
XC2S15	197,696	XC17S15A
XC2S30	336,768	XC17S30A
XC2S50	559,200	XC17S50A
XC2S100	781,216	XC17S100A
XC2S150	1,040,096	XC17S150A
XC2S200	1,335,840	XC17S200A
XC2S50E	630,048	XC17S50A
XC2S100E	863,840	XC17S100A
XC2S150E <sup>(1)</sup>	1,134,496	XC17S200A
XC2S200E	1,442,016	XC17S200A
XC2S300E	1,875,648	XC17S300A
XC2S400E	2,693,440	XC17V04 <sup>(2)</sup>
XC2S600E	3,961,632	XC17V04 <sup>(2)</sup>

### Notes:

1. Due to the higher configuration bit requirements of the XC2S150E device, an XC17S200A PROM is required to configure this FPGA.
2. See XC17V00 series configuration PROMs data sheet at: [http://www.xilinx.com/support/documentation/data\\_sheets/ds073.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds073.pdf)

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## **XC17S15A, XC17S30A, XC17S50A, XC17S100A, XC17S150A, XC17S200A, and XC17S300A**

### **Absolute Maximum Ratings<sup>(1)</sup>**

<b>Symbol</b>	<b>Description</b>	<b>Value</b>	<b>Units</b>
$V_{CC}$	Supply voltage relative to GND	-0.5 to +4.0	V
$V_{IN}$	Input voltage with respect to GND	-0.5 to $V_{CC} + 0.5$	V
$V_{TS}$	Voltage applied to High-Z output	-0.5 to $V_{CC} + 0.5$	V
$T_{STG}$	Storage temperature (ambient)	-65 to +150	°C

**Notes:**

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

### **Operating Conditions<sup>(1)</sup>**

<b>Symbol</b>	<b>Description</b>	<b>Min</b>	<b>Max</b>	<b>Units</b>	
$V_{CC}$	Commercial	Supply voltage relative to GND ( $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ )		V	
	Industrial	Supply voltage relative to GND ( $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ )		V	
$T_{VCC}$	$V_{CC}$ rise time from 0V to nominal voltage		1.0	50	ms

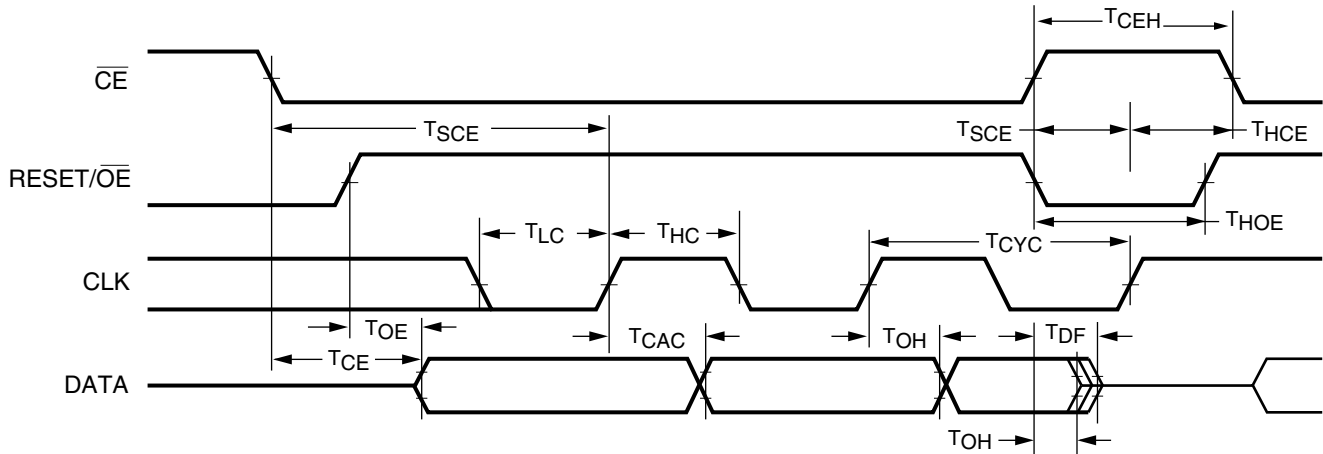
**Notes:**

- During normal read operation, both  $V_{CC}$  pins must be connected together.
- At power-up, the device requires the  $V_{CC}$  power supply to monotonically rise from 0V to nominal voltage within the specified  $V_{CC}$  rise time. If the power supply cannot meet this requirement, then the device may not perform a power-on-reset properly.

### **DC Characteristics Over Operating Condition**

<b>Symbol</b>	<b>Description</b>	<b>Min</b>	<b>Max</b>	<b>Units</b>
$V_{IH}$	High-level input voltage	2.0	$V_{CC}$	V
$V_{IL}$	Low-level input voltage	0	0.8	V
$V_{OH}$	High-level output voltage ( $I_{OH} = -3$ mA)	2.4	-	V
$V_{OL}$	Low-level output voltage ( $I_{OL} = +3$ mA)	-	0.4	V
$I_{CCA}$	Supply current, active mode (at maximum frequency)	-	15	mA
$I_{CCS}$	Supply current, standby mode	-	1	mA
$I_L$	Input or output leakage current	-10	10	μA
$C_{IN}$	Input Capacitance ( $V_{IN} = \text{GND}$ , $f = 1.0$ MHz)	-	10	pF
$C_{OUT}$	Output Capacitance ( $V_{IN} = \text{GND}$ , $f = 1.0$ MHz)	-	10	pF

## AC Characteristics Over Operating Condition<sup>(1)</sup>



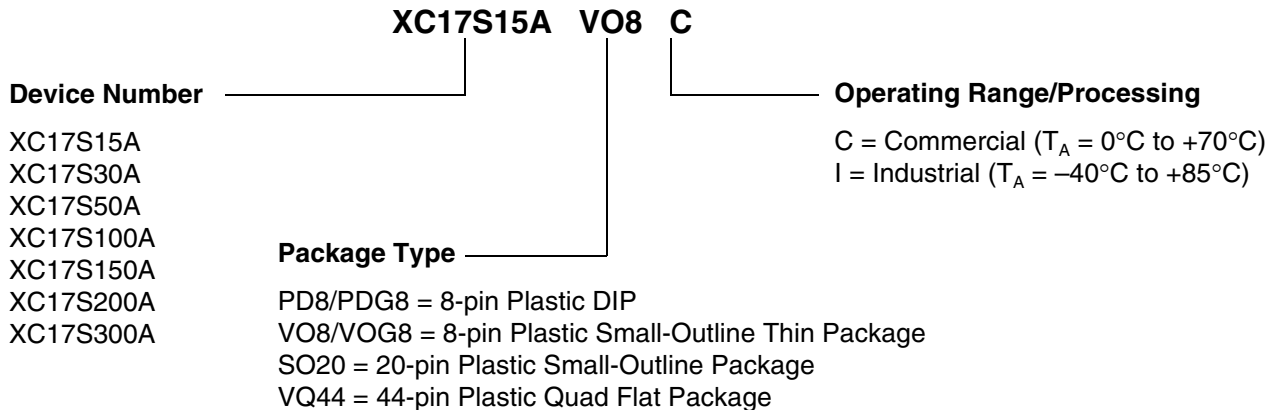
DS030\_03\_111502

Symbol	Description	Min	Max	Units
$T_{OE}$	RESET/ $\overline{OE}$ to Data Delay	–	45	ns
$T_{CE}$	$\overline{CE}$ to Data Delay	–	60	ns
$T_{CAC}$	CLK to Data Delay	–	80	ns
$T_{OH}$	Data Hold From $\overline{CE}$ , RESET/ $\overline{OE}$ , or CLK <sup>(2)</sup>	0	–	ns
$T_{DF}$	$\overline{CE}$ or RESET/ $\overline{OE}$ to Data Float Delay <sup>(2,3)</sup>	–	50	ns
$T_{CYC}$	Clock Periods	100	–	ns
$T_{LC}$	CLK Low Time <sup>(2)</sup>	50	–	ns
$T_{HC}$	CLK High Time <sup>(2)</sup>	50	–	ns
$T_{SCE}$	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	25	–	ns
$T_{HCE}$	$\overline{CE}$ Hold Time to CLK (to guarantee proper counting)	0	–	ns
$T_{HOE}$	RESET/ $\overline{OE}$ Hold Time (guarantees counters are reset)	25	–	ns
$T_{CEH}$	CE High time (guarantees counters are reset)	20	–	ns

**Notes:**

- AC test load = 50 pF
- Guaranteed by design, not tested.
- Float delays are measured with 5 pF AC loads. Transition is measured at  $\pm 200$  mV from steady state active levels.
- All AC parameters are measured with  $V_{IL} = 0.0V$  and  $V_{IH} = 3.0V$ .
- If  $T_{CEH}$  High < 2 $\mu$ s,  $T_{CE} = 2 \mu$ s.
- If  $T_{HOE}$  High < 2 $\mu$ s,  $T_{CE} = 2 \mu$ s.

## Ordering Information

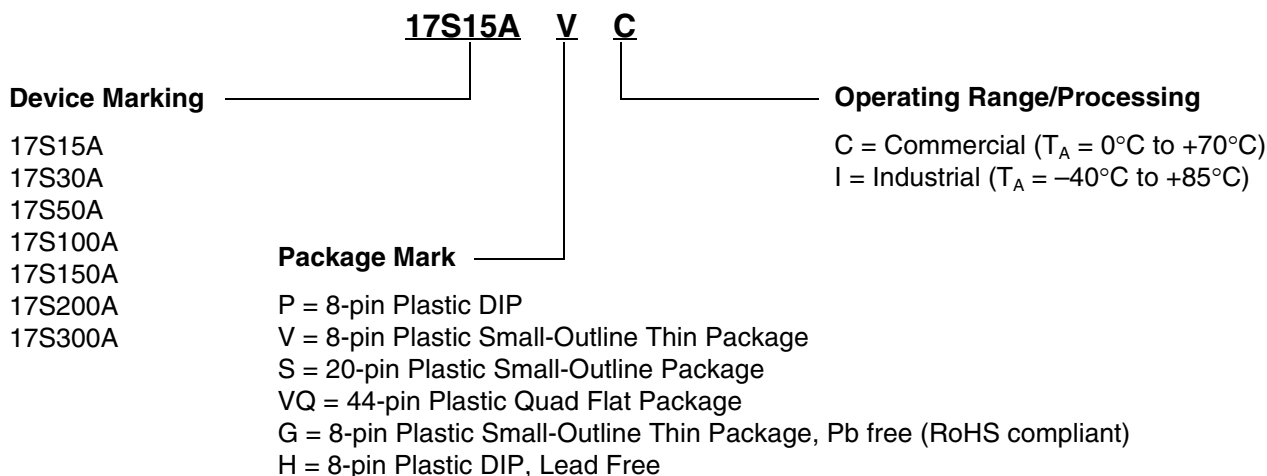


### 3.3V Valid Ordering Combinations

XC17S15APD8C	XC17S50APD8C	XC17S150APD8C
XC17S15AVO8C	XC17S50APDG8C	XC17S150AVO8C
XC17S15AVOG8C	XC17S50AVO8C	XC17S150ASO20C
XC17S15ASO20C	XC17S50AVOG8C	XC17S150APD8I
XC17S15APD8I	XC17S50ASO20C	XC17S150AVO8I
XC17S15AVO8I	XC17S50APD8I	XC17S150ASO20I
XC17S15ASO20I	XC17S50AVO8I	
	XC17S50ASO20I	
XC17S30APD8C	XC17S100APD8C	XC17S200APD8C
XC17S30AVO8C	XC17S100AVO8C	XC17S200APDG8C
XC17S30ASO20C	XC17S100AVOG8C	XC17S200AVO8C
XC17S30APD8I	XC17S100ASO20C	XC17S200AVOG8C
XC17S30AVO8I	XC17S100APD8I	XC17S200APD8I
XC17S30ASO20I	XC17S100AVO8I	XC17S200APDG8I
	XC17S100ASO20I	XC17S200AVO8I
		XC17S200AVOG8I
		XC17S200AVQ44C
		XC17S200AVQ44I
		XC17S300AVQ44C
		XC17S300AVQ44I

## Marking Information

Due to the small size of the PROM package, the complete ordering part number cannot be marked on the package. The XC prefix is deleted and the package code is simplified. Device marking is as follows.



## Revision History

The following table shows the revision history for this document.

Date	Revision	Revision
09/14/2000	1.0	Initial Xilinx release.
11/13/2000	1.1	Updated configuration bits.
04/07/2001	1.2	Added to features: "Guaranteed 20 year life data retention", removed "Programming the FPGA with counters" and related text.
06/20/2001	1.3	Revised <a href="#">Figure 1</a> resistor values to match Spartan-II data sheet.
10/09/2001	1.4	Added note for unlisted pins, changed $I_{CCA}$ and $I_{CCS}$ , and added power-on supply requirements and note regarding power-on reset.
11/15/2001	1.5	Updated for Spartan-IIE FPGA family.
06/25/2002	1.6	Changed <a href="#">Table 1, page 4</a> .
10/15/2002	1.7	Changed <a href="#">Table 1, page 4</a> . Added " <a href="#">Pinout Diagrams</a> ," <a href="#">page 2</a> .
11/18/2002	1.8	Added XC2S400E and XC2S600E to Compatible FPGAS table. Modified document title.
06/24/2005	1.9	Added Pb-free information to the " <a href="#">Pinout Diagrams</a> ", " <a href="#">Ordering Information</a> ", " <a href="#">3.3V Valid Ordering Combinations</a> ", and " <a href="#">Marking Information</a> " figures. Removed $T_{SOL}$ from the " <a href="#">Absolute Maximum Ratings(1)</a> " table.
06/25/2007	1.10	Updated format. Added Pb-free (RoHS-compliant) packaging. Timing diagram removed from <a href="#">Figure 1, page 3</a> . Part Numbers XC17S200APDG8I, and XC17S200AVOG8I added to " <a href="#">3.3V Valid Ordering Combinations</a> ," <a href="#">page 7</a> .
07/09/2021	2.0	Added " <a href="#">Notice of Disclaimer</a> ." This product is obsolete/discontinued per <a href="#">XCN07010</a> , <a href="#">XCN13019</a> , and <a href="#">XCN15006</a> .

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