

# XC2C384-10PQG208C Datasheet

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XC2C384-10PQG208C

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DiGi Electronics Part Number	XC2C384-10PQG208C-DG
Manufacturer	<a href="#">AMD</a>
Manufacturer Product Number	XC2C384-10PQG208C
Description	IC CPLD 384MC 9.2NS 208QFP
Detailed Description	Embedded, Integrated Circuits (ICs)



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## Purchase and inquiry

Manufacturer Product Number:

XC2C384-10PQG208C

Series:

CoolRunner II

DiGi-Electronics Programmable:

Verified

Delay Time tpd(1) Max:

9.2 ns

Number of Logic Elements/Blocks:

24

Number of Gates:

9000

Operating Temperature:

0°C ~ 70°C (TA)

Package / Case:

208-BFQFP

Base Product Number:

XC2C384

Manufacturer:

AMD

Product Status:

Obsolete

Programmable Type:

In System Programmable

Voltage Supply - Internal:

1.7V ~ 1.9V

Number of Macrocells:

384

Number of I/O:

173

Mounting Type:

Surface Mount

Supplier Device Package:

208-PQFP (28x28)

## Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

3 (168 Hours)

ECCN:

EAR99



## XC2C384 CoolRunner-II CPLD

DS095 (v3.2) March 8, 2007

### Product Specification

### Features

- Optimized for 1.8V systems
  - As fast as 7.1 ns pin-to-pin delays
  - As low as 14  $\mu$ A quiescent current
- Industry's best 0.18 micron CMOS CPLD
  - Optimized architecture for effective logic synthesis
  - Multi-voltage I/O operation — 1.5V to 3.3V
- Available in multiple package options
  - 144-pin TQFP with 118 user I/O
  - 208-pin PQFP with 173 user I/O
  - 256-ball FT (1.0mm) BGA with 212 user I/O
  - 324-ball FG (1.0mm) BGA with 240 user I/O
  - Pb-free available for all packages
- Advanced system features
  - Fastest in system programming
    - 1.8V ISP using IEEE 1532 (JTAG) interface
  - IEEE1149.1 JTAG Boundary Scan Test
  - Optional Schmitt-trigger input (per pin)
  - Unsurpassed low power management
    - DataGATE enable (DGE) signal control
  - Four separate I/O banks
  - RealDigital 100% CMOS product term generation
  - Flexible clocking modes
    - Optional DualEDGE triggered registers
    - Clock divider (divide by 2,4,6,8,10,12,14,16)
    - CoolCLOCK
  - Global signal options with macrocell control
    - Multiple global clocks with phase selection per macrocell
    - Multiple global output enables
    - Global set/reset
  - Advanced design security
  - PLA architecture
    - Superior pinout retention
    - 100% product term routability across function block
  - Open-drain output option for Wired-OR and LED drive
  - Optional bus-hold, 3-state or weak pullup on selected I/O pins
  - Optional configurable grounds on unused I/Os
  - Mixed I/O voltages compatible with 1.5V, 1.8V, 2.5V, and 3.3V logic levels
    - SSTL2-1, SSTL3-1, and HSTL-1 I/O compatibility
  - Hot pluggable

Refer to the CoolRunner™-II family data sheet for architecture description.

### Description

The CoolRunner-II 384-macrocell device is designed for both high performance and low power applications. This lends power savings to high-end communication equipment and high speed to battery operated devices. Due to the low power stand-by and dynamic operation, overall system reliability is improved.

This device consists of twenty four Function Blocks inter-connected by a low power Advanced Interconnect Matrix (AIM). The AIM feeds 40 true and complement inputs to each Function Block. The Function Blocks consist of a 40 by 56 P-term PLA and 16 macrocells which contain numerous configuration bits that allow for combinational or registered modes of operation.

Additionally, these registers can be globally reset or preset and configured as a D or T flip-flop or as a D latch. There are also multiple clock signals, both global and local product term types, configured on a per macrocell basis. Output pin configurations include slew rate limit, bus hold, pull-up, open drain and programmable grounds. A Schmitt-trigger input is available on a per input pin basis. In addition to storing macrocell output states, the macrocell registers may be configured as direct input registers to store signals directly from input pins.

Clocking is available on a global or Function Block basis. Three global clocks are available for all Function Blocks as a synchronous clock source. Macrocell registers can be individually configured to power up to the zero or one state. A global set/reset control line is also available to asynchronously set or reset selected registers during operation. Additional local clock, synchronous clock-enable, asynchronous set/reset and output enable signals can be formed using product terms on a per-macrocell or per-Function Block basis.

A DualEDGE flip-flop feature is also available on a per macrocell basis. This feature allows high performance synchronous operation based on lower frequency clocking to help reduce the total power consumption of the device.

Circuitry has also been included to divide one externally supplied global clock (GCK2) by eight different selections. This yields divide by even and odd clock frequencies.

The use of the clock divide (division by 2) and DualEDGE flip-flop gives the resultant CoolCLOCK feature.

DataGATE is a method to selectively disable inputs of the CPLD that are not of interest during certain points in time.

By mapping a signal to the DataGATE function, lower power can be achieved due to reduction in signal switching.

Another feature that eases voltage translation is I/O banking. Four I/O banks are available on the CoolRunner-II 384 macrocell device that permit easy interfacing to 3.3V, 2.5V, 1.8V, and 1.5V devices.

The CoolRunner-II 384 macrocell CPLD is I/O compatible with various I/O standards (see [Table 1](#)). This device is also 1.5V I/O compatible with the use of Schmitt-trigger inputs.

## RealDigital Design Technology

Xilinx CoolRunner-II CPLDs are fabricated on a 0.18 micron process technology which is derived from leading edge FPGA product development. CoolRunner-II CPLDs employ RealDigital a design technique that makes use of CMOS technology in both the fabrication and design methodology. RealDigital design technology employs a cascade of CMOS gates to implement sum of products instead of traditional sense amplifier methodology. Due to this technology, Xilinx CoolRunner-II CPLDs achieve both high-performance and low power operation.

## Supported I/O Standards

The CoolRunner-II 384 macrocell features LVCMOS, LVTTTL, SSTL and HSTL I/O implementations. See [Table 1](#)

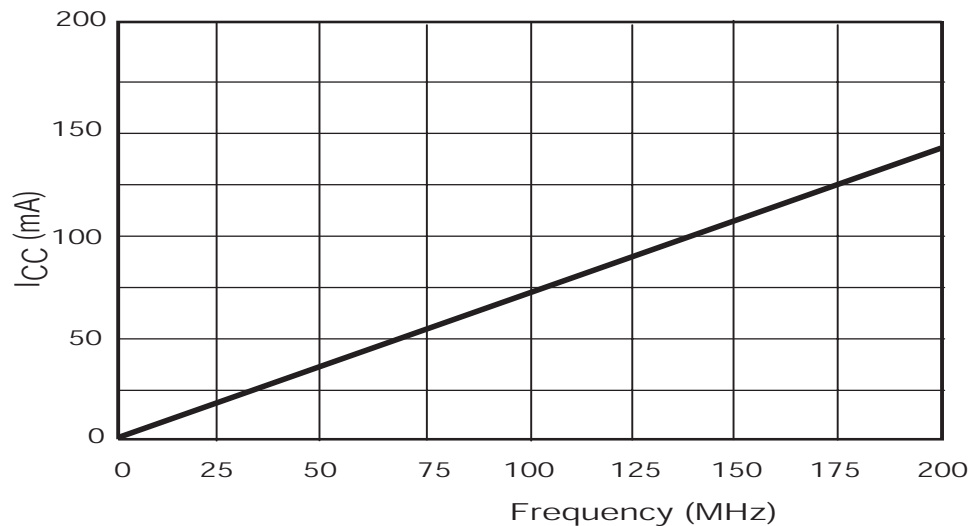
for I/O standard voltages. The LVTTTL I/O standard is a general purpose EIA/JEDEC standard for 3.3V applications that use an LVTTTL input buffer and Push-Pull output buffer. The LVCMOS standard is used in 3.3V, 2.5V, 1.8V applications. Both HSTL and SSTL I/O standards make use of a  $V_{REF}$  pin for JEDEC compliance. CoolRunner-II CPLDs are also 1.5V I/O compatible with the use of Schmitt-trigger inputs.

Table 1: I/O Standards for XC2C384<sup>(1)</sup>

IOSTANDARD Attribute	Output $V_{CCIO}$	Input $V_{CCIO}$	Input $V_{REF}$	Board Termination Voltage $V_{TT}$
LVTTTL	3.3	3.3	N/A	N/A
LVCMOS33	3.3	3.3	N/A	N/A
LVCMOS25	2.5	2.5	N/A	N/A
LVCMOS18	1.8	1.8	N/A	N/A
LVCMOS15 <sup>(2)</sup>	1.5	1.5	N/A	N/A
HSTL_1	1.5	1.5	0.75	0.75
SSTL2_1	2.5	2.5	1.25	1.25
SSTL3_1	3.3	3.3	1.5	1.5

(1) For information on assigning Vref pins, see [XAPP399](#).

(2) LVCMOS15 requires Schmitt-trigger inputs.



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Figure 1:  $I_{CC}$  vs Frequency

Table 2:  $I_{CC}$  vs Frequency (LVCMOS 1.8V  $T_A = 25^\circ\text{C}$ )<sup>(1)</sup>

	Frequency (MHz)								
	0	25	50	75	100	125	150	175	200
Typical $I_{CC}$ (mA)	0.023	17.5	35.03	52.53	70.03	87.53	105.03	122.35	140.03

### Notes:

- 16-bit up/down, Resettable binary counter (one counter per function block).

## Absolute Maximum Ratings (1)

Symbol	Description	Value	Units
$V_{CC}$	Supply voltage relative to ground	-0.5 to 2.0	V
$V_{CCIO}$	Supply voltage for output drivers	-0.5 to 4.0	V
$V_{JTAG}^{(2)}$	JTAG input voltage limits	-0.5 to 4.0	V
$V_{CCAUX}$	JTAG input supply voltage	-0.5 to 4.0	V
$V_{IN}^{(1)}$	Input voltage relative to ground	-0.5 to 4.0	V
$V_{TS}^{(1)}$	Voltage applied to 3-state output	-0.5 to 4.0	V
$T_{STG}^{(3)}$	Storage Temperature (ambient)	-65 to +150	°C
$T_J$	Junction Temperature	+150	°C

**Notes:**

- Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easiest to achieve. During transitions, the device pins may undershoot to -2.0v or overshoot to +4.5V, provided this over or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.
- Valid over commercial temperature range.
- For soldering guidelines and thermal considerations, see the [Device Packaging](#) information on the Xilinx website. For Pb free packages, see [XAPP427](#).

## Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units	
$V_{CC}$	Supply voltage for internal logic and input buffers	Commercial $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$	1.7	1.9	V
		Industrial $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	1.7	1.9	V
$V_{CCIO}$	Supply voltage for output drivers @ 3.3V operation	3.0	3.6	V	
	Supply voltage for output drivers @ 2.5V operation	2.3	2.7	V	
	Supply voltage for output drivers @ 1.8V operation	1.7	1.9	V	
	Supply voltage for output drivers @ 1.5V operation	1.4	1.6	V	
$V_{CCAUX}$	Supply voltage for JTAG programming	1.7	3.6	V	

## DC Electrical Characteristics (Over Recommended Operating Conditions)

Symbol	Parameter	Test Conditions	Typical	Max.	Units
$I_{CCSB}$	Standby current Commercial	$V_{CC} = 1.9\text{V}$ , $V_{CCIO} = 3.6\text{V}$	44	200	$\mu\text{A}$
$I_{CCSB}$	Standby current Industrial	$V_{CC} = 1.9\text{V}$ , $V_{CCIO} = 3.6\text{V}$	79	350	$\mu\text{A}$
$I_{CC}^{(1)}$	Dynamic current	$f = 1\text{ MHz}$		1.5	mA
		$f = 50\text{ MHz}$		45	mA
$C_{JTAG}$	JTAG input capacitance	$f = 1\text{ MHz}$	-	10	pF
$C_{CLK}$	Global clock input capacitance	$f = 1\text{ MHz}$	-	12	pF
$C_{IO}$	I/O capacitance	$f = 1\text{ MHz}$	-	10	pF
$I_{IL}^{(2)}$	Input leakage current	$V_{IN} = 0\text{V}$ or $V_{CCIO}$ to 3.9V	-	+/-1	$\mu\text{A}$
$I_{IH}^{(2)}$	I/O High-Z leakage	$V_{IN} = 0\text{V}$ or $V_{CCIO}$ to 3.9V	-	+/-1	$\mu\text{A}$

**Notes:**

- 16-bit up/down, Resettable binary counter (one counter per function block).
- See Quality and Reliability section of the CoolRunner-II family data sheet.

## LVC MOS and LV TTL 3.3V DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Max.	Units
$V_{CCIO}$	Input source voltage		3.0	3.6	V
$V_{IH}$	High level input voltage		2	3.9	V
$V_{IL}$	Low level input voltage		-0.3	0.8	V
$V_{OH}$	High level output voltage	$I_{OH} = -8\text{ mA}, V_{CCIO} = 3\text{V}$	$V_{CCIO} - 0.4\text{V}$	-	V
		$I_{OH} = -0.1\text{ mA}, V_{CCIO} = 3\text{V}$	$V_{CCIO} - 0.2\text{V}$	-	V
$V_{OL}$	Low level output voltage	$I_{OL} = 8\text{ mA}, V_{CCIO} = 3\text{V}$	-	0.4	V
		$I_{OL} = 0.1\text{ mA}, V_{CCIO} = 3\text{V}$	-	0.2	V

## LVC MOS 2.5V DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Max.	Units
$V_{CCIO}$	Input source voltage		2.3	2.7	V
$V_{IH}$	High level input voltage		1.7	$V_{CCIO} + 0.3^{(1)}$	V
$V_{IL}$	Low level input voltage		-0.3	0.7	V
$V_{OH}$	High level output voltage	$I_{OH} = -8\text{ mA}, V_{CCIO} = 2.3\text{V}$	$V_{CCIO} - 0.4\text{V}$	-	V
		$I_{OH} = -0.1\text{ mA}, V_{CCIO} = 2.3\text{V}$	$V_{CCIO} - 0.2\text{V}$	-	V
$V_{OL}$	Low level output voltage	$I_{OL} = 8\text{ mA}, V_{CCIO} = 2.3\text{V}$	-	0.4	V
		$I_{OL} = 0.1\text{ mA}, V_{CCIO} = 2.3\text{V}$	-	0.2	V

(1) The  $V_{IH}$  Max value represents the JEDEC specification for LVC MOS25. The CoolRunner-II input buffer can tolerate up to 3.9V without physical damage.

## LVC MOS 1.8V DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Max.	Units
$V_{CCIO}$	Input source voltage		1.7	1.9	V
$V_{IH}$	High level input voltage		$0.65 \times V_{CCIO}$	$V_{CCIO} + 0.3^{(1)}$	V
$V_{IL}$	Low level input voltage		-0.3	$0.35 \times V_{CCIO}$	V
$V_{OH}$	High level output voltage	$I_{OH} = -8\text{ mA}, V_{CCIO} = 1.7\text{V}$	$V_{CCIO} - 0.45$	-	V
		$I_{OH} = -0.1\text{ mA}, V_{CCIO} = 1.7\text{V}$	$V_{CCIO} - 0.2$	-	V
$V_{OL}$	Low level output voltage	$I_{OL} = 8\text{ mA}, V_{CCIO} = 1.7\text{V}$	-	0.45	V
		$I_{OL} = 0.1\text{ mA}, V_{CCIO} = 1.7\text{V}$	-	0.2	V

(1) The  $V_{IH}$  Max value represents the JEDEC specification for LVC MOS18. The CoolRunner-II input buffer can tolerate up to 3.9V without physical damage.

## LVC MOS 1.5V DC Voltage Specifications<sup>(1)</sup>

Symbol	Parameter	Test Conditions	Min.	Max.	Units
$V_{CCIO}$	Input source voltage		1.4	1.6	V
$V_{T+}$	Input hysteresis threshold voltage		$0.5 \times V_{CCIO}$	$0.8 \times V_{CCIO}$	V
$V_{T-}$			$0.2 \times V_{CCIO}$	$0.5 \times V_{CCIO}$	V
$V_{OH}$	High level output voltage	$I_{OH} = -8\text{ mA}, V_{CCIO} = 1.4\text{V}$	$V_{CCIO} - 0.45$	-	V
		$I_{OH} = -0.1\text{ mA}, V_{CCIO} = 1.4\text{V}$	$V_{CCIO} - 0.2$	-	V

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V <sub>OL</sub>	Low level output voltage	I <sub>OL</sub> = 8 mA, V <sub>CCIO</sub> = 1.4V	-	0.4	V
		I <sub>OL</sub> = 0.1 mA, V <sub>CCIO</sub> = 1.4V	-	0.2	V

**Notes:**

- Hysteresis used on 1.5V inputs.

## Schmitt Trigger Input DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V <sub>CCIO</sub>	Input source voltage		1.4	3.9	V
V <sub>T+</sub>	Input hysteresis threshold voltage		0.5 x V <sub>CCIO</sub>	0.8 x V <sub>CCIO</sub>	V
V <sub>T-</sub>			0.2 x V <sub>CCIO</sub>	0.5 x V <sub>CCIO</sub>	V

## SSTL2-1 DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Units
V <sub>CCIO</sub>	Input source voltage	-	2.3	2.5	2.7	V
V <sub>REF(1)</sub>	Input reference voltage	-	1.15	1.25	1.35	V
V <sub>TT(2)</sub>	Termination voltage	-	V <sub>REF</sub> - 0.04	1.25	V <sub>REF</sub> + 0.04	V
V <sub>IH</sub>	High level input voltage	-	V <sub>REF</sub> + 0.18	-	3.9	V
V <sub>IL</sub>	Low level input voltage	-	-0.3	-	V <sub>REF</sub> - 0.18	V
V <sub>OH</sub>	High level output voltage	I <sub>OH</sub> = -8 mA, V <sub>CCIO</sub> = 2.3V	V <sub>CCIO</sub> - 0.62	-	-	V
V <sub>OL</sub>	Low level output voltage	I <sub>OL</sub> = 8 mA, V <sub>CCIO</sub> = 2.3V	-	-	0.54	V

**Notes:**

- V<sub>REF</sub> should track the variations in V<sub>CCIO</sub>, also peak to peak AC noise on V<sub>REF</sub> may not exceed ±2% V<sub>REF</sub>.
- V<sub>TT</sub> of transmitting device must track V<sub>REF</sub> of receiving devices.

## SSTL3-1 DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Units
V <sub>CCIO</sub>	Input source voltage	-	3.0	3.3	3.6	V
V <sub>REF(1)</sub>	Input reference voltage	-	1.3	1.5	1.7	V
V <sub>TT(2)</sub>	Termination voltage	-	V <sub>REF</sub> - 0.05	1.5	V <sub>REF</sub> + 0.05	V
V <sub>IH</sub>	High level input voltage	-	V <sub>REF</sub> + 0.2	-	V <sub>CCIO</sub> + 0.3	V
V <sub>IL</sub>	Low level input voltage	-	-0.3	-	V <sub>REF</sub> - 0.2	V
V <sub>OH</sub>	High level output voltage	I <sub>OH</sub> = -8 mA, V <sub>CCIO</sub> = 3V	V <sub>CCIO</sub> - 1.1	-	-	V
V <sub>OL</sub>	Low level output voltage	I <sub>OL</sub> = 8 mA, V <sub>CCIO</sub> = 3V	-	-	0.7	V

**Notes:**

- V<sub>REF</sub> should track the variations in V<sub>CCIO</sub>, also peak to peak AC noise on V<sub>REF</sub> may not exceed ±2% V<sub>REF</sub>.
- V<sub>TT</sub> of transmitting device must track V<sub>REF</sub> of receiving devices.

## HSTL1 DC Voltage Specifications

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Units
V <sub>CCIO</sub>	Input source voltage		1.4	1.5	1.6	V
V <sub>REF(1)</sub>	Input reference voltage		0.68	0.75	0.90	V
V <sub>TT(2)</sub>	Termination voltage		-	V <sub>CCIO</sub> * 0.5	-	V
V <sub>IH</sub>	High level input voltage		V <sub>REF</sub> + 0.1	-	1.9	V

Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Units
$V_{IL}$	Low level input voltage		-0.3	-	$V_{REF} - 0.1$	V
$V_{OH}$	High level output voltage	$I_{OH} = -8 \text{ mA}, V_{CCIO} = 1.4\text{V}$	$V_{CCIO} - 0.4$	-	-	V
$V_{OL}$	Low level output voltage	$I_{OL} = 8 \text{ mA}, V_{CCIO} = 1.4\text{V}$	-	-	0.4	V

## AC Electrical Characteristics Over Recommended Operating Conditions

Symbol	Parameter	-7		-10		Units
		Min.	Max.	Min.	Max.	
T <sub>PD1</sub>	Propagation delay single p-term	-	7.1	-	9.2	ns
T <sub>PD2</sub>	Propagation delay OR array	-	7.5	-	10.0	ns
T <sub>SUD</sub>	Direct input register set-up time	4.1	-	4.2	-	ns
T <sub>SU1</sub>	Setup time fast (single p-term)	3.2	-	3.3	-	ns
T <sub>SU2</sub>	Setup time (OR array)	3.6	-	4.1	-	ns
T <sub>HD</sub>	Direct input register hold time	0.0	-	0.0	-	ns
T <sub>H</sub>	Hold time (OR array or p-term)	0.0	-	0.0	-	ns
T <sub>CO</sub>	Clock to output	-	5.3	-	7.9	ns
F <sub>TOGGLE</sub> <sup>(1)</sup>	Internal toggle rate	-	350	-	166	MHz
F <sub>SYSTEM1</sub> <sup>(2)</sup>	Maximum system frequency	-	217	-	125	MHz
F <sub>SYSTEM2</sub> <sup>(2)</sup>	Maximum system frequency	-	200	-	114	MHz
F <sub>EXT1</sub> <sup>(3)</sup>	Maximum external frequency	-	118	-	89	MHz
F <sub>EXT2</sub> <sup>(3)</sup>	Maximum external frequency	-	112	-	83	MHz
T <sub>PSUD</sub>	Direct input register p-term clock setup time	2.3	-	2.5	-	ns
T <sub>PSU1</sub>	P-term clock setup time (single p-term)	1.4	-	1.9	-	ns
T <sub>PSU2</sub>	P-term clock setup time (OR array)	1.8	-	2.7	-	ns
T <sub>PHD</sub>	Direct input register p-term clock hold time	0.9	-	0.4	-	ns
T <sub>PH</sub>	P-term clock hold	1.8	-	1.3	-	ns
T <sub>PCO</sub>	P-term clock to output	-	7.1	-	9.3	ns
T <sub>OE</sub> /T <sub>OD</sub>	Global OE to output enable/disable	-	6.0	-	9.2	ns
T <sub>POE</sub> /T <sub>POD</sub>	P-term OE to output enable/disable	-	7.0	-	10.2	ns
T <sub>MOE</sub> /T <sub>MOD</sub>	Macrocell driven OE to output enable/disable	-	8.0	-	12.5	ns
T <sub>PAO</sub>	P-term set/reset to output valid	-	7.5	-	11.6	ns
T <sub>AO</sub>	Global set/reset to output valid	-	6.0	-	11.5	ns
T <sub>SUEC</sub>	Register clock enable setup time	3.3	-	3.4	-	ns
T <sub>HEC</sub>	Register clock enable hold time	0.0	-	0.0	-	ns
T <sub>CW</sub>	Global clock pulse width High or Low	1.4	-	3.0	-	ns
T <sub>PCW</sub>	P-term pulse width High or Low	7.5	-	10.0	-	ns
T <sub>APRPW</sub>	Asynchronous preset/reset pulse width (High or Low)	7.5	-	10.0	-	ns
T <sub>DGSU</sub>	Set-up before DataGATE latch assertion	0.0	-	0.0	-	ns
T <sub>DGH</sub>	Hold to DataGATE latch assertion	4.0	-	6.0	-	ns
T <sub>DGR</sub>	DataGATE recovery to new data	-	8.5	-	11.0	ns
T <sub>DGW</sub>	DataGATE low pulse width	3.0	-	5.0	-	ns
T <sub>CDRSU</sub>	CDRST setup time before falling edge GCLK2	1.7	-	2.5	-	ns
T <sub>CDRH</sub>	CDRST hold time before falling edge GCLK2	0.0	-	0.0	-	ns
T <sub>CONFIG</sub>	Configuration time	-	200	-	200	μs

### Notes:

1. F<sub>TOGGLE</sub> is the maximum frequency of a T flip-flop can reliably toggle (see CoolRunner-II family data sheet).
2. F<sub>SYSTEM1</sub> (1/T<sub>CYCLE</sub>) is the internal operating frequency for a device with 16-bit Resettable binary counter through one p-term per macrocell while F<sub>SYSTEM2</sub> is through the OR array (one counter per function block)
3. F<sub>EXT1</sub>(1/T<sub>SU1</sub>+T<sub>CO</sub>) is the maximum external frequency using one p-term while F<sub>EXT2</sub> is through the OR array
4. Typical configuration current during T<sub>CONFIG</sub> is 25 mA.

## Internal Timing Parameters

Symbol	Parameter <sup>(1)</sup>	-7		-10		Units
		Min.	Max.	Min.	Max.	
<b>Buffer Delays</b>						
T <sub>IN</sub>	Input buffer delay	-	3.1	-	3.8	ns
T <sub>DIN</sub>	Direct data register input delay	-	4.5	-	5.5	ns
T <sub>GCK</sub>	Global Clock buffer delay	-	2.1	-	3.3	ns
T <sub>GSR</sub>	Global set/reset buffer delay	-	2.4	-	4.6	ns
T <sub>GTS</sub>	Global 3-state buffer delay	-	2.9	-	3.7	ns
T <sub>OUT</sub>	Output buffer delay	-	3.0	-	3.9	ns
T <sub>EN</sub>	Output buffer enable/disable delay	-	3.1	-	5.5	ns
<b>P-term Delays</b>						
T <sub>CT</sub>	Control term delay	-	0.8	-	0.9	ns
T <sub>LOGI1</sub>	Single P-term delay adder	-	0.5	-	0.8	ns
T <sub>LOGI2</sub>	Multiple P-term delay adder	-	0.4	-	0.8	ns
<b>Macrocell Delay</b>						
T <sub>PDI</sub>	Input to output valid	-	0.5	-	0.7	ns
T <sub>SUI</sub>	Setup before clock	1.7	-	2.0	-	ns
T <sub>HI</sub>	Hold after clock	0.0	-	0.0	-	ns
T <sub>ECSU</sub>	Enable clock setup time	1.5	-	2.0	-	ns
T <sub>ECHO</sub>	Enable clock hold time	0.0	-	0.0	-	ns
T <sub>COI</sub>	Clock to output valid	-	0.2	-	0.7	ns
T <sub>AOI</sub>	Set/reset to output valid	-	0.6	-	3.0	ns
T <sub>CDBL</sub>	Clock doubler delay	-	0	-	0	ns
<b>Feedback Delays</b>						
T <sub>F</sub>	Feedback delay	-	2.2	-	4.5	ns
T <sub>OEM</sub>	Macrocell to global OE delay	-	2.6	-	3.0	ns
<b>I/O Standard Time Adder Delays 1.5V CMOS</b>						
T <sub>HYS15</sub>	Hysteresis input adder	-	3.0	-	4.0	ns
T <sub>OUT15</sub>	Output adder	-	0.8	-	1.0	ns
T <sub>SLEW15</sub>	Output slew rate adder	-	4.0	-	4.0	ns
<b>I/O Standard Time Adder Delays 1.8V CMOS</b>						
T <sub>HYS18</sub>	Hysteresis input adder	-	2.0	-	4.0	ns
T <sub>OUT18</sub>	Output adder	-	0.0	-	0.0	ns
T <sub>SLEW</sub>	Output slew rate adder	-	2.0	-	4.0	ns
<b>I/O Standard Time Adder Delays 2.5V CMOS</b>						
T <sub>IN25</sub>	Standard input adder	-	0.6	-	1.0	ns
T <sub>HYS25</sub>	Hysteresis input adder	-	1.5	-	3.0	ns
T <sub>OUT25</sub>	Output adder	-	0.8	-	3.0	ns
T <sub>SLEW25</sub>	Output slew rate adder	-	3.0	-	4.0	ns

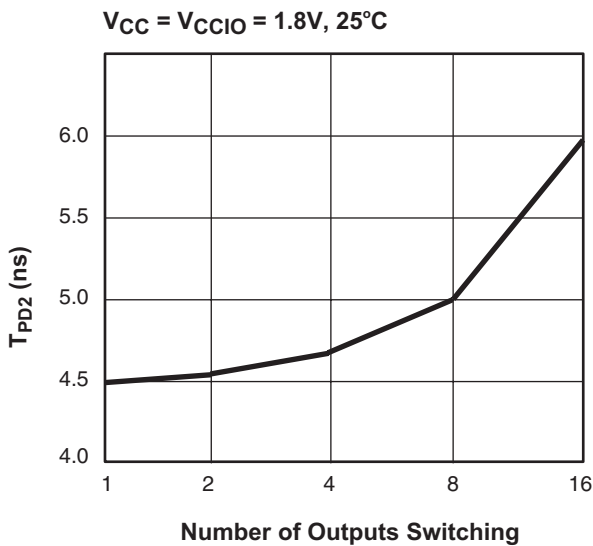
## Internal Timing Parameters (Continued)

Symbol	Parameter <sup>(1)</sup>	-7		-10		Units
		Min.	Max.	Min.	Max.	
<b>I/O Standard Time Adder Delays 3.3V CMOS/TTL</b>						
$T_{IN33}$	Standard input adder	-	0.5	-	2.0	ns
$T_{HYS33}$	Hysteresis input adder	-	1.2	-	3.0	ns
$T_{OUT33}$	Output adder	-	1.2	-	3.0	ns
$T_{SLEW33}$	Output slew rate adder	-	3.0	-	4.0	ns
<b>I/O Standard Time Adder Delays HSTL, SSTL</b>						
SSTL2-1	Input adder to $T_{IN}$ , $T_{DIN}$ , $T_{GCK}$ , $T_{GSR}$ , $T_{GTS}$	-	0.8	-	2.5	ns
	Output adder to $T_{OUT}$	-	-0.5	-	0.0	ns
SSTL3-1	Input adder to $T_{IN}$ , $T_{DIN}$ , $T_{GCK}$ , $T_{GSR}$ , $T_{GTS}$	-	0.8	-	2.5	ns
	Output adder to $T_{OUT}$	-	-0.50	-	0.00	ns
HSTL-1	Input adder to $T_{IN}$ , $T_{DIN}$ , $T_{GCK}$ , $T_{GSR}$ , $T_{GTS}$	-	1.0	-	2.5	ns
	Output adder to $T_{OUT}$	-	0.0	-	0.0	ns

**Notes:**

1. 1.5 ns input pin signal rise/fall.

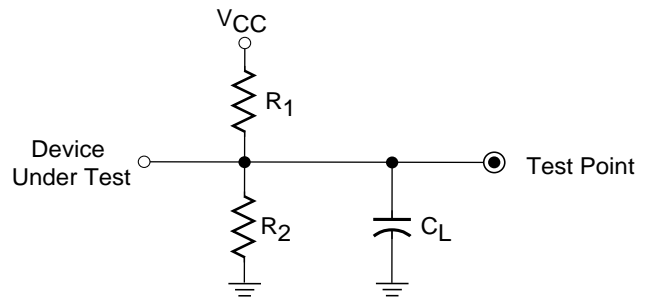
## Switching Characteristics



DS095\_02\_053103

Figure 2: Derating Curve for  $T_{PD}$

## Switching Test Conditions



Output Type	$R_1$	$R_2$	$C_L$
LVTTL33	268Ω	235Ω	35 pF
LVC MOS33	275Ω	275Ω	35 pF
LVC MOS25	188Ω	188Ω	35 pF
LVC MOS18	112.5Ω	112.5Ω	35 pF
LVC MOS15	150Ω	150Ω	35 pF

**Notes:**

1.  $C_L$  includes test fixtures and probe capacitance.
2. 1.5 nsec maximum rise/fall times on inputs.

DS092\_03\_092302

Figure 3: AC Load Circuit

## Typical I/V Output Curves

The I/V curve illustrates the nominal amount of current that an I/O can source/sink at different voltage levels.

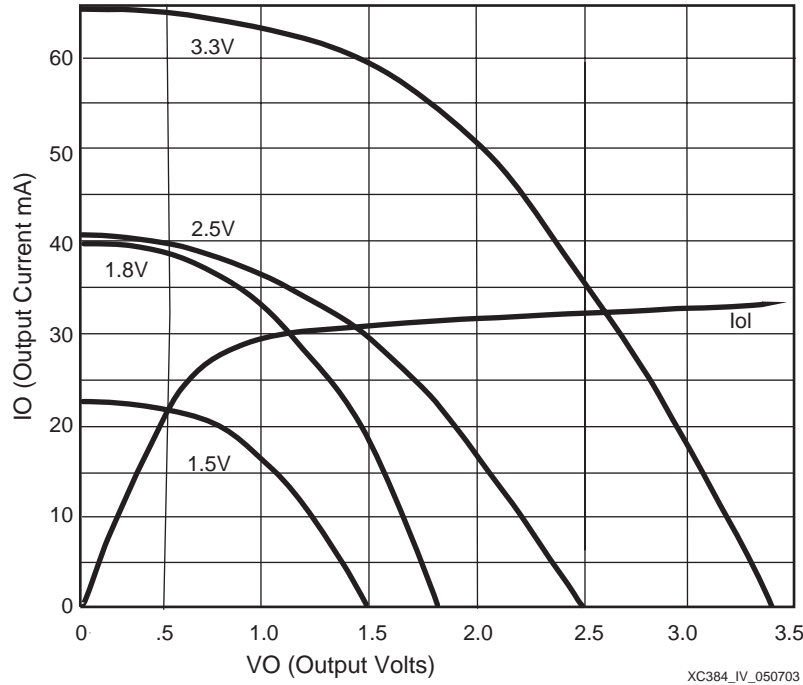


Figure 4: Typical I/V Curves for XC2C384

## Pin Descriptions

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
1	1	-	2	B3	C3	2
1	2	-	208	B4	A1	2
1(GSR)	3	143	206	C4	A2	2
1	4	142	205	A2	B3	2
1	5	-	-	-	C4	2
1	6	-	-	-	-	-
1	7	-	-	-	-	-
1	8	-	-	-	-	-
1	9	-	-	-	-	-
1	10	-	-	-	-	-
1	11	-	-	-	-	-
1	12	140	203	C5	B4	2
1	13	139	202	A3	C5	2
1	14	-	201	-	B5	2
1	15	-	200	E7	A3	2
1	16	-	199	-	A4	2

## Pin Descriptions (Continued)

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
2(GTS2)	1	2	3	D3	D3	2
2	2	-	4	C3	B2	2
2(GTS3)	3	3	5	E3	B1	2
2	4	4	6	B2	C2	2
2(GTS0)	5	5	7	D4	C1	2
2	6	-	-	-	-	-
2	7	-	-	-	-	-
2	8	-	-	-	-	-
2	9	-	-	-	-	-
2	10	-	-	-	-	-
2	11	-	-	-	-	-
2	12	-	-	A1	D2	2
2	13	-	8	D2	F4	2
2	14	-	-	C2	E2	2
2(GTS1)	15	6	9	E5	E1	2
2	16	7	10	B1	F2	2

**Pin Descriptions (Continued)**

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
3	1	-	198	A4	D6	2
3	2	-	197	-	A5	2
3	3	138	196	C6	C6	2
3	4	137	195	B5	B6	2
3	5	136	194	D6	A6	2
3	6	-	-	-	-	-
3	7	-	-	-	-	-
3	8	-	-	-	-	-
3	9	-	-	-	-	-
3	10	-	-	-	-	-
3	11	-	-	-	-	-
3	12	135	193	A5	D7	2
3	13	-	192	E8	C7	2
3	14	-	-	B6	B7	2
3	15	-	191	C7	A7	2
3	16	134	-	A6	D8	2
4	1	9	12	E4	G4	2
4	2	10	-	C1	G3	2
4	3	11	14	E2	G2	2
4	4	12	15	F2	G1	2
4	5	-	16	E6	H4	2
4	6	-	-	-	-	-
4	7	-	-	-	-	-
4	8	-	-	-	-	-
4	9	-	-	-	-	-
4	10	-	-	-	-	-
4	11	-	-	-	-	-
4	12	-	17	F3	H3	2
4	13	-	18	D1	H2	2
4	14	-	19	G4	H1	2
4	15	-	20	E1	J3	2
4	16	-	21	G3	J2	2

**Pin Descriptions (Continued)**

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
5	1	-	-	D7	C8	2
5	2	133	-	B7	B8	2
5	3	132	-	E9	A8	2
5	4	-	189	A7	D9	2
5	5	-	188	D8	C9	2
5	6	-	-	-	-	-
5	7	-	-	-	-	-
5	8	-	-	-	-	-
5	9	-	-	-	-	-
5	10	-	-	-	-	-
5	11	-	-	-	-	-
5	12	-	187	B8	B9	2
5	13	131	186	C8	A9	2
5	14	-	185	A8	D10	2
5	15	130	184	E11	C10	2
5	16	129	183	E10	B10	2
6	1	-	22	G2	J1	2
6	2	13	-	F5	K3	2
6	3	14	23	F1	K2	2
6	4	15	-	G5	K1	2
6	5	-	-	H2	L1	2
6	6	-	-	-	-	-
6	7	-	-	-	-	-
6	8	-	-	-	-	-
6	9	-	-	-	-	-
6	10	-	-	-	-	-
6	11	-	-	-	-	-
6	12	-	-	H4	L3	2
6	13	16	-	G1	L2	2
6	14	17	-	H3	M1	2
6	15	-	-	H1	M2	2
6	16	18	25	H5	M3	2

## Pin Descriptions (Continued)

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
7(CDRST)	1	35	51	P2	AB2	1
7	2	-	50	N3	AA2	1
7	3	-	49	R1	AA1	1
7	4	34	48	N4	W4	1
7	5	33	47	N2	Y2	1
7	6	-	-	-	-	-
7	7	-	-	-	-	-
7	8	-	-	-	-	-
7	9	-	-	-	-	-
7	10	-	-	-	-	-
7	11	-	-	-	-	-
7(GCK1)	12	32	46	M3	Y1	1
7	13	-	-	P1	W2	1
7	14	31	45	M4	W1	1
7(GCK0)	15	30	44	M2	V3	1
7	16	-	43	L3	U4	1
8	1	-	54	P4	Y4	1
8(GCK2)	2	38	55	P5	AB3	1
8	3	-	56	R2	AA4	1
8	4	-	57	T1	Y5	1
8(DGE)	5	39	58	T2	AA5	1
8	6	-	-	-	-	-
8	7	-	-	-	-	-
8	8	-	-	-	-	-
8	9	-	-	-	-	-
8	10	-	-	-	-	-
8	11	-	-	-	-	-
8	12	-	-	-	AB4	1
8	13	40	60	N5	W6	1
8	14	41	-	-	AB5	1
8	15	42	61	R4	Y6	1
8	16	43	-	M5	AA6	1

## Pin Descriptions (Continued)

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
9	1	-	41	N1	V2	1
9	2	28	40	L4	V1	1
9	3	-	39	M1	U3	1
9	4	-	38	L5	U2	1
9	5	-	37	K4	U1	1
9	6	-	-	-	-	-
9	7	-	-	-	-	-
9	8	-	-	-	-	-
9	9	-	-	-	-	-
9	10	-	-	-	-	-
9	11	--	-	-	-	-
9	12	-	36	L2	T4	1
9	13	-	35	K3	T3	1
9	14	-	34	L1	T2	1
9	15	26	32	-	T1	1
9	16	25	-	-	R4	1
10	1	44	62	-	AB6	1
10	2	45	63	R5	W7	1
10	3	-	-	-	Y7	1
10	4	46	64	R6	AA7	1
10	5	-	65	N6	AB7	1
10	6	-	-	-	-	-
10	7	-	-	-	-	-
10	8	-	-	-	-	-
10	9	-	-	-	-	-
10	10	-	-	-	-	-
10	11	-	-	-	-	-
10	12	-	66	R3	W8	1
10	13	-	67	M6	Y8	1
10	14	48	69	-	AA8	1
10	15	49	70	T3	AB8	1
10	16	50	71	P6	Y9	1

**Pin Descriptions (Continued)**

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
11	1	24	31	K5	R3	1
11	2	23	-	K2	R2	1
11	3	22	30	J4	R1	1
11	4	21	29	K1	P4	1
11	5	20	28	J3	P3	1
11	6	-	-	-	-	-
11	7	-	-	-	-	-
11	8	-	-	-	-	-
11	9	-	-	-	-	-
11	10	-	-	-	-	-
11	11	-	-	-	-	-
11	12	19	27	J2	P2	1
11	13	-	-	J5	P1	1
11	14	-	-	J1	N3	1
11	15	-	-	-	N2	1
11	16	-	-	-	N1	1
12	1	51	72	T4	AA9	1
12	2	52	73	P7	AB9	1
12	3	53	74	T5	W10	1
12	4	-	75	N7	Y10	1
12	5	54	76	R7	AA10	1
12	6	-	-	-	-	-
12	7	-	-	-	-	-
12	8	-	-	-	-	-
12	9	-	-	-	-	-
12	10	-	-	-	-	-
12	11	-	-	-	-	-
12	12	-	77	M7	AB10	1
12	13	-	-	-	AB11	1
12	14	-	-	-	W11	1
12	15	-	-	-	AA11	1
12	16	-	78	T6	Y11	1

**Pin Descriptions (Continued)**

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
13	1	-	-	B16	C21	4
13	2	-	-	G11	C20	4
13	3	112	160	C14	B22	4
13	4	113	161	B15	B21	4
13	5	-	-	A16	A22	4
13	6	-	-	-	-	-
13	7	-	-	-	-	-
13	8	-	-	-	-	-
13	9	-	-	-	-	-
13	10	-	-	-	-	-
13	11	-	-	-	-	-
13	12	114	162	B13	A21	4
13	13	115	163	B14	B20	4
13	14	-	-	C13	C19	4
13	15	-	-	A15	B19	4
13	16	-	164	C12	C18	4
14	1	111	159	D14	D19	4
14	2	110	158	C15	D20	4
14	3	107	155	G12	C22	4
14	4	106	154	D15	D21	4
14	5	105	153	E14	D22	4
14	6	-	-	-	-	-
14	7	-	-	-	-	-
14	8	-	-	-	-	-
14	9	-	-	-	-	-
14	10	-	-	-	-	-
14	11	-	-	-	-	-
14	12	-	-	C16	E20	4
14	13	104	152	F14	F19	4
14	14	-	151	D16	E21	4
14	15	-	-	F13	E22	4
14	16	-	150	E15	F20	4

### Pin Descriptions (Continued)

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
15	1	-	-	B12	B18	4
15	2	116	165	D13	A19	4
15	3	-	166	A14	D17	4
15	4	-	-	E13	A18	4
15	5	117	167	A13	C17	4
15	6	-	-	-	-	-
15	7	-	-	-	-	-
15	8	-	-	-	-	-
15	9	-	-	-	-	-
15	10	-	-	-	-	-
15	11	-	-	-	-	-
15	12	-	168	C11	B17	4
15	13	118	169	A12	D16	4
15	14	-	-	B11	C16	4
15	15	119	170	D11	B16	4
15	16	120	171	A11	D15	4
16	1	103	149	G13	F21	4
16	2	-	148	F15	F22	4
16	3	102	147	G14	G19	4
16	4	-	146	E16	G20	4
16	5	-	-	H12	G21	4
16	6	-	-	-	-	-
16	7	-	-	-	-	-
16	8	-	-	-	-	-
16	9	-	-	-	-	-
16	10	-	-	-	-	-
16	11	-	-	-	-	-
16	12	-	145	F16	G22	4
16	13	-	-	H16	H19	4
16	14	101	144	-	H21	4
16	15	-	-	-	H22	4
16	16	100	143	-	J19	4

### Pin Descriptions (Continued)

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
17	1	-	173	D10	C15	4
17	2	121	174	B10	B15	4
17	3	-	175	E12	D14	4
17	4	-	-	-	B14	4
17	5	-	-	F12	C13	4
17	6	-	-	-	-	-
17	7	-	-	-	-	-
17	8	-	-	-	-	-
17	9	-	-	-	-	-
17	10	-	-	-	-	-
17	11	-	-	-	-	-
17	12	124	178	B9	A13	4
17	13	125	179	C9	D12	4
17	14	126	180	C10	C12	4
17	15	-	-	A9	B11	4
17	16	128	182	D9	A10	4
18	1	-	-	G15	J20	4
18	2	-	142	-	J21	4
18	3	98	140	-	J22	4
18	4	97	139	H13	K19	4
18	5	96	138	G16	K20	4
18	6	-	-	-	-	-
18	7	-	-	-	-	-
18	8	-	-	-	-	-
18	9	-	-	-	-	-
18	10	-	-	-	-	-
18	11	-	-	-	-	-
18	12	95	137	H14	K21	4
18	13	94	136	H15	K22	4
18	14	-	135	J12	L19	4
18	15	-	134	K12	L20	4
18	16	-	-	J16	L21	4

**Pin Descriptions (Continued)**

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
19	1	-	103	P13	AA22	3
19	2	-	-	P14	Y20	3
19	3	74	106	P15	Y21	3
19	4	75	107	R15	W20	3
19	5	76	108	T16	W21	3
19	6	-	-	-	-	-
19	7	-	-	-	-	-
19	8	-	-	-	-	-
19	9	-	-	-	-	-
19	10	-	-	-	-	-
19	11	-	-	-	-	-
19	12	77	109	N14	Y22	3
19	13	78	110	R16	W22	3
19	14	79	111	N15	V20	3
19	15	-	112	M15	V21	3
19	16	-	113	M13	U19	3
20	1	71	102	R13	AB22	3
20	2	70	101	N13	AA21	3
20	3	69	100	R14	AB21	3
20	4	68	99	T15	W19	3
20	5	66	97	R12	AA20	3
20	6	-	-	-	-	-
20	7	-	-	-	-	-
20	8	-	-	-	-	-
20	9	-	-	-	-	-
20	10	-	-	-	-	-
20	11	-	-	-	-	-
20	12	-	-	T14	Y18	3
20	13	64	95	N11	AA19	3
20	14	-	-	P11	Y17	3
20	15	-	-	M11	AA18	3
20	16	-	-	T13	AB18	3

**Pin Descriptions (Continued)**

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
21	1	80	114	P16	V22	3
21	2	-	115	N16	U20	3
21	3	81	116	L14	U21	3
21	4	-	117	M14	U22	3
21	5	-	118	L15	T19	3
21	6	-	-	-	-	-
21	7	-	-	-	-	-
21	8	-	-	-	-	-
21	9	-	-	-	-	-
21	10	-	-	-	-	-
21	11	-	-	-	-	-
21	12	82	119	L13	T20	3
21	13	-	120	M12	T21	3
21	14	-	121	M16	T22	3
21	15	83	122	K14	R21	3
21	16	-	123	-	R22	3
22	1	-	-	N10	AA17	3
22	2	61	91	T12	AB17	3
22	3	-	90	P10	Y16	3
22	4	-	89	T11	AA16	3
22	5	-	-	R10	AB16	3
22	6	-	-	-	-	-
22	7	-	-	-	-	-
22	8	-	-	-	-	-
22	9	-	-	-	-	-
22	10	-	-	-	-	-
22	11	-	-	-	-	-
22	12	60	88	M10	W15	3
22	13	-	87	T10	Y15	3
22	14	59	86	M9	AA15	3
22	15	-	85	R9	AB15	3
22	16	-	-	P9	W14	3

## Pin Descriptions (Continued)

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
23	1	-	-	L16	P20	3
23	2	-	125	K15	P21	3
23	3	85	126	L12	N19	3
23	4	86	127	-	N21	3
23	5	87	-	K16	N22	3
23	6	-	-	-	-	-
23	7	-	-	-	-	-
23	8	-	-	-	-	-
23	9	-	-	-	-	-
23	10	-	-	-	-	-
23	11	-	-	-	-	-
23	12	88	128	J14	M22	3
23	13	91	-	J15	M19	3
23	14	92	131	J13	M20	3
23	15	-	-	-	M21	3
23	16	-	-	-	L22	3

## Pin Descriptions (Continued)

Function Block	Macro-cell	TQ144	PQ208	FT256	FG324	I/O Bank
24	1	-	-	N9	Y14	3
24	2	58	84	T9	AA14	3
24	3	-	-	-	AB14	3
24	4	-	83	-	Y13	3
24	5	-	82	M8	AA13	3
24	6	-	-	-	-	-
24	7	-	-	-	-	-
24	8	-	-	-	-	-
24	9	-	-	-	-	-
24	10	-	-	-	-	-
24	11	-	-	-	-	-
24	12	57	-	T8	AB13	3
24	13	-	-	P8	W12	3
24	14	56	80	R8	Y12	3
24	15	-	-	T7	AA12	3
24	16	-	-	N8	AB12	3

### Notes:

1. GTS = global output enable, GSR = global reset/set, GCK = global clock, CDRST = clock divide reset, DGE = DataGATE enable.
2. GCK, GSR, and GTS pins can also be used for general purpose I/O.

## XC2C384 JTAG, Power/Ground, No Connect Pins and Total User I/O

Pin Type	TQ144	PQ208	FT256	FG324
TCK	67	98	P12	Y19
TDI	63	94	R11	AB19
TDO	122	176	A10	C14
TMS	65	96	N12	AB20
V <sub>CCAUX</sub> (JTAG supply voltage)	8	11	F4	F1
Power internal (V <sub>CC</sub> )	1, 37, 84	1, 53, 124	P3, K13, D12, D5	AA3, N20, A20, D4, E3
Power Bank 1 I/O (V <sub>CCI01</sub> )	27, 55	33, 59, 79	J6, K6, L7, L8	M9, N9, P10, P11
Power Bank 2 I/O (V <sub>CCI02</sub> )	141	26, 204	F7, F8, G6, H6	J10, J11, K9, L9
Power Bank 3 I/O (V <sub>CCI03</sub> )	73, 93	92, 105, 132	J11, K11, L10, L9	M14, N14, P12, P13
Power Bank 4 I/O (V <sub>CCI04</sub> )	109, 127	133, 157, 172, 181	F10, F9, H11	J12, J13, K14, L14

**XC2C384 JTAG, Power/Ground, No Connect Pins and Total User I/O (Continued)**

Pin Type	TQ144	PQ208	FT256	FG324
Ground	29, 36, 47, 62, 72, 89, 90, 99, 108, 123, 144	13, 24, 42, 52, 68, 81, 93, 104, 129, 130, 141, 156, 177, 190, 207	F11, F6, G10, G7, G8, G9, H10, H7, H8, H9, J10, J7, J8, J9, K10, K7, K8, K9, L11, L6	D5, D18, E4, E19, J9, J14, K10, K11, K12, K13, L10, L11, L12, L13, M10, M11, M12, M13, N10, N11, N12, N13, P9, P14, V4, V19, W5, W18
No connects	-	-		A11,A12,A14,A15,A16,A17,B 12,B13,C11,D1,D11,D13,F3,H 20,J4,K4,L4,M4,N4,P19,P22, R19,R20,W3,W9,W13,W16,W 17,Y3,AB1
Total user I/O (includes dual function pins)	118	173	212	240

## Ordering Information

Part Number	Pin/Ball Spacing	$\theta_{JA}$ (C/Watt)	$\theta_{JC}$ (C/Watt)	Package Type	Package Body Dimensions	I/O	Comm. (C) Ind. (I) <sup>(1)</sup>
XC2C384-7TQ144C	0.5mm	34.1	6.5	Thin Quad Flat Pack	20mm x 20mm	118	C
XC2C384-10TQ144C	0.5mm	34.1	6.5	Thin Quad Flat Pack	20mm x 20mm	118	C
XC2C384-7PQ208C	0.5mm	36.1	8.4	Plastic Quad Flat Pack	28mm x 28mm	173	C
XC2C384-10PQ208C	0.5mm	36.1	8.4	Plastic Quad Flat Pack	28mm x 28mm	173	C
XC2C384-7FT256C	1.0mm	33.5	5.5	Fine Pitch Thin BGA	17mm x 17mm	212	C
XC2C384-10FT256C	1.0mm	33.5	5.5	Fine Pitch Thin BGA	17mm x 17mm	212	C
XC2C384-7FG324C	1.0mm	39.3	5.3	Fine Pitch BGA	23mm x 23mm	240	C
XC2C384-10FG324C	1.0mm	39.3	5.3	Fine Pitch BGA	23mm x 23mm	240	C
XC2C384-7TQG144C	0.5mm	34.1	6.5	Thin Quad Flat Pack; Pb-free	20mm x 20mm	118	C
XC2C384-10TQG144C	0.5mm	34.1	6.5	Thin Quad Flat Pack; Pb-free	20mm x 20mm	118	C
XC2C384-7PQG208C	0.5mm	36.1	8.4	Plastic Quad Flat Pack; Pb-free	28mm x 28mm	173	C
XC2C384-10PQG208C	0.5mm	36.1	8.4	Plastic Quad Flat Pack; Pb-free	28mm x 28mm	173	C
XC2C384-7FTG256C	1.0mm	33.5	5.5	Fine Pitch Thin BGA; Pb-free	17mm x 17mm	212	C
XC2C384-10FTG256C	1.0mm	33.5	5.5	Fine Pitch Thin BGA; Pb-free	17mm x 17mm	212	C
XC2C384-7FGG324C	1.0mm	39.3	5.3	Fine Pitch BGA; Pb-free	23mm x 23mm	240	C
XC2C384-10FGG324C	1.0mm	39.3	5.3	Fine Pitch BGA; Pb-free	23mm x 23mm	240	C
XC2C384-10TQ144I	0.5mm	34.1	6.5	Plastic Quad Flat Pack	20mm x 20mm	118	I
XC2C384-10PQ208I	0.5mm	36.1	8.4	Plastic Quad Flat Pack	28mm x 28mm	173	I
XC2C384-10FT256I	1.0mm	33.5	5.5	Fine Pitch Thin BGA	17mm x 17mm	212	I
XC2C384-10FG324I	1.0mm	39.3	5.3	Fine Pitch BGA	23mm x 23mm	240	I
XC2C384-10TQG144I	0.5mm	34.1	6.5	Plastic Quad Flat Pack; Pb-free	20mm x 20mm	118	I
XC2C384-10PQG208I	0.5mm	36.1	8.4	Plastic Quad Flat Pack; Pb-free	28mm x 28mm	173	I
XC2C384-10FTG256I	1.0mm	33.5	5.5	Fine Pitch Thin BGA; Pb-free	17mm x 17mm	212	I
XC2C384-10FGG324I	1.0mm	39.3	5.3	Fine Pitch BGA; Pb-free	23mm x 23mm	240	I

### Notes:

1. C = Commercial ( $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ); I = Industrial ( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ).

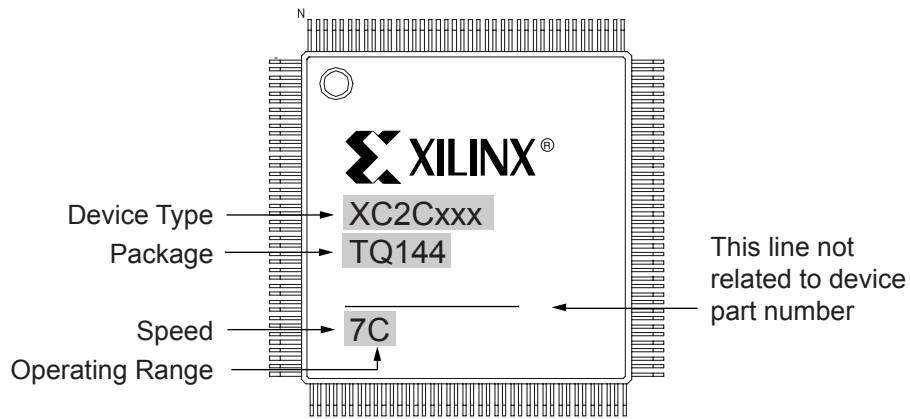
Standard Example: XC2C128 -7 TQ 144 C

Device \_\_\_\_\_  
 Speed Grade \_\_\_\_\_  
 Package Type \_\_\_\_\_  
 Number of Pins \_\_\_\_\_  
 Temperature Range \_\_\_\_\_

Pb-Free Example: XC2C128 -7 TQ G 144 C

Device \_\_\_\_\_  
 Speed Grade \_\_\_\_\_  
 Package Type \_\_\_\_\_  
 Pb-Free \_\_\_\_\_  
 Number of Pins \_\_\_\_\_  
 Temperature Range \_\_\_\_\_

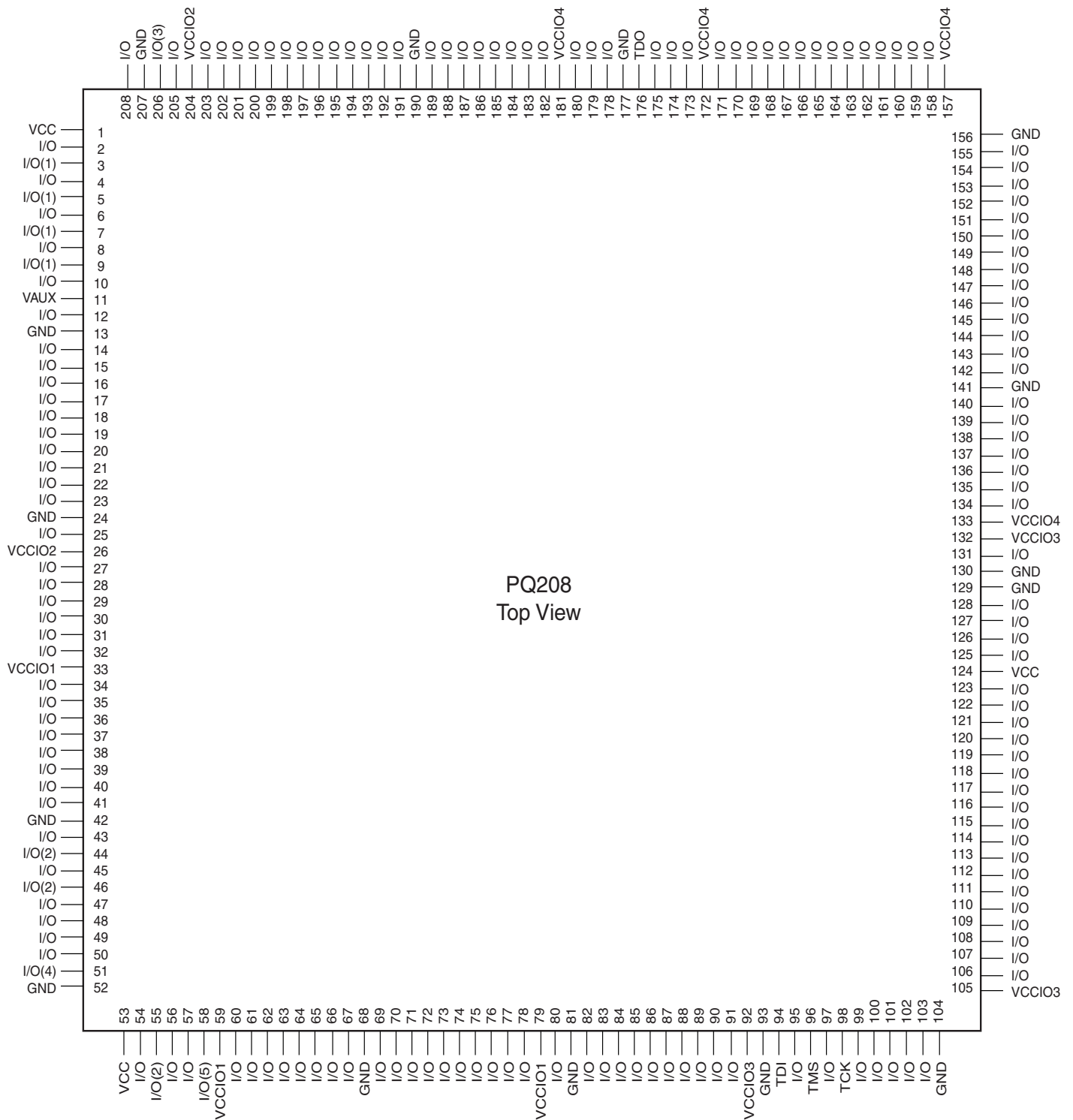
## Device Part Marking



Part marking for non-chip scale package

Figure 5: Sample Package with Part Marking





- (1) - Global Output Enable
- (2) - Global Clock
- (3) - Global Set/Reset
- (4) - Clock Divide Reset
- (5) - DataGATE Enable

Figure 7: PQ208 Plastic Quad Flat Package

	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	I/O	I/O	I/O	I/O	I/O	I/O	TDO	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
B	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
C	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O(3)	I/O	I/O	I/O
D	I/O	I/O	I/O	I/O	VCC	I/O	I/O	I/O	I/O	I/O	I/O	VCC	I/O(1)	I/O(1)	I/O	I/O
E	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O(1)	I/O	I/O(1)	I/O	I/O
F	I/O	I/O	I/O	I/O	I/O	GND	VCCIO4	VCCIO4	VCCIO2	VCCIO2	GND	I/O	VAUX	I/O	I/O	I/O
G	I/O	I/O	I/O	I/O	I/O	I/O	GND	GND	GND	GND	VCCIO2	I/O	I/O	I/O	I/O	I/O
H	I/O	I/O	I/O	I/O	I/O	VCCIO4	GND	GND	GND	GND	VCCIO2	I/O	I/O	I/O	I/O	I/O
J	I/O	I/O	I/O	I/O	I/O	VCCIO3	GND	GND	GND	GND	VCCIO1	I/O	I/O	I/O	I/O	I/O
K	I/O	I/O	I/O	VCC	I/O	VCCIO3	GND	GND	GND	GND	VCCIO1	I/O	I/O	I/O	I/O	I/O
L	I/O	I/O	I/O	I/O	I/O	GND	VCCIO3	VCCIO3	VCCIO1	VCCIO1	GND	I/O	I/O	I/O	I/O	I/O
M	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O(2)	I/O(2)	I/O
N	I/O	I/O	I/O	I/O	TMS	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
P	I/O	I/O	I/O	I/O	TCK	I/O	I/O	I/O	I/O	I/O	I/O	I/O(2)	I/O	VCC	I/O(4)	I/O
R	I/O	I/O	I/O	I/O	I/O	TDI	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O
T	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O(5)	I/O

FT256 Bottom View

- (1) - Global Output Enable
- (2) - Global Clock
- (3) - Global Set/Reset
- (4) - Clock Divide Reset
- (5) - DataGATE Enable

Figure 8: FT256 Fine Pitch Thin BGA

	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
A	I/O	I/O	VCC	I/O	I/O	NC	NC	NC	NC	I/O	NC	NC	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O(3)	I/O	
B	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC	NC	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O(1)	I/O(1)
C	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	TDO	I/O	I/O	NC	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O(1)	I/O(1)
D	I/O	I/O	I/O	I/O	GND	I/O	I/O	I/O	I/O	NC	I/O	NC	I/O	I/O	I/O	I/O	I/O	GND	VCC	I/O(1)	I/O	NC	NC
E	I/O	I/O	I/O	GND															GND	VCC	I/O	I/O(1)	I/O(1)
F	I/O	I/O	I/O	I/O															I/O	NC	I/O	VAUX	VAUX
G	I/O	I/O	I/O	I/O															I/O	I/O	I/O	I/O	I/O
H	I/O	I/O	NC	I/O															I/O	I/O	I/O	I/O	I/O
J	I/O	I/O	I/O	I/O					GND	VCCIO4	VCCIO4	VCCIO2	VCCIO2	GND					NC	I/O	I/O	I/O	I/O
K	I/O	I/O	I/O	I/O					VCCIO4	GND	GND	GND	GND	VCCIO2					NC	I/O	I/O	I/O	I/O
L	I/O	I/O	I/O	I/O					VCCIO4	GND	GND	GND	GND	VCCIO2					NC	I/O	I/O	I/O	I/O
M	I/O	I/O	I/O	I/O					VCCIO3	GND	GND	GND	GND	VCCIO1					NC	I/O	I/O	I/O	I/O
N	I/O	I/O	VCC	I/O					VCCIO3	GND	GND	GND	GND	VCCIO1					NC	I/O	I/O	I/O	I/O
P	NC	I/O	I/O	NC					GND	VCCIO3	VCCIO3	VCCIO1	VCCIO1	GND					I/O	I/O	I/O	I/O	I/O
R	I/O	I/O	NC	NC															I/O	I/O	I/O	I/O	I/O
T	I/O	I/O	I/O	I/O															I/O	I/O	I/O	I/O	I/O
U	I/O	I/O	I/O	I/O															I/O	I/O	I/O	I/O	I/O
V	I/O	I/O	I/O	GND															GND	I/O(2)	I/O	I/O	I/O
W	I/O	I/O	I/O	I/O	GND	NC	NC	I/O	I/O	NC	I/O	I/O	I/O	NC	I/O	I/O	I/O	GND	I/O	NC	I/O	I/O	I/O
Y	I/O	I/O	I/O	TCK	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	NC	I/O	I/O(2)	I/O(2)
AA	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O(5)	I/O	VCC	I/O	I/O	I/O
AB	I/O	I/O	TMS	TDI	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O	I/O(2)	I/O(4)	NC	NC

FG324 Bottom View

- (1) - Global Output Enable
- (2) - Global Clock
- (3) - Global Set/Reset
- (4) - Clock Divide Reset
- (5) - DataGATE Enable

Figure 9: FG324 Fine Pitch BGA

## Warranty Disclaimer

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## Additional Information

Additional information is available for the following CoolRunner-II topics:

- XAPP784: Bulletproof CPLD Design Practices
- XAPP375: Timing Model
- XAPP376: Logic Engine
- XAPP378: Advanced Features
- XAPP382: I/O Characteristics
- XAPP389: Powering CoolRunner-II
- XAPP399: Assigning VREF Pins

To access these and all application notes with their associated reference designs, click the following link and scroll down the page until you find the document you want:

[CoolRunner-II Data Sheets and Application Notes Device Packages](#)

## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
5/31/02	1.0	Initial Xilinx release
9/23/02	1.1	Updated FT256 and TQ144 pinouts
4/16/03	1.2	Updated FG324 package, updated No Connect pins
5/30/03	2.0	Added -6, -10 characterization data
11/7/03	2.1	Corrected typo on page 1. 324-ball FG BGA package has ball pitch of 1.0mm
1/26/04	2.2	Added links to Application notes and Data sheets
5/7/04	2.3	Corrected error in package dimensions of XC2C384-10TQ144I
8/03/04	2.4	Pb-free documentation
10/01/04	2.5	Add Asynchronous Preset/Reset Pulse Width specification to AC Electrical Characteristics
01/30/05	2.6	Change to I <sub>CCSB</sub> MAX for Industrial devices
03/07/05	2.7	Deleted -6 speed grade. Modifications to Table 1, IOSTANDARDS
2/06/06	2.8	Change to T <sub>SUJ</sub> for -7 speed grade. Previous value was typographical error
03/20/06	2.9	Add Warranty Disclaimer. Add note to Pin Descriptions that GCK, GSR, and GTS pins can also be used for general purpose I/O

Date	Version	Revision
07/14/06	3.0	Move to Product Specification. Changes to - 7 speed grade: $T_{SUD}$ , $T_{SU1}$ , $T_{SU2}$ , $T_{CO}$ , $T_{PCO}$ , $T_F$ , $F_{EXT1}$ , $T_{GCK}$ , $T_{ECSU}$ , $T_{COI}$ , $T_{SUEC}$ , $T_{CW}$ and $F_{EXT2}$ . Changes to -10 speed grade: $T_{SUD}$ , $T_{SU1}$ , $T_{SU2}$ , $T_{PSUD}$ , $F_{SYSTEM1}$ , $F_{SYSTEM2}$ , $F_{EXT}$ , and $F_{EXT2}$ . Change to Test Conditions for $V_{OH}$ and $V_{OL}$ on HSTL1 DC Voltage Specifications, page 5 ( $V_{CCIO}$ goes to 1.4V from 1.7V).
02/15/07	3.1	Corrections to timing parameters $t_{OEM}$ for -6 speed grade, and to $t_{DIN}$ , $t_{SUI}$ , $t_{ECSU}$ , $t_{PSU1}$ , $t_{PSU2}$ , $t_{PHD}$ , and $t_{SUEC}$ for the -7 speed grade. Values now match the software. There were no changes to silicon or characterization. Change to $V_{IH}$ specification for 2.5V and 1.8V LVCMOS.
03/08/07	3.2	Fixed typo in note for $V_{IL}$ for LVCMOS18; removed note for $V_{IL}$ for LVCMOS33.



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