

XC2C64A-7VQ44C Datasheet

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XC2C64A-7VQ44C

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| | |
|------------------------------|-------------------------------------|
| DiGi Electronics Part Number | XC2C64A-7VQ44C-DG |
| Manufacturer | AMD |
| Manufacturer Product Number | XC2C64A-7VQ44C |
| Description | IC CPLD 64MC 6.7NS 44VQFP |
| Detailed Description | Embedded, Integrated Circuits (ICs) |



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Purchase and inquiry

Manufacturer Product Number:

XC2C64A-7VQ44C

Series:

CoolRunner II

DiGi-Electronics Programmable:

Not Verified

Delay Time tpd(1) Max:

6.7 ns

Number of Logic Elements/Blocks:

4

Number of Gates:

1500

Operating Temperature:

0°C ~ 70°C (TA)

Package / Case:

44-TQFP

Base Product Number:

XC2C64

Manufacturer:

AMD

Product Status:

Last Time Buy

Programmable Type:

In System Programmable

Voltage Supply - Internal:

1.7V ~ 1.9V

Number of Macrocells:

64

Number of I/O:

33

Mounting Type:

Surface Mount

Supplier Device Package:

44-VQFP (10x10)

Environmental & Export classification

RoHS Status:

RoHS non-compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

3 (168 Hours)

ECCN:

EAR99



XC2C64A CoolRunner-II CPLD

DS311 (v2.3) November 19, 2008

Product Specification

Features

- Optimized for 1.8V systems
 - As fast as 4.6 ns pin-to-pin logic delays
 - As low as 15 μ A quiescent current
- Industry's best 0.18 micron CMOS CPLD
 - Optimized architecture for effective logic synthesis
 - Multi-voltage I/O operation — 1.5V to 3.3V
- Available in multiple package options
 - 44-pin VQFP with 33 user I/Os
 - 48-land QFN with 37 user I/Os
 - 56-ball CP BGA with 45 user I/Os
 - 100-pin VQFP with 64 user I/Os
 - Pb-free available for all packages
- Advanced system features
 - Fastest in system programming
 - 1.8V ISP using IEEE 1532 (JTAG) interface
 - IEEE1149.1 JTAG Boundary Scan Test
 - Optional Schmitt-trigger input (per pin)
 - Two separate I/O banks
 - RealDigital 100% CMOS product term generation
 - Flexible clocking modes
 - Optional DualEDGE triggered registers
 - Global signal options with macrocell control
 - Multiple global clocks with phase selection per macrocell
 - Multiple global output enables
 - Global set/reset
 - Efficient control term clocks, output enables, and set/resets for each macrocell and shared across function blocks
 - Advanced design security
 - Optional bus-hold, 3-state, or weak pullup on selected I/O pins
 - Open-drain output option for Wired-OR and LED drive
 - Optional configurable grounds on unused I/Os
 - Mixed I/O voltages compatible with 1.5V, 1.8V, 2.5V, and 3.3V logic levels
 - PLA architecture
 - Superior pinout retention
 - 100% product term routability across function block
 - Hot pluggable

Refer to the CoolRunner™-II family data sheet for architecture description.

Description

The CoolRunner-II 64-macrocell device is designed for both high performance and low power applications. This lends power savings to high-end communication equipment and high speed to battery operated devices. Due to the low power stand-by and dynamic operation, overall system reliability is improved.

This device consists of four Function Blocks inter-connected by a low power Advanced Interconnect Matrix (AIM). The AIM feeds 40 true and complement inputs to each Function Block. The Function Blocks consist of a 40 by 56 P-term PLA and 16 macrocells which contain numerous configuration bits that allow for combinational or registered modes of operation.

Additionally, these registers can be globally reset or preset and configured as a D or T flip-flop or as a D latch. There are also multiple clock signals, both global and local product term types, configured on a per macrocell basis. Output pin configurations include slew rate limit, bus hold, pull-up, open drain, and programmable grounds. A Schmitt trigger input is available on a per input pin basis. In addition to storing macrocell output states, the macrocell registers can be configured as "direct input" registers to store signals directly from input pins.

Clocking is available on a global or Function Block basis. Three global clocks are available for all Function Blocks as a synchronous clock source. Macrocell registers can be individually configured to power up to the zero or one state. A global set/reset control line is also available to asynchronously set or reset selected registers during operation. Additional local clock, synchronous clock-enable, asynchronous set/reset, and output enable signals can be formed using product terms on a per-macrocell or per-Function Block basis.

A DualEDGE flip-flop feature is also available on a per macrocell basis. This feature allows high performance synchronous operation based on lower frequency clocking to help reduce the total power consumption of the device.

The CoolRunner-II 64-macrocell CPLD is I/O compatible with standard LVTTTL and LVCMOS18, LVCMOS25, and LVCMOS33 (see [Table 1](#)). This device is also 1.5V I/O compatible with the use of Schmitt-trigger inputs.

Another feature that eases voltage translation is I/O banking. Two I/O banks are available on the CoolRunner-II 64A macrocell device that permit easy interfacing to 3.3V, 2.5V, 1.8V, and 1.5V devices.

RealDigital Design Technology

Xilinx® CoolRunner-II CPLDs are fabricated on a 0.18 micron process technology which is derived from leading edge FPGA product development. CoolRunner-II CPLDs employ RealDigital, a design technique that makes use of CMOS technology in both the fabrication and design methodology. RealDigital design technology employs a cascade of CMOS gates to implement sum of products instead of traditional sense amplifier methodology. Due to this technology, Xilinx CoolRunner-II CPLDs achieve both high performance and low power operation.

Supported I/O Standards

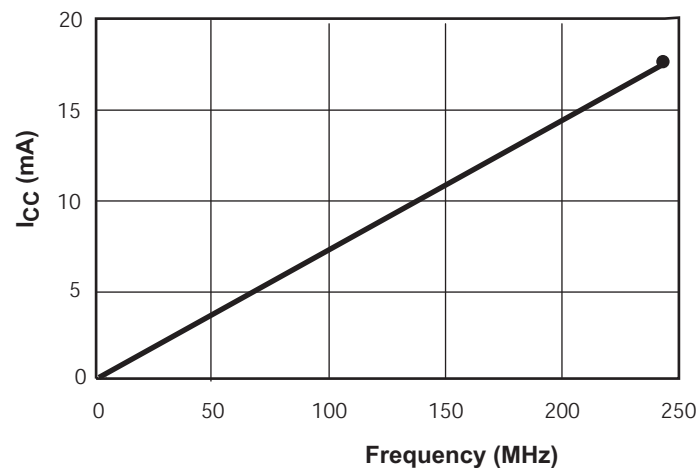
The CoolRunner-II 64 macrocell features both LVCMOS and LVTTTL I/O implementations. See [Table 1](#) for I/O standard voltages. The LVTTTL I/O standard is a general purpose EIA/JEDEC standard for 3.3V applications that use an

LVTTTL input buffer and Push-Pull output buffer. The LVCMOS standard is used in 3.3V, 2.5V, and 1.8V applications. CoolRunner-II CPLDs are also 1.5V I/O compatible with the use of Schmitt-trigger inputs.

Table 1: I/O Standards for XC2C64A

| IOSTANDARD Attribute | Output V_{CCIO} | Input V_{CCIO} | Input V_{REF} | Board Termination Voltage V_T |
|-------------------------|-------------------|------------------|-----------------|---------------------------------|
| LVTTTL | 3.3 | 3.3 | N/A | N/A |
| LVCMOS33 | 3.3 | 3.3 | N/A | N/A |
| LVCMOS25 | 2.5 | 2.5 | N/A | N/A |
| LVCMOS18 | 1.8 | 1.8 | N/A | N/A |
| LVCMOS15 ⁽¹⁾ | 1.5 | 1.5 | N/A | N/A |

1. LVCMOS15 requires Schmitt-trigger inputs.



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Figure 1: I_{CC} vs Frequency

Table 2: I_{CC} vs Frequency (LVCMOS 1.8V T_A = 25°C)⁽¹⁾

| | Frequency (MHz) | | | | | | | | | |
|------------------------------|-----------------|-----|-----|-----|------|------|------|------|------|-------|
| | 0 | 25 | 50 | 75 | 100 | 150 | 175 | 200 | 225 | 240 |
| Typical I _{CC} (mA) | 0.017 | 1.8 | 3.7 | 5.5 | 7.48 | 11.0 | 12.7 | 14.6 | 15.3 | 17.77 |

Notes:

- 16-bit up/down, Resettable binary counter (one counter per function block).

Absolute Maximum Ratings

| Symbol | Description | Value | Units |
|------------------|--|-------------|-------|
| V_{CC} | Supply voltage relative to ground | -0.5 to 2.0 | V |
| V_{CCIO} | Supply voltage for output drivers | -0.5 to 4.0 | V |
| $V_{JTAG}^{(2)}$ | JTAG input voltage limits | -0.5 to 4.0 | V |
| V_{CCAUX} | JTAG input supply voltage | -0.5 to 4.0 | V |
| $V_{IN}^{(1)}$ | Input voltage relative to ground ⁽¹⁾ | -0.5 to 4.0 | V |
| $V_{TS}^{(1)}$ | Voltage applied to 3-state output ⁽¹⁾ | -0.5 to 4.0 | V |
| $V_{STG}^{(3)}$ | Storage Temperature (ambient) | -65 to +150 | °C |
| T_J | Junction Temperature | +150 | °C |

Notes:

- Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easiest to achieve. During transitions, the device pins might undershoot to -2.0V or overshoot to +4.5V, provided this overshoot or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.
- Valid over commercial temperature range.
- For soldering guidelines and thermal considerations, see the [Device Packaging](#) information on the Xilinx website. For Pb free packages, see [XAPP427](#).

Recommended Operating Conditions

| Symbol | Parameter | | Min | Max | Units |
|-------------|---|---|-----|-----|-------|
| V_{CC} | Supply voltage for internal logic and input buffers | Commercial $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ | 1.7 | 1.9 | V |
| | | Industrial $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | 1.7 | 1.9 | V |
| V_{CCIO} | Supply voltage for output drivers @ 3.3V operation | | 3.0 | 3.6 | V |
| | Supply voltage for output drivers @ 2.5V operation | | 2.3 | 2.7 | V |
| | Supply voltage for output drivers @ 1.8V operation | | 1.7 | 1.9 | V |
| | Supply voltage for output drivers @ 1.5V operation | | 1.4 | 1.6 | V |
| V_{CCAUX} | JTAG programming pins | | 1.7 | 3.6 | V |

DC Electrical Characteristics Over Recommended Operating Conditions

| Symbol | Parameter | Test Conditions | Typical | Max. | Units |
|----------------|--------------------------------|---|---------|------|---------------|
| I_{CCSB} | Standby current Commercial | $V_{CC} = 1.9\text{V}$, $V_{CCIO} = 3.6\text{V}$ | 31 | 100 | μA |
| I_{CCSB} | Standby current Industrial | $V_{CC} = 1.9\text{V}$, $V_{CCIO} = 3.6\text{V}$ | 43 | 165 | μA |
| $I_{CC}^{(1)}$ | Dynamic current | $f = 1\text{ MHz}$ | - | 500 | μA |
| | | $f = 50\text{ MHz}$ | - | 5 | mA |
| C_{JTAG} | JTAG input capacitance | $f = 1\text{ MHz}$ | - | 10 | pF |
| C_{CLK} | Global clock input capacitance | $f = 1\text{ MHz}$ | - | 12 | pF |
| C_{IO} | I/O capacitance | $f = 1\text{ MHz}$ | - | 10 | pF |
| $I_{IL}^{(2)}$ | Input leakage current | $V_{IN} = 0\text{V}$ or V_{CCIO} to 3.9V | - | +/-1 | μA |
| $I_{IH}^{(2)}$ | I/O High-Z leakage | $V_{IN} = 0\text{V}$ or V_{CCIO} to 3.9V | - | +/-1 | μA |

Notes:

- 16-bit up/down, Resettable binary counter (one counter per function block) tested at $V_{CC}=V_{CCIO}= 1.9\text{V}$.
- See Quality and Reliability section of the CoolRunner-II family data sheet.

LVC MOS 3.3V and LV TTL 3.3V DC Voltage Specifications

| Symbol | Parameter | Test Conditions | Min. | Max. | Units |
|------------|---------------------------|--|--------------------------|------|-------|
| V_{CCIO} | Input source voltage | | 3.0 | 3.6 | V |
| V_{IH} | High level input voltage | | 2 | 3.9 | V |
| V_{IL} | Low level input voltage | | -0.3 | 0.8 | V |
| V_{OH} | High level output voltage | $I_{OH} = -8 \text{ mA}, V_{CCIO} = 3\text{V}$ | $V_{CCIO} - 0.4\text{V}$ | - | V |
| | | $I_{OH} = -0.1 \text{ mA}, V_{CCIO} = 3\text{V}$ | $V_{CCIO} - 0.2\text{V}$ | - | V |
| V_{OL} | Low level output voltage | $I_{OL} = 8 \text{ mA}, V_{CCIO} = 3\text{V}$ | - | 0.4 | V |
| | | $I_{OL} = 0.1 \text{ mA}, V_{CCIO} = 3\text{V}$ | - | 0.2 | V |

LVC MOS 2.5V DC Voltage Specifications

| Symbol | Parameter | Test Conditions | Min. | Max. | Units |
|------------|---------------------------|--|--------------------------|------------------------|-------|
| V_{CCIO} | Input source voltage | | 2.3 | 2.7 | V |
| V_{IH} | High level input voltage | | 1.7 | $V_{CCIO} + 0.3^{(1)}$ | V |
| V_{IL} | Low level input voltage | | -0.3 | 0.7 | V |
| V_{OH} | High level output voltage | $I_{OH} = -8 \text{ mA}, V_{CCIO} = 2.3\text{V}$ | $V_{CCIO} - 0.4\text{V}$ | - | V |
| | | $I_{OH} = -0.1 \text{ mA}, V_{CCIO} = 2.3\text{V}$ | $V_{CCIO} - 0.2\text{V}$ | - | V |
| V_{OL} | Low level output voltage | $I_{OL} = 8 \text{ mA}, V_{CCIO} = 2.3\text{V}$ | - | 0.4 | V |
| | | $I_{OL} = 0.1 \text{ mA}, V_{CCIO} = 2.3\text{V}$ | - | 0.2 | V |

1. The V_{IH} Max value represents the JEDEC specification for LVC MOS25. The CoolRunner-II CPLD input buffer can tolerate up to 3.9V without physical damage.

LVC MOS 1.8V DC Voltage Specifications

| Symbol | Parameter | Test Conditions | Min. | Max. | Units |
|------------|---------------------------|--|------------------------|------------------------|-------|
| V_{CCIO} | Input source voltage | - | 1.7 | 1.9 | V |
| V_{IH} | High level input voltage | - | $0.65 \times V_{CCIO}$ | $V_{CCIO} + 0.3^{(1)}$ | V |
| V_{IL} | Low level input voltage | - | -0.3 | $0.35 \times V_{CCIO}$ | V |
| V_{OH} | High level output voltage | $I_{OH} = -8 \text{ mA}, V_{CCIO} = 1.7\text{V}$ | $V_{CCIO} - 0.45$ | - | V |
| | | $I_{OH} = -0.1 \text{ mA}, V_{CCIO} = 1.7\text{V}$ | $V_{CCIO} - 0.2$ | - | V |
| V_{OL} | Low level output voltage | $I_{OL} = 8 \text{ mA}, V_{CCIO} = 1.7\text{V}$ | - | 0.45 | V |
| | | $I_{OL} = 0.1 \text{ mA}, V_{CCIO} = 1.7\text{V}$ | - | 0.2 | V |

1. The V_{IH} Max value represents the JEDEC specification for LVC MOS18. The CoolRunner-II CPLD input buffer can tolerate up to 3.9V without physical damage.

LVCMOS 1.5V DC Voltage Specifications

| Symbol | Parameter ⁽¹⁾ | Test Conditions | Min. | Max. | Units |
|------------|------------------------------------|--|-----------------------|-----------------------|-------|
| V_{CCIO} | Input source voltage | - | 1.4 | 1.6 | V |
| V_{T+} | Input hysteresis threshold voltage | - | $0.5 \times V_{CCIO}$ | $0.8 \times V_{CCIO}$ | V |
| V_{T-} | | - | $0.2 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | V |
| V_{OH} | High level output voltage | $I_{OH} = -8 \text{ mA}, V_{CCIO} = 1.4\text{V}$ | $V_{CCIO} - 0.45$ | - | V |
| | | $I_{OH} = -0.1 \text{ mA}, V_{CCIO} = 1.4\text{V}$ | $V_{CCIO} - 0.2$ | - | V |
| V_{OL} | Low level output voltage | $I_{OL} = 8 \text{ mA}, V_{CCIO} = 1.4\text{V}$ | - | 0.4 | V |
| | | $I_{OL} = 0.1 \text{ mA}, V_{CCIO} = 1.4\text{V}$ | - | 0.2 | V |

Notes:

1. Hysteresis used on 1.5V inputs.

Schmitt Trigger Input DC Voltage Specifications

| Symbol | Parameter | Test Conditions | Min. | Max. | Units |
|------------|------------------------------------|-----------------|-----------------------|-----------------------|-------|
| V_{CCIO} | Input source voltage | - | 1.4 | 3.9 | V |
| V_{T+} | Input hysteresis threshold voltage | - | $0.5 \times V_{CCIO}$ | $0.8 \times V_{CCIO}$ | V |
| V_{T-} | | - | $0.2 \times V_{CCIO}$ | $0.5 \times V_{CCIO}$ | V |

AC Electrical Characteristics Over Recommended Operating Conditions

| Symbol | Parameter | -5 | | -7 | | Units |
|-------------------------------------|---|------|------|------|------|-------|
| | | Min. | Max. | Min. | Max. | |
| T _{PD1} | Propagation delay single p-term | - | 4.6 | - | 6.7 | ns |
| T _{PD2} | Propagation delay OR array | - | 5.0 | - | 7.5 | ns |
| T _{SUD} | Direct input register clock setup time | 2.4 | - | 3.3 | - | ns |
| T _{SU1} | Setup time (single p-term) | 2.0 | - | 2.5 | - | ns |
| T _{SU2} | Setup time (OR array) | 2.4 | - | 3.3 | - | ns |
| T _{HD} | Direct input register hold time | 0 | - | 0 | - | ns |
| T _H | P-term hold time | 0 | - | 0 | - | ns |
| T _{CO} | Clock to output | - | 3.9 | - | 6.0 | ns |
| F _{TOGGLE} ⁽¹⁾ | Internal toggle rate ⁽¹⁾ | - | 500 | - | 300 | MHz |
| F _{SYSTEM1} ⁽²⁾ | Maximum system frequency ⁽²⁾ | - | 263 | - | 159 | MHz |
| F _{SYSTEM2} ⁽²⁾ | Maximum system frequency ⁽²⁾ | - | 238 | - | 141 | MHz |
| F _{EXT1} ⁽³⁾ | Maximum external frequency ⁽³⁾ | - | 169 | - | 118 | MHz |
| F _{EXT2} ⁽³⁾ | Maximum external frequency ⁽³⁾ | - | 159 | - | 108 | MHz |
| T _{PSUD} | Direct input register p-term clock setup time | 0.9 | - | 1.7 | - | ns |
| T _{PSU1} | P-term clock setup time (single p-term) | 0.6 | - | 0.9 | - | ns |
| T _{PSU2} | P-term clock setup time (OR array) | 1.0 | - | 1.7 | - | ns |
| T _{PHD} | Direct input register p-term clock hold time | 1.3 | - | 1.4 | - | ns |
| T _{PH} | P-term clock hold | 1.5 | - | 1.7 | - | ns |
| T _{PCO} | P-term clock to output | - | 6.0 | - | 8.4 | ns |
| T _{OE} /T _{OD} | Global OE to output enable/disable | - | 8.0 | - | 10.0 | ns |
| T _{POE} /T _{POD} | P-term OE to output enable/disable | - | 9.0 | - | 11.0 | ns |
| T _{MOE} /T _{MOD} | Macrocell driven OE to output enable/disable | - | 9.0 | - | 11.0 | ns |
| T _{PAO} | P-term set/reset to output valid | - | 7.3 | - | 9.7 | ns |
| T _{AO} | Global set/reset to output valid | - | 6.0 | - | 8.3 | ns |
| T _{SUEC} | Register clock enable setup time | 3.0 | - | 3.7 | - | ns |
| T _{HEC} | Register clock enable hold time | 0 | - | 0 | - | ns |
| T _{CW} | Global clock pulse width High or Low | 1.4 | - | 2.2 | - | ns |
| T _{PCW} | P-term pulse width High or Low | 5.0 | - | 7.5 | - | ns |
| T _{APRPW} | Asynchronous preset/reset pulse width (High or Low) | 5.0 | - | 7.5 | - | ns |
| T _{CONFIG} ⁽⁴⁾ | Configuration time | - | 50.0 | - | 50.0 | μs |

Notes:

1. F_{TOGGLE} is the maximum frequency of a dual edge triggered T flip-flop with output enabled.
2. F_{SYSTEM} (1/T_{CYCLE}) is the internal operating frequency for a device fully populated with 16-bit up/down, Resettable binary counter (one counter per function block).
3. F_{EXT} (1/T_{SU1}+T_{CO}) is the maximum external frequency.
4. Typical configuration current during T_{CONFIG} is 2.3 mA.

Internal Timing Parameters

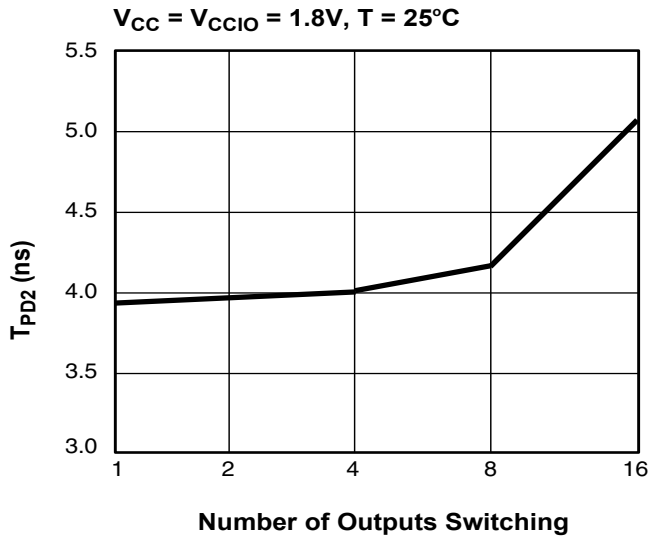
| Symbol | Parameter ⁽¹⁾ | -5 | | -7 | | Units |
|---|------------------------------------|------|------|------|------|-------|
| | | Min. | Max. | Min. | Max. | |
| Buffer Delays | | | | | | |
| T _{IN} | Input buffer delay | - | 1.7 | - | 2.4 | ns |
| T _{DIN} | Direct data register input delay | - | 2.6 | - | 4.0 | ns |
| T _{GCK} | Global clock buffer delay | - | 1.6 | - | 2.5 | ns |
| T _{GSR} | Global set/reset buffer delay | - | 2.4 | - | 3.5 | ns |
| T _{GTS} | Global 3-state buffer delay | - | 2.7 | - | 3.9 | ns |
| T _{OUT} | Output buffer delay | - | 1.9 | - | 2.8 | ns |
| T _{EN} | Output buffer enable/disable delay | - | 5.3 | - | 6.1 | ns |
| P-term Delays | | | | | | |
| T _{CT} | Control term delay | - | 2.0 | - | 2.5 | ns |
| T _{LOGI1} | Single P-term delay adder | - | 0.5 | - | 0.8 | ns |
| T _{LOGI2} | Multiple P-term delay adder | - | 0.4 | - | 0.8 | ns |
| Macrocell Delay | | | | | | |
| T _{PDI} | Input to output valid | - | 0.5 | - | 0.7 | ns |
| T _{SUI} | Setup before clock | 1.4 | - | 1.8 | - | ns |
| T _{HI} | Hold after clock | 0.0 | - | 0.0 | - | ns |
| T _{ECSU} | Enable clock setup time | 0.9 | - | 1.3 | - | ns |
| T _{ECHO} | Enable clock hold time | 0 | - | 0 | - | ns |
| T _{COI} | Clock to output valid | - | 0.4 | - | 0.7 | ns |
| T _{AOI} | Set/reset to output valid | - | 1.7 | - | 2.0 | ns |
| T _{CDBL} | Clock doubler delay | - | 0 | - | 0 | ns |
| Feedback Delays | | | | | | |
| T _F | Feedback delay | - | 1.5 | - | 3.0 | ns |
| T _{OEM} | Macrocell to global OE delay | - | 1.7 | - | 1.7 | ns |
| I/O Standard Time Adder Delays 1.5V CMOS | | | | | | |
| T _{HYS15} | Hysteresis input adder | - | 4.0 | - | 6.0 | ns |
| T _{OUT15} | Output adder | - | 0.9 | - | 1.5 | ns |
| T _{SLEW15} | Output slew rate adder | - | 4.0 | - | 6.0 | ns |
| I/O Standard Time Adder Delays 1.8V CMOS | | | | | | |
| T _{HYS18} | Hysteresis input adder | - | 3.0 | - | 4.0 | ns |
| T _{OUT18} | Output adder | - | 0 | - | 0 | ns |
| T _{SLEW} | Output slew rate adder | - | 3.5 | - | 5.0 | ns |

Internal Timing Parameters (Continued)

| Symbol | Parameter ⁽¹⁾ | -5 | | -7 | | Units |
|---|--------------------------|------|------|------|------|-------|
| | | Min. | Max. | Min. | Max. | |
| I/O Standard Time Adder Delays 2.5V CMOS | | | | | | |
| T _{IN25} | Standard input adder | - | 0.5 | - | 0.6 | ns |
| T _{HYS25} | Hysteresis input adder | - | 2.5 | - | 3.0 | ns |
| T _{OUT25} | Output adder | - | 0.8 | - | 0.9 | ns |
| T _{SLEW25} | Output slew rate adder | - | 4.0 | - | 5.0 | ns |
| I/O Standard Time Adder Delays 3.3V CMOS/TTL | | | | | | |
| T _{IN33} | Standard input adder | - | 0.5 | - | 0.6 | ns |
| T _{HYS33} | Hysteresis input adder | - | 2.0 | - | 3.0 | ns |
| T _{OUT33} | Output adder | - | 1.2 | - | 1.4 | ns |
| T _{SLEW33} | Output slew rate adder | - | 4.0 | - | 5.0 | ns |

1. 1.5 ns input pin signal rise/fall.

Switching Characteristics



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Figure 2: Derating Curve for T_{PD}

Typical I/O Output Curves

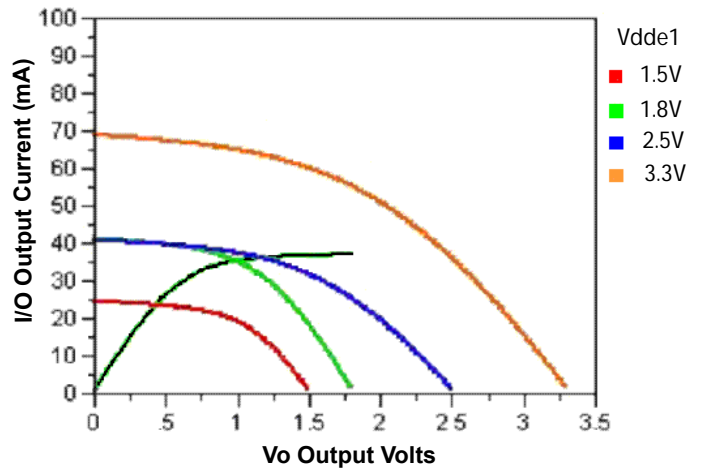
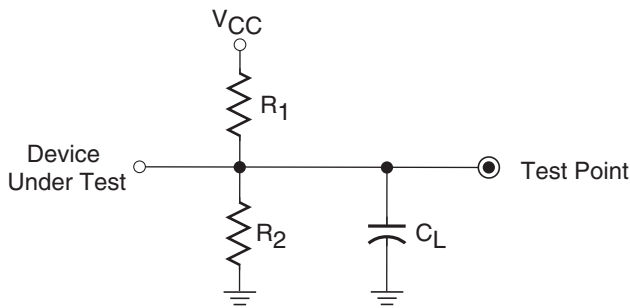


Figure 4: Typical I/O Output Curves

AC Test Circuit



| Output Type | R_1 | R_2 | C_L |
|-------------|----------------|----------------|-------|
| LVTTL33 | 268 Ω | 235 Ω | 35 pF |
| LVC MOS33 | 275 Ω | 275 Ω | 35 pF |
| LVC MOS25 | 188 Ω | 188 Ω | 35 pF |
| LVC MOS18 | 112.5 Ω | 112.5 Ω | 35 pF |
| LVC MOS15 | 150 Ω | 150 Ω | 35 pF |

Notes:

1. C_L includes test fixtures and probe capacitance.
2. 1.5 ns maximum rise/fall times on inputs.

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Figure 3: AC Load Circuit

Pin Descriptions

| Function Block | Macrocell | PC44 ⁽¹⁾ | VQ44 | QFG48 | CP56 | VQ100 | I/O Banking |
|----------------|-----------|---------------------|------|-------|------|-------|-------------|
| 1 | 1 | 44 | 38 | | F1 | 13 | Bank 2 |
| 1 | 2 | 43 | 37 | 5 | E3 | 12 | Bank 2 |
| 1 | 3 | 42 | 36 | 4 | E1 | 11 | Bank 2 |
| 1 | 4 | - | - | | - | 10 | Bank 2 |
| 1 | 5 | - | - | | - | 9 | Bank 2 |
| 1 | 6 | - | - | | - | 8 | Bank 2 |
| 1 | 7 | - | - | | - | 7 | Bank 2 |
| 1 | 8 | - | - | | - | 6 | Bank 2 |
| 1(GTS1) | 9 | 40 | 34 | 2 | D1 | 4 | Bank 2 |
| 1(GTS0) | 10 | 39 | 33 | 1 | C1 | 3 | Bank 2 |
| 1(GTS3) | 11 | 38 | 32 | 48 | A3 | 2 | Bank 2 |
| 1(GTS2) | 12 | 37 | 31 | 47 | A2 | 1 | Bank 2 |
| 1(GSR) | 13 | 36 | 30 | 46 | B1 | 99 | Bank 2 |
| 1 | 14 | - | - | | A1 | 97 | Bank 2 |
| 1 | 15 | - | - | | C3 | 94 | Bank 2 |
| 1 | 16 | - | - | | - | 92 | Bank 2 |
| 2 | 1 | 1 | 39 | 6 | G1 | 14 | Bank 1 |
| 2 | 2 | 2 | 40 | 7 | F3 | 15 | Bank 1 |
| 2 | 3 | - | - | 8 | - | 16 | Bank 1 |
| 2 | 4 | - | - | 9 | - | 17 | Bank 1 |
| 2 | 5 | 3 | 41 | 10 | H1 | 18 | Bank 1 |
| 2 | 6 | 4 | 42 | | G3 | 19 | Bank 1 |
| 2(GCK0) | 7 | 5 | 43 | 11 | J1 | 22 | Bank 1 |
| 2(GCK1) | 8 | 6 | 44 | 12 | K1 | 23 | Bank 1 |
| 2 | 9 | - | - | | K4 | 24 | Bank 1 |
| 2(GCK2) | 10 | 7 | 1 | 13 | K2 | 27 | Bank 1 |
| 2 | 11 | - | - | | - | 28 | Bank 1 |
| 2 | 12 | 8 | 2 | 14 | K3 | 29 | Bank 1 |
| 2 | 13 | 9 | 3 | 15 | H3 | 30 | Bank 1 |
| 2 | 14 | - | - | | K5 | 32 | Bank 1 |
| 2 | 15 | - | - | | - | 33 | Bank 1 |
| 2 | 16 | - | - | | - | 34 | Bank 1 |

Pin Descriptions (Continued)

| Function Block | Macrocell | PC44 ⁽¹⁾ | VQ44 | QFG48 | CP56 | VQ100 | I/O Banking |
|----------------|-----------|---------------------|------|-------|------|-------|-------------|
| 3 | 1 | 35 | 29 | 45 | C4 | 91 | Bank 2 |
| 3 | 2 | 34 | 28 | 44 | A4 | 90 | Bank 2 |
| 3 | 3 | 33 | 27 | 43 | C5 | 89 | Bank 2 |
| 3 | 4 | - | - | | A7 | 81 | Bank 2 |
| 3 | 5 | - | - | 39 | C8 | 79 | Bank 2 |
| 3 | 6 | 29 | 23 | 38 | A8 | 78 | Bank 2 |
| 3 | 7 | - | - | | A9 | 77 | Bank 2 |
| 3 | 8 | - | - | | - | 76 | Bank 2 |
| 3 | 9 | - | - | 37 | A5 | 74 | Bank 2 |
| 3 | 10 | 28 | 22 | 36 | A10 | 72 | Bank 2 |
| 3 | 11 | 27 | 21 | 35 | B10 | 71 | Bank 2 |
| 3 | 12 | 26 | 20 | 34 | C10 | 70 | Bank 2 |
| 3 | 13 | - | - | | D8 | 68 | Bank 2 |
| 3 | 14 | 25 | 19 | 33 | E8 | 67 | Bank 2 |
| 3 | 15 | 24 | 18 | 32 | D10 | 64 | Bank 2 |
| 3 | 16 | - | - | | - | 61 | Bank 2 |
| 4 | 1 | 11 | 5 | 17 | K6 | 35 | Bank 1 |
| 4 | 2 | 12 | 6 | 18 | H5 | 36 | Bank 1 |
| 4 | 3 | - | - | | K7 | 37 | Bank 1 |
| 4 | 4 | - | - | | - | 39 | Bank 1 |
| 4 | 5 | - | - | | H7 | 40 | Bank 1 |
| 4 | 6 | - | - | | - | 41 | Bank 1 |
| 4 | 7 | 14 | 8 | 20 | H8 | 42 | Bank 1 |
| 4 | 8 | - | - | | - | 43 | Bank 1 |
| 4 | 9 | - | - | | - | 49 | Bank 1 |
| 4 | 10 | - | - | 24 | K8 | 50 | Bank 1 |
| 4 | 11 | 18 | 12 | 25 | H10 | 52 | Bank 1 |
| 4 | 12 | - | - | 26 | - | 53 | Bank 1 |
| 4 | 13 | 19 | 13 | 27 | G10 | 55 | Bank 1 |
| 4 | 14 | 20 | 14 | 28 | - | 56 | Bank 1 |
| 4 | 15 | 22 | 16 | | F10 | 58 | Bank 1 |
| 4 | 16 | - | - | 30 | E10 | 60 | Bank 1 |

1. This is an obsolete package type. It remains here for legacy support only.
2. GTS = global output enable, GSR = global set reset, GCK = global clock.
3. GCK, GSR, and GTS pins can also be used for general purpose I/Os.

XC2C64A Global, JTAG, Power/Ground, and No Connect Pins

| Pin Type | PC44 ⁽¹⁾ | VQ44 | QFG48 | CP56 | VQ100 |
|--|---------------------|---------|------------|------------|--|
| TCK | 17 | 11 | 23 | K10 | 48 |
| TDI | 15 | 9 | 21 | J10 | 45 |
| TDO | 30 | 24 | 40 | A6 | 83 |
| TMS | 16 | 10 | 22 | K9 | 47 |
| V _{CCAUX} (JTAG supply voltage) | 41 | 35 | 3 | D3 | 5 |
| Power internal (V _{CC}) | 21 | 15 | 29 | G8 | 26,57 |
| Power bank 1 I/O (V _{CCIO1}) | 13 | 7 | 19 | H6 | 38, 51 |
| Power bank 2 I/O (V _{CCIO2}) | 32 | 26 | 42 | C6 | 88, 98 |
| Ground | 10, 23, 31 | 4,17,25 | 16, 31, 41 | H4, F8, C7 | 21, 31, 62, 69, 84,100 |
| No connects | | | | | 20, 25, 44, 46, 54, 59, 63, 65, 66, 73, 75, 80, 82, 85, 86, 87, 93, 95, 96 |
| Total user I/O | 33 | 33 | 37 | 45 | 64 |

1. This is an obsolete package type. It remains here for legacy support only.

Ordering Information

| Device Ordering No. and Part Marking No. | Pin/Ball Spacing | θ_{JA} (°C/Watt) | θ_{JC} (°C/Watt) | Package Type | Package Body Dimensions | I/O | Comm(C) Ind. (I) ⁽¹⁾ |
|--|------------------|-------------------------|-------------------------|-----------------------------------|-------------------------|-----|---------------------------------|
| XC2C64A-5QFG48C | 0.5mm | 31.2 | 21.2 | Quad Flat No Lead | 7mm x 7mm | 37 | C |
| XC2C64A-7QFG48C | 0.5mm | 31.2 | 21.2 | Quad Flat No Lead | 7mm x 7mm | 37 | C |
| XC2C64A-5VQ44C | 0.8mm | 46.6 | 8.2 | Very Thin Quad Flat Pack | 10mm x 10mm | 33 | C |
| XC2C64A-7VQ44C | 0.8mm | 46.6 | 8.2 | Very Thin Quad Flat Pack | 10mm x 10mm | 33 | C |
| XC2C64A-5CP56C | 0.5mm | 65.0 | 15.0 | Chip Scale Package | 6mm x 6mm | 45 | C |
| XC2C64A-7CP56C | 0.5mm | 65.0 | 15.0 | Chip Scale Package | 6mm x 6mm | 45 | C |
| XC2C64A-5VQ100C | 0.5mm | 53.2 | 14.6 | Very Thin Quad Flat Pack | 14mm x 14mm | 64 | C |
| XC2C64A-7VQ100C | 0.5mm | 53.2 | 14.6 | Very Thin Quad Flat Pack | 14mm x 14mm | 64 | C |
| XC2C64A-5VQG44C | 0.8mm | 46.6 | 8.2 | Very Thin Quad Flat Pack; Pb-free | 10mm x 10mm | 33 | C |
| XC2C64A-7VQG44C | 0.8mm | 46.6 | 8.2 | Very Thin Quad Flat Pack; Pb-free | 10mm x 10mm | 33 | C |
| XC2C64A-5CPG56C | 0.5mm | 65.0 | 15.0 | Chip Scale Package; Pb-free | 6mm x 6mm | 45 | C |
| XC2C64A-7CPG56C | 0.5mm | 65.0 | 15.0 | Chip Scale Package; Pb-free | 6mm x 6mm | 45 | C |
| XC2C64A-5VQG100C | 0.5mm | 53.2 | 14.6 | Very Thin Quad Flat Pack; Pb-free | 14mm x 14mm | 64 | C |
| XC2C64A-7VQG100C | 0.5mm | 53.2 | 14.6 | Very Thin Quad Flat Pack; Pb-free | 14mm x 14mm | 64 | C |
| XC2C64A-7VQ44I | 0.8mm | 46.6 | 8.2 | Very Thin Quad Flat Pack | 10mm x 10mm | 33 | I |
| XC2C64A-7QFG48I | 0.5mm | 31.2 | 21.2 | Quad Flat No Lead; Pb-free | 7mm x 7mm | 37 | I |
| XC2C64A-7CP56I | 0.5mm | 65.0 | 15.0 | Chip Scale Package | 6mm x 6mm | 45 | I |
| XC2C64A-7VQ100I | 0.5mm | 53.2 | 14.6 | Very Thin Quad Flat Pack | 14mm x 14mm | 64 | I |

Additional Information

Additional information is available for the following CoolRunner-II CPLD topics at

www.xilinx.com/support/documentation/coolrunner-ii.htm:

- Device pinouts in the density specific data sheets
- Termination, power sequencing, voltage thresholds, and slew rate data in the CPLD IO User Guide

- Reliability data in the Device Reliability Report
- Packaging thermal and electrical data in the Device Package User Guide

Package drawings and dimensions are available at:

www.xilinx.com/support/documentation/package_specifications.htm

Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|----------|---------|--|
| 5/15/04 | 1.0 | Initial Xilinx release. |
| 8/30/04 | 1.1 | Pb-free documentation |
| 10/01/04 | 1.2 | Add Asynchronous Preset/Reset Pulse Width specification to AC Electrical Characteristics. |
| 11/08/04 | 1.3 | Product Release. No change to documentation. |
| 11/29/04 | 1.4 | Change to QFG package drawing (Figure 8). Pin 29 relabelled. |
| 12/14/04 | 1.5 | Changes to Figure 4, Typical I/O Output Curves; Changes to t_{OUT25} and t_{OUT33} , Internal Timing Parameters, page 8. |
| 01/18/05 | 1.6 | Changes to I_{CCSB} , f_{TOGGLE} , t_{PSU1} , t_{PSU2} , t_{PHD} , t_{CW} , t_{SLEW25} , and t_{SLEW33} |
| 03/07/05 | 1.7 | Format change to specifications I_{IL} and I_{IH} , page 3. Improvement to pin-to-pin logic delay, page 1. Modifications to Table 1, IOSTANDARDS. |
| 06/28/05 | 1.8 | Move to Product Specification. Change to T_{IN25} , T_{OUT25} , T_{IN33} , and T_{OUT33} . |
| 01/30/06 | 1.9 | Modified footnote 1 from AC Specifications Table to remove incorrect equation. |
| 03/20/06 | 2.0 | Add Warranty Disclaimer. Add note to Pin Descriptions that GCK, GSR, and GTS pins can also be used for general purpose I/O. |
| 02/15/07 | 2.1 | Change to V_{IH} specification for 2.5V and 1.8V LVCMOS. Change T_F specification on -7 speed grade from 2.0 to 3.0 ns. |
| 03/08/07 | 2.2 | Fixed typo in note for V_{IL} for LVCMOS18; removed note for V_{IL} for LVCMOS33. |
| 11/19/08 | 2.3 | Added note to Pin Description tables to indicate the PC44 packages are obsolete. Removed part numbers for devices in PC44 packages the Features section and from the ordering information. See Product Discontinuation Notice xcn07022.pdf . |

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