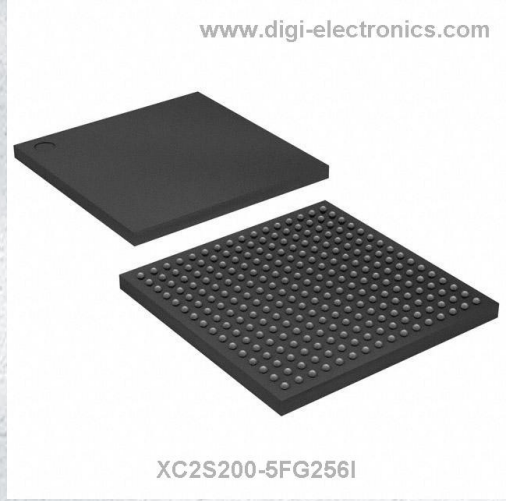
# XC2S200-5FG256I Datasheet

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| | |
|---|---|
| DiGi Electronics Part Number | XC2S200-5FG256I-DG |
| Manufacturer | AMD |
| Manufacturer Product Number | XC2S200-5FG256I |
| Description | IC FPGA 176 I/O 256FBGA |
| Detailed Description | Spartan®-II Field Programmable Gate Array (FPGA) IC 176 57344 5292 256-BGA |

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

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## Purchase and inquiry

| Manufacturer Product Number: | Manufacturer: |
| --- | --- |
| XC2S200-5FG256I | AMD |
| Series: | Product Status: |
| Spartan®-II | Last Time Buy |
| DiGi-Electronics Programmable: | Number of LABs/CLBs: |
| Not Verified | 1176 |
| Number of Logic Elements/Cells: | Total RAM Bits: |
| 5292 | 57344 |
| Number of I/O: | Number of Gates: |
| 176 | 200000 |
| Voltage - Supply: | Mounting Type: |
| 2.375V ~ 2.625V | Surface Mount |
| Operating Temperature: | Package / Case: |
| -40°C ~ 100°C (TJ) | 256-BGA |
| Supplier Device Package: | Base Product Number: |
| 256-FBGA (17x17) | XC2S200 |

## Environmental & Export classification

| RoHS Status: | Moisture Sensitivity Level (MSL): |
| --- | --- |
| RoHS non-compliant | 3 (168 Hours) |
| REACH Status: | ECCN: |
| REACH Unaffected | EAR99 |
| HTSUS: | |
| 8542.39.0001 | |

# Spartan-II FPGA Family Data Sheet

DS001 March 12, 2021 **Product Specification**

This document includes all four modules of the Spartan®-II FPGA data sheet.

## Module 1: Introduction and Ordering Information

**DS001-1 (v2.9) March 12, 2021**

- Introduction
- Features
- General Overview
- Product Availability
- User I/O Chart
- Ordering Information

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- Architectural Description
  - Spartan-II Array
  - Input/Output Block
  - Configurable Logic Block
  - Block RAM
  - Clock Distribution: Delay-Locked Loop
  - Boundary Scan
- Development System
- Configuration
  - Configuration Timing
- Design Considerations

## Module 3: DC and Switching Characteristics

**DS001-3 (v2.9) March 12, 2021**

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  - Absolute Maximum Ratings
  - Recommended Operating Conditions
  - DC Characteristics
  - Power-On Requirements
  - DC Input and Output Levels
- Switching Characteristics
  - Pin-to-Pin Parameters
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  - DLL Timing Parameters
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  - TBUF Switching Characteristics
  - JTAG Switching Characteristics

## Module 4: Pinout Tables

**DS001-4 (v2.9) March 12, 2021**

- Pin Definitions
- Pinout Tables

IMPORTANT NOTE: *This Spartan-II FPGA data sheet is in four modules. Each module has its own Revision History at the end. Use the PDF "Bookmarks" for easy navigation in this volume.*

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# Spartan-II FPGA Family: Introduction and Ordering Information

DS001-1 (v2.9) March 12, 2021

**Product Specification**

## Introduction

The Spartan®-II Field-Programmable Gate Array family gives users high performance, abundant logic resources, and a rich feature set, all at an exceptionally low price. The six-member family offers densities ranging from 15,000 to 200,000 system gates, as shown in Table 1. System performance is supported up to 200 MHz. Features include block RAM (to 56K bits), distributed RAM (to 75,264 bits), 16 selectable I/O standards, and four DLLs. Fast, predictable interconnect means that successive design iterations continue to meet timing requirements.

The Spartan-II family is a superior alternative to mask-programmed ASICs. The FPGA avoids the initial cost, lengthy development cycles, and inherent risk of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary (impossible with ASICs).

## Features

- Second generation ASIC replacement technology
  - Densities as high as 5,292 logic cells with up to 200,000 system gates
  - Streamlined features based on Virtex® FPGA architecture
  - Unlimited reprogrammability
  - Very low cost
  - Cost-effective 0.18 micron process
- System level features
  - SelectRAM™ hierarchical memory:
    - 16 bits/LUT distributed RAM
    - Configurable 4K bit block RAM
    - Fast interfaces to external RAM
  - Fully PCI compliant
  - Low-power segmented routing architecture
  - Full readback ability for verification/observability
  - Dedicated carry logic for high-speed arithmetic
  - Efficient multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with enable, set, reset
  - Four dedicated DLLs for advanced clock control
  - Four primary low-skew global clock distribution nets
  - IEEE 1149.1 compatible boundary scan logic
- Versatile I/O and packaging
  - Pb-free package options
  - Low-cost packages available in all densities
  - Family footprint compatibility in common packages
  - 16 high-performance interface standards
  - Hot swap Compact PCI friendly
  - Zero hold time simplifies system timing
- Core logic powered at 2.5V and I/Os powered at 1.5V, 2.5V, or 3.3V
- Fully supported by powerful Xilinx® ISE® development system
  - Fully automatic mapping, placement, and routing

*Table 1:* **Spartan-II FPGA Family Members**

| Device | Logic Cells | System Gates (Logic and RAM) | CLB Array (R x C) | Total CLBs | Maximum Available User I/O(1) | Total Distributed RAM Bits | Total Block RAM Bits |
|---|---|---|---|---|---|---|---|
| XC2S15 | 432 | 15,000 | 8 x 12 | 96 | 86 | 6,144 | 16K |
| XC2S30 | 972 | 30,000 | 12 x 18 | 216 | 92 | 13,824 | 24K |
| XC2S50 | 1,728 | 50,000 | 16 x 24 | 384 | 176 | 24,576 | 32K |
| XC2S100 | 2,700 | 100,000 | 20 x 30 | 600 | 176 | 38,400 | 40K |
| XC2S150 | 3,888 | 150,000 | 24 x 36 | 864 | 260 | 55,296 | 48K |
| XC2S200 | 5,292 | 200,000 | 28 x 42 | 1,176 | 284 | 75,264 | 56K |

**Notes:**
1. All user I/O counts do not include the four global clock/user input pins. See details in Table 2, page 4.

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## General Overview

The Spartan-II family of FPGAs have a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), surrounded by a perimeter of programmable Input/Output Blocks (IOBs). There are four Delay-Locked Loops (DLLs), one at each corner of the die. Two columns of block RAM lie on opposite sides of the die, between the CLBs and the IOB columns. These functional elements are interconnected by a powerful hierarchy of versatile routing channels (see Figure 1).

Spartan-II FPGAs are customized by loading configuration data into internal static memory cells. Unlimited reprogramming cycles are possible with this approach. Stored values in these cells determine logic functions and interconnections implemented in the FPGA. Configuration data can be read from an external serial PROM (master serial mode), or written into the FPGA in slave serial, slave parallel, or Boundary Scan modes.

Spartan-II FPGAs are typically used in high-volume applications where the versatility of a fast programmable solution adds benefits. Spartan-II FPGAs are ideal for shortening product development cycles while offering a cost-effective solution for high volume production.

Spartan-II FPGAs achieve high-performance, low-cost operation through advanced architecture and semiconductor technology. Spartan-II devices provide system clock rates up to 200 MHz. In addition to the conventional benefits of high-volume programmable logic solutions, Spartan-II FPGAs also offer on-chip synchronous single-port and dual-port RAM (block and distributed form), DLL clock drivers, programmable set and reset on all flip-flops, fast carry logic, and many other features.

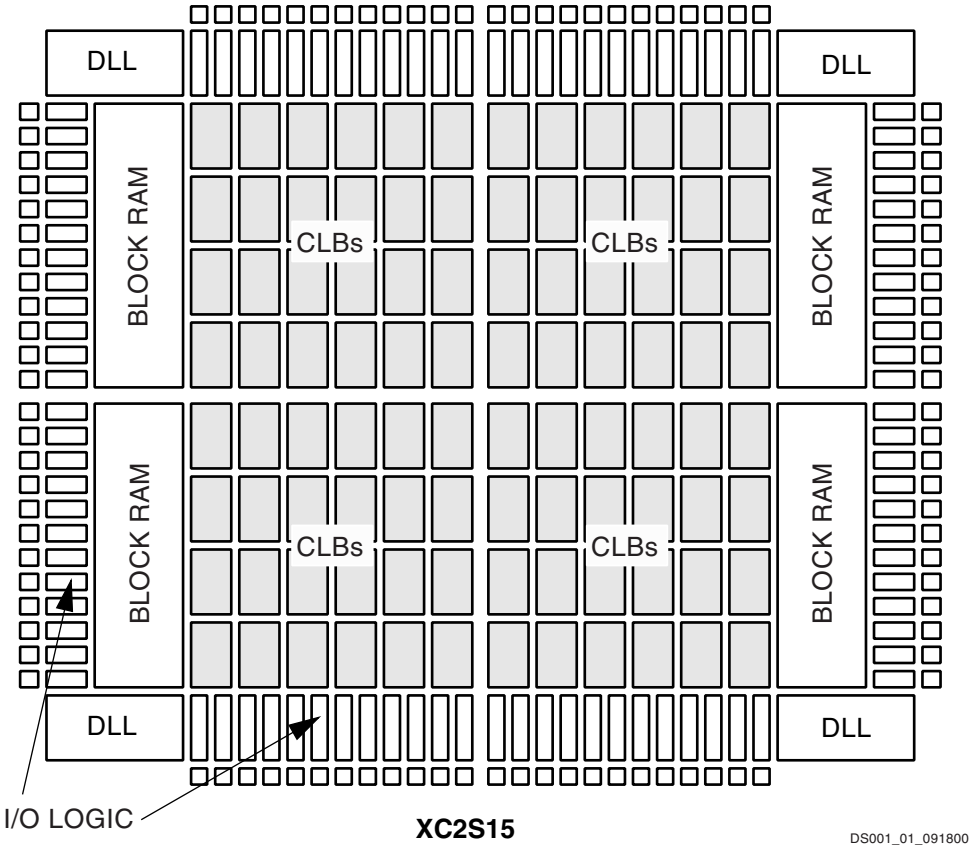



*Figure 1:* **Basic Spartan-II Family FPGA Block Diagram**

XC2S200-5FG256I AMD IC FPGA 176 I/O 256FBGA


## Spartan-II Product Availability

Table 2 shows the maximum user I/Os available on the device and the number of user I/Os available for each device/package combination. The four global clock pins are usable as additional user I/Os when not used as a global clock pin. These pins are not included in user I/O counts.

*Table 2:* **Spartan-II FPGA User I/O Chart(1)**

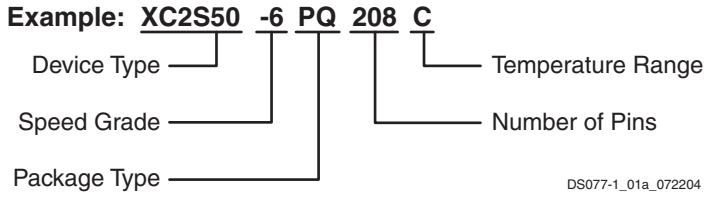
| Device | Maximum User I/O | Available User I/O According to Package Type | | | | | |
|---|---|---|---|---|---|---|---|
| | | VQ100 VQG100 | TQ144 TQG144 | CS144 CSG144 | PQ208 PQG208 | FG256 FGG256 | FG456 FGG456 |
| XC2S15 | 86 | 60 | 86 | (Note 2) | - | - | - |
| XC2S30 | 92 | 60 | 92 | 92 | (Note 2) | - | - |
| XC2S50 | 176 | - | 92 | - | 140(3) | 176 | - |
| XC2S100 | 176 | - | 92 | - | 140(3) | 176 | (Note 2) |
| XC2S150 | 260 | - | - | - | 140(3) | 176 | 260 |
| XC2S200 | 284 | - | - | - | 140(3) | 176 | 284 |

**Notes:**
1. All user I/O counts do not include the four global clock/user input pins.
2. Discontinued by PDN2004-01.
3. See XCN20012 for product discontinuation information regarding specific devices.

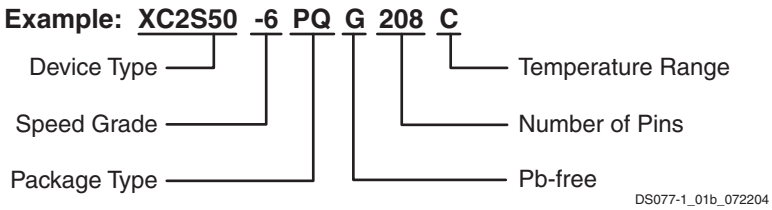
# Ordering Information

Spartan-II devices are available in both standard and Pb-free packaging options for all device/package combinations. The Pb-free packages include a special "G" character in the ordering code.

### *Standard Packaging*




### *Pb-Free Packaging*




## Device Ordering Options

| Device |
|---|
| XC2S15 |
| XC2S30 |
| XC2S50 |
| XC2S100 |
| XC2S150 |
| XC2S200 |

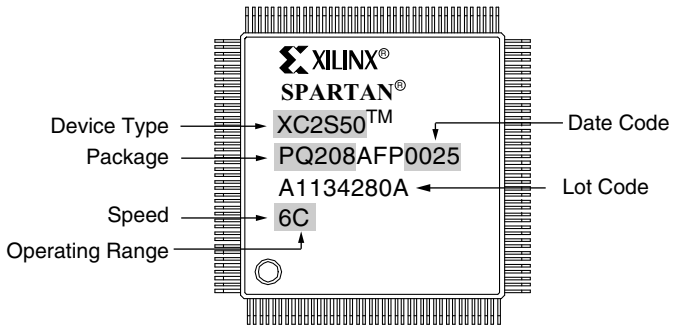
| Speed Grade | |
|---|---|
| -5 | Standard Performance |
| -6 | Higher Performance(1) |

| Number of Pins / Package Type | |
|---|---|
| VQ(G)100 | 100-pin Plastic Very Thin QFP |
| CS(G)144 | 144-ball Chip-Scale BGA |
| TQ(G)144 | 144-pin Plastic Thin QFP |
| PQ(G)208 | 208-pin Plastic QFP |
| FG(G)256 | 256-ball Fine Pitch BGA |
| FG(G)456 | 456-ball Fine Pitch BGA |

| Temperature Range ($T_J$) | |
|---|---|
| C = Commercial | 0°C to +85°C |
| I = Industrial | –40°C to +100°C |

**Notes:**
1. The -6 speed grade is exclusively available in the Commercial temperature range.

## Device Part Marking




Sample package with part marking for XC2S50-6PQ208C.

ds001-1_02_090303

XC2S200-5FG256I AMD IC FPGA 176 I/O 256FBGA


## Revision History

| Date | Version No. | Description |
|---|---|---|
| 09/18/00 | 2.0 | Sectioned the Spartan-II Family data sheet into four modules. Added industrial temperature range information. |
| 10/31/00 | 2.1 | Removed Power down feature. |
| 03/05/01 | 2.2 | Added statement on PROMs. |
| 11/01/01 | 2.3 | Updated Product Availability chart. Minor text edits. |
| 09/03/03 | 2.4 | Added device part marking. |
| 08/02/04 | 2.5 | Added information on Pb-free packaging options and removed discontinued options. |
| 06/13/08 | 2.8 | Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8. |
| 03/12/21 | 2.9 | Added note 3 to Table 2 (see XCN20012, *Product Discontinuation Notice for Spartan-II PQ(G)208 Package Pin Products*). |

# Spartan-II FPGA Family: Functional Description

DS001-2 (v2.9) March 12, 2021 **Product Specification**

## Architectural Description

### Spartan-II FPGA Array

The Spartan®-II field-programmable gate array, shown in Figure 2, is composed of five major configurable elements:

- IOBs provide the interface between the package pins and the internal logic
- CLBs provide the functional elements for constructing most logic
- Dedicated block RAM memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- Versatile multi-level interconnect structure

As can be seen in Figure 2, the CLBs form the central logic structure with easy access to all support and routing structures. The IOBs are located around all the logic and memory elements for easy and quick routing of signals on and off the chip.

Values stored in static memory cells control all the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

Each of these elements will be discussed in detail in the following sections.

### Input/Output Block

The Spartan-II FPGA IOB, as seen in Figure 2, features inputs and outputs that support a wide variety of I/O signaling standards. These high-speed inputs and outputs are capable of supporting various state of the art memory and bus interfaces. Table 3 lists several of the standards which are supported along with the required reference, output and termination voltages needed to meet the standard.

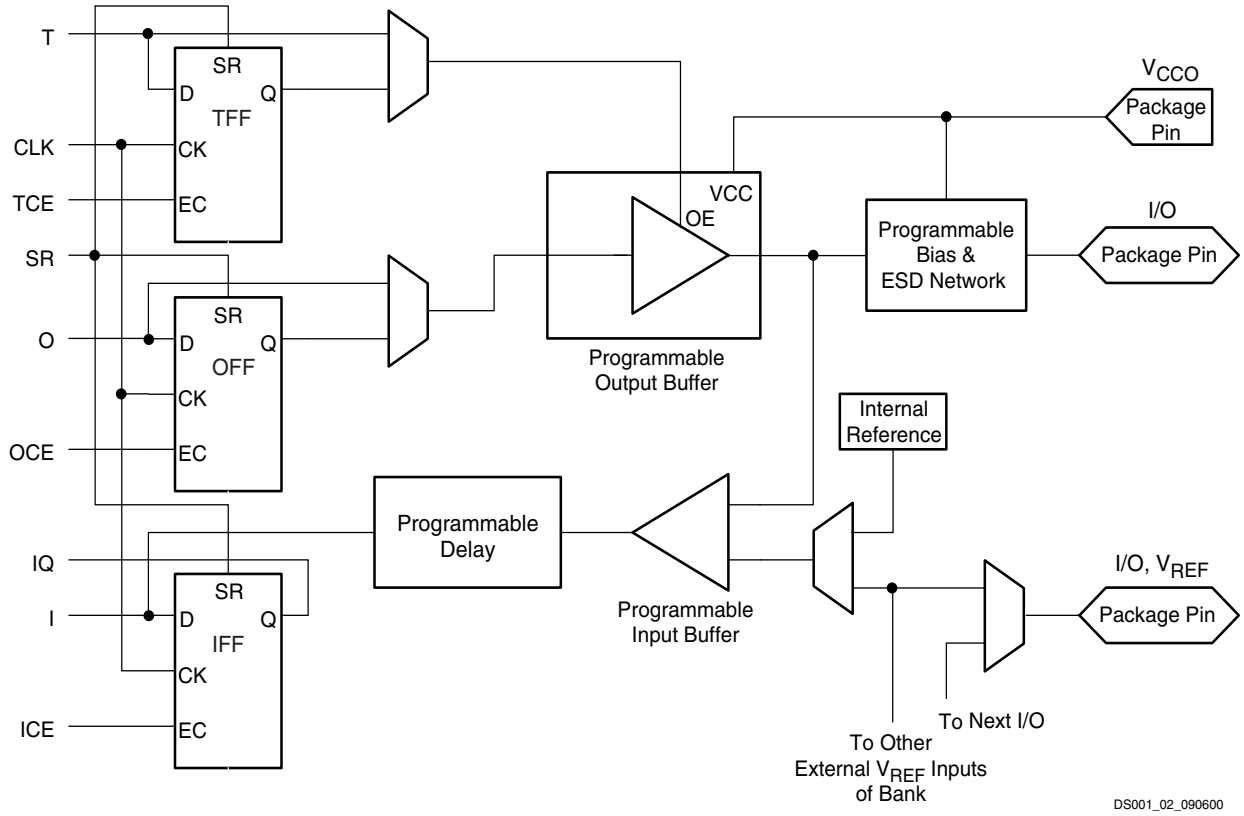



*Figure 2:* **Spartan-II FPGA Input/Output Block (IOB)**

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The three IOB registers function either as edge-triggered D-type flip-flops or as level-sensitive latches. Each IOB has a clock signal (CLK) shared by the three registers and independent Clock Enable (CE) signals for each register. In addition to the CLK and CE control signals, the three registers share a Set/Reset (SR). For each register, this signal can be independently configured as a synchronous Set, a synchronous Reset, an asynchronous Preset, or an asynchronous Clear.

A feature not shown in the block diagram, but controlled by the software, is polarity control. The input and output buffers and all of the IOB control signals have independent polarity controls.

Optional pull-up and pull-down resistors and an optional weak-keeper circuit are attached to each pad. Prior to configuration all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive, but inputs may optionally be pulled up.

*Table 3:* **Standards Supported by I/O (Typical Values)**

| I/O Standard | Input Reference Voltage ($V_{REF}$) | Output Source Voltage ($V_{CCO}$) | Board Termination Voltage ($V_{TT}$) |
|---|---|---|---|
| LVTTL (2-24 mA) | N/A | 3.3 | N/A |
| LVCMOS2 | N/A | 2.5 | N/A |
| PCI (3V/5V, 33 MHz/66 MHz) | N/A | 3.3 | N/A |
| GTL | 0.8 | N/A | 1.2 |
| GTL+ | 1.0 | N/A | 1.5 |
| HSTL Class I | 0.75 | 1.5 | 0.75 |
| HSTL Class III | 0.9 | 1.5 | 1.5 |
| HSTL Class IV | 0.9 | 1.5 | 1.5 |
| SSTL3 Class I and II | 1.5 | 3.3 | 1.5 |
| SSTL2 Class I and II | 1.25 | 2.5 | 1.25 |
| CTT | 1.5 | 3.3 | 1.5 |
| AGP-2X | 1.32 | 3.3 | N/A |

The activation of pull-up resistors prior to configuration is controlled on a global basis by the configuration mode pins. If the pull-up resistors are not activated, all the pins will float. Consequently, external pull-up or pull-down resistors must be provided on pins required to be at a well-defined logic level prior to configuration.

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. Two forms of over-voltage protection are provided, one that permits 5V compliance, and one that does not. For 5V compliance, a zener-like structure connected to ground turns on when the output rises to approximately 6.5V. When 5V compliance is not required, a conventional clamp diode may be connected to the output supply voltage, $V_{CCO}$. The type of over-voltage protection can be selected independently for each pad.

All Spartan-II FPGA IOBs support IEEE 1149.1-compatible boundary scan testing.

### *Input Path*

A buffer In the Spartan-II FPGA IOB input path routes the input signal either directly to internal logic or through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, $V_{REF}$. The need to supply $V_{REF}$ imposes constraints on which standards can used in close proximity to each other. See "I/O Banking," page 9.

There are optional pull-up and pull-down resistors at each input for use after configuration.

### *Output Path*

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signaling standards. Each output buffer can source up to 24 mA and sink up to 48 mA. Drive strength and slew rate controls minimize bus transients.

In most signaling standards, the output high voltage depends on an externally supplied $V_{CCO}$ voltage. The need to supply $V_{CCO}$ imposes constraints on which standards can be used in close proximity to each other. See "I/O Banking".

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all

drivers are disabled. Maintaining a valid logic level in this way helps eliminate bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate $V_{REF}$ voltage must be provided if the signaling standard requires one. The provision of this voltage must comply with the I/O banking rules.

### *I/O Banking*

Some of the I/O standards described above require $V_{CCO}$ and/or $V_{REF}$ voltages. These voltages are externally connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks (see Figure 3). Each bank has multiple $V_{CCO}$ pins which must be connected to the same voltage. Voltage is determined by the output standards in use.

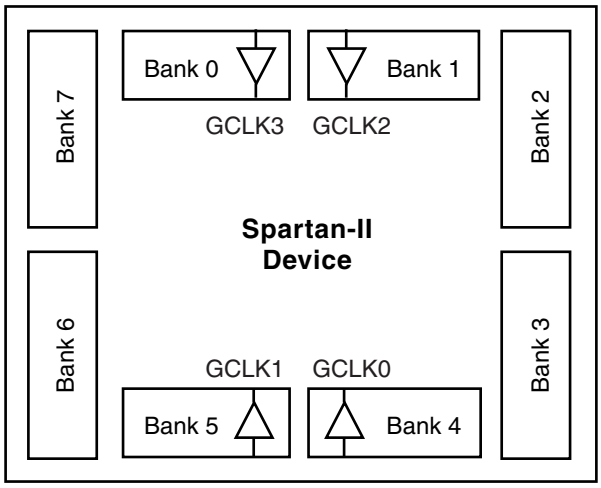


*Figure 3:* **Spartan-II I/O Banks**

Within a bank, output standards may be mixed only if they use the same $V_{CCO}$. Compatible standards are shown in Table 4. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on $V_{CCO}$.

*Table 4:* **Compatible Output Standards**

| $V_{CCO}$ | Compatible Standards |
|---|---|
| 3.3V | PCI, LVTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+ |
| 2.5V | SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+ |
| 1.5V | HSTL I, HSTL III, HSTL IV, GTL, GTL+ |

Some input standards require a user-supplied threshold voltage, $V_{REF}$. In this case, certain user-I/O pins are automatically configured as inputs for the $V_{REF}$ voltage. About one in six of the I/O pins in the bank assume this role.

$V_{REF}$ pins within a bank are interconnected internally and consequently only one $V_{REF}$ voltage can be used within each bank. All $V_{REF}$ pins in the bank, however, must be connected to the external voltage source for correct operation.

In a bank, inputs requiring $V_{REF}$ can be mixed with those that do not but only one $V_{REF}$ voltage may be used within a bank. Input buffers that use $V_{REF}$ are not 5V tolerant. LVTTL, LVCMOS2, and PCI are 5V tolerant. The $V_{CCO}$ and $V_{REF}$ pins for each bank appear in the device pinout tables.

Within a given package, the number of $V_{REF}$ and $V_{CCO}$ pins can vary depending on the size of device. In larger devices, more I/O pins convert to $V_{REF}$ pins. Since these are always a superset of the $V_{REF}$ pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device. All $V_{REF}$ pins for the largest device anticipated must be connected to the $V_{REF}$ voltage, and not used for I/O.

Independent Banks Available

| Package | VQ100<br>PQ208 | CS144<br>TQ144 | FG256<br>FG456 |
|---|---|---|---|
| Independent Banks | 1 | 4 | 8 |

## Configurable Logic Block

The basic building block of the Spartan-II FPGA CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and storage element. Output from the function generator in each LC drives the CLB output and the D input of the flip-flop. Each Spartan-II FPGA CLB contains four LCs, organized in two similar slices; a single slice is shown in Figure 4.

In addition to the four basic LCs, the Spartan-II FPGA CLB contains logic that combines function generators to provide functions of five or six inputs.

### *Look-Up Tables*

Spartan-II FPGA function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16 x 1-bit dual-port synchronous RAM.

The Spartan-II FPGA LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

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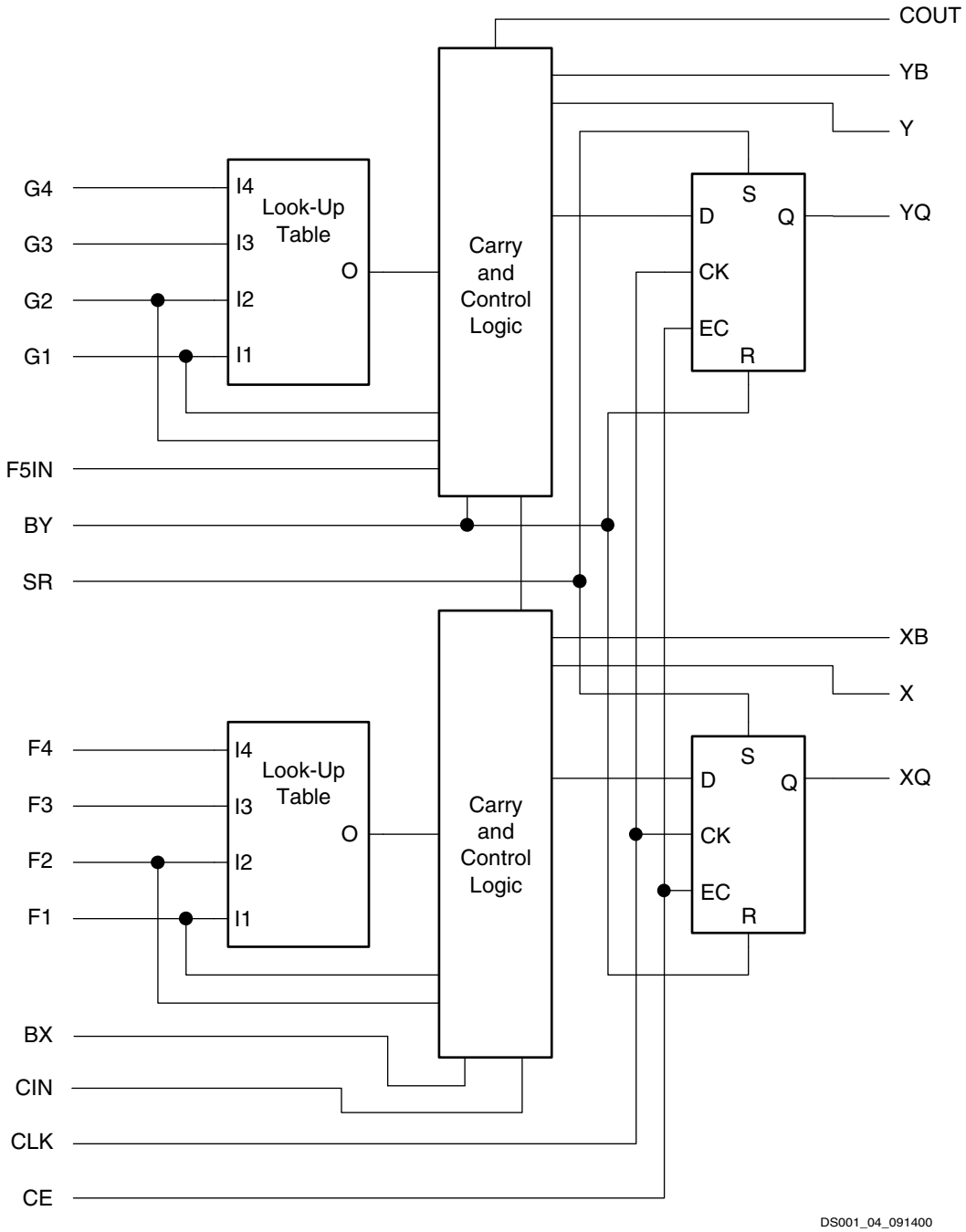


*Figure 4:* **Spartan-II CLB Slice** (two identical slices in each CLB)

### *Storage Elements*

Storage elements in the Spartan-II FPGA slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals may be configured to operate asynchronously.

All control signals are independently invertible, and are shared by the two flip-flops within the slice.

### *Additional Logic*

The F5 multiplexer in each slice combines the function generator outputs. This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.

Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB by selecting one of the F5-multiplexer outputs. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

Each CLB has four direct feedthrough paths, one per LC. These paths provide extra data input lines or additional local routing that does not consume logic resources.

### *Arithmetic Logic*

Dedicated carry logic provides capability for high-speed arithmetic functions. The Spartan-II FPGA CLB supports two separate carry chains, one per slice. The height of the carry chains is two bits per CLB.

The arithmetic logic includes an XOR gate that allows a 1-bit full adder to be implemented within an LC. In addition, a dedicated AND gate improves the efficiency of multiplier implementation.

The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

### *BUFTs*

Each Spartan-II FPGA CLB contains two 3-state drivers (BUFTs) that can drive on-chip busses. See "Dedicated Routing," page 12. Each Spartan-II FPGA BUFT has an independent 3-state control pin and an independent input pin.

## Block RAM

Spartan-II FPGAs incorporate several large block RAM memories. These complement the distributed RAM Look-Up Tables (LUTs) that provide shallow memory structures implemented in CLBs.

Block RAM memory blocks are organized in columns. All Spartan-II devices contain two such columns, one along each vertical edge. These columns extend the full height of the chip. Each memory block is four CLBs high, and consequently, a Spartan-II device eight CLBs high will contain two memory blocks per column, and a total of four blocks.

*Table 5:* **Spartan-II Block RAM Amounts**

| Spartan-II Device | # of Blocks | Total Block RAM Bits |
|---|---|---|
| XC2S15 | 4 | 16K |
| XC2S30 | 6 | 24K |
| XC2S50 | 8 | 32K |
| XC2S100 | 10 | 40K |
| XC2S150 | 12 | 48K |
| XC2S200 | 14 | 56K |

Each block RAM cell, as illustrated in Figure 5, is a fully synchronous dual-ported 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

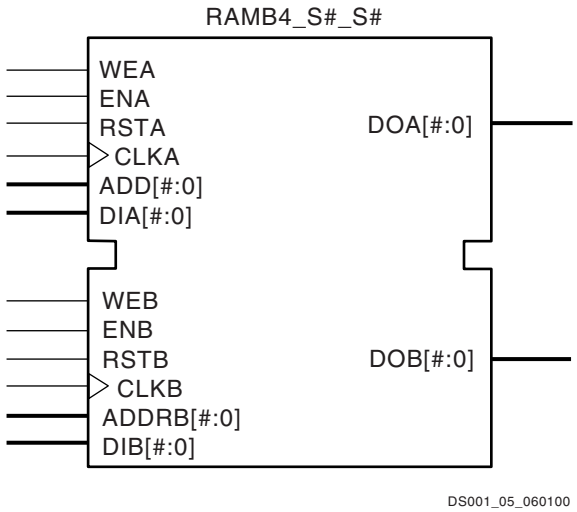


*Figure 5:* **Dual-Port Block RAM**

Table 6 shows the depth and width aspect ratios for the block RAM.

*Table 6:* **Block RAM Port Aspect Ratios**

| Width | Depth | ADDR Bus | Data Bus |
|---|---|---|---|
| 1 | 4096 | ADDR<11:0> | DATA<0> |
| 2 | 2048 | ADDR<10:0> | DATA<1:0> |
| 4 | 1024 | ADDR<9:0> | DATA<3:0> |
| 8 | 512 | ADDR<8:0> | DATA<7:0> |
| 16 | 256 | ADDR<7:0> | DATA<15:0> |

The Spartan-II FPGA block RAM also includes dedicated routing to provide an efficient interface with both CLBs and other block RAMs.

## Programmable Routing Matrix

It is the longest delay path that limits the speed of any worst-case design. Consequently, the Spartan-II routing architecture and its place-and-route software were defined in a single optimization process. This joint optimization minimizes long-path delays, and consequently, yields the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

### *Local Routing*

The local routing resources, as shown in Figure 6, provide the following three types of connections:

- Interconnections among the LUTs, flip-flops, and General Routing Matrix (GRM)
- Internal CLB feedback paths that provide high-speed connections to LUTs within the same CLB, chaining them together with minimal routing delay
- Direct paths that provide high-speed connections between horizontally adjacent CLBs, eliminating the delay of the GRM

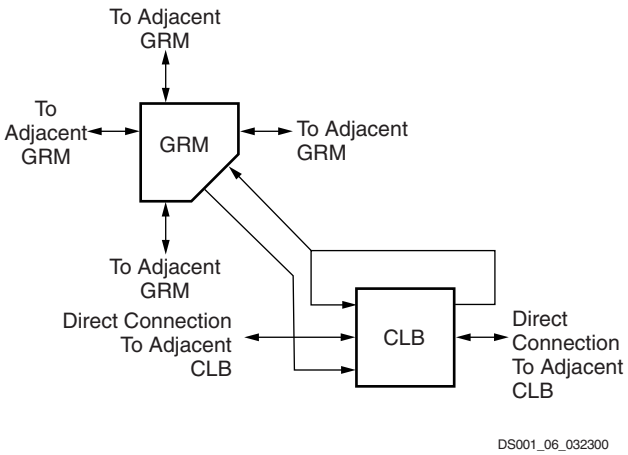


*Figure 6:* **Spartan-II Local Routing**

### *General Purpose Routing*

Most Spartan-II FPGA signals are routed on the general purpose routing, and consequently, the majority of interconnect resources are associated with this level of the routing hierarchy. The general routing resources are located in horizontal and vertical routing channels associated with the rows and columns CLBs. The general-purpose routing resources are listed below.

- Adjacent to each CLB is a General Routing Matrix (GRM). The GRM is the switch matrix through which horizontal and vertical routing resources connect, and is also the means by which the CLB gains access to the general purpose routing.
- 24 single-length lines route GRM signals to adjacent GRMs in each of the four directions.
- 96 buffered Hex lines route GRM signals to other GRMs six blocks away in each one of the four directions. Organized in a staggered pattern, Hex lines may be driven only at their endpoints. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source). One third of the Hex lines are bidirectional, while the remaining ones are unidirectional.
- 12 Longlines are buffered, bidirectional wires that distribute signals across the device quickly and efficiently. Vertical Longlines span the full height of the device, and horizontal ones span the full width of the device.

### *I/O Routing*

Spartan-II devices have additional routing resources around their periphery that form an interface between the CLB array and the IOBs. This additional routing, called the VersaRing, facilitates pin-swapping and pin-locking, such that logic redesigns can adapt to existing PCB layouts. Time-to-market is reduced, since PCBs and other system components can be manufactured while the logic design is still in progress.

### *Dedicated Routing*

Some classes of signal require dedicated routing resources to maximize performance. In the Spartan-II architecture, dedicated routing resources are provided for two classes of signal.

- Horizontal routing resources are provided for on-chip 3-state busses. Four partitionable bus lines are provided per CLB row, permitting multiple busses within a row, as shown in Figure 7.
- Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB.

## Global Routing

Global Routing resources distribute clocks and other signals with very high fanout throughout the device. Spartan-II devices include two tiers of global routing resources referred to as primary and secondary global routing resources.

- The primary global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The primary global nets may only be driven by global buffers. There are four global buffers, one for each global net.
- The secondary global routing resources consist of 24 backbone lines, 12 across the top of the chip and 12 across bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These secondary resources are more flexible than the primary resources since they are not restricted to routing only to clock pins.

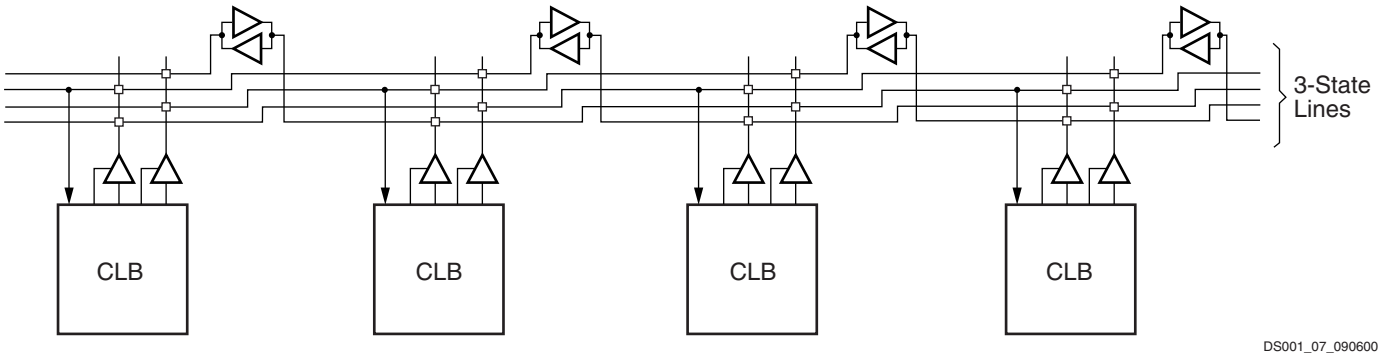


*Figure 7:* **BUFT Connections to Dedicated Horizontal Bus Lines**

## Clock Distribution

The Spartan-II family provides high-speed, low-skew clock distribution through the primary global routing resources described above. A typical clock distribution net is shown in Figure 8.

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four primary global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing. Global clock pins do not have the option for internal, weak pull-up resistors.

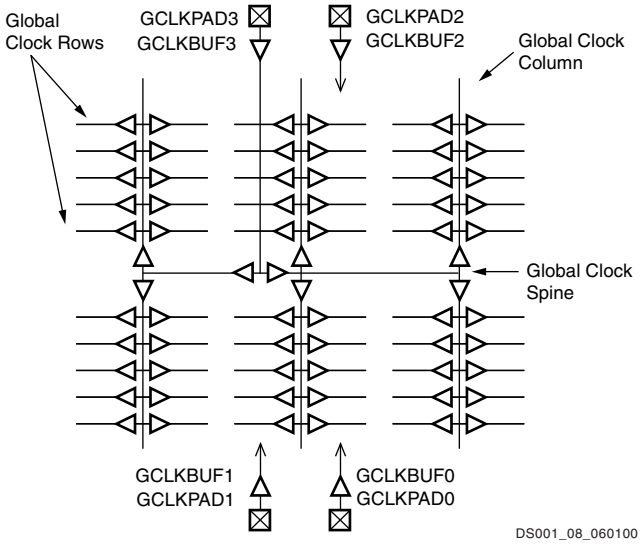


*Figure 8:* **Global Clock Distribution Network**

### *Delay-Locked Loop (DLL)*

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks. The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Additional delay is introduced such that clock edges reach internal flip-flops exactly one clock period after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16. It has six outputs.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to deskew a board level clock among multiple Spartan-II devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock.

## Boundary Scan

Spartan-II devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, SAMPLE/PRELOAD, and BYPASS instructions. The TAP also supports two USERCODE instructions and internal scan chains.

The TAP uses dedicated package pins that always operate using LVTTL. For TDO to operate using LVTTL, the $V_{CCO}$ for Bank 2 must be 3.3V. Otherwise, TDO switches rail-to-rail between ground and $V_{CCO}$. TDI, TMS, and TCK have a default internal weak pull-up resistor, and TDO has no default resistor. Bitstream options allow setting any of the four TAP pins to have an internal pull-up, pull-down, or neither.

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Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including unbonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections.

Table 7 lists the boundary-scan instructions supported in Spartan-II FPGAs. Internal signals can be captured during EXTEST by connecting them to unbonded or unused IOBs. They may also be connected to the unused outputs of IOBs defined as unidirectional input pins.

*Table 7:* **Boundary-Scan Instructions**

| Boundary-Scan Command | Binary Code[4:0] | Description |
|---|---|---|
| EXTEST | 00000 | Enables boundary-scan EXTEST operation |
| SAMPLE | 00001 | Enables boundary-scan SAMPLE operation |
| USR1 | 00010 | Access user-defined register 1 |
| USR2 | 00011 | Access user-defined register 2 |
| CFG_OUT | 00100 | Access the configuration bus for Readback |
| CFG_IN | 00101 | Access the configuration bus for Configuration |
| INTEST | 00111 | Enables boundary-scan INTEST operation |
| USRCODE | 01000 | Enables shifting out USER code |
| IDCODE | 01001 | Enables shifting out of ID Code |
| HIZ | 01010 | Disables output pins while enabling the Bypass Register |
| JSTART | 01100 | Clock the start-up sequence when StartupClk is TCK |
| BYPASS | 11111 | Enables BYPASS |
| RESERVED | All other codes | Xilinx® reserved instructions |

The public boundary-scan instructions are available prior to configuration. After configuration, the public instructions remain available together with any USERCODE instructions installed during the configuration. While the SAMPLE and BYPASS instructions are available during configuration, it is recommended that boundary-scan operations not be performed during this transitional period.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

To facilitate internal scan chains, the User Register provides three outputs (Reset, Update, and Shift) that represent the corresponding states in the boundary-scan internal state machine.

Figure 9 is a diagram of the Spartan-II family boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

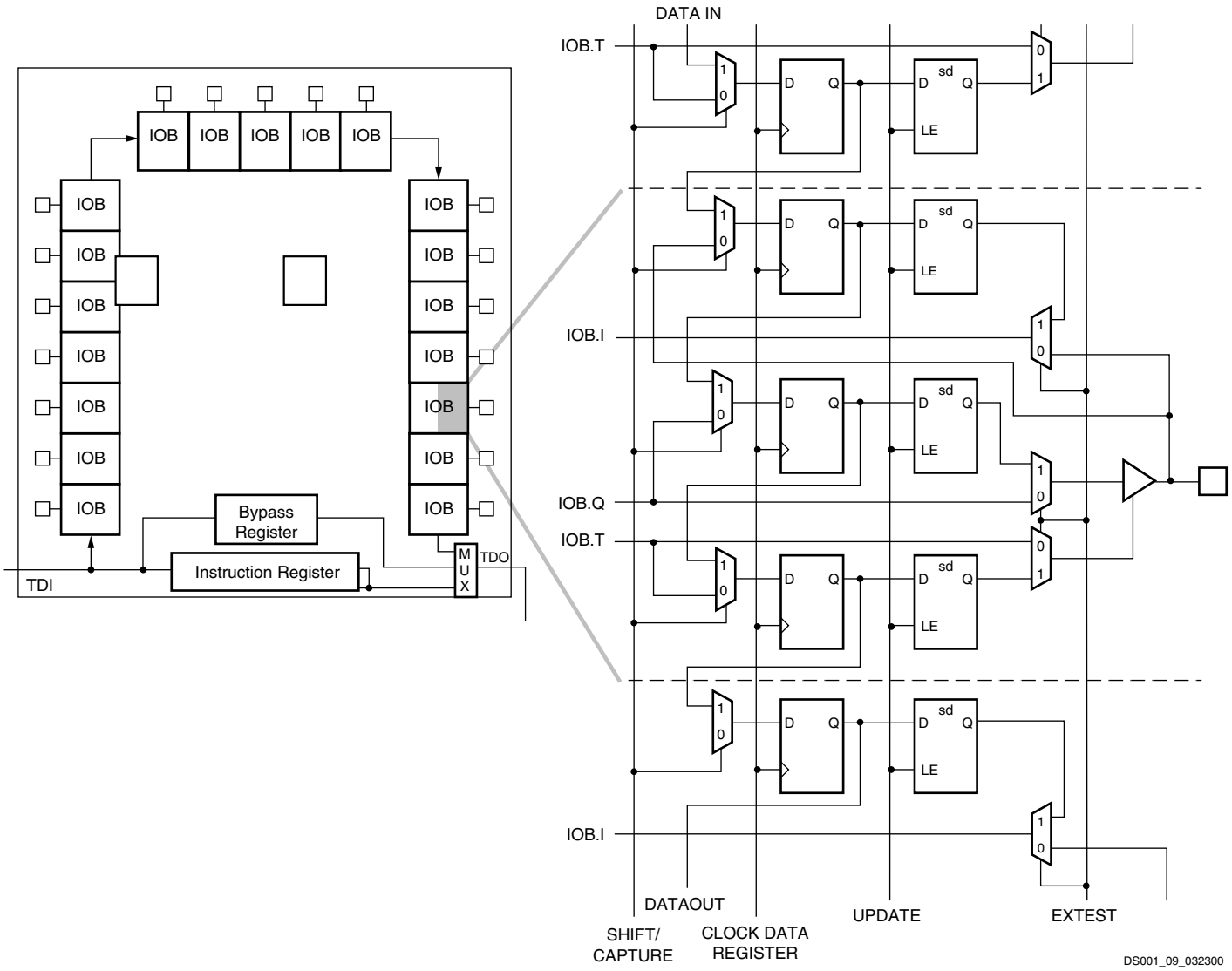


*Figure 9:* **Spartan-II Family Boundary Scan Logic**

### *Bit Sequence*

The bit sequence within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

From a cavity-up view of the chip (as shown in the FPGA Editor), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 10.

BSDL (Boundary Scan Description Language) files for Spartan-II family devices are available on the Xilinx website, in the Downloads area.

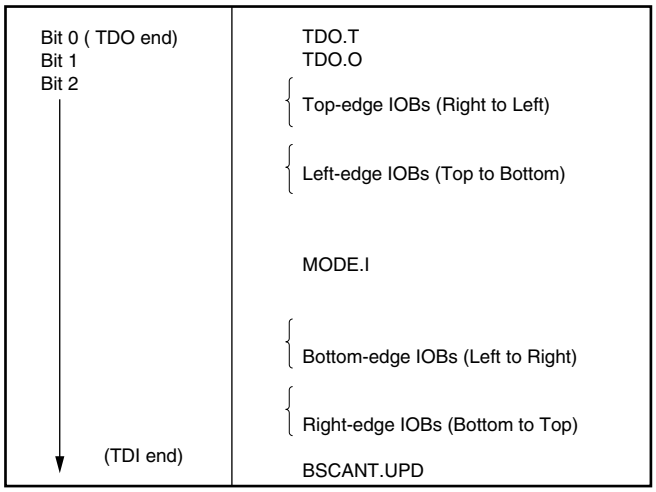


*Figure 10:* **Boundary Scan Bit Sequence**

## Development System

Spartan-II FPGAs are supported by the Xilinx ISE® development tools. The basic methodology for Spartan-II FPGA design consists of three interrelated steps: design entry, implementation, and verification. Industry-standard tools are used for design entry and simulation, while Xilinx provides proprietary architecture-specific tools for implementation.

The Xilinx development system is integrated under a single graphical interface, providing designers with a common user interface regardless of their choice of entry and verification tools. The software simplifies the selection of implementation options with pull-down menus and on-line help.

For HDL design entry, the Xilinx FPGA development system provides interfaces to several synthesis design environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Spartan-II FPGAs supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The design environment supports hierarchical design entry. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical design, thus allowing the most convenient entry method to be used for each portion of the design.

### Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF netlist for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floorplanning.

The implementation software incorporates timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

Timing requirements are entered in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

### Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the netlist for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the static timing analyzer.

For in-circuit debugging, the development system includes a download cable, which connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can read back the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

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# Configuration

Configuration is the process by which the bitstream of a design, as generated by the Xilinx software, is loaded into the internal configuration memory of the FPGA. Spartan-II devices support both serial configuration, using the master/slave serial and JTAG modes, as well as byte-wide configuration employing the Slave Parallel mode.

## Configuration File

Spartan-II devices are configured by sequentially loading frames of data that have been concatenated into a configuration file. Table 8 shows how much nonvolatile storage space is needed for Spartan-II devices.

It is important to note that, while a PROM is commonly used to store configuration data before loading them into the FPGA, it is by no means required. Any of a number of different kinds of under populated nonvolatile storage already available either on or off the board (i.e., hard drives, FLASH cards, etc.) can be used. For more information on configuration without a PROM, refer to XAPP098, *The Low-Cost, Efficient Serial Configuration of Spartan FPGAs*.

*Table 8:* **Spartan-II Configuration File Size**

| Device | Configuration File Size (Bits) |
|---|---|
| XC2S15 | 197,696 |
| XC2S30 | 336,768 |
| XC2S50 | 559,200 |
| XC2S100 | 781,216 |
| XC2S150 | 1,040,096 |
| XC2S200 | 1,335,840 |

## Modes

Spartan-II devices support the following four configuration modes:

- Slave Serial mode
- Master Serial mode
- Slave Parallel mode
- Boundary-scan mode

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to the end of configuration. The selection codes are listed in Table 9.

Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected.

*Table 9:* **Configuration Modes**

| Configuration Mode | Preconfiguration Pull-ups | M0 | M1 | M2 | CCLK Direction | Data Width | Serial $D_{OUT}$ |
|---|---|---|---|---|---|---|---|
| Master Serial mode | No | 0 | 0 | 0 | Out | 1 | Yes |
| | Yes | 0 | 0 | 1 | | | |
| Slave Parallel mode | Yes | 0 | 1 | 0 | In | 8 | No |
| | No | 0 | 1 | 1 | | | |
| Boundary-Scan mode | Yes | 1 | 0 | 0 | N/A | 1 | No |
| | No | 1 | 0 | 1 | | | |
| Slave Serial mode | Yes | 1 | 1 | 0 | In | 1 | Yes |
| | No | 1 | 1 | 1 | | | |

**Notes:**
1. During power-on and throughout configuration, the I/O drivers will be in a high-impedance state. After configuration, all unused I/Os (those not assigned signals) will remain in a high-impedance state. Pins used as outputs may pulse High at the end of configuration (see Answer 10504).
2. If the Mode pins are set for preconfiguration pull-ups, those resistors go into effect once the rising edge of INIT samples the Mode pins. They will stay in effect until GTS is released during startup, after which the UnusedPin bitstream generator option will determine whether the unused I/Os have a pull-up, pull-down, or no resistor.

## Signals

There are two kinds of pins that are used to configure Spartan-II devices: Dedicated pins perform only specific configuration-related functions; the other pins can serve as general purpose I/Os once user operation has begun.

The dedicated pins comprise the mode pins (M2, M1, M0), the configuration clock pin (CCLK), the $\overline{\text{PROGRAM}}$ pin, the DONE pin and the boundary-scan pins (TDI, TDO, TMS, TCK). Depending on the selected configuration mode, CCLK may be an output generated by the FPGA, or may be generated externally, and provided to the FPGA as an input.

Note that some configuration pins can act as outputs. For correct operation, these pins require a $V_{CCO}$ of 3.3V to drive an LVTTL signal or 2.5V to drive an LVCMOS signal. All the relevant pins fall in banks 2 or 3. The $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$ pins for Slave Parallel mode are located in bank 1.

For a more detailed description than that given below, see "Pinout Tables" in Module 4 and XAPP176, *Spartan-II FPGA Series Configuration and Readback*.

## The Process

The sequence of steps necessary to configure Spartan-II devices are shown in Figure 11. The overall flow can be divided into three different phases.

- Initiating Configuration
- Configuration memory clear
- Loading data frames
- Start-up

The memory clearing and start-up phases are the same for all configuration modes; however, the steps for the loading of data frames are different. Thus, the details for data frame loading are described separately in the sections devoted to each mode.

### *Initiating Configuration*

There are two different ways to initiate the configuration process: applying power to the device or asserting the $\overline{\text{PROGRAM}}$ input.

Configuration on power-up occurs automatically unless it is delayed by the user, as described in a separate section below. The waveform for configuration on power-up is shown in Figure 12, page 19. Before configuration can begin, $V_{CCO}$ Bank 2 must be greater than 1.0V. Furthermore, all $V_{CCINT}$ power pins must be connected to a 2.5V supply. For more information on delaying configuration, see "Clearing Configuration Memory," page 19.

Once in user operation, the device can be re-configured simply by pulling the $\overline{\text{PROGRAM}}$ pin Low. The device acknowledges the beginning of the configuration process by driving DONE Low, then enters the memory-clearing phase.

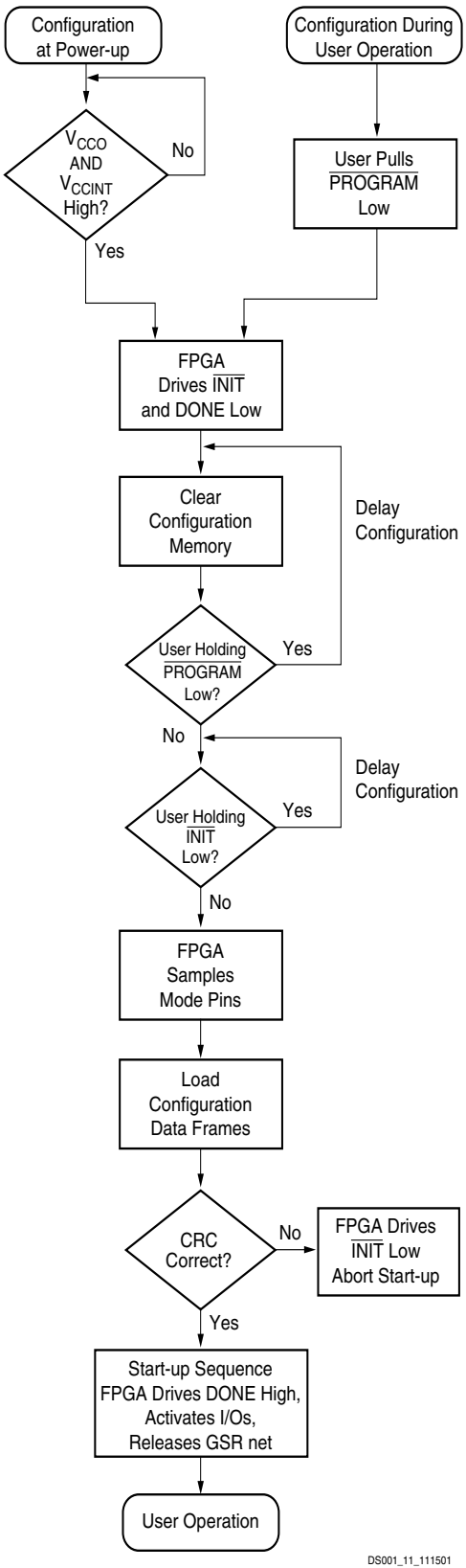
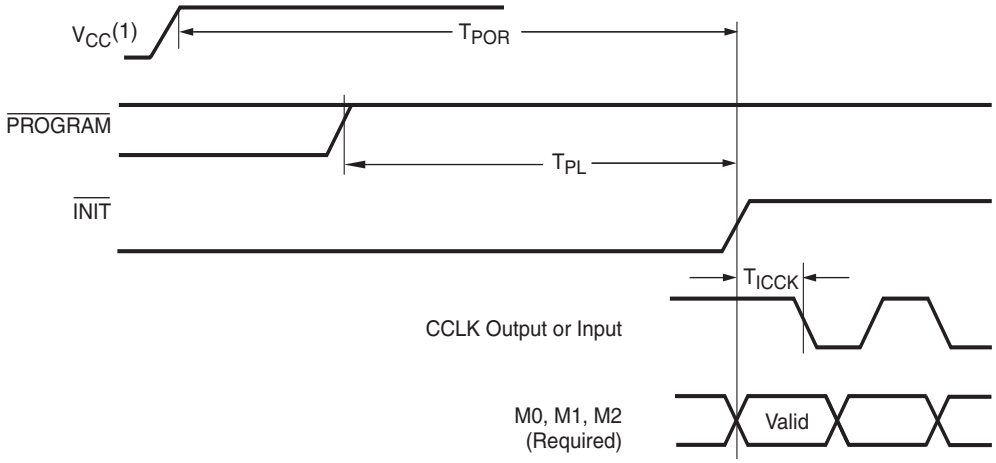



*Figure 11:* **Configuration Flow Diagram**




| Symbol | Description | Min | Max |
|---|---|---|---|
| $T_{POR}$ | Power-on reset | - | 2 ms |
| $T_{PL}$ | Program latency | - | 100 µs |
| $T_{ICCK}$ | CCLK output delay (Master Serial mode only) | 0.5 µs | 4 µs |
| $T_{PROGRAM}$ | Program pulse width | 300 ns | - |

**Notes: (referring to waveform above)**
1. Before configuration can begin, $V_{CCINT}$ must be greater than 1.6V and $V_{CCO}$ Bank 2 must be greater than 1.0V.

*Figure 12:* **Configuration Timing on Power-Up**

### *Clearing Configuration Memory*

The device indicates that clearing the configuration memory is in progress by driving $\overline{INIT}$ Low. At this time, the user can delay configuration by holding either $\overline{PROGRAM}$ or $\overline{INIT}$ Low, which causes the device to remain in the memory clearing phase. Note that the bidirectional $\overline{INIT}$ line is driving a Low logic level during memory clearing. To avoid contention, use an open-drain driver to keep $\overline{INIT}$ Low.

With no delay in force, the device indicates that the memory is completely clear by driving $\overline{INIT}$ High. The FPGA samples its mode pins on this Low-to-High transition.

### *Loading Configuration Data*

Once $\overline{INIT}$ is High, the user can begin loading configuration data frames into the device. The details of loading the configuration data are discussed in the sections treating the configuration modes individually. The sequence of operations necessary to load configuration data using the serial modes is shown in Figure 14. Loading data using the Slave Parallel mode is shown in Figure 19, page 25.

#### CRC Error Checking

During the loading of configuration data, a CRC value embedded in the configuration file is checked against a CRC value calculated within the FPGA. If the CRC values do not match, the FPGA drives $\overline{INIT}$ Low to indicate that a frame error has occurred and configuration is aborted.

To reconfigure the device, the $\overline{PROGRAM}$ pin should be asserted to reset the configuration logic. Recycling power also resets the FPGA for configuration. See "Clearing Configuration Memory".

### *Start-up*

The start-up sequence oversees the transition of the FPGA from the configuration state to full user operation. A match of CRC values, indicating a successful loading of the configuration data, initiates the sequence.

During start-up, the device performs four operations:

1. The assertion of DONE. The failure of DONE to go High may indicate the unsuccessful loading of configuration data.
2. The release of the Global Three State net. This activates I/Os to which signals are assigned. The remaining I/Os stay in a high-impedance state with internal weak pull-down resistors present.
3. Negates Global Set Reset (GSR). This allows all flip-flops to change state.
4. The assertion of Global Write Enable (GWE). This allows all RAMs and flip-flops to change state.

By default, these operations are synchronized to CCLK. The entire start-up sequence lasts eight cycles, called C0-C7, after which the loaded design is fully functional. The default timing for start-up is shown in the top half of Figure 13. The four operations can be selected to switch on any CCLK cycle C1-C6 through settings in the Xilinx software. Heavy lines show default settings.

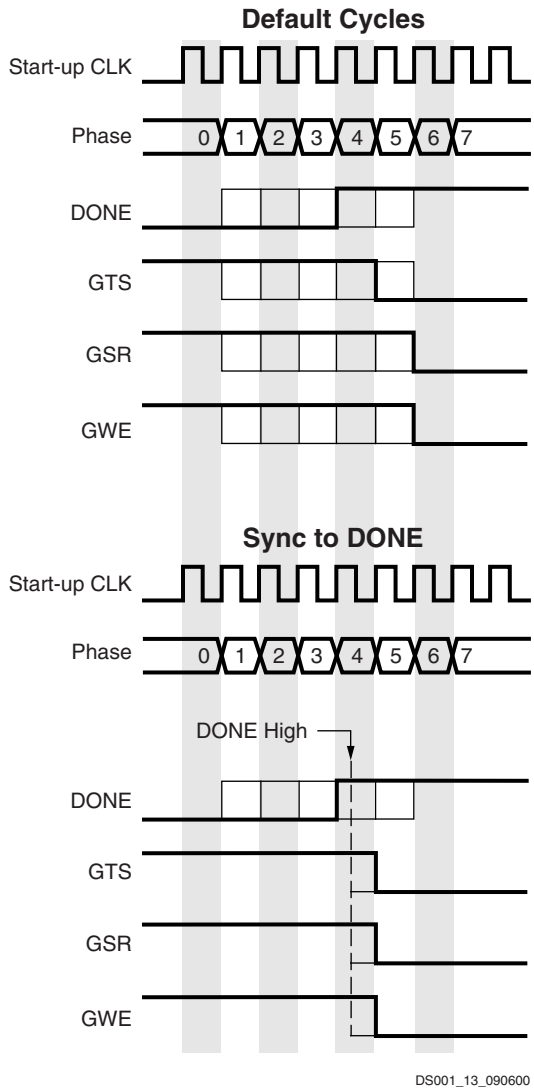



*Figure 13:* **Start-Up Waveforms**

The bottom half of Figure 13 shows another commonly used version of the start-up timing known as Sync-to-DONE. This version makes the GTS, GSR, and GWE events conditional upon the DONE pin going High. This timing is important for a daisy chain of multiple FPGAs in serial mode, since it ensures that all FPGAs go through start-up together, after all their DONE pins have gone High.

Sync-to-DONE timing is selected by setting the GTS, GSR, and GWE cycles to a value of DONE in the configuration options. This causes these signals to transition one clock cycle after DONE externally transitions High.

## Serial Modes

There are two serial configuration modes: In Master Serial mode, the FPGA controls the configuration process by driving CCLK as an output. In Slave Serial mode, the FPGA passively receives CCLK as an input from an external agent (e.g., a microprocessor, CPLD, or second FPGA in master mode) that is controlling the configuration process. In both modes, the FPGA is configured by loading one bit per CCLK cycle. The MSB of each configuration data byte is always written to the DIN pin first.

See Figure 14 for the sequence for loading data into the Spartan-II FPGA serially. This is an expansion of the "Load Configuration Data Frames" block in Figure 11. Note that $\overline{CS}$ and $\overline{WRITE}$ normally are not used during serial configuration. To ensure successful loading of the FPGA, do not toggle $\overline{WRITE}$ with $\overline{CS}$ Low during serial configuration.

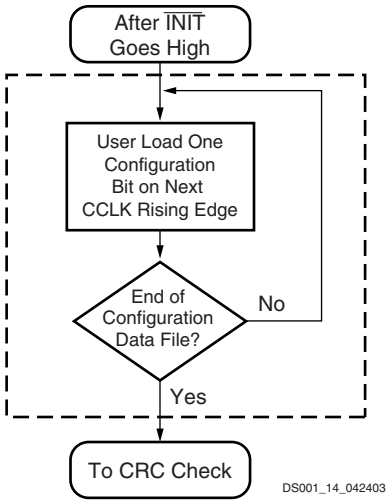



*Figure 14:* **Loading Serial Mode Configuration Data**

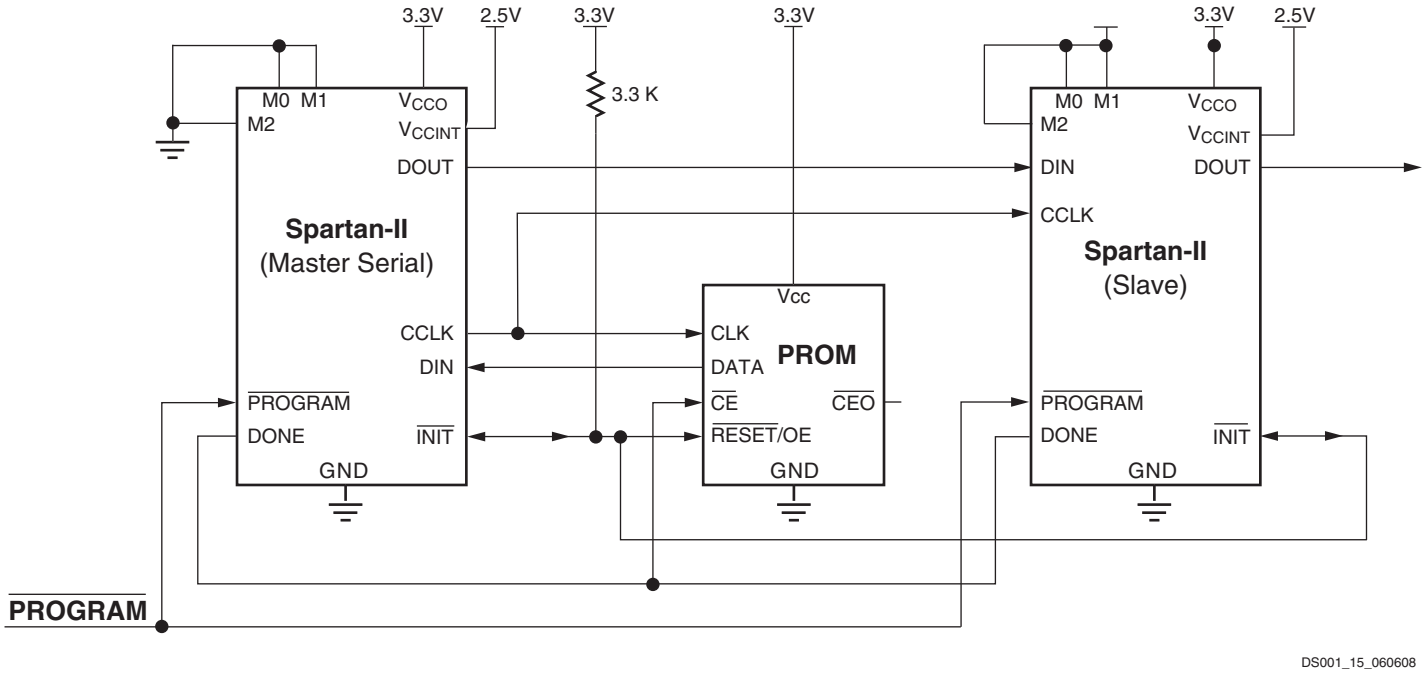
### *Slave Serial Mode*

In Slave Serial mode, the FPGA's CCLK pin is driven by an external source, allowing FPGAs to be configured from other logic devices such as microprocessors or in a daisy-chain configuration. Figure 15 shows connections for a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-II device in slave serial mode should be connected as shown for the third device from the left. Slave Serial mode is selected by a <11x> on the mode pins (M0, M1, M2).

Figure 16 shows the timing for Slave Serial configuration. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.

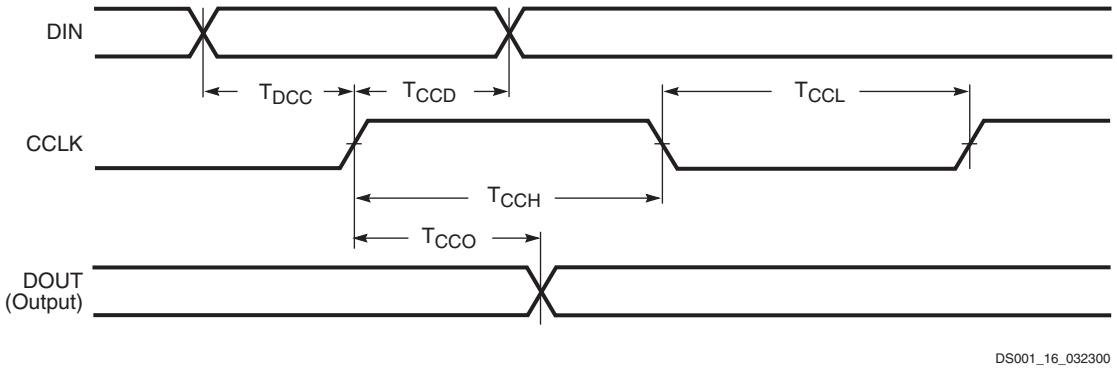
Multiple FPGAs in Slave Serial mode can be daisy-chained for configuration from a single source. The maximum amount of data that can be sent to the DOUT pin for a serial daisy chain is $2^{20}$-1 (1,048,575) 32-bit words, or 33,554,400 bits, which is approximately 25 XC2S200 bitstreams. The configuration bitstream of downstream devices is limited to this size.

After an FPGA is configured, data for the next device is routed to the DOUT pin. Data on the DOUT pin changes on the rising edge of CCLK. Configuration must be delayed until $\overline{\text{INIT}}$ pins of all daisy-chained FPGAs are High. For more information, see "Start-up," page 19.




**Notes:**
1. If the DriveDone configuration option is not active for any of the FPGAs, pull up DONE with a 330Ω resistor.

*Figure 15:* **Master/Slave Serial Configuration Circuit Diagram**



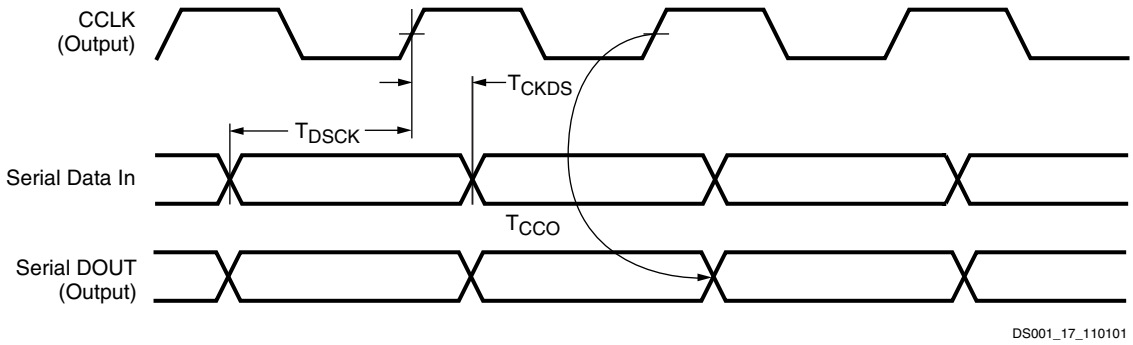

| Symbol | | Description | | Units |
|---|---|---|---|---|
| $T_{DCC}$ | CCLK | DIN setup | 5 | ns, min |
| $T_{CCD}$ | | DIN hold | 0 | ns, min |
| $T_{CCO}$ | | DOUT | 12 | ns, max |
| $T_{CCH}$ | | High time | 5 | ns, min |
| $T_{CCL}$ | | Low time | 5 | ns, min |
| $F_{CC}$ | | Maximum frequency | 66 | MHz, max |

*Figure 16:* **Slave Serial Mode Timing**

### *Master Serial Mode*

In Master Serial mode, the CCLK output of the FPGA drives a Xilinx PROM which feeds a serial stream of configuration data to the FPGA's DIN input. Figure 15 shows a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-II device in Master Serial mode should be connected as shown for the device on the left side. Master Serial mode is selected by a <00x> on the mode pins (M0, M1, M2). The PROM RESET pin is driven by $\overline{\text{INIT}}$, and CE input is driven by DONE. The interface is identical to the slave serial mode except that an oscillator internal to the FPGA is used to generate the configuration clock (CCLK). Any of a number of different frequencies ranging from 4 to 60 MHz can be set using the ConfigRate option in the Xilinx software. On power-up, while the first 60 bytes of the configuration data are being loaded, the CCLK frequency is always 2.5 MHz. This frequency is used until the ConfigRate bits, part of the configuration file, have been loaded into the FPGA, at which point, the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz. The frequency of the CCLK signal created by the internal oscillator has a variance of +45%, –30% from the specified value.

Figure 17 shows the timing for Master Serial configuration. The FPGA accepts one bit of configuration data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge.




| Symbol | | Description | | Units |
|---|---|---|---|---|
| $T_{DSCK}$ | CCLK | DIN setup | 5.0 | ns, min |
| $T_{CKDS}$ | | DIN hold | 0.0 | ns, min |
| | | Frequency tolerance with respect to nominal | +45%, –30% | - |

*Figure 17:* **Master Serial Mode Timing**

## Slave Parallel Mode

The Slave Parallel mode is the fastest configuration option. Byte-wide data is written into the FPGA. A BUSY flag is provided for controlling the flow of data at a clock frequency $F_{CCNH}$ above 50 MHz.

Figure 18, page 24 shows the connections for two Spartan-II devices using the Slave Parallel mode. Slave Parallel mode is selected by a <011> on the mode pins (M0, M1, M2).

If a configuration file of the format .bit, .rbt, or non-swapped HEX is used for parallel programming, then the most significant bit (i.e. the left-most bit of each configuration byte, as displayed in a text editor) must be routed to the D0 input on the FPGA.

The agent controlling configuration is not shown. Typically, a processor, a microcontroller, or CPLD controls the Slave Parallel interface. The controlling agent provides byte-wide configuration data, CCLK, a Chip Select ($\overline{\text{CS}}$) signal and a Write signal ($\overline{\text{WRITE}}$). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

After configuration, the pins of the Slave Parallel port (D0-D7) can be used as additional user I/O. Alternatively, the port may be retained to permit high-speed 8-bit readback. Then data can be read by de-asserting $\overline{\text{WRITE}}$. See "Readback," page 25.

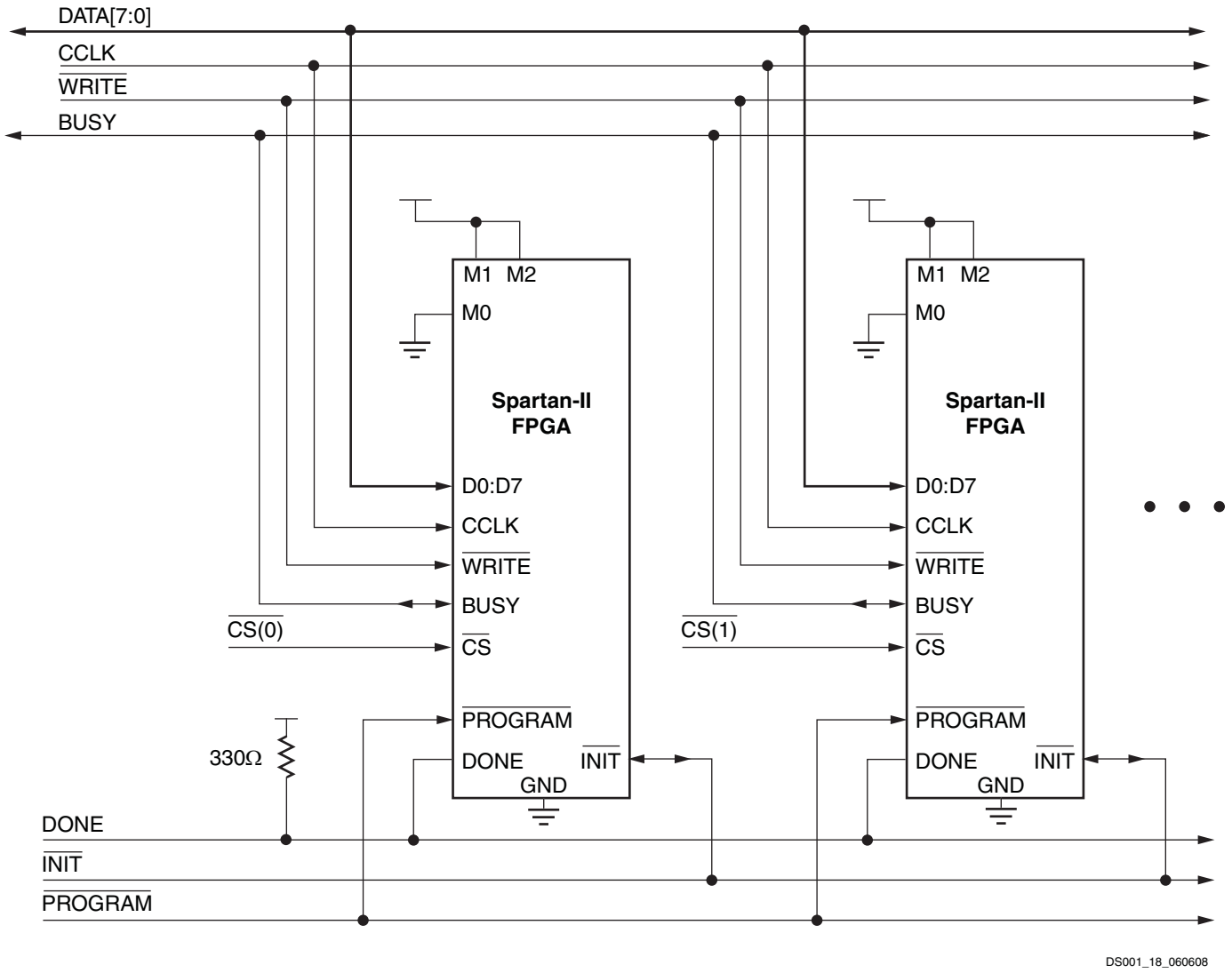



*Figure 18:* **Slave Parallel Configuration Circuit Diagram**

Multiple Spartan-II FPGAs can be configured using the Slave Parallel mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, $\overline{\text{WRITE}}$, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the $\overline{\text{CS}}$ pin of each device in turn and writing the appropriate data. Sync-to-DONE start-up timing is used to ensure that the start-up sequence does not begin until all the FPGAs have been loaded. See "Start-up," page 19.

### *Write*

When using the Slave Parallel Mode, write operations send packets of byte-wide configuration data into the FPGA. Figure 19, page 25 shows a flowchart of the write sequence used to load data into the Spartan-II FPGA. This is an expansion of the "Load Configuration Data Frames" block in Figure 11, page 18. The timing for write operations is shown in Figure 20, page 26.

For the present example, the user holds $\overline{\text{WRITE}}$ and $\overline{\text{CS}}$ Low throughout the sequence of write operations. Note that when $\overline{\text{CS}}$ is asserted on successive CCLKs, $\overline{\text{WRITE}}$ must remain either asserted or de-asserted. Otherwise an abort will be initiated, as in the next section.

1. Drive data onto D0-D7. Note that to avoid contention, the data source should not be enabled while $\overline{\text{CS}}$ is Low and $\overline{\text{WRITE}}$ is High. Similarly, while $\overline{\text{WRITE}}$ is High, no more than one device's $\overline{\text{CS}}$ should be asserted.
2. On the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this happens.
3. Repeat steps 1 and 2 until all the data has been sent.
4. De-assert $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$.

If CCLK is slower than $F_{CCNH}$, the FPGA will never assert BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

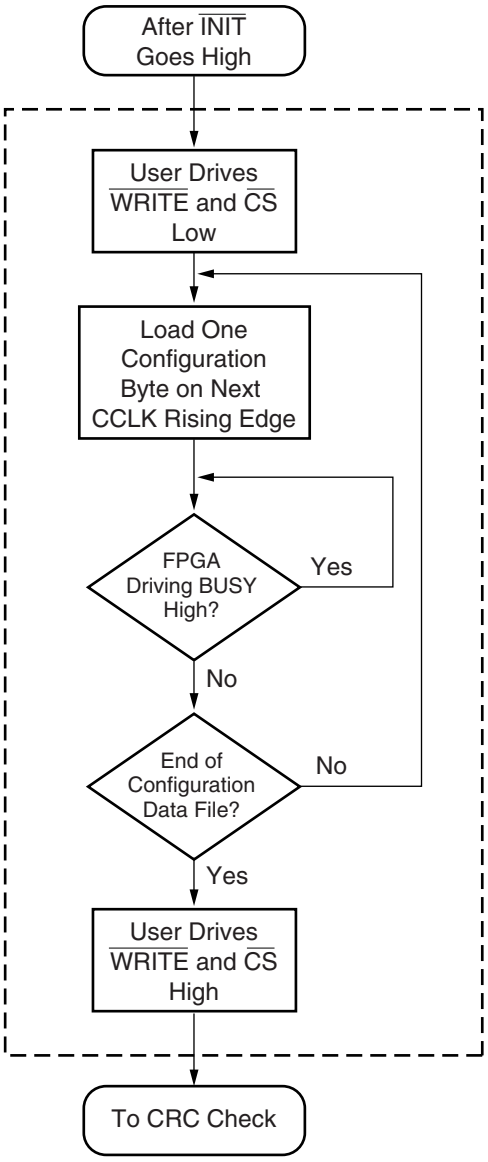



*Figure 19:* **Loading Configuration Data for the Slave Parallel Mode**

A configuration packet does not have to be written in one continuous stretch, rather it can be split into many write sequences. Each sequence would involve assertion of $\overline{CS}$.

In applications where multiple clock cycles may be required to access the configuration data before each byte can be loaded into the Slave Parallel interface, a new byte of data may not be ready for each consecutive CCLK edge. In such a case the $\overline{CS}$ signal may be de-asserted until the next byte is valid on D0-D7. While $\overline{CS}$ is High, the Slave Parallel interface does not expect any data and ignores all CCLK transitions. However, to avoid aborting configuration, $\overline{WRITE}$ must continue to be asserted while $\overline{CS}$ is asserted.

### *Abort*

To abort configuration during a write sequence, de-assert $\overline{WRITE}$ while holding $\overline{CS}$ Low. The abort operation is initiated at the rising edge of CCLK, as shown in Figure 21, page 26. The device will remain BUSY until the aborted operation is complete. After aborting configuration, data is assumed to be unaligned to word boundaries and the FPGA requires a new synchronization word prior to accepting any new packets.

## Boundary-Scan Mode

In the boundary-scan mode, no nondedicated pins are required, configuration being done entirely through the IEEE 1149.1 Test Access Port.

Configuration through the TAP uses the special CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port.

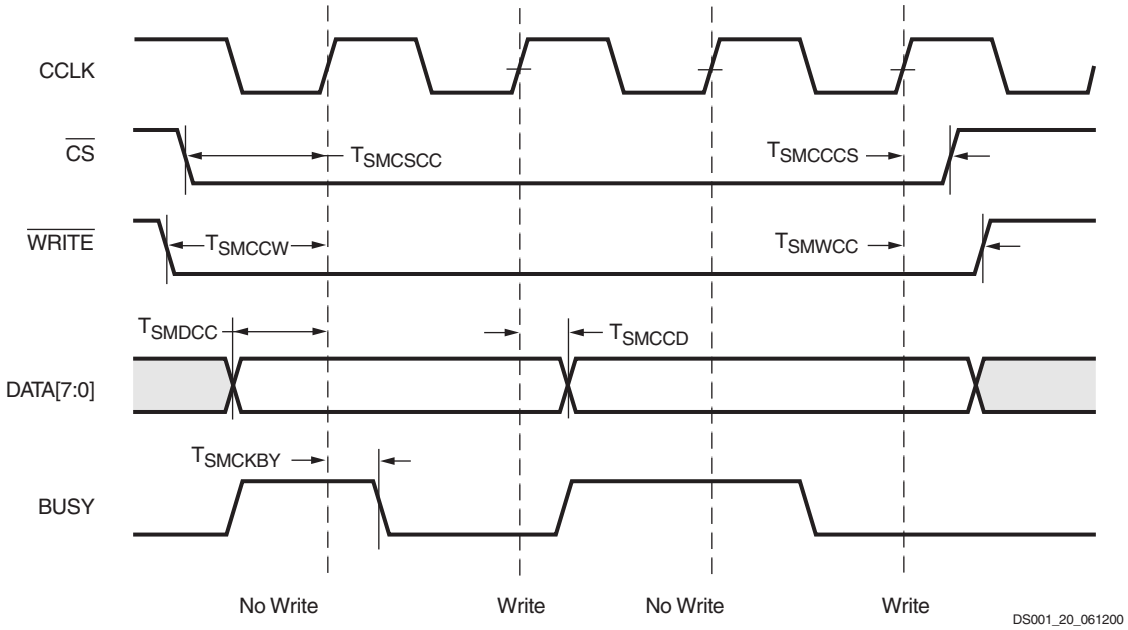
1. Load the CFG_IN instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a standard configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the JSTART instruction into IR
6. Enter the SDR state
7. Clock TCK through the sequence (the length is programmable)
8. Return to RTI

Configuration and readback via the TAP is always available. The boundary-scan mode simply locks out the other modes. The boundary-scan mode is selected by a <10x> on the mode pins (M0, M1, M2).

# Readback

The configuration data stored in the Spartan-II FPGA configuration memory can be readback for verification. Along with the configuration data it is possible to readback the contents of all flip-flops/latches, LUT RAMs, and block RAMs. This capability is used for real-time debugging.

For more detailed information see XAPP176, *Spartan-II FPGA Family Configuration and Readback.*




| Symbol | | Description | | Units |
|---|---|---|---|---|
| $T_{SMDCC}$ | CCLK | D0-D7 setup/hold | 5 | ns, min |
| $T_{SMCCD}$ | | D0-D7 hold | 0 | ns, min |
| $T_{SMCSCC}$ | | $\overline{CS}$ setup | 7 | ns, min |
| $T_{SMCCCS}$ | | $\overline{CS}$ hold | 0 | ns, min |
| $T_{SMCCW}$ | | $\overline{WRITE}$ setup | 7 | ns, min |
| $T_{SMWCC}$ | | $\overline{WRITE}$ hold | 0 | ns, min |
| $T_{SMCKBY}$ | | BUSY propagation delay | 12 | ns, max |
| $F_{CC}$ | | Maximum frequency | 66 | MHz, max |
| $F_{CCNH}$ | | Maximum frequency with no handshake | 50 | MHz, max |

*Figure 20:* **Slave Parallel Write Timing**

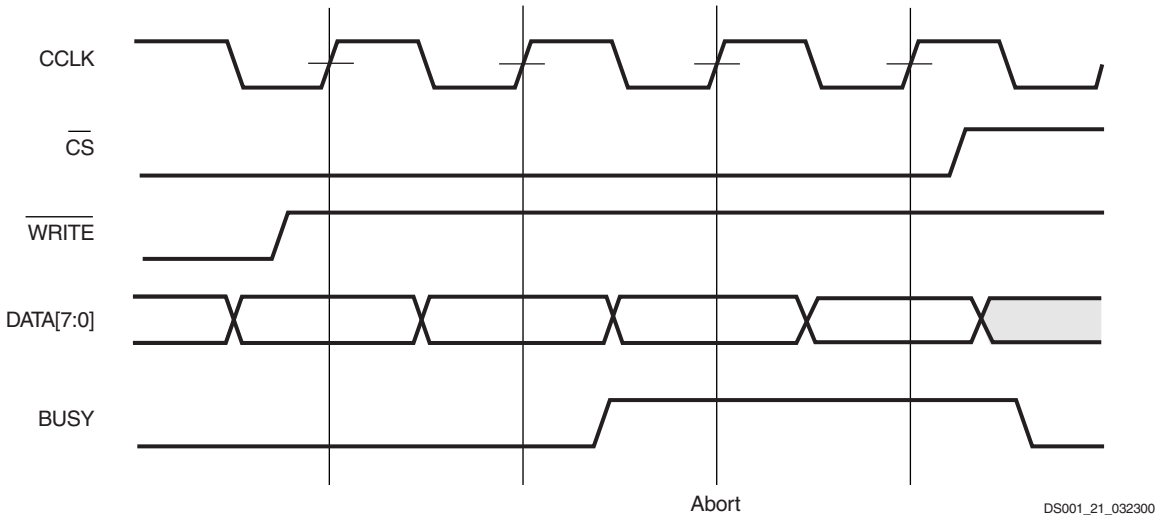



*Figure 21:* **Slave Parallel Write Abort Waveforms**

# Design Considerations

This section contains more detailed design information on the following features:


- Delay-Locked Loop . . . see page 27
- Block RAM . . . see page 32
- Versatile I/O . . . see page 36


# Using Delay-Locked Loops

The Spartan-II FPGA family provides up to four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay, low clock skew between output clock signals distributed throughout the device, and advanced clock domain control. These dedicated DLLs can be used to implement several circuits that improve and simplify system level design.

## Introduction

Quality on-chip clock distribution is important. Clock skew and clock delay impact device performance and the task of managing clock skew and clock delay with conventional clock trees becomes more difficult in large devices. The Spartan-II family of devices resolve this potential problem by providing up to four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay and low clock skew between output clock signals distributed throughout the device.

Each DLL can drive up to two global clock routing networks within the device. The global clock distribution network minimizes clock skews due to loading differences. By monitoring a sample of the DLL output clock, the DLL can compensate for the delay on the routing network, effectively eliminating the delay from the external input port to the individual clock loads within the device.

In addition to providing zero delay with respect to a user source clock, the DLL can provide multiple phases of the source clock. The DLL can also act as a clock doubler or it can divide the user source clock by up to 16.

Clock multiplication gives the designer a number of design alternatives. For instance, a 50 MHz source clock doubled by the DLL can drive an FPGA design operating at 100 MHz. This technique can simplify board design because the clock path on the board no longer distributes such a high-speed signal. A multiplied clock also provides designers the option of time-domain-multiplexing, using one circuit twice per clock cycle, consuming less area than two copies of the same circuit.

The DLL can also act as a clock mirror. By driving the DLL output off-chip and then back in again, the DLL can be used to de-skew a board level clock between multiple devices.

In order to guarantee the system clock establishes prior to the device "waking up," the DLL can delay the completion of the device configuration process until after the DLL achieves lock.

By taking advantage of the DLL to remove on-chip clock delay, the designer can greatly simplify and improve system level design involving high-fanout, high-performance clocks.

## Library DLL Primitives

Figure 22 shows the simplified Xilinx library DLL macro, BUFGDLL. This macro delivers a quick and efficient way to provide a system clock with zero propagation delay throughout the device. Figure 23 and Figure 24 show the two library DLL primitives. These primitives provide access to the complete set of DLL features when implementing more complex applications.

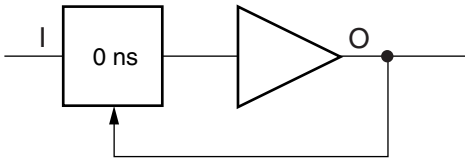



*Figure 22:* **Simplified DLL Macro BUFGDLL**

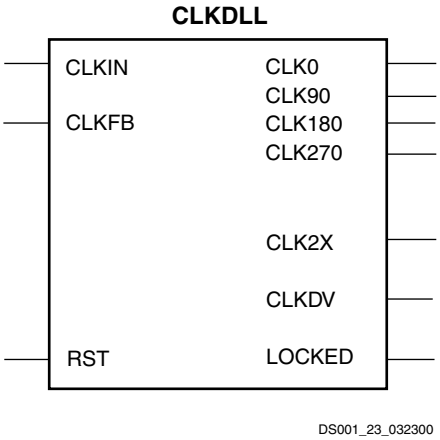



*Figure 23:* **Standard DLL Primitive CLKDLL**

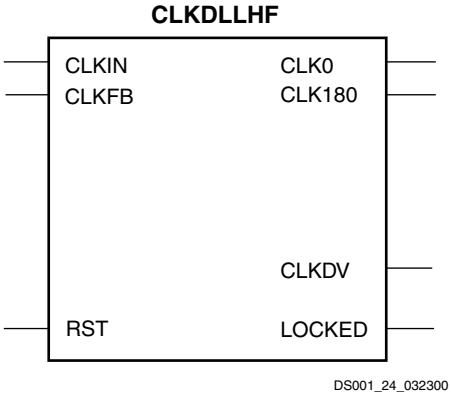



*Figure 24:* **High-Frequency DLL Primitive CLKDLLHF**

## BUFGDLL Pin Descriptions

Use the BUFGDLL macro as the simplest way to provide zero propagation delay for a high-fanout on-chip clock from an external input. This macro uses the IBUFG, CLKDLL and BUFG primitives to implement the most basic DLL application as shown in Figure 25.

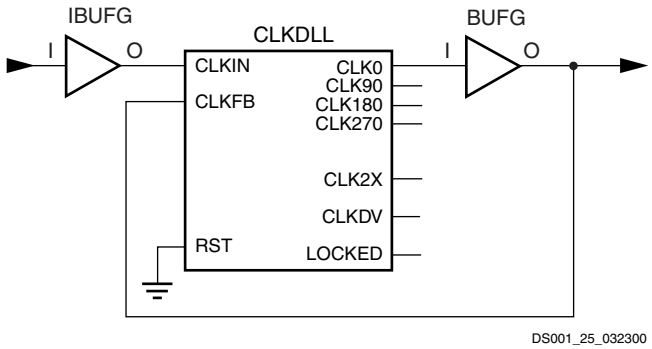



*Figure 25:* **BUFGDLL Block Diagram**

This macro does not provide access to the advanced clock domain controls or to the clock multiplication or clock division features of the DLL. This macro also does not provide access to the RST or LOCKED pins of the DLL. For access to these features, a designer must use the DLL primitives described in the following sections.

### *Source Clock Input — I*

The I pin provides the user source clock, the clock signal on which the DLL operates, to the BUFGDLL. For the BUFGDLL macro the source clock frequency must fall in the low frequency range as specified in the data sheet. The BUFGDLL requires an external signal source clock. Therefore, only an external input port can source the signal that drives the BUFGDLL I pin.

### *Clock Output — O*

The clock output pin O represents a delay-compensated version of the source clock (I) signal. This signal, sourced by a global clock buffer BUFG primitive, takes advantage of the dedicated global clock routing resources of the device.

The output clock has a 50/50 duty cycle unless you deactivate the duty cycle correction property.

## CLKDLL Primitive Pin Descriptions

The library CLKDLL primitives provide access to the complete set of DLL features needed when implementing more complex applications with the DLL.

### *Source Clock Input — CLKIN*

The CLKIN pin provides the user source clock (the clock signal on which the DLL operates) to the DLL. The CLKIN frequency must fall in the ranges specified in the data sheet. A global clock buffer (BUFG) driven from another CLKDLL or one of the global clock input buffers (IBUFG) on the same edge of the device (top or bottom) must source this clock signal.

### *Feedback Clock Input — CLKFB*

The DLL requires a reference or feedback signal to provide the delay-compensated output. Connect only the CLK0 or CLK2X DLL outputs to the feedback clock input (CLKFB) pin to provide the necessary feedback to the DLL. Either a global clock buffer (BUFG) or one of the global clock input buffers (IBUFG) on the same edge of the device (top or bottom) must source this clock signal.

If an IBUFG sources the CLKFB pin, the following special rules apply.

1. An external input port must source the signal that drives the IBUFG I pin.
2. The CLK2X output must feed back to the device if both the CLK0 and CLK2X outputs are driving off chip devices.
3. That signal must directly drive only OBUFs and nothing else.

These rules enable the software to determine which DLL clock output sources the CLKFB pin.

### *Reset Input — RST*

When the reset pin RST activates, the LOCKED signal deactivates within four source clock cycles. The RST pin, active High, must either connect to a dynamic signal or be tied to ground. As the DLL delay taps reset to zero, glitches can occur on the DLL clock output pins. Activation of the RST pin can also severely affect the duty cycle of the clock output pins. Furthermore, the DLL output clocks no longer deskew with respect to one another. The DLL must be reset when the input clock frequency changes, if the device is reconfigured in Boundary-Scan mode, if the device undergoes a hot swap, and after the device is configured if the input clock is not stable during the startup sequence.

### *2x Clock Output — CLK2X*

The output pin CLK2X provides a frequency-doubled clock with an automatic 50/50 duty-cycle correction. Until the CLKDLL has achieved lock, the CLK2X output appears as a 1x version of the input clock with a 25/75 duty cycle. This behavior allows the DLL to lock on the correct edge with respect to source clock. This pin is not available on the CLKDLLHF primitive.

### *Clock Divide Output — CLKDV*

The clock divide output pin CLKDV provides a lower frequency version of the source clock. The CLKDV_DIVIDE property controls CLKDV such that the source clock is divided by N where N is either 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

This feature provides automatic duty cycle correction. The CLKDV output pin has a 50/50 duty cycle for all values of the

division factor N except for non-integer division in High Frequency (HF) mode. For division factor 1.5 the duty cycle in the HF mode is 33.3% High and 66.7% Low. For division factor 2.5, the duty cycle in the HF mode is 40.0% High and 60.0% Low.

### *1x Clock Outputs — CLK[0|90|180|270]*

The 1x clock output pin CLK0 represents a delay-compensated version of the source clock (CLKIN) signal. The CLKDLL primitive provides three phase-shifted versions of the CLK0 signal while CLKDLLHF provides only the 180 degree phase-shifted version. The relationship between phase shift and the corresponding period shift appears in Table 10.

The timing diagrams in Figure 26 illustrate the DLL clock output characteristics.

*Table 10:* **Relationship of Phase-Shifted Output Clock to Period Shift**

| Phase (degrees) | Period Shift (percent) |
|---|---|
| 0 | 0% |
| 90 | 25% |
| 180 | 50% |
| 270 | 75% |

The DLL provides duty cycle correction on all 1x clock outputs such that all 1x clock outputs by default have a 50/50 duty cycle. The DUTY_CYCLE_CORRECTION property (TRUE by default), controls this feature. In order to deactivate the DLL duty cycle correction, attach the DUTY_CYCLE_CORRECTION=FALSE property to the DLL primitive. When duty cycle correction deactivates, the output clock has the same duty cycle as the source clock.

The DLL clock outputs can drive an OBUF, a BUFG, or they can route directly to destination clock pins. The DLL clock outputs can only drive the BUFGs that reside on the same edge (top or bottom).

### *Locked Output — LOCKED*

In order to achieve lock, the DLL may need to sample several thousand clock cycles. After the DLL achieves lock the LOCKED signal activates. The "DLL Timing Parameters" section of Module 3 provides estimates for locking times.

In order to guarantee that the system clock is established prior to the device "waking up," the DLL can delay the completion of the device configuration process until after the DLL locks. The STARTUP_WAIT property activates this feature.

Until the LOCKED signal activates, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement. In particular the CLK2X output will appear as a 1x clock with a 25/75 duty cycle.

### *DLL Properties*

Properties provide access to some of the Spartan-II family DLL features, (for example, clock division and duty cycle correction).

### *Duty Cycle Correction Property*

The 1x clock outputs, CLK0, CLK90, CLK180, and CLK270, use the duty-cycle corrected default, such that they exhibit a 50/50 duty cycle. The DUTY_CYCLE_CORRECTION property (by default TRUE) controls this feature. To deactivate the DLL duty-cycle correction for the 1x clock outputs, attach the DUTY_CYCLE_CORRECTION=FALSE property to the DLL primitive.

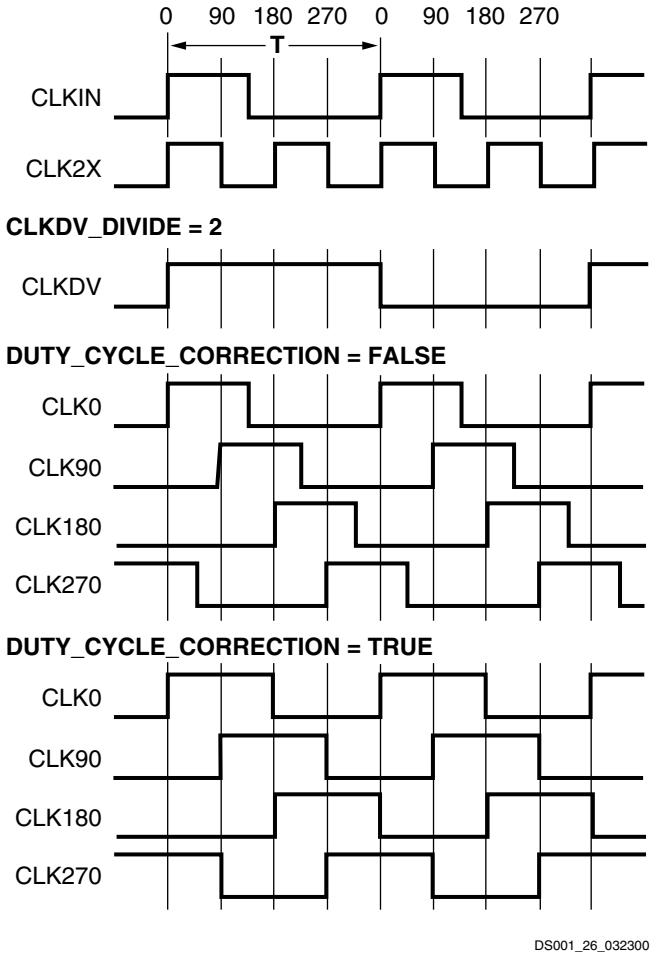



*Figure 26:* **DLL Output Characteristics**

### *Clock Divide Property*

The CLKDV_DIVIDE property specifies how the signal on the CLKDV pin is frequency divided with respect to the CLK0 pin. The values allowed for this property are 1.5, 2, 2.5, 3, 4, 5, 8, or 16; the default value is 2.

### Startup Delay Property

This property, STARTUP_WAIT, takes on a value of TRUE or FALSE (the default value). When TRUE the Startup Sequence following device configuration is paused at a user-specified point until the DLL locks. **XAPP176**: *Configuration and Readback of the Spartan-II and Spartan-IIE Families* explains how this can result in delaying the assertion of the DONE pin until the DLL locks.

### DLL Location Constraints

The DLLs are distributed such that there is one DLL in each corner of the device. The location constraint LOC, attached to the DLL primitive with the numeric identifier 0, 1, 2, or 3, controls DLL location. The orientation of the four DLLs and their corresponding clock resources appears in Figure 27.

The LOC property uses the following form.

LOC = DLL2

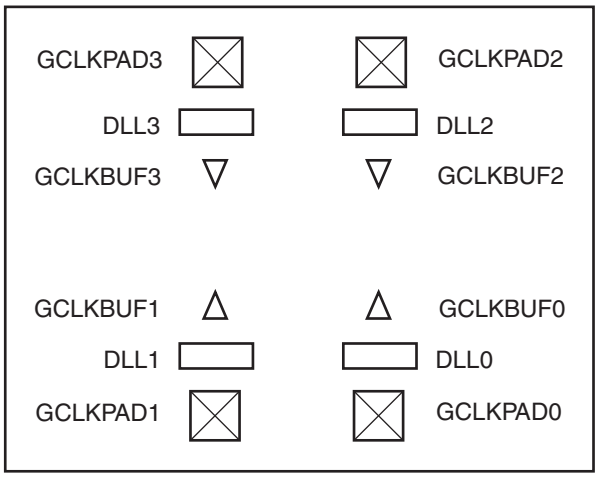



*Figure 27:* **Orientation of DLLs**

## Design Considerations

Use the following design considerations to avoid pitfalls and improve success designing with Xilinx devices.

### Input Clock

The output clock signal of a DLL, essentially a delayed version of the input clock signal, reflects any instability on the input clock in the output waveform. For this reason the quality of the DLL input clock relates directly to the quality of the output clock waveforms generated by the DLL. The DLL input clock requirements are specified in the "DLL Timing Parameters" section of the data sheet.

In most systems a crystal oscillator generates the system clock. The DLL can be used with any commercially available quartz crystal oscillator. For example, most crystal oscillators produce an output waveform with a frequency tolerance of 100 PPM, meaning 0.01 percent change in the clock period. The DLL operates reliably on an input waveform with a frequency drift of up to 1 ns — orders of magnitude in excess of that needed to support any crystal oscillator in the industry. However, the cycle-to-cycle jitter must be kept to less than 300 ps in the low frequencies and 150 ps for the high frequencies.

### Input Clock Changes

Changing the period of the input clock beyond the maximum drift amount requires a manual reset of the CLKDLL. Failure to reset the DLL will produce an unreliable lock signal and output clock.

It is possible to stop the input clock in a way that has little impact to the DLL. Stopping the clock should be limited to less than approximately 100 µs to keep device cooling to a minimum and maintain the validity of the current tap setting. The clock should be stopped during a Low phase, and when restored the full High period should be seen. During this time LOCKED will stay High and remain High when the clock is restored. If these conditions may not be met in the design, apply a manual reset to the DLL after re-starting the input clock, even if the LOCKED signal has not changed.

When the clock is stopped, one to four more clocks will still be observed as the delay line is flushed. When the clock is restarted, the output clocks will not be observed for one to four clocks as the delay line is filled. The most common case will be two or three clocks.

In a similar manner, a phase shift of the input clock is also possible. The phase shift will propagate to the output one to four clocks after the original shift, with no disruption to the CLKDLL control.

### Output Clocks

As mentioned earlier in the DLL pin descriptions, some restrictions apply regarding the connectivity of the output pins. The DLL clock outputs can drive an OBUF, a global clock buffer BUFG, or route directly to destination clock pins. The only BUFGs that the DLL clock outputs can drive are the two on the same edge of the device (top or bottom). One DLL output can drive more than one OBUF; however, this adds skew.

Do not use the DLL output clock signals until after activation of the LOCKED signal. Prior to the activation of the LOCKED signal, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement.

## Useful Application Examples

The Spartan-II FPGA DLL can be used in a variety of creative and useful applications. The following examples show some of the more common applications.

### *Standard Usage*

The circuit shown in Figure 28 resembles the BUFGDLL macro implemented to provide access to the RST and LOCKED pins of the CLKDLL.

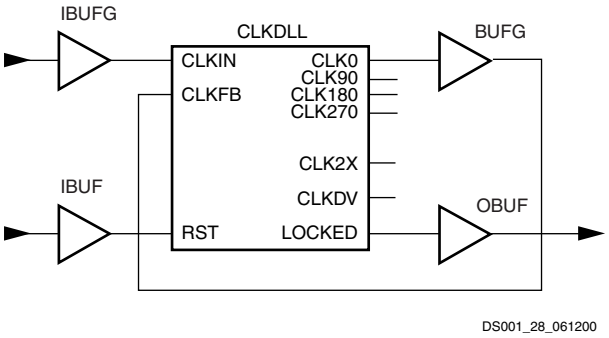



*Figure 28:* **Standard DLL Implementation**

### *Deskew of Clock and Its 2x Multiple*

The circuit shown in Figure 29 implements a 2x clock multiplier and also uses the CLK0 clock output with zero ns skew between registers on the same chip. A clock divider circuit could alternatively be implemented using similar connections.

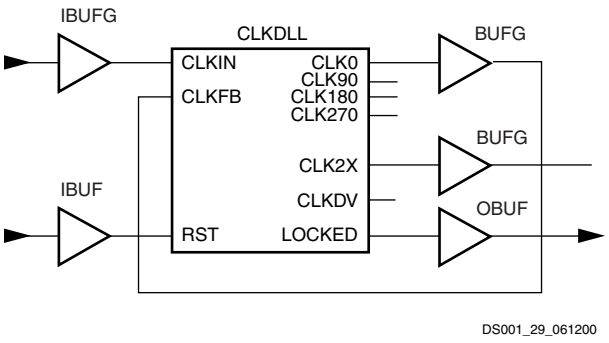



*Figure 29:* **DLL Deskew of Clock and 2x Multiple**

Because any single DLL can only access at most two BUFGs, any additional output clock signals must be routed from the DLL in this example on the high speed backbone routing.

### *Generating a 4x Clock*

By connecting two DLL circuits each implementing a 2x clock multiplier in series as shown in Figure 30, a 4x clock multiply can be implemented with zero skew between registers in the same device.

If other clock output is needed, the clock could access a BUFG only if the DLLs are constrained to exist on opposite edges (Top or Bottom) of the device.

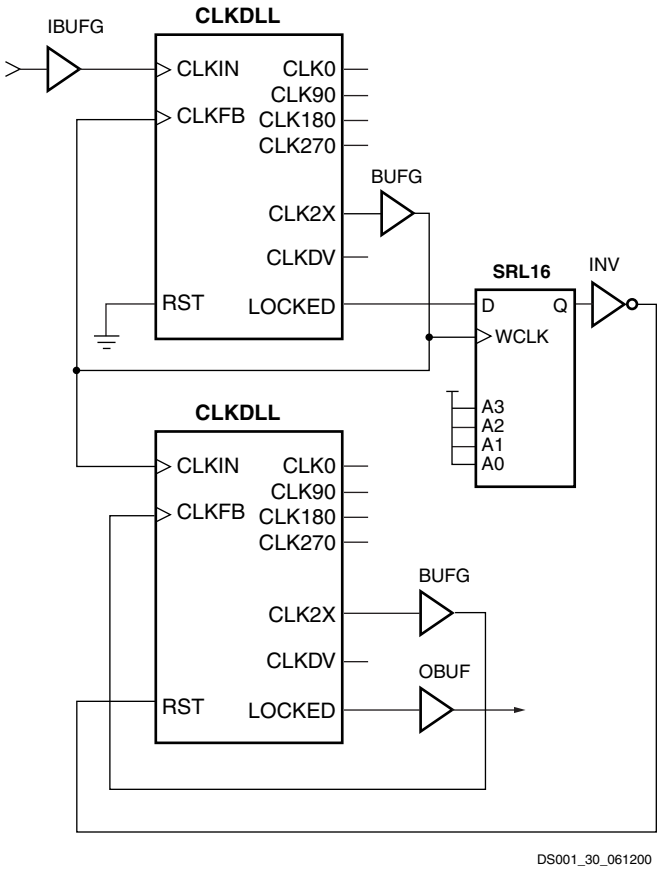



*Figure 30:* **DLL Generation of 4x Clock**

When using this circuit it is vital to use the SRL16 cell to reset the second DLL after the initial chip reset. If this is not done, the second DLL may not recognize the change of frequencies from when the input changes from a 1x (25/75) waveform to a 2x (50/50) waveform. It is not recommended to cascade more than two DLLs.

For design examples and more information on using the DLL, see XAPP174, *Using Delay-Locked Loops in Spartan-II FPGAs*.

# Using Block RAM Features

The Spartan-II FPGA family provides dedicated blocks of on-chip, true dual-read/write port synchronous RAM, with 4096 memory cells. Each port of the block RAM memory can be independently configured as a read/write port, a read port, a write port, and can be configured to a specific data width. The block RAM memory offers new capabilities allowing the FPGA designer to simplify designs.

## Operating Modes

Block RAM memory supports two operating modes.

- Read Through
- Write Back

### *Read Through (One Clock Edge)*

The read address is registered on the read port clock edge and data appears on the output after the RAM access time. Some memories may place the latch/register at the outputs depending on the desire to have a faster clock-to-out versus setup time. This is generally considered to be an inferior solution since it changes the read operation to an asynchronous function with the possibility of missing an address/control line transition during the generation of the read pulse clock.

### *Write Back (One Clock Edge)*

The write address is registered on the write port clock edge and the data input is written to the memory and mirrored on the write port input.

## Block RAM Characteristics

1. All inputs are registered with the port clock and have a setup to clock timing specification.
2. All outputs have a read through or write back function depending on the state of the port WE pin. The outputs relative to the port clock are available after the clock-to-out timing specification.
3. The block RAM are true SRAM memories and do not have a combinatorial path from the address to the output. The LUT cells in the CLBs are still available with this function.
4. The ports are completely independent from each other (*i.e.,* clocking, control, address, read/write function, and data width) without arbitration.
5. A write operation requires only one clock edge.
6. A read operation requires only one clock edge.

The output ports are latched with a self timed circuit to guarantee a glitch free read. The state of the output port will not change until the port executes another read or write operation.

## Library Primitives

Figure 31 and Figure 32 show the two generic library block RAM primitives. Table 11 describes all of the available primitives for synthesis and simulation.

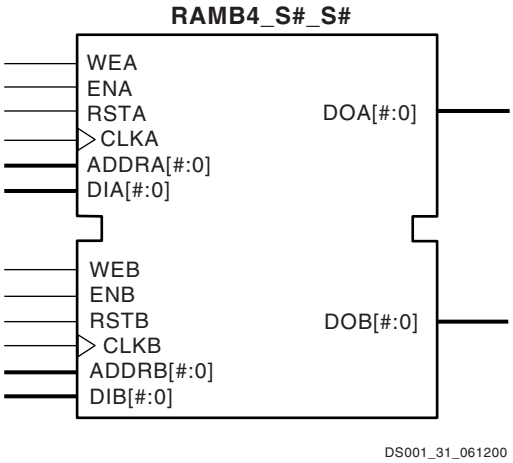



*Figure 31:* **Dual-Port Block RAM Memory**

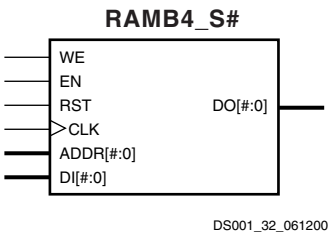



*Figure 32:* **Single-Port Block RAM Memory**

*Table 11:* **Available Library Primitives**

| Primitive | Port A Width | Port B Width |
|---|---|---|
| RAMB4_S1 | 1 | N/A |
| RAMB4_S1_S1 | | 1 |
| RAMB4_S1_S2 | | 2 |
| RAMB4_S1_S4 | | 4 |
| RAMB4_S1_S8 | | 8 |
| RAMB4_S1_S16 | | 16 |
| RAMB4_S2 | 2 | N/A |
| RAMB4_S2_S2 | | 2 |
| RAMB4_S2_S4 | | 4 |
| RAMB4_S2_S8 | | 8 |
| RAMB4_S2_S16 | | 16 |

*Table 11:* **Available Library Primitives**

| Primitive | Port A Width | Port B Width |
|---|---|---|
| RAMB4_S4<br>RAMB4_S4_S4<br>RAMB4_S4_S8<br>RAMB4_S4_S16 | 4 | N/A<br>4<br>8<br>16 |
| RAMB4_S8<br>RAMB4_S8_S8<br>RAMB4_S8_S16 | 8 | N/A<br>8<br>16 |
| RAMB4_S16<br>RAMB4_S16_S16 | 16 | N/A<br>16 |

## Port Signals

Each block RAM port operates independently of the others while accessing the same set of 4096 memory cells.

Table 12 describes the depth and width aspect ratios for the block RAM memory.

*Table 12:* **Block RAM Port Aspect Ratios**

| Width | Depth | ADDR Bus | Data Bus |
|---|---|---|---|
| 1 | 4096 | ADDR<11:0> | DATA<0> |
| 2 | 2048 | ADDR<10:0> | DATA<1:0> |
| 4 | 1024 | ADDR<9:0> | DATA<3:0> |
| 8 | 512 | ADDR<8:0> | DATA<7:0> |
| 16 | 256 | ADDR<7:0> | DATA<15:0> |

### *Clock—CLK[A|B]*

Each port is fully synchronous with independent clock pins. All port input pins have setup time referenced to the port CLK pin. The data output bus has a clock-to-out time referenced to the CLK pin.

### *Enable—EN[A|B]*

The enable pin affects the read, write and reset functionality of the port. Ports with an inactive enable pin keep the output pins in the previous state and do not write data to the memory cells.

### *Write Enable—WE[A|B]*

Activating the write enable pin allows the port to write to the memory cells. When active, the contents of the data input bus are written to the RAM at the address pointed to by the address bus, and the new data also reflects on the data out bus. When inactive, a read operation occurs and the contents of the memory cells referenced by the address bus reflect on the data out bus.

### Reset—RST[A|B]

The reset pin forces the data output bus latches to zero synchronously. This does not affect the memory cells of the RAM and does not disturb a write operation on the other port.

### *Address Bus—ADDR[A|B]<#:0>*

The address bus selects the memory cells for read or write. The width of the port determines the required width of this bus as shown in Table 12.

### *Data In Bus—DI[A|B]<#:0>*

The data in bus provides the new data value to be written into the RAM. This bus and the port have the same width, as shown in Table 12.

### *Data Output Bus—DO[A|B]<#:0>*

The data out bus reflects the contents of the memory cells referenced by the address bus at the last active clock edge. During a write operation, the data out bus reflects the data in bus. The width of this bus equals the width of the port. The allowed widths appear in Table 12.

## Inverting Control Pins

The four control pins (CLK, EN, WE and RST) for each port have independent inversion control as a configuration option.

## Address Mapping

Each port accesses the same set of 4096 memory cells using an addressing scheme dependent on the width of the port. The physical RAM location addressed for a particular width are described in the following formula (of interest only when the two ports use different aspect ratios).

$$Start = ([ADDR_{port} + 1] * Width_{port}) - 1$$

$$End = ADDR_{port} * Width_{port}$$

Table 13 shows low order address mapping for each port width.

*Table 13:* **Port Address Mapping**

| Port Width | Port Addresses | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 4095... | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
| 2 | 2047... | 07 | | 06 | | 05 | | 04 | | 03 | | 02 | | 01 | | 00 | |
| 4 | 1023... | 03 | | | | 02 | | | | 01 | | | | 00 | | | |
| 8 | 511... | 01 | | | | | | | | 00 | | | | | | | |
| 16 | 255... | 00 | | | | | | | | | | | | | | | |

## Creating Larger RAM Structures

The block RAM columns have specialized routing to allow cascading blocks together with minimal routing delays. This achieves wider or deeper RAM structures with a smaller timing penalty than when using normal routing channels.

## Location Constraints

Block RAM instances can have LOC properties attached to them to constrain the placement. The block RAM placement locations are separate from the CLB location naming convention, allowing the LOC properties to transfer easily from array to array.

The LOC properties use the following form:

LOC = RAMB4_R#C#

RAMB4_R0C0 is the upper left RAMB4 location on the device.

## Conflict Resolution

The block RAM memory is a true dual-read/write port RAM that allows simultaneous access of the same memory cell from both ports. When one port writes to a given memory cell, the other port must not address that memory cell (for a write or a read) within the clock-to-clock setup window. The following lists specifics of port and memory cell write conflict resolution.

- If both ports write to the same memory cell simultaneously, violating the clock-to-clock setup requirement, consider the data stored as invalid.
- If one port attempts a read of the same memory cell the other simultaneously writes, violating the clock-to-clock setup requirement, the following occurs.
  - The write succeeds
  - The data out on the writing port accurately reflects the data written.
  - The data out on the reading port is invalid.

Conflicts do not cause any physical damage.

### *Single Port Timing*

Figure 33 shows a timing diagram for a single port of a block RAM memory. The block RAM AC switching characteristics are specified in the data sheet. The block RAM memory is initially disabled.

At the first rising edge of the CLK pin, the ADDR, DI, EN, WE, and RST pins are sampled. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location, 0x00, as indicated by the ADDR bus.

At the second rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN and WE pins are High indicating a write operation. The DO bus mirrors the DI bus. The DI bus is written to the memory location 0x0F.

At the third rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location 0x7E as indicated by the ADDR bus.

At the fourth rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is Low indicating that the block RAM memory is now disabled. The DO bus retains the last value.

### *Dual Port Timing*

Figure 34 shows a timing diagram for a true dual-port read/write block RAM memory. The clock on port A has a longer period than the clock on Port B. The timing parameter $T_{BCCS}$, (clock-to-clock setup) is shown on this diagram. The parameter, $T_{BCCS}$ is violated once in the diagram. All other timing parameters are identical to the single port version shown in Figure 33.

$T_{BCCS}$ is only of importance when the address of both ports are the same and at least one port is performing a write operation. When the clock-to-clock set-up parameter is violated for a WRITE-WRITE condition, the contents of the memory at that location will be invalid. When the clock-to-clock set-up parameter is violated for a WRITE-READ condition, the contents of the memory will be correct, but the read port will have invalid data. At the first rising edge of the CLKA, memory location 0x00 is to be written with the value 0xAAAA and is mirrored on the DOA bus. The last operation of Port B was a read to the same memory location 0x00. The DOB bus of Port B does not change with the new value on Port A, and retains the last read value. A short time later, Port B executes another read to memory location 0x00, and the DOB bus now reflects the new memory value written by Port A.

At the second rising edge of CLKA, memory location 0x7E is written with the value 0x9999 and is mirrored on the DOA bus. Port B then executes a read operation to the same memory location without violating the $T_{BCCS}$ parameter and the DOB reflects the new memory values written by Port A.

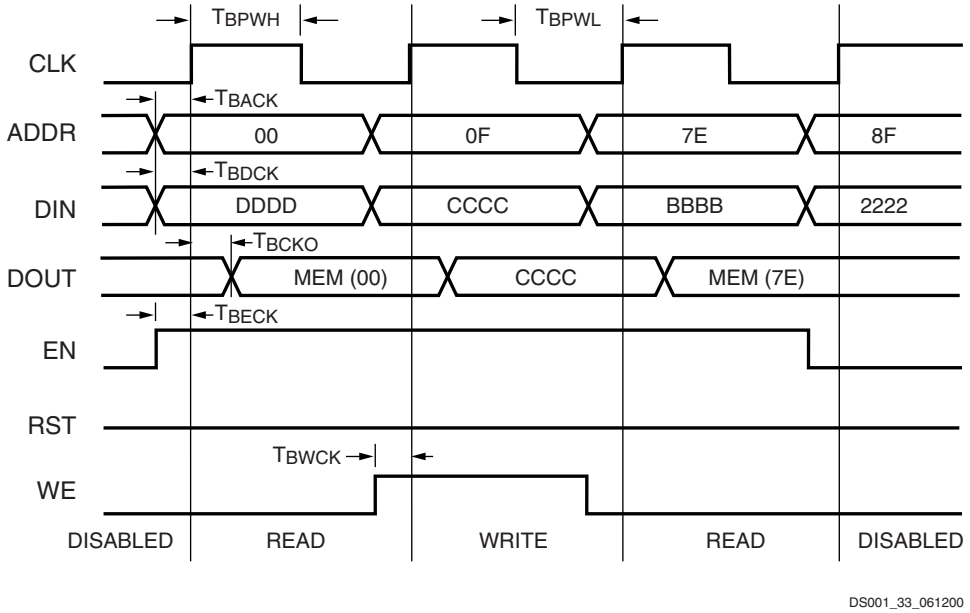



*Figure 33:* **Timing Diagram for Single-Port Block RAM Memory**

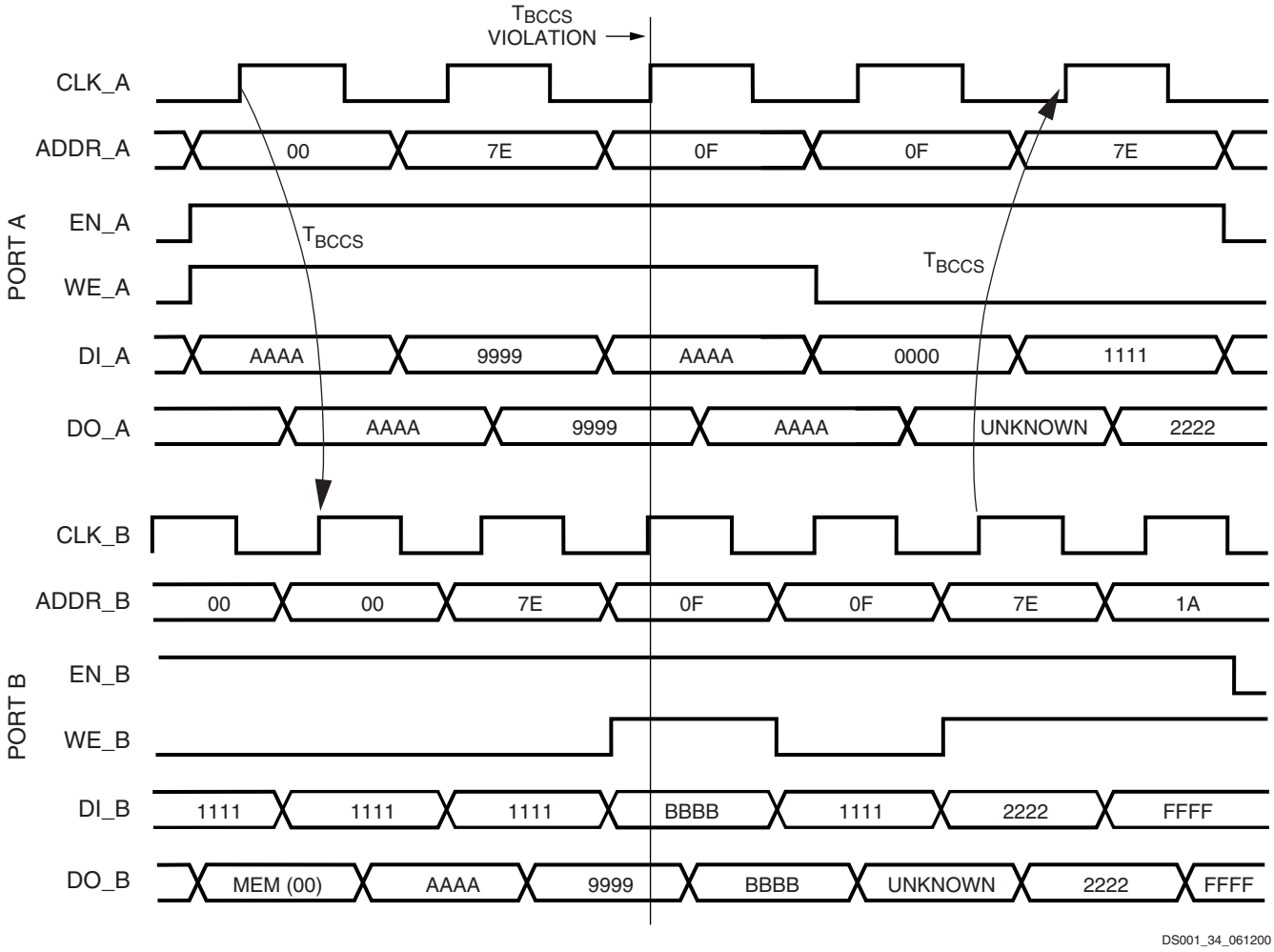



*Figure 34:* **Timing Diagram for a True Dual-Port Read/Write Block RAM Memory**

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At the third rising edge of CLKA, the $T_{BCCS}$ parameter is violated with two writes to memory location 0x0F. The DOA and DOB busses reflect the contents of the DIA and DIB busses, but the stored value at 0x7E is invalid.

At the fourth rising edge of CLKA, a read operation is performed at memory location 0x0F and invalid data is present on the DOA bus. Port B also executes a read operation to memory location 0x0F and also reads invalid data.

At the fifth rising edge of CLKA a read operation is performed that does not violate the $T_{BCCS}$ parameter to the previous write of 0x7E by Port B. THe DOA bus reflects the recently written value by Port B.

## Initialization

The block RAM memory can initialize during the device configuration sequence. The 16 initialization properties of 64 hex values each (a total of 4096 bits) set the initialization of each RAM. These properties appear in Table 14. Any initialization properties not explicitly set configure as zeros. Partial initialization strings pad with zeros. Initialization strings greater than 64 hex values generate an error. The RAMs can be simulated with the initialization values using generics in VHDL simulators and parameters in Verilog simulators.

## Initialization in VHDL

The block RAM structures may be initialized in VHDL for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the VHDL code uses a generic to pass the initialization.

## Initialization in Verilog

The block RAM structures may be initialized in Verilog for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the Verilog code uses a defparam to pass the initialization.

## Block Memory Generation

The CORE Generator™ software generates memory structures using the block RAM features. This program outputs VHDL or Verilog simulation code templates and an EDIF file for inclusion in a design.

*Table 14:* **RAM Initialization Properties**

| Property | Memory Cells |
|---|---|
| INIT_00 | 255 to 0 |
| INIT_01 | 511 to 256 |
| INIT_02 | 767 to 512 |
| INIT_03 | 1023 to 768 |
| INIT_04 | 1279 to 1024 |
| INIT_05 | 1535 to 1280 |
| INIT_06 | 1791 to 1536 |
| INIT_07 | 2047 to 1792 |
| INIT_08 | 2303 to 2048 |
| INIT_09 | 2559 to 2304 |
| INIT_0a | 2815 to 2560 |
| INIT_0b | 3071 to 2816 |
| INIT_0c | 3327 to 3072 |
| INIT_0d | 3583 to 3328 |
| INIT_0e | 3839 to 3584 |
| INIT_0f | 4095 to 3840 |

For design examples and more information on using the Block RAM, see XAPP173, *Using Block SelectRAM+ Memory in Spartan-II FPGAs*.

# Using Versatile I/O

The Spartan-II FPGA family includes a highly configurable, high-performance I/O resource called Versatile I/O to provide support for a wide variety of I/O standards. The Versatile I/O resource is a robust set of features including programmable control of output drive strength, slew rate, and input delay and hold time. Taking advantage of the flexibility and Versatile I/O features and the design considerations described in this document can improve and simplify system level design.

## Introduction

As FPGAs continue to grow in size and capacity, the larger and more complex systems designed for them demand an increased variety of I/O standards. Furthermore, as system clock speeds continue to increase, the need for high-performance I/O becomes more important. While chip-to-chip delays have an increasingly substantial impact on overall system speed, the task of achieving the desired system performance becomes more difficult with the proliferation of low-voltage I/O standards. Versatile I/O, the revolutionary input/output resources of Spartan-II devices, has resolved this potential problem by providing a highly configurable, high-performance alternative to the I/O resources of more conventional programmable devices. The Spartan-II FPGA Versatile I/O features combine the flexibility and time-to-market advantages of programmable logic with the high performance previously available only with ASICs and custom ICs.

Each Versatile I/O block can support up to 16 I/O standards. Supporting such a variety of I/O standards allows the

support of a wide variety of applications, from general purpose standard applications to high-speed low-voltage memory busses.

Versatile I/O blocks also provide selectable output drive strengths and programmable slew rates for the LVTTL output buffers, as well as an optional, programmable weak pull-up, weak pull-down, or weak "keeper" circuit ideal for use in external bussing applications.

Each Input/Output Block (IOB) includes three registers, one each for the input, output, and 3-state signals within the IOB. These registers are optionally configurable as either a D-type flip-flop or as a level sensitive latch.

The input buffer has an optional delay element used to guarantee a zero hold time requirement for input signals registered within the IOB.

The Versatile I/O features also provide dedicated resources for input reference voltage ($V_{REF}$) and output source voltage ($V_{CCO}$), along with a convenient banking system that simplifies board design.

By taking advantage of the built-in features and wide variety of I/O standards supported by the Versatile I/O features, system-level design and board design can be greatly simplified and improved.

## Fundamentals

Modern bus applications, pioneered by the largest and most influential companies in the digital electronics industry, are commonly introduced with a new I/O standard tailored specifically to the needs of that application. The bus I/O standards provide specifications to other vendors who create products designed to interface with these applications. Each standard often has its own specifications for current, voltage, I/O buffering, and termination techniques.

The ability to provide the flexibility and time-to-market advantages of programmable logic is increasingly dependent on the capability of the programmable logic device to support an ever increasing variety of I/O standards

The Versatile I/O resources feature highly configurable input and output buffers which provide support for a wide variety of I/O standards. As shown in Table 15, each buffer type can support a variety of voltage requirements.

*Table 15:* **Versatile I/O Supported Standards (Typical Values)**

| I/O Standard | Input Reference Voltage ($V_{REF}$) | Output Source Voltage ($V_{CCO}$) | Board Termination Voltage ($V_{TT}$) |
|---|---|---|---|
| LVTTL (2-24 mA) | N/A | 3.3 | N/A |
| LVCMOS2 | N/A | 2.5 | N/A |
| PCI (3V/5V, 33 MHz/66 MHz) | N/A | 3.3 | N/A |
| GTL | 0.8 | N/A | 1.2 |
| GTL+ | 1.0 | N/A | 1.5 |
| HSTL Class I | 0.75 | 1.5 | 0.75 |
| HSTL Class III | 0.9 | 1.5 | 1.5 |
| HSTL Class IV | 0.9 | 1.5 | 1.5 |
| SSTL3 Class I and II | 1.5 | 3.3 | 1.5 |
| SSTL2 Class I and II | 1.25 | 2.5 | 1.25 |
| CTT | 1.5 | 3.3 | 1.5 |
| AGP-2X | 1.32 | 3.3 | N/A |

## Overview of Supported I/O Standards

This section provides a brief overview of the I/O standards supported by all Spartan-II devices.

While most I/O standards specify a range of allowed voltages, this document records typical voltage values only. Detailed information on each specification may be found on the Electronic Industry Alliance JEDEC website at http://www.jedec.org. For more details on the I/O standards and termination application examples, see XAPP179, "*Using SelectIO Interfaces in Spartan-II and Spartan-IIE FPGAs.*"

### *LVTTL — Low-Voltage TTL*

The Low-Voltage TTL (LVTTL) standard is a general purpose EIA/JESDSA standard for 3.3V applications that uses an LVTTL input buffer and a Push-Pull output buffer. This standard requires a 3.3V output source voltage ($V_{CCO}$), but does not require the use of a reference voltage ($V_{REF}$) or a termination voltage ($V_{TT}$).

### *LVCMOS2 — Low-Voltage CMOS for 2.5V*

The Low-Voltage CMOS for 2.5V or lower (LVCMOS2) standard is an extension of the LVCMOS standard (JESD 8.5) used for general purpose 2.5V applications. This standard requires a 2.5V output source voltage ($V_{CCO}$), but does not require the use of a reference voltage ($V_{REF}$) or a board termination voltage ($V_{TT}$).

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### *PCI — Peripheral Component Interface*

The Peripheral Component Interface (PCI) standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses a LVTTL input buffer and a push-pull output buffer. This standard does not require the use of a reference voltage ($V_{REF}$) or a board termination voltage ($V_{TT}$), however, it does require a 3.3V output source voltage ($V_{CCO}$). I/Os configured for the PCI, 33 MHz, 5V standard are also 5V-tolerant.

### *GTL — Gunning Transceiver Logic Terminated*

The Gunning Transceiver Logic (GTL) standard is a high-speed bus standard (JESD8.3). Xilinx has implemented the terminated variation of this standard. This standard requires a differential amplifier input buffer and an open-drain output buffer.

### *GTL+ — Gunning Transceiver Logic Plus*

The Gunning Transceiver Logic Plus (GTL+) standard is a high-speed bus standard (JESD8.3).

### *HSTL — High-Speed Transceiver Logic*

The High-Speed Transceiver Logic (HSTL) standard is a general purpose high-speed, 1.5V bus standard (EIA/JESD 8-6). This standard has four variations or classes. Versatile I/O devices support Class I, III, and IV. This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

### *SSTL3 — Stub Series Terminated Logic for 3.3V*

The Stub Series Terminated Logic for 3.3V (SSTL3) standard is a general purpose 3.3V memory bus standard (JESD8-8). This standard has two classes, I and II. Versatile I/O devices support both classes for the SSTL3 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

### *SSTL2 — Stub Series Terminated Logic for 2.5V*

The Stub Series Terminated Logic for 2.5V (SSTL2) standard is a general purpose 2.5V memory bus standard (JESD8-9). This standard has two classes, I and II. Versatile I/O devices support both classes for the SSTL2 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

### *CTT — Center Tap Terminated*

The Center Tap Terminated (CTT) standard is a 3.3V memory bus standard (JESD8-4). This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

### *AGP-2X — Advanced Graphics Port*

The AGP standard is a 3.3V Advanced Graphics Port-2X bus standard used with processors for graphics applications. This standard requires a Push-Pull output buffer and a Differential Amplifier input buffer.

## Library Primitives

The Xilinx library includes an extensive list of primitives designed to provide support for the variety of Versatile I/O features. Most of these primitives represent variations of the five generic Versatile I/O primitives:

- IBUF (input buffer)
- IBUFG (global clock input buffer)
- OBUF (output buffer)
- OBUFT (3-state output buffer)
- IOBUF (input/output buffer)

These primitives are available with various extensions to define the desired I/O standard. However, it is recommended that customers use a a property or attribute on the generic primitive to specify the I/O standard. See "Versatile I/O Properties".

### *IBUF*

Signals used as inputs to the Spartan-II device must source an input buffer (IBUF) via an external input port. The generic IBUF primitive appears in Figure 35. The assumed standard is LVTTL when the generic IBUF has no specified extension or property.

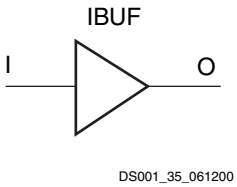


*Figure 35:* **Input Buffer (IBUF) Primitive**

When the IBUF primitive supports an I/O standard such as LVTTL, LVCMOS, or PCI33_5, the IBUF automatically configures as a 5V tolerant input buffer unless the $V_{CCO}$ for the bank is less than 2V. If the single-ended IBUF is placed in a bank with an HSTL standard ($V_{CCO}$ < 2V), the input buffer is not 5V tolerant.

The voltage reference signal is "banked" within the Spartan-II device on a half-edge basis such that for all packages there are eight independent $V_{REF}$ banks internally. See Figure 36 for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a $V_{REF}$ input.

IBUF placement restrictions require that any differential amplifier input signals within a bank be of the same standard. How to specify a specific location for the IBUF via

the LOC property is described below. Table 16 summarizes the input standards compatibility requirements.

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element by default activates to ensure a zero hold-time requirement. The NODELAY=TRUE property overrides this default.

When the IBUF does not drive a flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

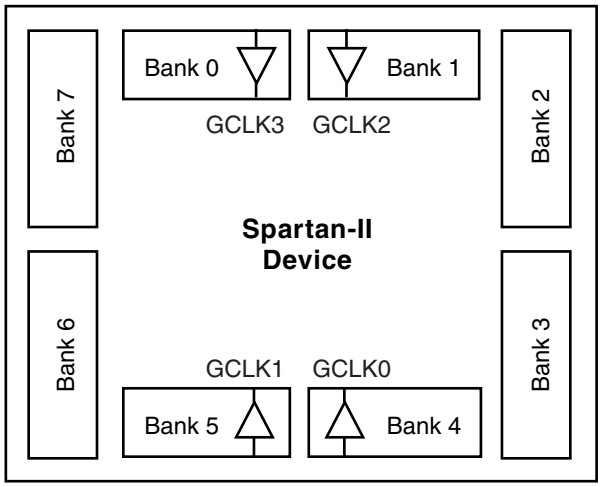


*Figure 36:* **I/O Banks**

*Table 16:* **Xilinx Input Standards Compatibility Requirements**

| | |
|---|---|
| Rule 1 | All differential amplifier input signals within a bank are required to be of the same standard. |
| Rule 2 | There are no placement restrictions for inputs with standards that require a single-ended input buffer. |

### *IBUFG*

Signals used as high fanout clock inputs to the Spartan-II device should drive a global clock input buffer (IBUFG) via an external input port in order to take advantage of one of the four dedicated global clock distribution networks. The output of the IBUFG primitive can only drive a CLKDLL, CLKDLLHF, or a BUFG primitive. The generic IBUFG primitive appears in Figure 37.

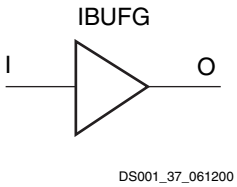


*Figure 37:* **Global Clock Input Buffer (IBUFG) Primitive**

With no extension or property specified for the generic IBUFG primitive, the assumed standard is LVTTL.

The voltage reference signal is "banked" within the Spartan-II device on a half-edge basis such that for all packages there are eight independent $V_{REF}$ banks internally. See Figure 36 for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a $V_{REF}$ input.

IBUFG placement restrictions require any differential amplifier input signals within a bank be of the same standard. The LOC property can specify a location for the IBUFG.

As an added convenience, the BUFGP can be used to instantiate a high fanout clock input. The BUFGP primitive represents a combination of the LVTTL IBUFG and BUFG primitives, such that the output of the BUFGP can connect directly to the clock pins throughout the design.

The Spartan-II FPGA BUFGP primitive can only be placed in a global clock pad location. The LOC property can specify a location for the BUFGP.

### *OBUF*

An OBUF must drive outputs through an external output port. The generic output buffer (OBUF) primitive appears in Figure 38.

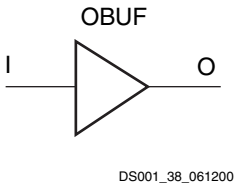


*Figure 38:* **Output Buffer (OBUF) Primitive**

With no extension or property specified for the generic OBUF primitive, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

The LVTTL OBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

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LVTTL output buffers have selectable drive strengths.

The format for LVTTL OBUF primitive names is as follows.

OBUF_<slew_rate>_<drive_strength>

<slew_rate> is either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24). The default is slew rate limited with 12 mA drive.

OBUF placement restrictions require that within a given $V_{CCO}$ bank each OBUF share the same output source drive voltage. Input buffers of any type and output buffers that do not require $V_{CCO}$ can be placed within any $V_{CCO}$ bank. Table 17 summarizes the output compatibility requirements. The LOC property can specify a location for the OBUF.

*Table 17:* **Output Standards Compatibility Requirements**

| | |
|---|---|
| Rule 1 | Only outputs with standards which share compatible $V_{CCO}$ may be used within the same bank. |
| Rule 2 | There are no placement restrictions for outputs with standards that do not require a $V_{CCO}$. |
| $V_{CCO}$ | Compatible Standards |
| 3.3 | LVTTL, SSTL3_I, SSTL3_II, CTT, AGP, GTL, GTL+, PCI33_3, PCI66_3 |
| 2.5 | SSTL2_I, SSTL2_II, LVCMOS2, GTL, GTL+ |
| 1.5 | HSTL_I, HSTL_III, HSTL_IV, GTL, GTL+ |

### *OBUFT*

The generic 3-state output buffer OBUFT, shown in Figure 39, typically implements 3-state outputs or bidirectional I/O.

With no extension or property specified for the generic OBUFT primitive, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

The LVTTL OBUFT can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL 3-state output buffers have selectable drive strengths.

The format for LVTTL OBUFT primitive names is as follows.

OBUFT_<slew_rate>_<drive_strength>

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

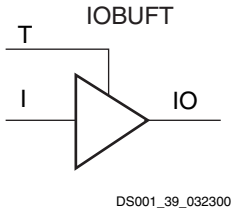


*Figure 39:* **3-State Output Buffer Primitive (OBUFT**

The Versatile I/O OBUFT placement restrictions require that within a given $V_{CCO}$ bank each OBUFT share the same output source drive voltage. Input buffers of any type and output buffers that do not require $V_{CCO}$ can be placed within the same $V_{CCO}$ bank.

The LOC property can specify a location for the OBUFT.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak "keeper" circuit. Control this feature by adding the appropriate primitive to the output net of the OBUFT (PULLUP, PULLDOWN, or KEEPER).

The weak "keeper" circuit requires the input buffer within the IOB to sample the I/O signal. So, OBUFTs programmed for an I/O standard that requires a $V_{REF}$ have automatic placement of a $V_{REF}$ in the bank with an OBUFT configured with a weak "keeper" circuit. This restriction does not affect most circuit design as applications using an OBUFT configured with a weak "keeper" typically implement a bidirectional I/O. In this case the IBUF (and the corresponding $V_{REF}$) are explicitly placed.

The LOC property can specify a location for the OBUFT.

### *IOBUF*

Use the IOBUF primitive for bidirectional signals that require both an input buffer and a 3-state output buffer with an active high 3-state pin. The generic input/output buffer IOBUF appears in Figure 40.

With no extension or property specified for the generic IOBUF primitive, the assumed standard is LVTTL input buffer and slew rate limited LVTTL with 12 mA drive strength for the output buffer.

The LVTTL IOBUF can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL bidirectional buffers have selectable output drive strengths.

The format for LVTTL IOBUF primitive names is as follows:

IOBUF_<slew_rate>_<drive_strength>

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

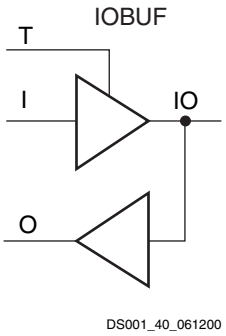


*Figure 40:* **Input/Output Buffer Primitiveprimitive (IOBUF)**

When the IOBUF primitive supports an I/O standard such as LVTTL, LVCMOS, or PCI33_5, the IBUF automatically configures as a 5V tolerant input buffer unless the $V_{CCO}$ for the bank is less than 2V. If the single-ended IBUF is placed in a bank with an HSTL standard ($V_{CCO}$ < 2V), the input buffer is not 5V tolerant.

The voltage reference signal is "banked" within the Spartan-II device on a half-edge basis such that for all packages there are eight independent $V_{REF}$ banks internally. See Figure 36, page 39 for a representation of the Spartan-II FPGA I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a $V_{REF}$ input.

Additional restrictions on the Versatile I/O IOBUF placement require that within a given $V_{CCO}$ bank each IOBUF must share the same output source drive voltage. Input buffers of any type and output buffers that do not require $V_{CCO}$ can be placed within the same $V_{CCO}$ bank. The LOC property can specify a location for the IOBUF.

An optional delay element is associated with the input path in each IOBUF. When the IOBUF drives an input flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Override this default with the NODELAY=TRUE property.

In the case when the IOBUF does not drive an input flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak "keeper" circuit. Control this feature by adding the appropriate primitive to the output net of the IOBUF (PULLUP, PULLDOWN, or KEEPER).

## Versatile I/O Properties

Access to some of the Versatile I/O features (for example, location constraints, input delay, output drive strength, and slew rate) is available through properties associated with these features.

### *Input Delay Properties*

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Use the NODELAY=TRUE property to override this default.

In the case when the IBUF does not drive a flip-flop within the IOB, the delay element by default de-activates to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

### *IOB Flip-Flop/Latch Property*

The I/O Block (IOB) includes an optional register on the input path, an optional register on the output path, and an optional register on the 3-state control pin. The design implementation software automatically takes advantage of these registers when the following option for the Map program is specified:

map -pr b <filename>

Alternatively, the IOB = TRUE property can be placed on a register to force the mapper to place the register in an IOB.

### *Location Constraints*

Specify the location of each Versatile I/O primitive with the location constraint LOC attached to the Versatile I/O primitive. The external port identifier indicates the value of the location constrain. The format of the port identifier depends on the package chosen for the specific design.

The LOC properties use the following form:

LOC=A42

LOC=P37

### *Output Slew Rate Property*

In the case of the LVTTL output buffers (OBUF, OBUFT, and IOBUF), slew rate control can be programmed with the SLEW= property. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals. The SLEW= property has one of the two following values.

SLEW=SLOW

SLEW=FAST

### *Output Drive Strength Property*

For the LVTTL output buffers (OBUF, OBUFT, and IOBUF, the desired drive strength can be specified with the DRIVE=

property. This property could have one of the following seven values.

DRIVE=2

DRIVE=4

DRIVE=6

DRIVE=8

DRIVE=12 (Default)

DRIVE=16

DRIVE=24

## Design Considerations

### Reference Voltage ($V_{REF}$) Pins

Low-voltage I/O standards with a differential amplifier input buffer require an input reference voltage ($V_{REF}$). Provide the $V_{REF}$ as an external signal to the device.

The voltage reference signal is "banked" within the device on a half-edge basis such that for all packages there are eight independent $V_{REF}$ banks internally. See Figure 36, page 39 for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a $V_{REF}$ input.

Within each $V_{REF}$ bank, any input buffers that require a $V_{REF}$ signal must be of the same type. Output buffers of any type and input buffers can be placed without requiring a reference voltage within the same $V_{REF}$ bank.

### Output Drive Source Voltage ($V_{CCO}$) Pins

Many of the low voltage I/O standards supported by Versatile I/Os require a different output drive source voltage ($V_{CCO}$). As a result each device can often have to support multiple output drive source voltages.

The $V_{CCO}$ supplies are internally tied together for some packages. The VQ100 and the PQ208 provide one combined $V_{CCO}$ supply. The TQ144 and the CS144 packages provide four independent $V_{CCO}$ supplies. The FG256 and the FG456 provide eight independent $V_{CCO}$ supplies.

Output buffers within a given $V_{CCO}$ bank must share the same output drive source voltage. Input buffers for LVTTL, LVCMOS2, PCI33_3, and PCI 66_3 use the $V_{CCO}$ voltage for Input $V_{CCO}$ voltage.

### Transmission Line Effects

The delay of an electrical signal along a wire is dominated by the rise and fall times when the signal travels a short distance. Transmission line delays vary with inductance and capacitance, but a well-designed board can experience delays of approximately 180 ps per inch.

Transmission line effects, or reflections, typically start at 1.5" for fast (1.5 ns) rise and fall times. Poor (or non-existent) termination or changes in the transmission line impedance cause these reflections and can cause additional delay in longer traces. As system speeds continue to increase, the effect of I/O delays can become a limiting factor and therefore transmission line termination becomes increasingly more important.

### Termination Techniques

A variety of termination techniques reduce the impact of transmission line effects.

The following lists output termination techniques:

None
Series
Parallel (Shunt)
Series and Parallel (Series-Shunt)

Input termination techniques include the following:

None
Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in Figure 41.

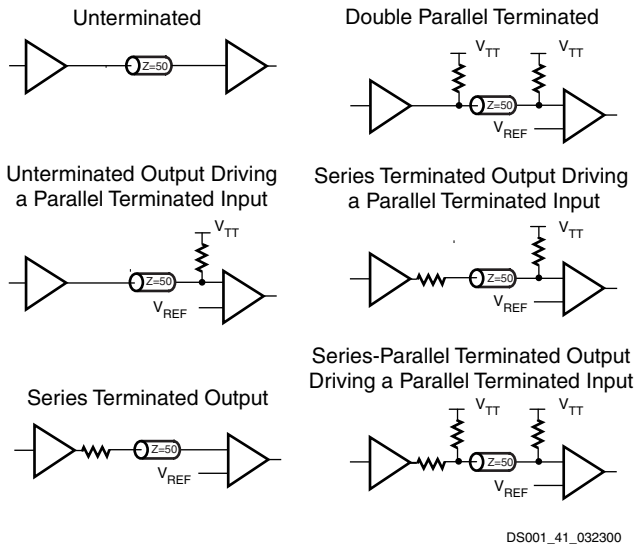


*Figure 41:* **Overview of Standard Input and Output Termination Methods**

### Simultaneous Switching Guidelines

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and

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ground metallization. The IC internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously.

Ground bounce affects stable Low outputs and all inputs because they interpret the incoming signal by comparing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input can be interpreted as a short pulse with a polarity opposite to the ground bounce.

Table 18 provides the guidelines for the maximum number of simultaneously switching outputs allowed per output power/ground pair to avoid the effects of ground bounce. Refer to Table 19 for the number of effective output power/ground pairs for each Spartan-II device and package combination.

*Table 18:* **Maximum Number of Simultaneously Switching Outputs per Power/Ground Pair**

| Standard | Package | |
|---|---|---|
| | CS, FG | PQ, TQ, VQ |
| LVTTL Slow Slew Rate, 2 mA drive | 68 | 36 |
| LVTTL Slow Slew Rate, 4 mA drive | 41 | 20 |
| LVTTL Slow Slew Rate, 6 mA drive | 29 | 15 |
| LVTTL Slow Slew Rate, 8 mA drive | 22 | 12 |
| LVTTL Slow Slew Rate, 12 mA drive | 17 | 9 |
| LVTTL Slow Slew Rate, 16 mA drive | 14 | 7 |
| LVTTL Slow Slew Rate, 24 mA drive | 9 | 5 |
| LVTTL Fast Slew Rate, 2 mA drive | 40 | 21 |
| LVTTL Fast Slew Rate, 4 mA drive | 24 | 12 |
| LVTTL Fast Slew Rate, 6 mA drive | 17 | 9 |
| LVTTL Fast Slew Rate, 8 mA drive | 13 | 7 |
| LVTTL Fast Slew Rate, 12 mA drive | 10 | 5 |
| LVTTL Fast Slew Rate, 16 mA drive | 8 | 4 |
| LVTTL Fast Slew Rate, 24 mA drive | 5 | 3 |
| LVCMOS2 | 10 | 5 |
| PCI | 8 | 4 |
| GTL | 4 | 4 |
| GTL+ | 4 | 4 |
| HSTL Class I | 18 | 9 |
| HSTL Class III | 9 | 5 |
| HSTL Class IV | 5 | 3 |
| SSTL2 Class I | 15 | 8 |
| SSTL2 Class II | 10 | 5 |
| SSTL3 Class I | 11 | 6 |
| SSTL3 Class II | 7 | 4 |
| CTT | 14 | 7 |
| AGP | 9 | 5 |

**Notes:**
1. This analysis assumes a 35 pF load for each output.

*Table 19:* **Effective Output Power/Ground Pairs for Spartan-II Devices**

| Pkg. | Spartan-II Devices | | | | | |
|---|---|---|---|---|---|---|
| | XC2S 15 | XC2S 30 | XC2S 50 | XC2S 100 | XC2S 150 | XC2S 200 |
| VQ100 | 8 | 8 | - | - | - | - |
| CS144 | 12 | 12 | - | - | - | - |
| TQ144 | 12 | 12 | 12 | 12 | - | - |
| PQ208 | - | 16 | 16 | 16 | 16 | 16 |
| FG256 | - | - | 16 | 16 | 16 | 16 |
| FG456 | - | - | - | 48 | 48 | 48 |

## Termination Examples

Creating a design with the Versatile I/O features requires the instantiation of the desired library primitive within the design code. At the board level, designers need to know the termination techniques required for each I/O standard.

This section describes some common application examples illustrating the termination techniques recommended by each of the standards supported by the Versatile I/O features. For a full range of accepted values for the DC voltage specifications for each standard, refer to the table associated with each figure.

The resistors used in each termination technique example and the transmission lines depicted represent board level components and are not meant to represent components on the device.

### GTL

A sample circuit illustrating a valid termination technique for GTL is shown in Figure 42. Table 20 lists DC voltage specifications for the GTL standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

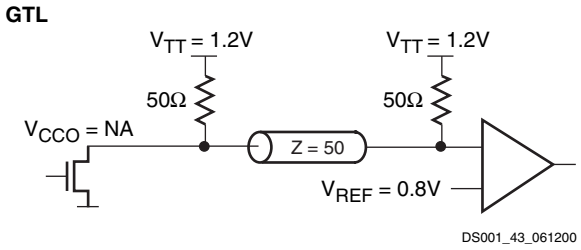


*Figure 42:* **Terminated GTL**

*Table 20:* **GTL Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | - | N/A | - |
| $V_{REF} = N \times V_{TT}$ (1) | 0.74 | 0.8 | 0.86 |
| $V_{TT}$ | 1.14 | 1.2 | 1.26 |
| $V_{IH} \geq V_{REF} + 0.05$ | 0.79 | 0.85 | - |
| $V_{IL} \leq V_{REF} - 0.05$ | - | 0.75 | 0.81 |
| $V_{OH}$ | - | - | - |
| $V_{OL}$ | - | 0.2 | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | - | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) at 0.4V | 32 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) at 0.2V | - | - | 40 |

**Notes:**
1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

### GTL+

A sample circuit illustrating a valid termination technique for GTL+ appears in Figure 43. DC voltage specifications appear in Table 21 for the GTL+ standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

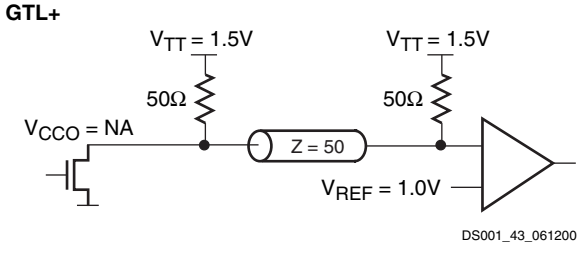


*Figure 43:* **Terminated GTL+**

*Table 21:* **GTL+ Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | - | - | - |
| $V_{REF} = N \times V_{TT}$ (1) | 0.88 | 1.0 | 1.12 |
| $V_{TT}$ | 1.35 | 1.5 | 1.65 |
| $V_{IH} \geq V_{REF} + 0.1$ | 0.98 | 1.1 | - |
| $V_{IL} \leq V_{REF} - 0.1$ | - | 0.9 | 1.02 |
| $V_{OH}$ | - | - | - |
| $V_{OL}$ | 0.3 | 0.45 | 0.6 |
| $I_{OH}$ at $V_{OH}$ (mA) | - | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) at 0.6V | 36 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) at 0.3V | - | - | 48 |

**Notes:**
1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

### HSTL Class I

A sample circuit illustrating a valid termination technique for HSTL_I appears in Figure 44. DC voltage specifications appear in Table 22 for the HSTL_1 standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

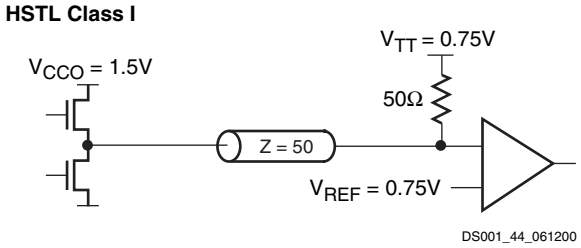


*Figure 44:* **Terminated HSTL Class I**

*Table 22:* **HSTL Class I Voltage Specification**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 1.40 | 1.50 | 1.60 |
| $V_{REF}$ | 0.68 | 0.75 | 0.90 |
| $V_{TT}$ | - | $V_{CCO} \times 0.5$ | - |
| $V_{IH}$ | $V_{REF} + 0.1$ | - | - |
| $V_{IL}$ | - | - | $V_{REF} - 0.1$ |
| $V_{OH}$ | $V_{CCO} - 0.4$ | - | - |
| $V_{OL}$ | | | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 8 | - | - |

### HSTL Class III

A sample circuit illustrating a valid termination technique for HSTL_III appears in Figure 45. DC voltage specifications appear in Table 23 for the HSTL_III standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

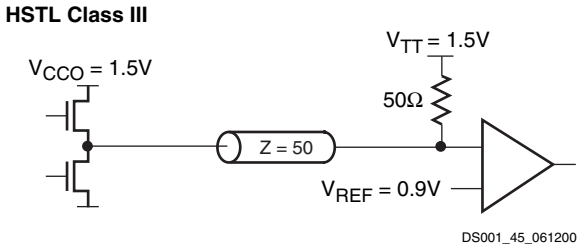


*Figure 45:* **Terminated HSTL Class III**

*Table 23:* **HSTL Class III Voltage Specification**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 1.40 | 1.50 | 1.60 |
| $V_{REF}$ (1) | - | 0.90 | - |
| $V_{TT}$ | - | $V_{CCO}$ | - |
| $V_{IH}$ | $V_{REF}$ + 0.1 | - | - |
| $V_{IL}$ | - | - | $V_{REF}$ – 0.1 |
| $V_{OH}$ | $V_{CCO}$ – 0.4 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 24 | - | - |

**Notes:**
1. Per EIA/JESD8-6, "The value of $V_{REF}$ is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

### HSTL Class IV

A sample circuit illustrating a valid termination technique for HSTL_IV appears in Figure 46.DC voltage specifications appear in Table 23 for the HSTL_IV standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics

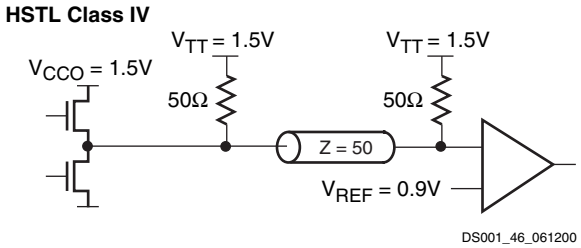


*Figure 46:* **Terminated HSTL Class IV**

*Table 24:* **HSTL Class IV Voltage Specification**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 1.40 | 1.50 | 1.60 |
| $V_{REF}$ | - | 0.90 | - |
| $V_{TT}$ | - | $V_{CCO}$ | - |
| $V_{IH}$ | $V_{REF}$ + 0.1 | - | - |
| $V_{IL}$ | - | - | $V_{REF}$ – 0.1 |
| $V_{OH}$ | $V_{CCO}$ – 0.4 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 48 | - | - |

**Notes:**
1. Per EIA/JESD8-6, "The value of $V_{REF}$ is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

### SSTL3 Class I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in Figure 47. DC voltage specifications appear in Table 25 for the SSTL3_I standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

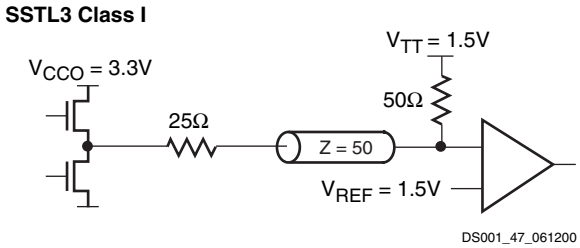


*Figure 47:* **Terminated SSTL3 Class I**

*Table 25:* **SSTL3_I Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF} = 0.45 \times V_{CCO}$ | 1.3 | 1.5 | 1.7 |
| $V_{TT} = V_{REF}$ | 1.3 | 1.5 | 1.7 |
| $V_{IH} \geq V_{REF} + 0.2$ | 1.5 | 1.7 | 3.9(1) |
| $V_{IL} \leq V_{REF} - 0.2$ | –0.3(2) | 1.3 | 1.5 |
| $V_{OH} \geq V_{REF} + 0.6$ | 1.9 | - | - |
| $V_{OL} \leq V_{REF} - 0.6$ | - | - | 1.1 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 8 | - | - |

**Notes:**
1. $V_{IH}$ maximum is $V_{CCO}$ + 0.3.
2. $V_{IL}$ minimum does not conform to the formula.

### SSTL3 Class II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in Figure 48. DC voltage specifications appear in Table 26 for the SSTL3_II standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

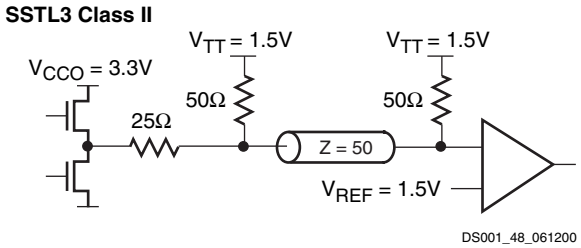


*Figure 48:* **Terminated SSTL3 Class II**

*Table 26:* **SSTL3_II Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF} = 0.45 \times V_{CCO}$ | 1.3 | 1.5 | 1.7 |
| $V_{TT} = V_{REF}$ | 1.3 | 1.5 | 1.7 |
| $V_{IH} \geq V_{REF} + 0.2$ | 1.5 | 1.7 | 3.9(1) |
| $V_{IL} \leq V_{REF} - 0.2$ | –0.3(2) | 1.3 | 1.5 |
| $V_{OH} \geq V_{REF} + 0.8$ | 2.1 | - | - |
| $V_{OL} \leq V_{REF} - 0.8$ | - | - | 0.9 |
| $I_{OH}$ at $V_{OH}$ (mA) | –16 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 16 | - | - |

**Notes:**
1. $V_{IH}$ maximum is $V_{CCO}$ + 0.3
2. $V_{IL}$ minimum does not conform to the formula

### SSTL2_I

A sample circuit illustrating a valid termination technique for SSTL2_I appears in Figure 49. DC voltage specifications appear in Table 27 for the SSTL2_I standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics

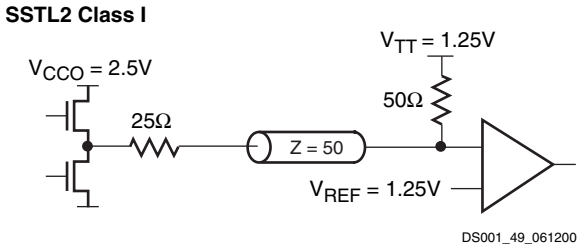


*Figure 49:* **Terminated SSTL2 Class I**

*Table 27:* **SSTL2_I Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 2.3 | 2.5 | 2.7 |
| $V_{REF} = 0.5 \times V_{CCO}$ | 1.15 | 1.25 | 1.35 |
| $V_{TT} = V_{REF} + N^{(1)}$ | 1.11 | 1.25 | 1.39 |
| $V_{IH} \geq V_{REF} + 0.18$ | 1.33 | 1.43 | $3.0^{(2)}$ |
| $V_{IL} \leq V_{REF} - 0.18$ | $-0.3^{(3)}$ | 1.07 | 1.17 |
| $V_{OH} \geq V_{REF} + 0.61$ | 1.76 | - | - |
| $V_{OL} \leq V_{REF} - 0.61$ | - | - | 0.74 |
| $I_{OH}$ at $V_{OH}$ (mA) | –7.6 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 7.6 | - | - |

**Notes:**
1. N must be greater than or equal to –0.04 and less than or equal to 0.04.
2. $V_{IH}$ maximum is $V_{CCO}$ + 0.3.
3. $V_{IL}$ minimum does not conform to the formula.

### SSTL2 Class II

A sample circuit illustrating a valid termination technique for SSTL2_II appears in Figure 50. DC voltage specifications appear in Table 28 for the SSTL2_II standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

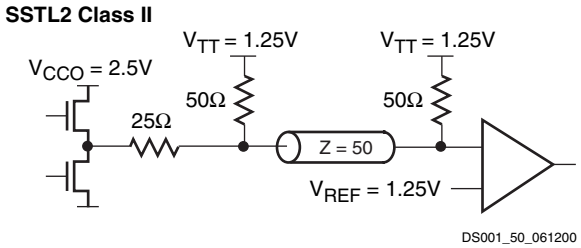


*Figure 50:* **Terminated SSTL2 Class II**

*Table 28:* **SSTL2_II Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 2.3 | 2.5 | 2.7 |
| $V_{REF} = 0.5 \times V_{CCO}$ | 1.15 | 1.25 | 1.35 |
| $V_{TT} = V_{REF} + N^{(1)}$ | 1.11 | 1.25 | 1.39 |
| $V_{IH} \geq V_{REF} + 0.18$ | 1.33 | 1.43 | $3.0^{(2)}$ |
| $V_{IL} \leq V_{REF} - 0.18$ | $-0.3^{(3)}$ | 1.07 | 1.17 |
| $V_{OH} \geq V_{REF} + 0.8$ | 1.95 | - | - |
| $V_{OL} \leq V_{REF} - 0.8$ | - | - | 0.55 |
| $I_{OH}$ at $V_{OH}$ (mA) | –15.2 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 15.2 | - | - |

**Notes:**
1. N must be greater than or equal to –0.04 and less than or equal to 0.04.
2. $V_{IH}$ maximum is $V_{CCO}$ + 0.3.
3. $V_{IL}$ minimum does not conform to the formula.

### CTT

A sample circuit illustrating a valid termination technique for CTT appear in Figure 51. DC voltage specifications appear in Table 29 for the CTT standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics .

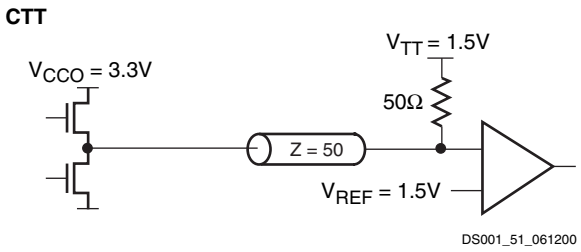


*Figure 51:* **Terminated CTT**

*Table 29:* **CTT Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 2.05(1) | 3.3 | 3.6 |
| $V_{REF}$ | 1.35 | 1.5 | 1.65 |
| $V_{TT}$ | 1.35 | 1.5 | 1.65 |
| $V_{IH} \geq V_{REF} + 0.2$ | 1.55 | 1.7 | - |
| $V_{IL} \leq V_{REF} - 0.2$ | - | 1.3 | 1.45 |
| $V_{OH} \geq V_{REF} + 0.4$ | 1.75 | 1.9 | - |
| $V_{OL} \leq V_{REF} - 0.4$ | - | 1.1 | 1.25 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 8 | - | - |

**Notes:**
1. Timing delays are calculated based on $V_{CCO}$ min of 3.0V.

### PCI33_3 and PCI66_3

PCI33_3 or PCI66_3 require no termination. DC voltage specifications appear in Table 30 for the PCI33_3 and PCI66_3 standards. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

*Table 30:* **PCI33_3 and PCI66_3 Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH} = 0.5 \times V_{CCO}$ | 1.5 | 1.65 | $V_{CCO}$+ 0.5 |
| $V_{IL} = 0.3 \times V_{CCO}$ | –0.5 | 0.99 | 1.08 |
| $V_{OH} = 0.9 \times V_{CCO}$ | 2.7 | - | - |
| $V_{OL} = 0.1 \times V_{CCO}$ | - | - | 0.36 |
| $I_{OH}$ at $V_{OH}$ (mA) | Note 1 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | Note 1 | - | - |

**Notes:**
1. Tested according to the relevant specification.

### PCI33_5

PCI33_5 requires no termination. DC voltage specifications appear in Table 31 for the PCI33_5 standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

*Table 31:* **PCI33_5 Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH}$ | 1.425 | 1.5 | 5.5 |
| $V_{IL}$ | –0.5 | 1.0 | 1.05 |
| $V_{OH}$ | 2.4 | - | - |
| $V_{OL}$ | - | - | 0.55 |
| $I_{OH}$ at $V_{OH}$ (mA) | Note 1 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | Note 1 | - | - |

**Notes:**
1. Tested according to the relevant specification.

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### LVTTL

LVTTL requires no termination. DC voltage specifications appears in Table 32 for the LVTTL standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

*Table 32:* **LVTTL Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH}$ | 2.0 | - | 5.5 |
| $V_{IL}$ | –0.5 | - | 0.8 |
| $V_{OH}$ | 2.4 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –24 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 24 | - | - |

**Notes:**
1. $V_{OL}$ and $V_{OH}$ for lower drive currents sample tested.

### LVCMOS2

LVCMOS2 requires no termination. DC voltage specifications appear in Table 33 for the LVCMOS2 standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

*Table 33:* **LVCMOS2 Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 2.3 | 2.5 | 2.7 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH}$ | 1.7 | - | 5.5 |
| $V_{IL}$ | –0.5 | - | 0.7 |
| $V_{OH}$ | 1.9 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –12 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 12 | - | - |

### AGP-2X

The specification for the AGP-2X standard does not document a recommended termination technique. DC voltage specifications appear in Table 34 for the AGP-2X standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

*Table 34:* **AGP-2X Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF} = N \times V_{CCO}$(1) | 1.17 | 1.32 | 1.48 |
| $V_{TT}$ | - | - | - |
| $V_{IH} \geq V_{REF} + 0.2$ | 1.37 | 1.52 | - |
| $V_{IL} \leq V_{REF} - 0.2$ | - | 1.12 | 1.28 |
| $V_{OH} \geq 0.9 \times V_{CCO}$ | 2.7 | 3.0 | - |
| $V_{OL} \leq 0.1 \times V_{CCO}$ | - | 0.33 | 0.36 |
| $I_{OH}$ at $V_{OH}$ (mA) | Note 2 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | Note 2 | - | - |

**Notes:**
1. N must be greater than or equal to 0.39 and less than or equal to 0.41.
2. Tested according to the relevant specification.

For design examples and more information on using the I/O, see XAPP179, *Using SelectIO Interfaces in Spartan-II and Spartan-IIE FPGAs*.

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# Revision History

| Date | Version | Description |
|---|---|---|
| 09/18/00 | 2.0 | Sectioned the Spartan-II Family data sheet into four modules. Corrected banking description. |
| 03/05/01 | 2.1 | Clarified guidelines for applying power to $V_{CCINT}$ and $V_{CCO}$ |
| 09/03/03 | 2.2 | The following changes were made:<br>• "Serial Modes," page 20 cautions about toggling $\overline{\text{WRITE}}$ during serial configuration.<br>• Maximum $V_{IH}$ values in Table 32 and Table 33 changed to 5.5V.<br>• In "Boundary Scan," page 13, removed sentence about lack of INTEST support.<br>• In Table 9, page 17, added note about the state of I/Os after power-on.<br>• In "Slave Parallel Mode," page 23, explained configuration bit alignment to SelectMap port. |
| 06/13/08 | 2.8 | Added note that TDI, TMS, and TCK have a default pull-up resistor. Added note on maximum daisy chain limit. Updated Figure 15 and Figure 18 since Mode pins can be pulled up to either 2.5V or 3.3V. Updated DLL section. Recommended using property or attribute instead of primitive to define I/O properties. Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8. |
| 03/12/21 | 2.9 | Added note 3 to Table 2 (see XCN20012, *Product Discontinuation Notice for Spartan-II PQ(G)208 Package Pin Products*). |

# Spartan-II FPGA Family: DC and Switching Characteristics

DS001-3 (v2.9) March 12, 2021 **Product Specification**

## Definition of Terms

In this document, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

**Advance:** Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

**Preliminary:** Based on preliminary characterization. Further changes are not expected.

**Unmarked:** Specifications not identified as either Advance or Preliminary are to be considered Final.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All limits are representative of worst-case supply voltage and junction temperature conditions. Typical numbers are based on measurements taken at a nominal $V_{CCINT}$ level of 2.5V and a junction temperature of 25°C. The parameters included are common to popular designs and typical applications. **All specifications are subject to change without notice.**

## DC Specifications

### Absolute Maximum Ratings(1)

| Symbol | Description | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage relative to GND(2) | | –0.5 | 3.0 | V |
| $V_{CCO}$ | Supply voltage relative to GND(2) | | –0.5 | 4.0 | V |
| $V_{REF}$ | Input reference voltage | | –0.5 | 3.6 | V |
| $V_{IN}$ | Input voltage relative to GND(3) | 5V tolerant I/O(4) | –0.5 | 5.5 | V |
| | | No 5V tolerance(5) | –0.5 | $V_{CCO}$ + 0.5 | V |
| $V_{TS}$ | Voltage applied to 3-state output | 5V tolerant I/O(4) | –0.5 | 5.5 | V |
| | | No 5V tolerance(5) | –0.5 | $V_{CCO}$ + 0.5 | V |
| $T_{STG}$ | Storage temperature (ambient) | | –65 | +150 | °C |
| $T_J$ | Junction temperature | | - | +125 | °C |

**Notes:**
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. Power supplies may turn on in any order.
3. $V_{IN}$ should not exceed $V_{CCO}$ by more than 3.6V over extended periods of time (e.g., longer than a day).
4. Spartan®-II device I/Os are 5V Tolerant whenever the LVTTL, LVCMOS2, or PCI33_5 signal standard has been selected. With 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either +5.5V or 10 mA, and undershoot must be limited to either –0.5V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to –2.0V or overshoot to +7.0V, provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
5. Without 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either $V_{CCO}$ + 0.5V or 10 mA, and undershoot must be limited to –0.5V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to –2.0V or overshoot to $V_{CCO}$ + 2.0V, provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
6. For soldering guidelines, see the Packaging Information on the Xilinx® web site.

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## Recommended Operating Conditions

| Symbol | Description | | Min | Max | Units |
|---|---|---|---|---|---|
| $T_J$ | Junction temperature(1) | Commercial | 0 | 85 | °C |
| | | Industrial | –40 | 100 | °C |
| $V_{CCINT}$ | Supply voltage relative to GND(2,5) | Commercial | 2.5 – 5% | 2.5 + 5% | V |
| | | Industrial | 2.5 – 5% | 2.5 + 5% | V |
| $V_{CCO}$ | Supply voltage relative to GND(3,5) | Commercial | 1.4 | 3.6 | V |
| | | Industrial | 1.4 | 3.6 | V |
| $T_{IN}$ | Input signal transition time(4) | | - | 250 | ns |

**Notes:**
1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
2. Functional operation is guaranteed down to a minimum $V_{CCINT}$ of 2.25V (Nominal $V_{CCINT}$ – 10%). For every 50 mV reduction in $V_{CCINT}$ below 2.375V (nominal $V_{CCINT}$ – 5%), all delay parameters increase by 3%.
3. Minimum and maximum values for $V_{CCO}$ vary according to the I/O standard selected.
4. Input and output measurement threshold is ~50% of $V_{CCO}$. See "Delay Measurement Methodology," page 60 for specific levels.
5. Supply voltages may be applied in any order desired.

## DC Characteristics Over Operating Conditions

| Symbol | Description | | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{DRINT}$ | Data Retention $V_{CCINT}$ voltage (below which configuration data may be lost) | | | 2.0 | - | - | V |
| $V_{DRIO}$ | Data Retention $V_{CCO}$ voltage (below which configuration data may be lost) | | | 1.2 | - | - | V |
| $I_{CCINTQ}$ | Quiescent $V_{CCINT}$ supply current(1) | XC2S15 | Commercial | - | 10 | 30 | mA |
| | | | Industrial | - | 10 | 60 | mA |
| | | XC2S30 | Commercial | - | 10 | 30 | mA |
| | | | Industrial | - | 10 | 60 | mA |
| | | XC2S50 | Commercial | - | 12 | 50 | mA |
| | | | Industrial | - | 12 | 100 | mA |
| | | XC2S100 | Commercial | - | 12 | 50 | mA |
| | | | Industrial | - | 12 | 100 | mA |
| | | XC2S150 | Commercial | - | 15 | 50 | mA |
| | | | Industrial | - | 15 | 100 | mA |
| | | XC2S200 | Commercial | - | 15 | 75 | mA |
| | | | Industrial | - | 15 | 150 | mA |
| $I_{CCOQ}$ | Quiescent $V_{CCO}$ supply current(1) | | | - | - | 2 | mA |
| $I_{REF}$ | $V_{REF}$ current per $V_{REF}$ pin | | | - | - | 20 | µA |
| $I_L$ | Input or output leakage current(2) | | | –10 | - | +10 | µA |
| $C_{IN}$ | Input capacitance (sample tested) | VQ, CS, TQ, PQ, FG packages | | - | - | 8 | pF |
| $I_{RPU}$ | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 3.3V (sample tested)(3) | | | - | - | 0.25 | mA |
| $I_{RPD}$ | Pad pull-down (when selected) @ $V_{IN}$ = 3.6V (sample tested)(3) | | | - | - | 0.15 | mA |

**Notes:**
1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. The I/O leakage current specification applies only when the $V_{CCINT}$ and $V_{CCO}$ supply voltages have reached their respective minimum Recommended Operating Conditions.
3. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not provide valid logic levels when input pins are connected to other circuits.

## Power-On Requirements

Spartan-II FPGAs require that a minimum supply current $I_{CCPO}$ be provided to the $V_{CCINT}$ lines for a successful power-on. If more current is available, the FPGA can consume more than $I_{CCPO}$ minimum, though this cannot adversely affect reliability.

A maximum limit for $I_{CCPO}$ is not specified. Therefore the use of foldback/crowbar supplies and fuses deserves special attention. In these cases, limit the $I_{CCPO}$ current to a level below the trip point for over-current protection in order to avoid inadvertently shutting down the supply.

| Symbol | Description | Conditions | | New Requirements(1) For Devices with Date Code 0321 or Later | | Old Requirements(1) For Devices with Date Code before 0321 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Junction Temperature(2) | Device Temperature Grade | Min | Max | Min | Max | |
| $I_{CCPO}$(3) | Total $V_{CCINT}$ supply current required during power-on | –40°C ≤ $T_J$ <–20°C | Industrial | 1.50 | - | 2.00 | - | A |
| | | –20°C ≤ $T_J$ < 0°C | Industrial | 1.00 | - | 2.00 | - | A |
| | | 0°C ≤ $T_J$ ≤ 85°C | Commercial | 0.25 | - | 0.50 | - | A |
| | | 85°C < $T_J$ ≤ 100°C | Industrial | 0.50 | - | 0.50 | - | A |
| $T_{CCPO}$(4,5) | $V_{CCINT}$ ramp time | –40°C≤ $T_J$≤ 100°C | All | - | 50 | - | 50 | ms |

**Notes:**

1. The date code is printed on the top of the device's package. See the "Device Part Marking" section in Module 1.
2. The expected $T_J$ range for the design determines the $I_{CCPO}$ minimum requirement. Use the applicable ranges in the junction temperature column to find the associated current values in the appropriate new or old requirements column according to the date code. Then choose the highest of these current values to serve as the minimum $I_{CCPO}$ requirement that must be met. For example, if the junction temperature for a given design is -25°C ≤ $T_J$ ≤ 75°C, then the new minimum $I_{CCPO}$ requirement is 1.5A. If 5°C ≤ $T_J$ ≤ 90°C, then the new minimum $I_{CCPO}$ requirement is 0.5A.
3. The $I_{CCPO}$ requirement applies for a brief time (commonly only a few milliseconds) when $V_{CCINT}$ ramps from 0 to 2.5V.
4. The ramp time is measured from GND to $V_{CCINT}$ max on a fully loaded board.
5. During power-on, the $V_{CCINT}$ ramp must increase steadily in voltage with no dips.
6. For more information on designing to meet the power-on specifications, refer to the application note **XAPP450 "Power-On Current Requirements for the Spartan-II and Spartan-IIE Families"**

## DC Input and Output Levels

Values for $V_{IL}$ and $V_{IH}$ are recommended input voltages. Values for $V_{OL}$ and $V_{OH}$ are guaranteed output voltages over the recommended operating conditions. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum $V_{CCO}$ with the respective $I_{OL}$ and $I_{OH}$ currents shown. Other standards are sample tested.

| Input/Output Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| LVTTL(1) | –0.5 | 0.8 | 2.0 | 5.5 | 0.4 | 2.4 | 24 | –24 |
| LVCMOS2 | –0.5 | 0.7 | 1.7 | 5.5 | 0.4 | 1.9 | 12 | –12 |
| PCI, 3.3V | –0.5 | 44% $V_{CCINT}$ | 60% $V_{CCINT}$ | $V_{CCO}$ + 0.5 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | Note (2) | Note (2) |
| PCI, 5.0V | –0.5 | 0.8 | 2.0 | 5.5 | 0.55 | 2.4 | Note (2) | Note (2) |
| GTL | –0.5 | $V_{REF}$ – 0.05 | $V_{REF}$ + 0.05 | 3.6 | 0.4 | N/A | 40 | N/A |
| GTL+ | –0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.6 | N/A | 36 | N/A |
| HSTL I | –0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCO}$ – 0.4 | 8 | –8 |
| HSTL III | –0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCO}$ – 0.4 | 24 | –8 |
| HSTL IV | –0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCO}$ – 0.4 | 48 | –8 |
| SSTL3 I | –0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | $V_{REF}$ – 0.6 | $V_{REF}$ + 0.6 | 8 | –8 |
| SSTL3 II | –0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | $V_{REF}$ – 0.8 | $V_{REF}$ + 0.8 | 16 | –16 |
| SSTL2 I | –0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | $V_{REF}$ – 0.6 | $V_{REF}$ + 0.6 | 7.6 | –7.6 |
| SSTL2 II | –0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | $V_{REF}$ – 0.8 | $V_{REF}$ + 0.8 | 15.2 | –15.2 |

| Input/Output Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| CTT | –0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | $V_{REF}$ – 0.4 | $V_{REF}$ + 0.4 | 8 | –8 |
| AGP | –0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | Note (2) | Note (2) |

**Notes:**
1. $V_{OL}$ and $V_{OH}$ for lower drive currents are sample tested.
2. Tested according to the relevant specifications.

## Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-II devices unless otherwise noted.

### Global Clock Input to Output Delay for LVTTL, *with* DLL (Pin-to-Pin)(1)

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | All | -6 | -5 | |
| | | | Min | Max | Max | |
| $T_{ICKOFDLL}$ | Global clock input to output delay using output flip-flop for LVTTL, 12 mA, fast slew rate, *with* DLL. | All | | 2.9 | 3.3 | ns |

**Notes:**
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see the tables "Constants for Calculating $T_{IOOP}$" and "Delay Measurement Methodology," page 60.
3. DLL output jitter is already included in the timing calculation.
4. For data *output* with different standards, adjust delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59. For a global clock input with standards other than LVTTL, adjust delays with values from the "I/O Standard Global Clock Input Adjustments," page 61.

### Global Clock Input to Output Delay for LVTTL, *without* DLL (Pin-to-Pin)(1)

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | All | -6 | -5 | |
| | | | Min | Max | Max | |
| $T_{ICKOF}$ | Global clock input to output delay using output flip-flop for LVTTL, 12 mA, fast slew rate, *without* DLL. | XC2S15 | | 4.5 | 5.4 | ns |
| | | XC2S30 | | 4.5 | 5.4 | ns |
| | | XC2S50 | | 4.5 | 5.4 | ns |
| | | XC2S100 | | 4.6 | 5.5 | ns |
| | | XC2S150 | | 4.6 | 5.5 | ns |
| | | XC2S200 | | 4.7 | 5.6 | ns |

**Notes:**
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see the tables "Constants for Calculating $T_{IOOP}$" and "Delay Measurement Methodology," page 60.
3. For data *output* with different standards, adjust delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59. For a global clock input with standards other than LVTTL, adjust delays with values from the "I/O Standard Global Clock Input Adjustments," page 61.

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## Global Clock Setup and Hold for LVTTL Standard, *with* DLL (Pin-to-Pin)

| Symbol | Description | Device | Speed Grade | | Units |
|---|---|---|---|---|---|
| | | | -6 | -5 | |
| | | | Min | Min | |
| $T_{PSDLL}$ / $T_{PHDLL}$ | Input setup and hold time relative to global clock input signal for LVTTL standard, no delay, IFF,(1) with DLL | All | 1.7 / 0 | 1.9 / 0 | ns |

**Notes:**
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DLL output jitter is already included in the timing calculation.
4. A zero hold time listing indicates no hold time or a negative hold time.
5. For data input with different standards, adjust the setup time delay by the values shown in "IOB Input Delay Adjustments for Different Standards," page 57. For a global clock input with standards other than LVTTL, adjust delays with values from the "I/O Standard Global Clock Input Adjustments," page 61.

## Global Clock Setup and Hold for LVTTL Standard, *without* DLL (Pin-to-Pin)

| Symbol | Description | Device | Speed Grade | | Units |
|---|---|---|---|---|---|
| | | | -6 | -5 | |
| | | | Min | Min | |
| $T_{PSFD}$ / $T_{PHFD}$ | Input setup and hold time relative to global clock input signal for LVTTL standard, no delay, IFF,(1) without DLL | XC2S15 | 2.2 / 0 | 2.7 / 0 | ns |
| | | XC2S30 | 2.2 / 0 | 2.7 / 0 | ns |
| | | XC2S50 | 2.2 / 0 | 2.7 / 0 | ns |
| | | XC2S100 | 2.3 / 0 | 2.8 / 0 | ns |
| | | XC2S150 | 2.4 / 0 | 2.9 / 0 | ns |
| | | XC2S200 | 2.4 / 0 | 3.0 / 0 | ns |

**Notes:**
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A zero hold time listing indicates no hold time or a negative hold time.
4. For data input with different standards, adjust the setup time delay by the values shown in "IOB Input Delay Adjustments for Different Standards," page 57. For a global clock input with standards other than LVTTL, adjust delays with values from the "I/O Standard Global Clock Input Adjustments," page 61.

## IOB Input Switching Characteristics(1)

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in "IOB Input Delay Adjustments for Different Standards," page 57.

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -6 | | -5 | | |
| | | | Min | Max | Min | Max | |
| **Propagation Delays** | | | | | | | |
| $T_{IOPI}$ | Pad to I output, no delay | All | - | 0.8 | - | 1.0 | ns |
| $T_{IOPID}$ | Pad to I output, with delay | All | - | 1.5 | - | 1.8 | ns |
| $T_{IOPLI}$ | Pad to output IQ via transparent latch, no delay | All | - | 1.7 | - | 2.0 | ns |
| $T_{IOPLID}$ | Pad to output IQ via transparent latch, with delay | XC2S15 | - | 3.8 | - | 4.5 | ns |
| | | XC2S30 | - | 3.8 | - | 4.5 | ns |
| | | XC2S50 | - | 3.8 | - | 4.5 | ns |
| | | XC2S100 | - | 3.8 | - | 4.5 | ns |
| | | XC2S150 | - | 4.0 | - | 4.7 | ns |
| | | XC2S200 | - | 4.0 | - | 4.7 | ns |
| **Sequential Delays** | | | | | | | |
| $T_{IOCKIQ}$ | Clock CLK to output IQ | All | - | 0.7 | - | 0.8 | ns |
| **Setup/Hold Times with Respect to Clock CLK(2)** | | | | | | | |
| $T_{IOPICK}$ / $T_{IOICKP}$ | Pad, no delay | All | 1.7 / 0 | - | 1.9 / 0 | - | ns |
| $T_{IOPICKD}$ / $T_{IOICKPD}$ | Pad, with delay(1) | XC2S15 | 3.8 / 0 | - | 4.4 / 0 | - | ns |
| | | XC2S30 | 3.8 / 0 | - | 4.4 / 0 | - | ns |
| | | XC2S50 | 3.8 / 0 | - | 4.4 / 0 | - | ns |
| | | XC2S100 | 3.8 / 0 | - | 4.4 / 0 | - | ns |
| | | XC2S150 | 3.9 / 0 | - | 4.6 / 0 | - | ns |
| | | XC2S200 | 3.9 / 0 | - | 4.6 / 0 | - | ns |
| $T_{IOICECK}$ / $T_{IOCKICE}$ | ICE input | All | 0.9 / 0.01 | - | 0.9 / 0.01 | - | ns |
| **Set/Reset Delays** | | | | | | | |
| $T_{IOSRCKI}$ | SR input (IFF, synchronous) | All | - | 1.1 | - | 1.2 | ns |
| $T_{IOSRIQ}$ | SR input to IQ (asynchronous) | All | - | 1.5 | - | 1.7 | ns |
| $T_{GSRQ}$ | GSR to output IQ | All | - | 9.9 | - | 11.7 | ns |

**Notes:**
1. Input timing for LVTTL is measured at 1.4V. For other I/O standards, see the table "Delay Measurement Methodology," page 60.
2. A zero hold time listing indicates no hold time or a negative hold time.

## IOB Input Delay Adjustments for Different Standards(1)

Input delays associated with the pad are specified for LVTTL. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

| Symbol | Description | Standard | Speed Grade | | Units |
|---|---|---|---|---|---|
| | | | -6 | -5 | |
| **Data Input Delay Adjustments** | | | | | |
| $T_{ILVTTL}$ | Standard-specific data input delay adjustments | LVTTL | 0 | 0 | ns |
| $T_{ILVCMOS2}$ | | LVCMOS2 | –0.04 | –0.05 | ns |
| $T_{IPCI33_3}$ | | PCI, 33 MHz, 3.3V | –0.11 | –0.13 | ns |
| $T_{IPCI33_5}$ | | PCI, 33 MHz, 5.0V | 0.26 | 0.30 | ns |
| $T_{IPCI66_3}$ | | PCI, 66 MHz, 3.3V | –0.11 | –0.13 | ns |
| $T_{IGTL}$ | | GTL | 0.20 | 0.24 | ns |
| $T_{IGTLP}$ | | GTL+ | 0.11 | 0.13 | ns |
| $T_{IHSTL}$ | | HSTL | 0.03 | 0.04 | ns |
| $T_{ISSTL2}$ | | SSTL2 | –0.08 | –0.09 | ns |
| $T_{ISSTL3}$ | | SSTL3 | –0.04 | –0.05 | ns |
| $T_{ICTT}$ | | CTT | 0.02 | 0.02 | ns |
| $T_{IAGP}$ | | AGP | –0.06 | –0.07 | ns |

**Notes:**
1. Input timing for LVTTL is measured at 1.4V. For other I/O standards, see the table "Delay Measurement Methodology," page 60.

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## IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59.

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -6 | | -5 | | |
| | | Min | Max | Min | Max | |
| **Propagation Delays** | | | | | | |
| $T_{IOOP}$ | O input to pad | - | 2.9 | - | 3.4 | ns |
| $T_{IOOLP}$ | O input to pad via transparent latch | - | 3.4 | - | 4.0 | ns |
| **3-state Delays** | | | | | | |
| $T_{IOTHZ}$ | T input to pad high-impedance(1) | - | 2.0 | - | 2.3 | ns |
| $T_{IOTON}$ | T input to valid data on pad | - | 3.0 | - | 3.6 | ns |
| $T_{IOTLPHZ}$ | T input to pad high impedance via transparent latch(1) | - | 2.5 | - | 2.9 | ns |
| $T_{IOTLPON}$ | T input to valid data on pad via transparent latch | - | 3.5 | - | 4.2 | ns |
| $T_{GTS}$ | GTS to pad high impedance(1) | - | 5.0 | - | 5.9 | ns |
| **Sequential Delays** | | | | | | |
| $T_{IOCKP}$ | Clock CLK to pad | - | 2.9 | - | 3.4 | ns |
| $T_{IOCKHZ}$ | Clock CLK to pad high impedance (synchronous)(1) | - | 2.3 | - | 2.7 | ns |
| $T_{IOCKON}$ | Clock CLK to valid data on pad (synchronous) | - | 3.3 | - | 4.0 | ns |
| **Setup/Hold Times with Respect to Clock CLK(2)** | | | | | | |
| $T_{IOOCK}$ / $T_{IOCKO}$ | O input | 1.1 / 0 | - | 1.3 / 0 | - | ns |
| $T_{IOOCECK}$ / $T_{IOCKOCE}$ | OCE input | 0.9 / 0.01 | - | 0.9 / 0.01 | - | ns |
| $T_{IOSRCKO}$ / $T_{IOCKOSR}$ | SR input (OFF) | 1.2 / 0 | - | 1.3 / 0 | - | ns |
| $T_{IOTCK}$ / $T_{IOCKT}$ | 3-state setup times, T input | 0.8 / 0 | - | 0.9 / 0 | - | ns |
| $T_{IOTCECK}$ / $T_{IOCKTCE}$ | 3-state setup times, TCE input | 1.0 / 0 | - | 1.0 / 0 | - | ns |
| $T_{IOSRCKT}$ / $T_{IOCKTSR}$ | 3-state setup times, SR input (TFF) | 1.1 / 0 | - | 1.2 / 0 | - | ns |
| **Set/Reset Delays** | | | | | | |
| $T_{IOSRP}$ | SR input to pad (asynchronous) | - | 3.7 | - | 4.4 | ns |
| $T_{IOSRHZ}$ | SR input to pad high impedance (asynchronous)(1) | - | 3.1 | - | 3.7 | ns |
| $T_{IOSRON}$ | SR input to valid data on pad (asynchronous) | - | 4.1 | - | 4.9 | ns |
| $T_{IOGSRQ}$ | GSR to pad | - | 9.9 | - | 11.7 | ns |

**Notes:**
1. Three-state turn-off delays should not be adjusted.
2. A zero hold time listing indicates no hold time or a negative hold time.

## IOB Output Delay Adjustments for Different Standards(1)

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

| Symbol | Description | Standard | Speed Grade | | Units |
|---|---|---|---|---|---|
| | | | -6 | -5 | |
| **Output Delay Adjustments (Adj)** | | | | | |
| $T_{OLVTTL_S2}$ | Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, $C_{SL}$) | LVTTL, Slow, 2 mA | 14.2 | 16.9 | ns |
| $T_{OLVTTL_S4}$ | | 4 mA | 7.2 | 8.6 | ns |
| $T_{OLVTTL_S6}$ | | 6 mA | 4.7 | 5.5 | ns |
| $T_{OLVTTL_S8}$ | | 8 mA | 2.9 | 3.5 | ns |
| $T_{OLVTTL_S12}$ | | 12 mA | 1.9 | 2.2 | ns |
| $T_{OLVTTL_S16}$ | | 16 mA | 1.7 | 2.0 | ns |
| $T_{OLVTTL_S24}$ | | 24 mA | 1.3 | 1.5 | ns |
| $T_{OLVTTL_F2}$ | | LVTTL, Fast, 2 mA | 12.6 | 15.0 | ns |
| $T_{OLVTTL_F4}$ | | 4 mA | 5.1 | 6.1 | ns |
| $T_{OLVTTL_F6}$ | | 6 mA | 3.0 | 3.6 | ns |
| $T_{OLVTTL_F8}$ | | 8 mA | 1.0 | 1.2 | ns |
| $T_{OLVTTL_F12}$ | | 12 mA | 0 | 0 | ns |
| $T_{OLVTTL_F16}$ | | 16 mA | –0.1 | –0.1 | ns |
| $T_{OLVTTL_F24}$ | | 24 mA | –0.1 | –0.2 | ns |
| $T_{OLVCMOS2}$ | | LVCMOS2 | 0.2 | 0.2 | ns |
| $T_{OPCI33_3}$ | | PCI, 33 MHz, 3.3V | 2.4 | 2.9 | ns |
| $T_{OPCI33_5}$ | | PCI, 33 MHz, 5.0V | 2.9 | 3.5 | ns |
| $T_{OPCI66_3}$ | | PCI, 66 MHz, 3.3V | –0.3 | –0.4 | ns |
| $T_{OGTL}$ | | GTL | 0.6 | 0.7 | ns |
| $T_{OGTLP}$ | | GTL+ | 0.9 | 1.1 | ns |
| $T_{OHSTL_I}$ | | HSTL I | –0.4 | –0.5 | ns |
| $T_{OHSTL_III}$ | | HSTL III | –0.8 | –1.0 | ns |
| $T_{OHSTL_IV}$ | | HSTL IV | –0.9 | –1.1 | ns |
| $T_{OSSTL2_I}$ | | SSTL2 I | –0.4 | –0.5 | ns |
| $T_{OSSLT2_II}$ | | SSTL2 II | –0.8 | –1.0 | ns |
| $T_{OSSTL3_I}$ | | SSTL3 I | –0.4 | –0.5 | ns |
| $T_{OSSTL3_II}$ | | SSTL3 II | –0.9 | –1.1 | ns |
| $T_{OCTT}$ | | CTT | –0.5 | –0.6 | ns |
| $T_{OAGP}$ | | AGP | –0.8 | –1.0 | ns |

**Notes:**

1. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see the tables "Constants for Calculating $T_{IOOP}$" and "Delay Measurement Methodology," page 60.

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## Calculation of $T_{IOOP}$ as a Function of Capacitance

$T_{IOOP}$ is the propagation delay from the O Input of the IOB to the pad. The values for $T_{IOOP}$ are based on the standard capacitive load ($C_{SL}$) for each I/O standard as listed in the table "Constants for Calculating $T_{IOOP}$", below.

For other capacitive loads, use the formulas below to calculate an adjusted propagation delay, $T_{IOOP1}$.

$$T_{IOOP1} = T_{IOOP} + Adj + (C_{LOAD} - C_{SL}) * F_L$$

Where:

- Adj is selected from "IOB Output Delay Adjustments for Different Standards", page 59, according to the I/O standard used
- $C_{LOAD}$ is the capacitive load for the design
- $F_L$ is the capacitance scaling factor

## Delay Measurement Methodology

| Standard | $V_L$ (1) | $V_H$ (1) | Meas. Point | $V_{REF}$ Typ (2) |
|---|---|---|---|---|
| LVTTL | 0 | 3 | 1.4 | - |
| LVCMOS2 | 0 | 2.5 | 1.125 | - |
| PCI33_5 | Per PCI Spec | | | - |
| PCI33_3 | Per PCI Spec | | | - |
| PCI66_3 | Per PCI Spec | | | - |
| GTL | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | $V_{REF}$ | 0.80 |
| GTL+ | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | $V_{REF}$ | 1.0 |
| HSTL Class I | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.75 |
| HSTL Class III | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.90 |
| HSTL Class IV | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.90 |
| SSTL3 I and II | $V_{REF}$ – 1.0 | $V_{REF}$ + 1.0 | $V_{REF}$ | 1.5 |
| SSTL2 I and II | $V_{REF}$ – 0.75 | $V_{REF}$ + 0.75 | $V_{REF}$ | 1.25 |
| CTT | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | $V_{REF}$ | 1.5 |
| AGP | $V_{REF}$ – (0.2x$V_{CCO}$) | $V_{REF}$ + (0.2x$V_{CCO}$) | $V_{REF}$ | Per AGP Spec |

**Notes:**
1. Input waveform switches between $V_L$ and $V_H$.
2. Measurements are made at $V_{REF}$ Typ, Maximum, and Minimum. Worst-case values are reported.
3. I/O parameter measurements are made with the capacitance values shown in the table, "Constants for Calculating $T_{IOOP}$". See Xilinx application note XAPP179 for the appropriate terminations.
4. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

## Constants for Calculating $T_{IOOP}$

| Standard | $C_{SL}$ (1) (pF) | $F_L$ (ns/pF) |
|---|---|---|
| LVTTL Fast Slew Rate, 2 mA drive | 35 | 0.41 |
| LVTTL Fast Slew Rate, 4 mA drive | 35 | 0.20 |
| LVTTL Fast Slew Rate, 6 mA drive | 35 | 0.13 |
| LVTTL Fast Slew Rate, 8 mA drive | 35 | 0.079 |
| LVTTL Fast Slew Rate, 12 mA drive | 35 | 0.044 |
| LVTTL Fast Slew Rate, 16 mA drive | 35 | 0.043 |
| LVTTL Fast Slew Rate, 24 mA drive | 35 | 0.033 |
| LVTTL Slow Slew Rate, 2 mA drive | 35 | 0.41 |
| LVTTL Slow Slew Rate, 4 mA drive | 35 | 0.20 |
| LVTTL Slow Slew Rate, 6 mA drive | 35 | 0.100 |
| LVTTL Slow Slew Rate, 8 mA drive | 35 | 0.086 |
| LVTTL Slow Slew Rate, 12 mA drive | 35 | 0.058 |
| LVTTL Slow Slew Rate, 16 mA drive | 35 | 0.050 |
| LVTTL Slow Slew Rate, 24 mA drive | 35 | 0.048 |
| LVCMOS2 | 35 | 0.041 |
| PCI 33 MHz 5V | 50 | 0.050 |
| PCI 33 MHZ 3.3V | 10 | 0.050 |
| PCI 66 MHz 3.3V | 10 | 0.033 |
| GTL | 0 | 0.014 |
| GTL+ | 0 | 0.017 |
| HSTL Class I | 20 | 0.022 |
| HSTL Class III | 20 | 0.016 |
| HSTL Class IV | 20 | 0.014 |
| SSTL2 Class I | 30 | 0.028 |
| SSTL2 Class II | 30 | 0.016 |
| SSTL3 Class I | 30 | 0.029 |
| SSTL3 Class II | 30 | 0.016 |
| CTT | 20 | 0.035 |
| AGP | 10 | 0.037 |

**Notes:**
1. I/O parameter measurements are made with the capacitance values shown above. See Xilinx application note XAPP179 for the appropriate terminations.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

## Clock Distribution Guidelines(1)

| Symbol | Description | Speed Grade | | Units |
|---|---|---|---|---|
| | | -6 | -5 | |
| | | Max | Max | |
| **GCLK Clock Skew** | | | | |
| $T_{GSKEWIOB}$ | Global clock skew between IOB flip-flops | 0.13 | 0.14 | ns |

**Notes:**
1. These clock distribution delays are provided for guidance only. They reflect the delays encountered in a typical design under worst-case conditions. Precise values for a particular design are provided by the timing analyzer.

## Clock Distribution Switching Characteristics

$T_{GPIO}$ is specified for LVTTL levels. For other standards, adjust $T_{GPIO}$ with the values shown in "I/O Standard Global Clock Input Adjustments".

| Symbol | Description | Speed Grade | | Units |
|---|---|---|---|---|
| | | -6 | -5 | |
| | | Max | Max | |
| **GCLK IOB and Buffer** | | | | |
| $T_{GPIO}$ | Global clock pad to output | 0.7 | 0.8 | ns |
| $T_{GIO}$ | Global clock buffer I input to O output | 0.7 | 0.8 | ns |

## I/O Standard Global Clock Input Adjustments

Delays associated with a global clock input pad are specified for LVTTL levels. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

| Symbol | Description | Standard | Speed Grade | | Units |
|---|---|---|---|---|---|
| | | | -6 | -5 | |
| **Data Input Delay Adjustments** | | | | | |
| $T_{GPLVTTL}$ | Standard-specific global clock input delay adjustments | LVTTL | 0 | 0 | ns |
| $T_{GPLVCMOS2}$ | | LVCMOS2 | –0.04 | –0.05 | ns |
| $T_{GPPCI33_3}$ | | PCI, 33 MHz, 3.3V | –0.11 | –0.13 | ns |
| $T_{GPPCI33_5}$ | | PCI, 33 MHz, 5.0V | 0.26 | 0.30 | ns |
| $T_{GPPCI66_3}$ | | PCI, 66 MHz, 3.3V | –0.11 | –0.13 | ns |
| $T_{GPGTL}$ | | GTL | 0.80 | 0.84 | ns |
| $T_{GPGTLP}$ | | GTL+ | 0.71 | 0.73 | ns |
| $T_{GPHSTL}$ | | HSTL | 0.63 | 0.64 | ns |
| $T_{GPSSTL2}$ | | SSTL2 | 0.52 | 0.51 | ns |
| $T_{GPSSTL3}$ | | SSTL3 | 0.56 | 0.55 | ns |
| $T_{GPCTT}$ | | CTT | 0.62 | 0.62 | ns |
| $T_{GPAGP}$ | | AGP | 0.54 | 0.53 | ns |

**Notes:**
1. Input timing for GPLVTTL is measured at 1.4V. For other I/O standards, see the table "Delay Measurement Methodology," page 60.

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## DLL Timing Parameters

All devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -6 | | -5 | | |
| | | Min | Max | Min | Max | |
| $F_{CLKINHF}$ | Input clock frequency (CLKDLLHF) | 60 | 200 | 60 | 180 | MHz |
| $F_{CLKINLF}$ | Input clock frequency (CLKDLL) | 25 | 100 | 25 | 90 | MHz |
| $T_{DLLPWHF}$ | Input clock pulse width (CLKDLLHF) | 2.0 | - | 2.4 | - | ns |
| $T_{DLLPWLF}$ | Input clock pulse width (CLKDLL) | 2.5 | - | 3.0 | - | ns |

## DLL Clock Tolerance, Jitter, and Phase Information

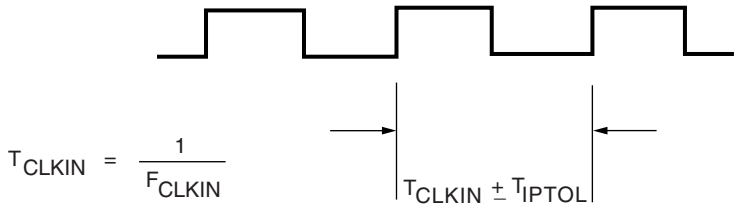
All DLL output jitter and phase specifications were determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

Figure 52, page 63, provides definitions for various parameters in the table below.

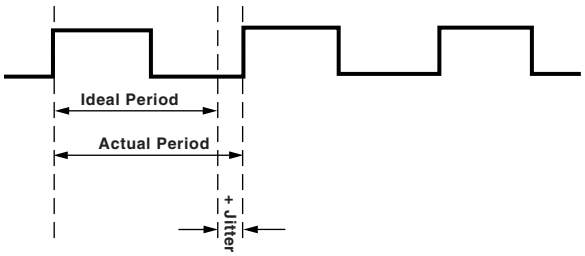
| Symbol | Description | $F_{CLKIN}$ | CLKDLLHF | | CLKDLL | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $T_{IPTOL}$ | Input clock period tolerance | | - | 1.0 | - | 1.0 | ns |
| $T_{IJITCC}$ | Input clock jitter tolerance (cycle-to-cycle) | | - | ±150 | - | ±300 | ps |
| $T_{LOCK}$ | Time required for DLL to acquire lock | > 60 MHz | - | 20 | - | 20 | µs |
| | | 50-60 MHz | - | - | - | 25 | µs |
| | | 40-50 MHz | - | - | - | 50 | µs |
| | | 30-40 MHz | - | - | - | 90 | µs |
| | | 25-30 MHz | - | - | - | 120 | µs |
| $T_{OJITCC}$ | Output jitter (cycle-to-cycle) for any DLL clock output(1) | | - | ±60 | - | ±60 | ps |
| $T_{PHIO}$ | Phase offset between CLKIN and CLKO(2) | | - | ±100 | - | ±100 | ps |
| $T_{PHOO}$ | Phase offset between clock outputs on the DLL(3) | | - | ±140 | - | ±140 | ps |
| $T_{PHIOM}$ | Maximum phase difference between CLKIN and CLKO(4) | | - | ±160 | - | ±160 | ps |
| $T_{PHOOM}$ | Maximum phase difference between clock outputs on the DLL(5) | | - | ±200 | - | ±200 | ps |

**Notes:**
1. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
2. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* output jitter and input clock jitter.
3. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
4. **Maximum Phase Difference between CLKIN an CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
5. **Maximum Phase Difference between Clock Outputs on the DLL** is the sum of Output JItter and Phase Offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (*excluding* input clock jitter).

***Period Tolerance:*** the allowed input clock period change in nanoseconds.




***Output Jitter:*** the difference between an ideal reference clock edge and the actual design.




***Phase Offset and Maximum Phase Difference***

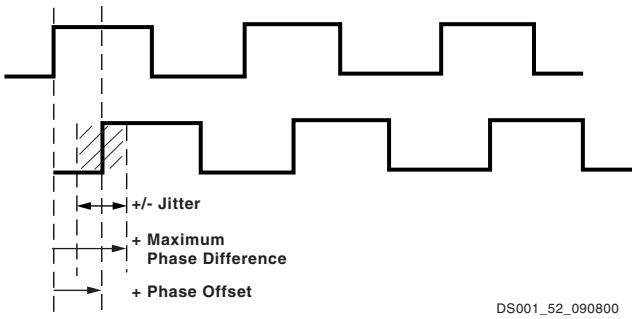



*Figure 52:* **Period Tolerance and Clock Jitter**

## CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -6 | | -5 | | |
| | | Min | Max | Min | Max | |
| **Combinatorial Delays** | | | | | | |
| $T_{ILO}$ | 4-input function: F/G inputs to X/Y outputs | - | 0.6 | - | 0.7 | ns |
| $T_{IF5}$ | 5-input function: F/G inputs to F5 output | - | 0.7 | - | 0.9 | ns |
| $T_{IF5X}$ | 5-input function: F/G inputs to X output | - | 0.9 | - | 1.1 | ns |
| $T_{IF6Y}$ | 6-input function: F/G inputs to Y output via F6 MUX | - | 1.0 | - | 1.1 | ns |
| $T_{F5INY}$ | 6-input function: F5IN input to Y output | - | 0.4 | - | 0.4 | ns |
| $T_{IFNCTL}$ | Incremental delay routing through transparent latch to XQ/YQ outputs | - | 0.7 | - | 0.9 | ns |
| $T_{BYYB}$ | BY input to YB output | - | 0.6 | - | 0.7 | ns |
| **Sequential Delays** | | | | | | |
| $T_{CKO}$ | FF clock CLK to XQ/YQ outputs | - | 1.1 | - | 1.3 | ns |
| $T_{CKLO}$ | Latch clock CLK to XQ/YQ outputs | - | 1.2 | - | 1.5 | ns |
| **Setup/Hold Times with Respect to Clock CLK(1)** | | | | | | |
| $T_{ICK}$ / $T_{CKI}$ | 4-input function: F/G inputs | 1.3 / 0 | - | 1.4 / 0 | - | ns |
| $T_{IF5CK}$ / $T_{CKIF5}$ | 5-input function: F/G inputs | 1.6 / 0 | - | 1.8 / 0 | - | ns |
| $T_{F5INCK}$ / $T_{CKF5IN}$ | 6-input function: F5IN input | 1.0 / 0 | - | 1.1 / 0 | - | ns |
| $T_{IF6CK}$ / $T_{CKIF6}$ | 6-input function: F/G inputs via F6 MUX | 1.6 / 0 | - | 1.8 / 0 | - | ns |
| $T_{DICK}$ / $T_{CKDI}$ | BX/BY inputs | 0.8 / 0 | - | 0.8 / 0 | - | ns |
| $T_{CECK}$ / $T_{CKCE}$ | CE input | 0.9 / 0 | - | 0.9 / 0 | - | ns |
| $T_{RCK}$ / $T_{CKR}$ | SR/BY inputs (synchronous) | 0.8 / 0 | - | 0.8 / 0 | - | ns |
| **Clock CLK** | | | | | | |
| $T_{CH}$ | Minimum pulse width, High | - | 1.9 | - | 1.9 | ns |
| $T_{CL}$ | Minimum pulse width, Low | - | 1.9 | - | 1.9 | ns |
| **Set/Reset** | | | | | | |
| $T_{RPW}$ | Minimum pulse width, SR/BY inputs | 3.1 | - | 3.1 | - | ns |
| $T_{RQ}$ | Delay from SR/BY inputs to XQ/YQ outputs (asynchronous) | - | 1.1 | - | 1.3 | ns |
| $T_{IOGSRQ}$ | Delay from GSR to XQ/YQ outputs | - | 9.9 | - | 11.7 | ns |
| $F_{TOG}$ | Toggle frequency (for export control) | - | 263 | - | 263 | MHz |

**Notes:**
1. A zero hold time listing indicates no hold time or a negative hold time.

## CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -6 | | -5 | | |
| | | Min | Max | Min | Max | |
| **Combinatorial Delays** | | | | | | |
| $T_{OPX}$ | F operand inputs to X via XOR | - | 0.8 | - | 0.9 | ns |
| $T_{OPXB}$ | F operand input to XB output | - | 1.3 | - | 1.5 | ns |
| $T_{OPY}$ | F operand input to Y via XOR | - | 1.7 | - | 2.0 | ns |
| $T_{OPYB}$ | F operand input to YB output | - | 1.7 | - | 2.0 | ns |
| $T_{OPCYF}$ | F operand input to COUT output | - | 1.3 | - | 1.5 | ns |
| $T_{OPGY}$ | G operand inputs to Y via XOR | - | 0.9 | - | 1.1 | ns |
| $T_{OPGYB}$ | G operand input to YB output | - | 1.6 | - | 2.0 | ns |
| $T_{OPCYG}$ | G operand input to COUT output | - | 1.2 | - | 1.4 | ns |
| $T_{BXCY}$ | BX initialization input to COUT | - | 0.9 | - | 1.0 | ns |
| $T_{CINX}$ | CIN input to X output via XOR | - | 0.4 | - | 0.5 | ns |
| $T_{CINXB}$ | CIN input to XB | - | 0.1 | - | 0.1 | ns |
| $T_{CINY}$ | CIN input to Y via XOR | - | 0.5 | - | 0.6 | ns |
| $T_{CINYB}$ | CIN input to YB | - | 0.6 | - | 0.7 | ns |
| $T_{BYP}$ | CIN input to COUT output | - | 0.1 | - | 0.1 | ns |
| **Multiplier Operation** | | | | | | |
| $T_{FANDXB}$ | F1/2 operand inputs to XB output via AND | - | 0.5 | - | 0.5 | ns |
| $T_{FANDYB}$ | F1/2 operand inputs to YB output via AND | - | 0.9 | - | 1.1 | ns |
| $T_{FANDCY}$ | F1/2 operand inputs to COUT output via AND | - | 0.5 | - | 0.6 | ns |
| $T_{GANDYB}$ | G1/2 operand inputs to YB output via AND | - | 0.6 | - | 0.7 | ns |
| $T_{GANDCY}$ | G1/2 operand inputs to COUT output via AND | - | 0.2 | - | 0.2 | ns |
| **Setup/Hold Times with Respect to Clock CLK(1)** | | | | | | |
| $T_{CCKX}$ / $T_{CKCX}$ | CIN input to FFX | 1.1 / 0 | - | 1.2 / 0 | - | ns |
| $T_{CCKY}$ / $T_{CKCY}$ | CIN input to FFY | 1.2 / 0 | - | 1.3 / 0 | - | ns |

**Notes:**
1. A zero hold time listing indicates no hold time or a negative hold time.

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## CLB Distributed RAM Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -6 | | -5 | | |
| | | Min | Max | Min | Max | |
| **Sequential Delays** | | | | | | |
| $T_{SHCKO16}$ | Clock CLK to X/Y outputs (WE active, 16 x 1 mode) | - | 2.2 | - | 2.6 | ns |
| $T_{SHCKO32}$ | Clock CLK to X/Y outputs (WE active, 32 x 1 mode) | - | 2.5 | - | 3.0 | ns |
| **Setup/Hold Times with Respect to Clock CLK(1)** | | | | | | |
| $T_{AS}$ / $T_{AH}$ | F/G address inputs | 0.7 / 0 | - | 0.7 / 0 | - | ns |
| $T_{DS}$ / $T_{DH}$ | BX/BY data inputs (DIN) | 0.8 / 0 | - | 0.9 / 0 | - | ns |
| $T_{WS}$ / $T_{WH}$ | CE input (WS) | 0.9 / 0 | - | 1.0 / 0 | - | ns |
| **Clock CLK** | | | | | | |
| $T_{WPH}$ | Minimum pulse width, High | - | 2.9 | - | 2.9 | ns |
| $T_{WPL}$ | Minimum pulse width, Low | - | 2.9 | - | 2.9 | ns |
| $T_{WC}$ | Minimum clock period to meet address write cycle time | - | 5.8 | - | 5.8 | ns |

**Notes:**
1. A zero hold time listing indicates no hold time or a negative hold time.

## CLB Shift Register Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -6 | | -5 | | |
| | | Min | Max | Min | Max | |
| **Sequential Delays** | | | | | | |
| $T_{REG}$ | Clock CLK to X/Y outputs | - | 3.47 | - | 3.88 | ns |
| **Setup Times with Respect to Clock CLK** | | | | | | |
| $T_{SHDICK}$ | BX/BY data inputs (DIN) | 0.8 | - | 0.9 | - | ns |
| $T_{SHCECK}$ | CE input (WS) | 0.9 | - | 1.0 | - | ns |
| **Clock CLK** | | | | | | |
| $T_{SRPH}$ | Minimum pulse width, High | - | 2.9 | - | 2.9 | ns |
| $T_{SRPL}$ | Minimum pulse width, Low | - | 2.9 | - | 2.9 | ns |

## Block RAM Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -6 | | -5 | | |
| | | Min | Max | Min | Max | |
| **Sequential Delays** | | | | | | |
| $T_{BCKO}$ | Clock CLK to DOUT output | - | 3.4 | - | 4.0 | ns |
| **Setup/Hold Times with Respect to Clock CLK(1)** | | | | | | |
| $T_{BACK}$ / $T_{BCKA}$ | ADDR inputs | 1.4 / 0 | - | 1.4 / 0 | - | ns |
| $T_{BDCK}$/ $T_{BCKD}$ | DIN inputs | 1.4 / 0 | - | 1.4 / 0 | - | ns |
| $T_{BECK}$/ $T_{BCKE}$ | EN inputs | 2.9 / 0 | - | 3.2 / 0 | - | ns |
| $T_{BRCK}$/ $T_{BCKR}$ | RST input | 2.7 / 0 | - | 2.9 / 0 | - | ns |
| $T_{BWCK}$/ $T_{BCKW}$ | WEN input | 2.6 / 0 | - | 2.8 / 0 | - | ns |
| **Clock CLK** | | | | | | |
| $T_{BPWH}$ | Minimum pulse width, High | - | 1.9 | - | 1.9 | ns |
| $T_{BPWL}$ | Minimum pulse width, Low | - | 1.9 | - | 1.9 | ns |
| $T_{BCCS}$ | CLKA -> CLKB setup time for different ports | - | 3.0 | - | 4.0 | ns |

**Notes:**
1. A zero hold time listing indicates no hold time or a negative hold time.

## TBUF Switching Characteristics

| Symbol | Description | Speed Grade | | Units |
|---|---|---|---|---|
| | | -6 | -5 | |
| | | Max | Max | |
| **Combinatorial Delays** | | | | |
| $T_{IO}$ | IN input to OUT output | 0 | 0 | ns |
| $T_{OFF}$ | TRI input to OUT output high impedance | 0.1 | 0.2 | ns |
| $T_{ON}$ | TRI input to valid data on OUT output | 0.1 | 0.2 | ns |

## JTAG Test Access Port Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -6 | | -5 | | |
| | | Min | Max | Min | Max | |
| **Setup and Hold Times with Respect to TCK** | | | | | | |
| $T_{TAPTCK}$ / $T_{TCKTAP}$ | TMS and TDI setup and hold times | 4.0 / 2.0 | - | 4.0 / 2.0 | - | ns |
| **Sequential Delays** | | | | | | |
| $T_{TCKTDO}$ | Output delay from clock TCK to output TDO | - | 11.0 | - | 11.0 | ns |
| FTCK | Maximum TCK clock frequency | - | 33 | - | 33 | MHz |

# Revision History

| Date | Version No. | Description |
|---|---|---|
| 09/18/00 | 2.0 | Sectioned the Spartan-II Family data sheet into four modules. Updated timing to reflect the latest speed files. Added current supply numbers and XC2S200 -5 timing numbers. Approved -5 timing numbers as preliminary information with exceptions as noted. |
| 11/02/00 | 2.1 | Removed Power Down feature. |
| 01/19/01 | 2.2 | DC and timing numbers updated to Preliminary for the XC2S50 and XC2S100. Industrial power-on current specifications and -6 DLL timing numbers added. Power-on specification clarified. |
| 03/09/01 | 2.3 | Added note on power sequencing. Clarified power-on current requirement. |
| 08/28/01 | 2.4 | Added -6 preliminary timing. Added typical and industrial standby current numbers. Specified min. power-on current by junction temperature instead of by device type (Commercial vs. Industrial). Eliminated minimum $V_{CCINT}$ ramp time requirement. Removed footnote limiting DLL operation to the Commercial temperature range. |
| 07/26/02 | 2.5 | Clarified that I/O leakage current is specified over the Recommended Operating Conditions for $V_{CCINT}$ and $V_{CCO}$. |
| 08/26/02 | 2.6 | Added references for XAPP450 to Power-On Current Specification. |
| 09/03/03 | 2.7 | Added relaxed minimum power-on current ($I_{CCPO}$) requirements to page 53. On page 64, moved $T_{RPW}$ values from maximum to minimum column. |
| 06/13/08 | 2.8 | Updated I/O measurement thresholds. Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8. |
| 03/12/21 | 2.9 | Added note 3 to Table 2 (see XCN20012, *Product Discontinuation Notice for Spartan-II PQ(G)208 Package Pin Products*). |

# Spartan-II FPGA Family: Pinout Tables

DS001-4 (v2.9) March 12, 2021 **Product Specification**

## Introduction

This section describes how the various pins on a Spartan®-II FPGA connect within the supported component packages, and provides device-specific thermal characteristics. Spartan-II FPGAs are available in both standard and Pb-free, RoHS versions of each package, with the Pb-free version adding a “G” to the middle of the package code. Except for the thermal characteristics, all information for the standard package applies equally to the Pb-free package.

## Pin Types

Most pins on a Spartan-II FPGA are general-purpose, user-defined I/O pins. There are, however, different functional types of pins on Spartan-II FPGA packages, as outlined in Table 35.

*Table 35:* **Pin Definitions**

| Pin Name | Dedicated | Direction | Description |
|---|---|---|---|
| GCK0, GCK1, GCK2, GCK3 | No | Input | Clock input pins that connect to Global Clock Buffers. These pins become user inputs when not needed for clocks. |
| M0, M1, M2 | Yes | Input | Mode pins are used to specify the configuration mode. |
| CCLK | Yes | Input or Output | The configuration Clock I/O pin. It is an input for slave-parallel and slave-serial modes, and output in master-serial mode. |
| $\overline{\text{PROGRAM}}$ | Yes | Input | Initiates a configuration sequence when asserted Low. |
| DONE | Yes | Bidirectional | Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output may be open drain. |
| $\overline{\text{INIT}}$ | No | Bidirectional (Open-drain) | When Low, indicates that the configuration memory is being cleared. This pin becomes a user I/O after configuration. |
| BUSY/DOUT | No | Output | In Slave Parallel mode, BUSY controls the rate at which configuration data is loaded. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.<br>In serial modes, DOUT provides configuration data to downstream devices in a daisy-chain. This pin becomes a user I/O after configuration. |
| D0/DIN, D1, D2, D3, D4, D5, D6, D7 | No | Input or Output | In Slave Parallel mode, D0-D7 are configuration data input pins. During readback, D0-D7 are output pins. These pins become user I/Os after configuration unless the Slave Parallel port is retained.<br>In serial modes, DIN is the single data input. This pin becomes a user I/O after configuration. |
| $\overline{\text{WRITE}}$ | No | Input | In Slave Parallel mode, the active-low Write Enable signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained. |
| $\overline{\text{CS}}$ | No | Input | In Slave Parallel mode, the active-low Chip Select signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained. |
| TDI, TDO, TMS, TCK | Yes | Mixed | Boundary Scan Test Access Port pins (IEEE 1149.1). |
| $V_{CCINT}$ | Yes | Input | Power supply pins for the internal core logic. |
| $V_{CCO}$ | Yes | Input | Power supply pins for output drivers (subject to banking rules) |
| $V_{REF}$ | No | Input | Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules). |
| GND | Yes | Input | Ground. |
| IRDY, TRDY | No | See PCI core documentation | These signals can only be accessed when using Xilinx® PCI cores. If the cores are not used, these pins are available as user I/Os. |

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*Table 36:* **Spartan-II Family Package Options**

| Package | Leads | Type | Maximum I/O | Lead Pitch (mm) | Footprint Area (mm) | Height (mm) | Mass[1] (g) |
|---|---|---|---|---|---|---|---|
| VQ100 / VQG100 | 100 | Very Thin Quad Flat Pack (VQFP) | 60 | 0.5 | 16 x 16 | 1.20 | 0.6 |
| TQ144 / TQG144 | 144 | Thin Quad Flat Pack (TQFP) | 92 | 0.5 | 22 x 22 | 1.60 | 1.4 |
| CS144 / CSG144 | 144 | Chip Scale Ball Grid Array (CSBGA) | 92 | 0.8 | 12 x 12 | 1.20 | 0.3 |
| PQ208 / PQG208 | 208 | Plastic Quad Flat Pack (PQFP) | 140 | 0.5 | 30.6 x 30.6 | 3.70 | 5.3 |
| FG256 / FGG256 | 256 | Fine-pitch Ball Grid Array (FBGA) | 176 | 1.0 | 17 x 17 | 2.00 | 0.9 |
| FG456 / FGG456 | 456 | Fine-pitch Ball Grid Array (FBGA) | 284 | 1.0 | 23 x 23 | 2.60 | 2.2 |

**Notes:**

1. Package mass is ±10%.

Note: Some early versions of Spartan-II devices, including the XC2S15 and XC2S30 ES devices and the XC2S150 with date code 0045 or earlier, included a power-down pin. For more information, see Answer Record 10500.

## VCCO Banks

Some of the I/O standards require specific $V_{CCO}$ voltages. These voltages are externally connected to device pins that serve groups of IOBs, called banks. Eight I/O banks result from separating each edge of the FPGA into two banks (see Figure 3 in Module 2). Each bank has multiple $V_{CCO}$ pins which must be connected to the same voltage. In the smaller packages, the $V_{CCO}$ pins are connected between banks, effectively reducing the number of independent banks available (see Table 37). These interconnected banks are shown in the Pinout Tables with $V_{CCO}$ pads for multiple banks connected to the same pin.

*Table 37:* **Independent VCCO Banks Available**

| Package | VQ100 PQ208 | CS144 TQ144 | FG256 FG456 |
|---|---|---|---|
| Independent Banks | 1 | 4 | 8 |

## Package Overview

Table 36 shows the six low-cost, space-saving production package styles for the Spartan-II family.

Each package style is available in an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra ‘G’ in the package style name. For example, the standard “CS144” package becomes “CSG144” when ordered as the Pb-free option. Leaded (non-Pb-free) packages may be available for selected devices, with the same pin-out and without the "G" in the ordering code; contact Xilinx sales for more information. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 38.

For additional package information, see UG112: *Device Package User Guide*.

## Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx web site at the specified location in Table 38.

Material Declaration Data Sheets (MDDS) are also available on the Xilinx web site for each package.

*Table 38:* **Xilinx Package Documentation**

| Package | Drawing | MDDS |
|---|---|---|
| VQ100 | Package Drawing | PK173_VQ100 |
| VQG100 | | PK130_VQG100 |
| TQ144 | Package Drawing | PK169_TQ144 |
| TQG144 | | PK126_TQG144 |
| CS144 | Package Drawing | PK149_CS144 |
| CSG144 | | PK103_CSG144 |
| PQ208 | Package Drawing | PK166_PQ208 |
| PQG208 | | PK123_PQG208 |
| FG256 | Package Drawing | PK151_FG256 |
| FGG256 | | PK105_FGG256 |
| FG456 | Package Drawing | PK154_FG456 |
| FGG456 | | PK109_FGG456 |

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## Package Thermal Characteristics

Table 39 provides the thermal characteristics for the various Spartan-II FPGA package offerings. This information is also available using the Thermal Query tool on xilinx.com (www.xilinx.com/cgi-bin/thermal/thermal.pl).

The junction-to-case thermal resistance ($\theta_{JC}$) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board ($\theta_{JB}$) value similarly reports the difference between the board and junction temperature. The junction-to-ambient ($\theta_{JA}$) value reports the temperature difference between the ambient environment and the junction temperature. The $\theta_{JA}$ value is reported at different air velocities, measured in linear feet per minute (LFM). The “Still Air (0 LFM)” column shows the $\theta_{JA}$ value in a system without a fan. The thermal resistance drops with increasing air flow.

*Table 39:* **Spartan-II Package Thermal Characteristics**

| Package | Device | Junction-to-Case ($\theta_{JC}$) | Junction-to-Board ($\theta_{JB}$) | Junction-to-Ambient ($\theta_{JA}$) at Different Air Flows | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | Still Air (0 LFM) | 250 LFM | 500 LFM | 750 LFM | |
| VQ100 VQG100 | XC2S15 | 11.3 | N/A | 44.1 | 36.7 | 34.2 | 33.3 | °C/Watt |
| | XC2S30 | 10.1 | N/A | 40.7 | 33.9 | 31.5 | 30.8 | °C/Watt |
| TQ144 TQG144 | XC2S15 | 7.3 | N/A | 38.6 | 30.0 | 25.7 | 24.1 | °C/Watt |
| | XC2S30 | 6.7 | N/A | 34.7 | 27.0 | 23.1 | 21.7 | °C/Watt |
| | XC2S50 | 5.8 | N/A | 32.2 | 25.1 | 21.4 | 20.1 | °C/Watt |
| | XC2S100 | 5.3 | N/A | 31.4 | 24.4 | 20.9 | 19.6 | °C/Watt |
| CS144 CSG144 | XC2S30 | 2.8 | N/A | 34.0 | 26.0 | 23.9 | 23.2 | °C/Watt |
| PQ208 PQG208 | XC2S50 | 6.7 | N/A | 25.2 | 18.6 | 16.4 | 15.2 | °C/Watt |
| | XC2S100 | 5.9 | N/A | 24.6 | 18.1 | 16.0 | 14.9 | °C/Watt |
| | XC2S150 | 5.0 | N/A | 23.8 | 17.6 | 15.6 | 14.4 | °C/Watt |
| | XC2S200 | 4.1 | N/A | 23.0 | 17.0 | 15.0 | 13.9 | °C/Watt |
| FG256 FGG256 | XC2S50 | 7.1 | 17.6 | 27.2 | 21.4 | 20.3 | 19.8 | °C/Watt |
| | XC2S100 | 5.8 | 15.1 | 25.1 | 19.5 | 18.3 | 17.8 | °C/Watt |
| | XC2S150 | 4.6 | 12.7 | 23.0 | 17.6 | 16.3 | 15.8 | °C/Watt |
| | XC2S200 | 3.5 | 10.7 | 21.4 | 16.1 | 14.7 | 14.2 | °C/Watt |
| FG456 FGG456 | XC2S150 | 2.0 | N/A | 21.9 | 17.3 | 15.8 | 15.2 | °C/Watt |
| | XC2S200 | 2.0 | N/A | 21.0 | 16.6 | 15.1 | 14.5 | °C/Watt |

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# Pinout Tables

The following device-specific pinout tables include all packages available for each Spartan®-II device. They follow the pad locations around the die, and include Boundary Scan register locations.

## XC2S15 Device Pinouts

| XC2S15 Pad Name | | VQ100 | TQ144 | CS144 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| GND | - | P1 | P143 | A1 | - |
| TMS | - | P2 | P142 | B1 | - |
| I/O | 7 | P3 | P141 | C2 | 77 |
| I/O | 7 | - | P140 | C1 | 80 |
| I/O, $V_{REF}$ | 7 | P4 | P139 | D4 | 83 |
| I/O | 7 | P5 | P137 | D2 | 86 |
| I/O | 7 | P6 | P136 | D1 | 89 |
| GND | - | - | P135 | E4 | - |
| I/O | 7 | P7 | P134 | E3 | 92 |
| I/O | 7 | - | P133 | E2 | 95 |
| I/O, $V_{REF}$ | 7 | P8 | P132 | E1 | 98 |
| I/O | 7 | P9 | P131 | F4 | 101 |
| I/O | 7 | - | P130 | F3 | 104 |
| I/O, IRDY(1) | 7 | P10 | P129 | F2 | 107 |
| GND | - | P11 | P128 | F1 | - |
| $V_{CCO}$ | 7 | P12 | P127 | G2 | - |
| $V_{CCO}$ | 6 | P12 | P127 | G2 | - |
| I/O, TRDY(1) | 6 | P13 | P126 | G1 | 110 |
| $V_{CCINT}$ | - | P14 | P125 | G3 | - |
| I/O | 6 | - | P124 | G4 | 113 |
| I/O | 6 | P15 | P123 | H1 | 116 |
| I/O, $V_{REF}$ | 6 | P16 | P122 | H2 | 119 |
| I/O | 6 | - | P121 | H3 | 122 |
| I/O | 6 | P17 | P120 | H4 | 125 |
| GND | - | - | P119 | J1 | - |
| I/O | 6 | P18 | P118 | J2 | 128 |
| I/O | 6 | P19 | P117 | J3 | 131 |
| I/O, $V_{REF}$ | 6 | P20 | P115 | K1 | 134 |
| I/O | 6 | - | P114 | K2 | 137 |
| I/O | 6 | P21 | P113 | K3 | 140 |
| I/O | 6 | P22 | P112 | L1 | 143 |
| M1 | - | P23 | P111 | L2 | 146 |
| GND | - | P24 | P110 | L3 | - |
| M0 | - | P25 | P109 | M1 | 147 |
| $V_{CCO}$ | 6 | P26 | P108 | M2 | - |
| $V_{CCO}$ | 5 | P26 | P107 | N1 | - |

## XC2S15 Device Pinouts *(Continued)*

| XC2S15 Pad Name | | VQ100 | TQ144 | CS144 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| M2 | - | P27 | P106 | N2 | 148 |
| I/O | 5 | - | P103 | K4 | 155 |
| I/O, $V_{REF}$ | 5 | P30 | P102 | L4 | 158 |
| I/O | 5 | P31 | P100 | N4 | 161 |
| I/O | 5 | P32 | P99 | K5 | 164 |
| GND | - | - | P98 | L5 | - |
| $V_{CCINT}$ | - | P33 | P97 | M5 | - |
| I/O | 5 | - | P96 | N5 | 167 |
| I/O | 5 | - | P95 | K6 | 170 |
| I/O, $V_{REF}$ | 5 | P34 | P94 | L6 | 173 |
| I/O | 5 | - | P93 | M6 | 176 |
| $V_{CCINT}$ | - | P35 | P92 | N6 | - |
| I, GCK1 | 5 | P36 | P91 | M7 | 185 |
| $V_{CCO}$ | 5 | P37 | P90 | N7 | - |
| $V_{CCO}$ | 4 | P37 | P90 | N7 | - |
| GND | - | P38 | P89 | L7 | - |
| I, GCK0 | 4 | P39 | P88 | K7 | 186 |
| I/O | 4 | P40 | P87 | N8 | 190 |
| I/O | 4 | - | P86 | M8 | 193 |
| I/O, $V_{REF}$ | 4 | P41 | P85 | L8 | 196 |
| I/O | 4 | - | P84 | K8 | 199 |
| I/O | 4 | - | P83 | N9 | 202 |
| $V_{CCINT}$ | - | P42 | P82 | M9 | - |
| GND | - | - | P81 | L9 | - |
| I/O | 4 | P43 | P80 | K9 | 205 |
| I/O | 4 | P44 | P79 | N10 | 208 |
| I/O, $V_{REF}$ | 4 | P45 | P77 | L10 | 211 |
| I/O | 4 | - | P76 | N11 | 214 |
| I/O | 4 | P46 | P75 | M11 | 217 |
| I/O | 4 | P47 | P74 | L11 | 220 |
| GND | - | P48 | P73 | N12 | - |
| DONE | 3 | P49 | P72 | M12 | 223 |
| $V_{CCO}$ | 4 | P50 | P71 | N13 | - |
| $V_{CCO}$ | 3 | P50 | P70 | M13 | - |
| $\overline{PROGRAM}$ | - | P51 | P69 | L12 | 226 |
| I/O ($\overline{INIT}$) | 3 | P52 | P68 | L13 | 227 |
| I/O (D7) | 3 | P53 | P67 | K10 | 230 |
| I/O | 3 | - | P66 | K11 | 233 |
| I/O, $V_{REF}$ | 3 | P54 | P65 | K12 | 236 |
| I/O | 3 | P55 | P63 | J10 | 239 |
| I/O (D6) | 3 | P56 | P62 | J11 | 242 |

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## XC2S15 Device Pinouts *(Continued)*

| XC2S15 Pad Name | | VQ100 | TQ144 | CS144 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| GND | - | - | P61 | J12 | - |
| I/O (D5) | 3 | P57 | P60 | J13 | 245 |
| I/O | 3 | P58 | P59 | H10 | 248 |
| I/O, $V_{REF}$ | 3 | P59 | P58 | H11 | 251 |
| I/O (D4) | 3 | P60 | P57 | H12 | 254 |
| I/O | 3 | - | P56 | H13 | 257 |
| $V_{CCINT}$ | - | P61 | P55 | G12 | - |
| I/O, TRDY(1) | 3 | P62 | P54 | G13 | 260 |
| $V_{CCO}$ | 3 | P63 | P53 | G11 | - |
| $V_{CCO}$ | 2 | P63 | P53 | G11 | - |
| GND | - | P64 | P52 | G10 | - |
| I/O, IRDY(1) | 2 | P65 | P51 | F13 | 263 |
| I/O | 2 | - | P50 | F12 | 266 |
| I/O (D3) | 2 | P66 | P49 | F11 | 269 |
| I/O, $V_{REF}$ | 2 | P67 | P48 | F10 | 272 |
| I/O | 2 | P68 | P47 | E13 | 275 |
| I/O (D2) | 2 | P69 | P46 | E12 | 278 |
| GND | - | - | P45 | E11 | - |
| I/O (D1) | 2 | P70 | P44 | E10 | 281 |
| I/O | 2 | P71 | P43 | D13 | 284 |
| I/O, $V_{REF}$ | 2 | P72 | P41 | D11 | 287 |
| I/O | 2 | - | P40 | C13 | 290 |
| I/O (DIN, D0) | 2 | P73 | P39 | C12 | 293 |
| I/O (DOUT, BUSY) | 2 | P74 | P38 | C11 | 296 |
| CCLK | 2 | P75 | P37 | B13 | 299 |
| $V_{CCO}$ | 2 | P76 | P36 | B12 | - |
| $V_{CCO}$ | 1 | P76 | P35 | A13 | - |
| TDO | 2 | P77 | P34 | A12 | - |
| GND | - | P78 | P33 | B11 | - |
| TDI | - | P79 | P32 | A11 | - |
| I/O ($\overline{CS}$) | 1 | P80 | P31 | D10 | 0 |
| I/O ($\overline{WRITE}$) | 1 | P81 | P30 | C10 | 3 |
| I/O | 1 | - | P29 | B10 | 6 |
| I/O, $V_{REF}$ | 1 | P82 | P28 | A10 | 9 |
| I/O | 1 | P83 | P27 | D9 | 12 |
| I/O | 1 | P84 | P26 | C9 | 15 |
| GND | - | - | P25 | B9 | - |
| $V_{CCINT}$ | - | P85 | P24 | A9 | - |
| I/O | 1 | - | P23 | D8 | 18 |
| I/O | 1 | - | P22 | C8 | 21 |

## XC2S15 Device Pinouts *(Continued)*

| XC2S15 Pad Name | | VQ100 | TQ144 | CS144 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| I/O, $V_{REF}$ | 1 | P86 | P21 | B8 | 24 |
| I/O | 1 | - | P20 | A8 | 27 |
| I/O | 1 | P87 | P19 | B7 | 30 |
| I, GCK2 | 1 | P88 | P18 | A7 | 36 |
| GND | - | P89 | P17 | C7 | - |
| $V_{CCO}$ | 1 | P90 | P16 | D7 | - |
| $V_{CCO}$ | 0 | P90 | P16 | D7 | - |
| I, GCK3 | 0 | P91 | P15 | A6 | 37 |
| $V_{CCINT}$ | - | P92 | P14 | B6 | - |
| I/O | 0 | - | P13 | C6 | 44 |
| I/O, $V_{REF}$ | 0 | P93 | P12 | D6 | 47 |
| I/O | 0 | - | P11 | A5 | 50 |
| I/O | 0 | - | P10 | B5 | 53 |
| $V_{CCINT}$ | - | P94 | P9 | C5 | - |
| GND | - | - | P8 | D5 | - |
| I/O | 0 | P95 | P7 | A4 | 56 |
| I/O | 0 | P96 | P6 | B4 | 59 |
| I/O, $V_{REF}$ | 0 | P97 | P5 | C4 | 62 |
| I/O | 0 | - | P4 | A3 | 65 |
| I/O | 0 | P98 | P3 | B3 | 68 |
| TCK | - | P99 | P2 | C3 | - |
| $V_{CCO}$ | 0 | P100 | P1 | A2 | - |
| $V_{CCO}$ | 7 | P100 | P144 | B2 | - |

04/18/01

**Notes:**

1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. See "VCCO Banks" for details on $V_{CCO}$ banking.

## Additional XC2S15 Package Pins

**VQ100**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P28 | P29 | - | - | - | - |

11/02/00

**TQ144**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P42 | P64 | P78 | P101 | P104 | P105 |
| P116 | P138 | - | - | - | - |

11/02/00

**CS144**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| D3 | D12 | J4 | K13 | M3 | M4 |
| M10 | N3 | - | - | - | - |

11/02/00

## XC2S30 Device Pinouts

| XC2S30 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| Function | Bank | VQ100 | TQ144 | CS144 | PQ208 | Bndry Scan |
| GND | - | P1 | P143 | A1 | P1 | - |
| TMS | - | P2 | P142 | B1 | P2 | - |
| I/O | 7 | P3 | P141 | C2 | P3 | 113 |
| I/O | 7 | - | P140 | C1 | P4 | 116 |
| I/O | 7 | - | - | - | P5 | 119 |
| I/O, $V_{REF}$ | 7 | P4 | P139 | D4 | P6 | 122 |
| I/O | 7 | - | P138 | D3 | P8 | 125 |
| I/O | 7 | P5 | P137 | D2 | P9 | 128 |
| I/O | 7 | P6 | P136 | D1 | P10 | 131 |
| GND | - | - | P135 | E4 | P11 | - |
| $V_{CCO}$ | 7 | - | - | - | P12 | - |
| I/O | 7 | P7 | P134 | E3 | P14 | 134 |
| I/O | 7 | - | P133 | E2 | P15 | 137 |
| I/O | 7 | - | - | - | P16 | 140 |
| I/O | 7 | - | - | - | P17 | 143 |
| I/O | 7 | - | - | - | P18 | 146 |
| GND | - | - | - | - | P19 | - |
| I/O, $V_{REF}$ | 7 | P8 | P132 | E1 | P20 | 149 |
| I/O | 7 | P9 | P131 | F4 | P21 | 152 |
| I/O | 7 | - | P130 | F3 | P22 | 155 |
| I/O | 7 | - | - | - | P23 | 158 |
| I/O, IRDY(1) | 7 | P10 | P129 | F2 | P24 | 161 |
| GND | - | P11 | P128 | F1 | P25 | - |
| $V_{CCO}$ | 7 | P12 | P127 | G2 | P26 | - |
| $V_{CCO}$ | 6 | P12 | P127 | G2 | P26 | - |
| I/O, TRDY(1) | 6 | P13 | P126 | G1 | P27 | 164 |
| $V_{CCINT}$ | - | P14 | P125 | G3 | P28 | - |
| I/O | 6 | - | P124 | G4 | P29 | 170 |
| I/O | 6 | P15 | P123 | H1 | P30 | 173 |
| I/O, $V_{REF}$ | 6 | P16 | P122 | H2 | P31 | 176 |
| GND | - | - | - | - | P32 | - |
| I/O | 6 | - | - | - | P33 | 179 |
| I/O | 6 | - | - | - | P34 | 182 |
| I/O | 6 | - | - | - | P35 | 185 |
| I/O | 6 | - | P121 | H3 | P36 | 188 |
| I/O | 6 | P17 | P120 | H4 | P37 | 191 |
| $V_{CCO}$ | 6 | - | - | - | P39 | - |
| GND | - | - | P119 | J1 | P40 | - |
| I/O | 6 | P18 | P118 | J2 | P41 | 194 |
| I/O | 6 | P19 | P117 | J3 | P42 | 197 |
| I/O | 6 | - | P116 | J4 | P43 | 200 |

## XC2S30 Device Pinouts *(Continued)*

| XC2S30 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| Function | Bank | VQ100 | TQ144 | CS144 | PQ208 | Bndry Scan |
| I/O, $V_{REF}$ | 6 | P20 | P115 | K1 | P45 | 203 |
| I/O | 6 | - | - | - | P46 | 206 |
| I/O | 6 | - | P114 | K2 | P47 | 209 |
| I/O | 6 | P21 | P113 | K3 | P48 | 212 |
| I/O | 6 | P22 | P112 | L1 | P49 | 215 |
| M1 | - | P23 | P111 | L2 | P50 | 218 |
| GND | - | P24 | P110 | L3 | P51 | - |
| M0 | - | P25 | P109 | M1 | P52 | 219 |
| $V_{CCO}$ | 6 | P26 | P108 | M2 | P53 | - |
| $V_{CCO}$ | 5 | P26 | P107 | N1 | P53 | - |
| M2 | - | P27 | P106 | N2 | P54 | 220 |
| I/O | 5 | - | P103 | K4 | P57 | 227 |
| I/O | 5 | - | - | - | P58 | 230 |
| I/O, $V_{REF}$ | 5 | P30 | P102 | L4 | P59 | 233 |
| I/O | 5 | - | P101 | M4 | P61 | 236 |
| I/O | 5 | P31 | P100 | N4 | P62 | 239 |
| I/O | 5 | P32 | P99 | K5 | P63 | 242 |
| GND | - | - | P98 | L5 | P64 | - |
| $V_{CCO}$ | 5 | - | - | - | P65 | - |
| $V_{CCINT}$ | - | P33 | P97 | M5 | P66 | - |
| I/O | 5 | - | P96 | N5 | P67 | 245 |
| I/O | 5 | - | P95 | K6 | P68 | 248 |
| I/O | 5 | - | - | - | P69 | 251 |
| I/O | 5 | - | - | - | P70 | 254 |
| I/O | 5 | - | - | - | P71 | 257 |
| GND | - | - | - | - | P72 | - |
| I/O, $V_{REF}$ | 5 | P34 | P94 | L6 | P73 | 260 |
| I/O | 5 | - | - | - | P74 | 263 |
| I/O | 5 | - | P93 | M6 | P75 | 266 |
| $V_{CCINT}$ | - | P35 | P92 | N6 | P76 | - |
| I, GCK1 | 5 | P36 | P91 | M7 | P77 | 275 |
| $V_{CCO}$ | 5 | P37 | P90 | N7 | P78 | - |
| $V_{CCO}$ | 4 | P37 | P90 | N7 | P78 | - |
| GND | - | P38 | P89 | L7 | P79 | - |
| I, GCK0 | 4 | P39 | P88 | K7 | P80 | 276 |
| I/O | 4 | P40 | P87 | N8 | P81 | 280 |
| I/O | 4 | - | P86 | M8 | P82 | 283 |
| I/O | 4 | - | - | - | P83 | 286 |
| I/O, $V_{REF}$ | 4 | P41 | P85 | L8 | P84 | 289 |
| GND | - | - | - | - | P85 | - |
| I/O | 4 | - | - | - | P86 | 292 |

XC2S200-5FG256I AMD IC FPGA 176 I/O 256FBGA



## XC2S30 Device Pinouts *(Continued)*

| XC2S30 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| Function | Bank | VQ100 | TQ144 | CS144 | PQ208 | Bndry Scan |
| I/O | 4 | - | - | - | P87 | 295 |
| I/O | 4 | - | - | - | P88 | 298 |
| I/O | 4 | - | P84 | K8 | P89 | 301 |
| I/O | 4 | - | P83 | N9 | P90 | 304 |
| $V_{CCINT}$ | - | P42 | P82 | M9 | P91 | - |
| $V_{CCO}$ | 4 | - | - | - | P92 | - |
| GND | - | - | P81 | L9 | P93 | - |
| I/O | 4 | P43 | P80 | K9 | P94 | 307 |
| I/O | 4 | P44 | P79 | N10 | P95 | 310 |
| I/O | 4 | - | P78 | M10 | P96 | 313 |
| I/O, $V_{REF}$ | 4 | P45 | P77 | L10 | P98 | 316 |
| I/O | 4 | - | - | - | P99 | 319 |
| I/O | 4 | - | P76 | N11 | P100 | 322 |
| I/O | 4 | P46 | P75 | M11 | P101 | 325 |
| I/O | 4 | P47 | P74 | L11 | P102 | 328 |
| GND | - | P48 | P73 | N12 | P103 | - |
| DONE | 3 | P49 | P72 | M12 | P104 | 331 |
| $V_{CCO}$ | 4 | P50 | P71 | N13 | P105 | - |
| $V_{CCO}$ | 3 | P50 | P70 | M13 | P105 | - |
| $\overline{PROGRAM}$ | - | P51 | P69 | L12 | P106 | 334 |
| I/O ($\overline{INIT}$) | 3 | P52 | P68 | L13 | P107 | 335 |
| I/O (D7) | 3 | P53 | P67 | K10 | P108 | 338 |
| I/O | 3 | - | P66 | K11 | P109 | 341 |
| I/O | 3 | - | - | - | P110 | 344 |
| I/O, $V_{REF}$ | 3 | P54 | P65 | K12 | P111 | 347 |
| I/O | 3 | - | P64 | K13 | P113 | 350 |
| I/O | 3 | P55 | P63 | J10 | P114 | 353 |
| I/O (D6) | 3 | P56 | P62 | J11 | P115 | 356 |
| GND | - | - | P61 | J12 | P116 | - |
| $V_{CCO}$ | 3 | - | - | - | P117 | - |
| I/O (D5) | 3 | P57 | P60 | J13 | P119 | 359 |
| I/O | 3 | P58 | P59 | H10 | P120 | 362 |
| I/O | 3 | - | - | - | P121 | 365 |
| I/O | 3 | - | - | - | P122 | 368 |
| I/O | 3 | - | - | - | P123 | 371 |
| GND | - | - | - | - | P124 | - |
| I/O, $V_{REF}$ | 3 | P59 | P58 | H11 | P125 | 374 |
| I/O (D4) | 3 | P60 | P57 | H12 | P126 | 377 |
| I/O | 3 | - | P56 | H13 | P127 | 380 |
| $V_{CCINT}$ | - | P61 | P55 | G12 | P128 | - |
| I/O, TRDY(1) | 3 | P62 | P54 | G13 | P129 | 386 |

## XC2S30 Device Pinouts *(Continued)*

| XC2S30 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| Function | Bank | VQ100 | TQ144 | CS144 | PQ208 | Bndry Scan |
| $V_{CCO}$ | 3 | P63 | P53 | G11 | P130 | - |
| $V_{CCO}$ | 2 | P63 | P53 | G11 | P130 | - |
| GND | - | P64 | P52 | G10 | P131 | - |
| I/O, IRDY(1) | 2 | P65 | P51 | F13 | P132 | 389 |
| I/O | 2 | - | - | - | P133 | 392 |
| I/O | 2 | - | P50 | F12 | P134 | 395 |
| I/O (D3) | 2 | P66 | P49 | F11 | P135 | 398 |
| I/O, $V_{REF}$ | 2 | P67 | P48 | F10 | P136 | 401 |
| GND | - | - | - | - | P137 | - |
| I/O | 2 | - | - | - | P138 | 404 |
| I/O | 2 | - | - | - | P139 | 407 |
| I/O | 2 | - | - | - | P140 | 410 |
| I/O | 2 | P68 | P47 | E13 | P141 | 413 |
| I/O (D2) | 2 | P69 | P46 | E12 | P142 | 416 |
| $V_{CCO}$ | 2 | - | - | - | P144 | - |
| GND | - | - | P45 | E11 | P145 | - |
| I/O (D1) | 2 | P70 | P44 | E10 | P146 | 419 |
| I/O | 2 | P71 | P43 | D13 | P147 | 422 |
| I/O | 2 | - | P42 | D12 | P148 | 425 |
| I/O, $V_{REF}$ | 2 | P72 | P41 | D11 | P150 | 428 |
| I/O | 2 | - | - | - | P151 | 431 |
| I/O | 2 | - | P40 | C13 | P152 | 434 |
| I/O (DIN, D0) | 2 | P73 | P39 | C12 | P153 | 437 |
| I/O (DOUT, BUSY) | 2 | P74 | P38 | C11 | P154 | 440 |
| CCLK | 2 | P75 | P37 | B13 | P155 | 443 |
| $V_{CCO}$ | 2 | P76 | P36 | B12 | P156 | - |
| $V_{CCO}$ | 1 | P76 | P35 | A13 | P156 | - |
| TDO | 2 | P77 | P34 | A12 | P157 | - |
| GND | - | P78 | P33 | B11 | P158 | - |
| TDI | - | P79 | P32 | A11 | P159 | - |
| I/O ($\overline{CS}$) | 1 | P80 | P31 | D10 | P160 | 0 |
| I/O ($\overline{WRITE}$) | 1 | P81 | P30 | C10 | P161 | 3 |
| I/O | 1 | - | P29 | B10 | P162 | 6 |
| I/O | 1 | - | - | - | P163 | 9 |
| I/O, $V_{REF}$ | 1 | P82 | P28 | A10 | P164 | 12 |
| I/O | 1 | - | - | - | P166 | 15 |
| I/O | 1 | P83 | P27 | D9 | P167 | 18 |
| I/O | 1 | P84 | P26 | C9 | P168 | 21 |
| GND | - | - | P25 | B9 | P169 | - |
| $V_{CCO}$ | 1 | - | - | - | P170 | - |

## XC2S30 Device Pinouts *(Continued)*

| XC2S30 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| Function | Bank | VQ100 | TQ144 | CS144 | PQ208 | Bndry Scan |
| $V_{CCINT}$ | - | P85 | P24 | A9 | P171 | - |
| I/O | 1 | - | P23 | D8 | P172 | 24 |
| I/O | 1 | - | P22 | C8 | P173 | 27 |
| I/O | 1 | - | - | - | P174 | 30 |
| I/O | 1 | - | - | - | P175 | 33 |
| I/O | 1 | - | - | - | P176 | 36 |
| GND | - | - | - | - | P177 | - |
| I/O, $V_{REF}$ | 1 | P86 | P21 | B8 | P178 | 39 |
| I/O | 1 | - | - | - | P179 | 42 |
| I/O | 1 | - | P20 | A8 | P180 | 45 |
| I/O | 1 | P87 | P19 | B7 | P181 | 48 |
| I, GCK2 | 1 | P88 | P18 | A7 | P182 | 54 |
| GND | - | P89 | P17 | C7 | P183 | - |
| $V_{CCO}$ | 1 | P90 | P16 | D7 | P184 | - |
| $V_{CCO}$ | 0 | P90 | P16 | D7 | P184 | - |
| I, GCK3 | 0 | P91 | P15 | A6 | P185 | 55 |
| $V_{CCINT}$ | - | P92 | P14 | B6 | P186 | - |
| I/O | 0 | - | P13 | C6 | P187 | 62 |
| I/O | 0 | - | - | - | P188 | 65 |
| I/O, $V_{REF}$ | 0 | P93 | P12 | D6 | P189 | 68 |
| GND | - | - | - | - | P190 | - |
| I/O | 0 | - | - | - | P191 | 71 |
| I/O | 0 | - | - | - | P192 | 74 |
| I/O | 0 | - | - | - | P193 | 77 |
| I/O | 0 | - | P11 | A5 | P194 | 80 |
| I/O | 0 | - | P10 | B5 | P195 | 83 |
| $V_{CCINT}$ | - | P94 | P9 | C5 | P196 | - |
| $V_{CCO}$ | 0 | - | - | - | P197 | - |
| GND | - | - | P8 | D5 | P198 | - |
| I/O | 0 | P95 | P7 | A4 | P199 | 86 |
| I/O | 0 | P96 | P6 | B4 | P200 | 89 |
| I/O | 0 | - | - | - | P201 | 92 |

## XC2S30 Device Pinouts *(Continued)*

| XC2S30 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| Function | Bank | VQ100 | TQ144 | CS144 | PQ208 | Bndry Scan |
| I/O, $V_{REF}$ | 0 | P97 | P5 | C4 | P203 | 95 |
| I/O | 0 | - | - | - | P204 | 98 |
| I/O | 0 | - | P4 | A3 | P205 | 101 |
| I/O | 0 | P98 | P3 | B3 | P206 | 104 |
| TCK | - | P99 | P2 | C3 | P207 | - |
| $V_{CCO}$ | 0 | P100 | P1 | A2 | P208 | - |
| $V_{CCO}$ | 7 | P100 | P144 | B2 | P208 | - |

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**Notes:**
1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. See "VCCO Banks" for details on $V_{CCO}$ banking.

## Additional XC2S30 Package Pins

**VQ100**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P28 | P29 | - | - | - | - |

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**TQ144**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P104 | P105 | - | - | - | - |

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**CS144**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| M3 | N3 | - | - | - | - |

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**PQ208**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P7 | P13 | P38 | P44 | P55 | P56 |
| P60 | P97 | P112 | P118 | P143 | P149 |
| P165 | P202 | - | - | - | - |

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**Notes:**
1. For the PQ208 package, P13, P38, P118, and P143, which are Not Connected Pins on the XC2S30, are assigned to $V_{CCINT}$ on larger devices.

XC2S200-5FG256I AMD IC FPGA 176 I/O 256FBGA



## XC2S50 Device Pinouts

| XC2S50 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | Bndry Scan |
| GND | - | P143 | P1 | GND* | - |
| TMS | - | P142 | P2 | D3 | - |
| I/O | 7 | P141 | P3 | C2 | 149 |
| I/O | 7 | - | - | A2 | 152 |
| I/O | 7 | P140 | P4 | B1 | 155 |
| I/O | 7 | - | - | E3 | 158 |
| I/O | 7 | - | P5 | D2 | 161 |
| GND | - | - | - | GND* | - |
| I/O, $V_{REF}$ | 7 | P139 | P6 | C1 | 164 |
| I/O | 7 | - | P7 | F3 | 167 |
| I/O | 7 | - | - | E2 | 170 |
| I/O | 7 | P138 | P8 | E4 | 173 |
| I/O | 7 | P137 | P9 | D1 | 176 |
| I/O | 7 | P136 | P10 | E1 | 179 |
| GND | - | P135 | P11 | GND* | - |
| $V_{CCO}$ | 7 | - | P12 | $V_{CCO}$ Bank 7* | - |
| $V_{CCINT}$ | - | - | P13 | $V_{CCINT}$* | - |
| I/O | 7 | P134 | P14 | F2 | 182 |
| I/O | 7 | P133 | P15 | G3 | 185 |
| I/O | 7 | - | - | F1 | 188 |
| I/O | 7 | - | P16 | F4 | 191 |
| I/O | 7 | - | P17 | F5 | 194 |
| I/O | 7 | - | P18 | G2 | 197 |
| GND | - | - | P19 | GND* | - |
| I/O, $V_{REF}$ | 7 | P132 | P20 | H3 | 200 |
| I/O | 7 | P131 | P21 | G4 | 203 |
| I/O | 7 | - | - | H2 | 206 |
| I/O | 7 | P130 | P22 | G5 | 209 |
| I/O | 7 | - | P23 | H4 | 212 |
| I/O, IRDY(1) | 7 | P129 | P24 | G1 | 215 |
| GND | - | P128 | P25 | GND* | - |
| $V_{CCO}$ | 7 | P127 | P26 | $V_{CCO}$ Bank 7* | - |
| $V_{CCO}$ | 6 | P127 | P26 | $V_{CCO}$ Bank 6* | - |
| I/O, TRDY(1) | 6 | P126 | P27 | J2 | 218 |
| $V_{CCINT}$ | - | P125 | P28 | $V_{CCINT}$* | - |
| I/O | 6 | P124 | P29 | H1 | 224 |
| I/O | 6 | - | - | J4 | 227 |
| I/O | 6 | P123 | P30 | J1 | 230 |
| I/O, $V_{REF}$ | 6 | P122 | P31 | J3 | 233 |

## XC2S50 Device Pinouts *(Continued)*

| XC2S50 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | Bndry Scan |
| GND | - | - | P32 | GND* | - |
| I/O | 6 | - | P33 | K5 | 236 |
| I/O | 6 | - | P34 | K2 | 239 |
| I/O | 6 | - | P35 | K1 | 242 |
| I/O | 6 | - | - | K3 | 245 |
| I/O | 6 | P121 | P36 | L1 | 248 |
| I/O | 6 | P120 | P37 | L2 | 251 |
| $V_{CCINT}$ | - | - | P38 | $V_{CCINT}$* | - |
| $V_{CCO}$ | 6 | - | P39 | $V_{CCO}$ Bank 6* | - |
| GND | - | P119 | P40 | GND* | - |
| I/O | 6 | P118 | P41 | K4 | 254 |
| I/O | 6 | P117 | P42 | M1 | 257 |
| I/O | 6 | P116 | P43 | L4 | 260 |
| I/O | 6 | - | - | M2 | 263 |
| I/O | 6 | - | P44 | L3 | 266 |
| I/O, $V_{REF}$ | 6 | P115 | P45 | N1 | 269 |
| GND | - | - | - | GND* | - |
| I/O | 6 | - | P46 | P1 | 272 |
| I/O | 6 | - | - | L5 | 275 |
| I/O | 6 | P114 | P47 | N2 | 278 |
| I/O | 6 | - | - | M4 | 281 |
| I/O | 6 | P113 | P48 | R1 | 284 |
| I/O | 6 | P112 | P49 | M3 | 287 |
| M1 | - | P111 | P50 | P2 | 290 |
| GND | - | P110 | P51 | GND* | - |
| M0 | - | P109 | P52 | N3 | 291 |
| $V_{CCO}$ | 6 | P108 | P53 | $V_{CCO}$ Bank 6* | - |
| $V_{CCO}$ | 5 | P107 | P53 | $V_{CCO}$ Bank 5* | - |
| M2 | - | P106 | P54 | R3 | 292 |
| I/O | 5 | - | - | N5 | 299 |
| I/O | 5 | P103 | P57 | T2 | 302 |
| I/O | 5 | - | - | P5 | 305 |
| I/O | 5 | - | P58 | T3 | 308 |
| GND | - | - | - | GND* | - |
| I/O, $V_{REF}$ | 5 | P102 | P59 | T4 | 311 |
| I/O | 5 | - | P60 | M6 | 314 |
| I/O | 5 | - | - | T5 | 317 |
| I/O | 5 | P101 | P61 | N6 | 320 |
| I/O | 5 | P100 | P62 | R5 | 323 |

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## XC2S50 Device Pinouts *(Continued)*

| XC2S50 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | Bndry Scan |
| I/O | 5 | P99 | P63 | P6 | 326 |
| GND | - | P98 | P64 | GND* | - |
| $V_{CCO}$ | 5 | - | P65 | $V_{CCO}$ Bank 5* | - |
| $V_{CCINT}$ | - | P97 | P66 | $V_{CCINT}$* | - |
| I/O | 5 | P96 | P67 | R6 | 329 |
| I/O | 5 | P95 | P68 | M7 | 332 |
| I/O | 5 | - | P69 | N7 | 338 |
| I/O | 5 | - | P70 | T6 | 341 |
| I/O | 5 | - | P71 | P7 | 344 |
| GND | - | - | P72 | GND* | - |
| I/O, $V_{REF}$ | 5 | P94 | P73 | P8 | 347 |
| I/O | 5 | - | P74 | R7 | 350 |
| I/O | 5 | - | - | T7 | 353 |
| I/O | 5 | P93 | P75 | T8 | 356 |
| $V_{CCINT}$ | - | P92 | P76 | $V_{CCINT}$* | - |
| I, GCK1 | 5 | P91 | P77 | R8 | 365 |
| $V_{CCO}$ | 5 | P90 | P78 | $V_{CCO}$ Bank 5* | - |
| $V_{CCO}$ | 4 | P90 | P78 | $V_{CCO}$ Bank 4* | - |
| GND | - | P89 | P79 | GND* | - |
| I, GCK0 | 4 | P88 | P80 | N8 | 366 |
| I/O | 4 | P87 | P81 | N9 | 370 |
| I/O | 4 | P86 | P82 | R9 | 373 |
| I/O | 4 | - | - | N10 | 376 |
| I/O | 4 | - | P83 | T9 | 379 |
| I/O, $V_{REF}$ | 4 | P85 | P84 | P9 | 382 |
| GND | - | - | P85 | GND* | - |
| I/O | 4 | - | P86 | M10 | 385 |
| I/O | 4 | - | P87 | R10 | 388 |
| I/O | 4 | - | P88 | P10 | 391 |
| I/O | 4 | P84 | P89 | T10 | 397 |
| I/O | 4 | P83 | P90 | R11 | 400 |
| $V_{CCINT}$ | - | P82 | P91 | $V_{CCINT}$* | - |
| $V_{CCO}$ | 4 | - | P92 | $V_{CCO}$ Bank 4* | - |
| GND | - | P81 | P93 | GND* | - |
| I/O | 4 | P80 | P94 | M11 | 403 |
| I/O | 4 | P79 | P95 | T11 | 406 |
| I/O | 4 | P78 | P96 | N11 | 409 |
| I/O | 4 | - | - | R12 | 412 |

## XC2S50 Device Pinouts *(Continued)*

| XC2S50 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | Bndry Scan |
| I/O | 4 | - | P97 | P11 | 415 |
| I/O, $V_{REF}$ | 4 | P77 | P98 | T12 | 418 |
| GND | - | - | - | GND* | - |
| I/O | 4 | - | P99 | T13 | 421 |
| I/O | 4 | - | - | N12 | 424 |
| I/O | 4 | P76 | P100 | R13 | 427 |
| I/O | 4 | - | - | P12 | 430 |
| I/O | 4 | P75 | P101 | P13 | 433 |
| I/O | 4 | P74 | P102 | T14 | 436 |
| GND | - | P73 | P103 | GND* | - |
| DONE | 3 | P72 | P104 | R14 | 439 |
| $V_{CCO}$ | 4 | P71 | P105 | $V_{CCO}$ Bank 4* | - |
| $V_{CCO}$ | 3 | P70 | P105 | $V_{CCO}$ Bank 3* | - |
| $\overline{PROGRAM}$ | - | P69 | P106 | P15 | 442 |
| I/O ($\overline{INIT}$) | 3 | P68 | P107 | N15 | 443 |
| I/O (D7) | 3 | P67 | P108 | N14 | 446 |
| I/O | 3 | - | - | T15 | 449 |
| I/O | 3 | P66 | P109 | M13 | 452 |
| I/O | 3 | - | - | R16 | 455 |
| I/O | 3 | - | P110 | M14 | 458 |
| GND | - | - | - | GND* | - |
| I/O, $V_{REF}$ | 3 | P65 | P111 | L14 | 461 |
| I/O | 3 | - | P112 | M15 | 464 |
| I/O | 3 | - | - | L12 | 467 |
| I/O | 3 | P64 | P113 | P16 | 470 |
| I/O | 3 | P63 | P114 | L13 | 473 |
| I/O (D6) | 3 | P62 | P115 | N16 | 476 |
| GND | - | P61 | P116 | GND* | - |
| $V_{CCO}$ | 3 | - | P117 | $V_{CCO}$ Bank 3* | - |
| $V_{CCINT}$ | - | - | P118 | $V_{CCINT}$* | - |
| I/O (D5) | 3 | P60 | P119 | M16 | 479 |
| I/O | 3 | P59 | P120 | K14 | 482 |
| I/O | 3 | - | - | L16 | 485 |
| I/O | 3 | - | P121 | K13 | 488 |
| I/O | 3 | - | P122 | L15 | 491 |
| I/O | 3 | - | P123 | K12 | 494 |
| GND | - | - | P124 | GND* | - |
| I/O, $V_{REF}$ | 3 | P58 | P125 | K16 | 497 |
| I/O (D4) | 3 | P57 | P126 | J16 | 500 |

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## XC2S50 Device Pinouts *(Continued)*

| XC2S50 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | Bndry Scan |
| I/O | 3 | - | - | J14 | 503 |
| I/O | 3 | P56 | P127 | K15 | 506 |
| $V_{CCINT}$ | - | P55 | P128 | $V_{CCINT}$* | - |
| I/O, TRDY(1) | 3 | P54 | P129 | J15 | 512 |
| $V_{CCO}$ | 3 | P53 | P130 | $V_{CCO}$ Bank 3* | - |
| $V_{CCO}$ | 2 | P53 | P130 | $V_{CCO}$ Bank 2* | - |
| GND | - | P52 | P131 | GND* | - |
| I/O, IRDY(1) | 2 | P51 | P132 | H16 | 515 |
| I/O | 2 | - | P133 | H14 | 518 |
| I/O | 2 | P50 | P134 | H15 | 521 |
| I/O | 2 | - | - | J13 | 524 |
| I/O (D3) | 2 | P49 | P135 | G16 | 527 |
| I/O, $V_{REF}$ | 2 | P48 | P136 | H13 | 530 |
| GND | - | - | P137 | GND* | - |
| I/O | 2 | - | P138 | G14 | 533 |
| I/O | 2 | - | P139 | G15 | 536 |
| I/O | 2 | - | P140 | G12 | 539 |
| I/O | 2 | - | - | F16 | 542 |
| I/O | 2 | P47 | P141 | G13 | 545 |
| I/O (D2) | 2 | P46 | P142 | F15 | 548 |
| $V_{CCINT}$ | - | - | P143 | $V_{CCINT}$* | - |
| $V_{CCO}$ | 2 | - | P144 | $V_{CCO}$ Bank 2* | - |
| GND | - | P45 | P145 | GND* | - |
| I/O (D1) | 2 | P44 | P146 | E16 | 551 |
| I/O | 2 | P43 | P147 | F14 | 554 |
| I/O | 2 | P42 | P148 | D16 | 557 |
| I/O | 2 | - | - | F12 | 560 |
| I/O | 2 | - | P149 | E15 | 563 |
| I/O, $V_{REF}$ | 2 | P41 | P150 | F13 | 566 |
| GND | - | - | - | GND* | - |
| I/O | 2 | - | P151 | E14 | 569 |
| I/O | 2 | - | - | C16 | 572 |
| I/O | 2 | P40 | P152 | E13 | 575 |
| I/O | 2 | - | - | B16 | 578 |
| I/O (DIN, D0) | 2 | P39 | P153 | D14 | 581 |
| I/O (DOUT, BUSY) | 2 | P38 | P154 | C15 | 584 |
| CCLK | 2 | P37 | P155 | D15 | 587 |
| $V_{CCO}$ | 2 | P36 | P156 | $V_{CCO}$ Bank 2* | - |

## XC2S50 Device Pinouts *(Continued)*

| XC2S50 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | Bndry Scan |
| $V_{CCO}$ | 1 | P35 | P156 | $V_{CCO}$ Bank 1* | - |
| TDO | 2 | P34 | P157 | B14 | - |
| GND | - | P33 | P158 | GND* | - |
| TDI | - | P32 | P159 | A15 | - |
| I/O ($\overline{CS}$) | 1 | P31 | P160 | B13 | 0 |
| I/O ($\overline{WRITE}$) | 1 | P30 | P161 | C13 | 3 |
| I/O | 1 | - | - | C12 | 6 |
| I/O | 1 | P29 | P162 | A14 | 9 |
| I/O | 1 | - | - | D12 | 12 |
| I/O | 1 | - | P163 | B12 | 15 |
| GND | - | - | - | GND* | - |
| I/O, $V_{REF}$ | 1 | P28 | P164 | C11 | 18 |
| I/O | 1 | - | P165 | A13 | 21 |
| I/O | 1 | - | - | D11 | 24 |
| I/O | 1 | - | P166 | A12 | 27 |
| I/O | 1 | P27 | P167 | E11 | 30 |
| I/O | 1 | P26 | P168 | B11 | 33 |
| GND | - | P25 | P169 | GND* | - |
| $V_{CCO}$ | 1 | - | P170 | $V_{CCO}$ Bank 1* | - |
| $V_{CCINT}$ | - | P24 | P171 | $V_{CCINT}$* | - |
| I/O | 1 | P23 | P172 | A11 | 36 |
| I/O | 1 | P22 | P173 | C10 | 39 |
| I/O | 1 | - | P174 | B10 | 45 |
| I/O | 1 | - | P175 | D10 | 48 |
| I/O | 1 | - | P176 | A10 | 51 |
| GND | - | - | P177 | GND* | - |
| I/O, $V_{REF}$ | 1 | P21 | P178 | B9 | 54 |
| I/O | 1 | - | P179 | E10 | 57 |
| I/O | 1 | - | - | A9 | 60 |
| I/O | 1 | P20 | P180 | D9 | 63 |
| I/O | 1 | P19 | P181 | A8 | 66 |
| I, GCK2 | 1 | P18 | P182 | C9 | 72 |
| GND | - | P17 | P183 | GND* | - |
| $V_{CCO}$ | 1 | P16 | P184 | $V_{CCO}$ Bank 1* | - |
| $V_{CCO}$ | 0 | P16 | P184 | $V_{CCO}$ Bank 0* | - |
| I, GCK3 | 0 | P15 | P185 | B8 | 73 |
| $V_{CCINT}$ | - | P14 | P186 | $V_{CCINT}$* | - |
| I/O | 0 | P13 | P187 | A7 | 80 |

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## XC2S50 Device Pinouts *(Continued)*

| XC2S50 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | Bndry Scan |
| I/O | 0 | - | - | D8 | 83 |
| I/O | 0 | - | P188 | A6 | 86 |
| I/O, $V_{REF}$ | 0 | P12 | P189 | B7 | 89 |
| GND | - | - | P190 | GND* | - |
| I/O | 0 | - | P191 | C8 | 92 |
| I/O | 0 | - | P192 | D7 | 95 |
| I/O | 0 | - | P193 | E7 | 98 |
| I/O | 0 | P11 | P194 | C7 | 104 |
| I/O | 0 | P10 | P195 | B6 | 107 |
| $V_{CCINT}$ | - | P9 | P196 | $V_{CCINT}$* | - |
| $V_{CCO}$ | 0 | - | P197 | $V_{CCO}$ Bank 0* | - |
| GND | - | P8 | P198 | GND* | - |
| I/O | 0 | P7 | P199 | A5 | 110 |
| I/O | 0 | P6 | P200 | C6 | 113 |
| I/O | 0 | - | P201 | B5 | 116 |
| I/O | 0 | - | - | D6 | 119 |
| I/O | 0 | - | P202 | A4 | 122 |
| I/O, $V_{REF}$ | 0 | P5 | P203 | B4 | 125 |
| GND | - | - | - | GND* | - |
| I/O | 0 | - | P204 | E6 | 128 |
| I/O | 0 | - | - | D5 | 131 |
| I/O | 0 | P4 | P205 | A3 | 134 |
| I/O | 0 | - | - | C5 | 137 |
| I/O | 0 | P3 | P206 | B3 | 140 |
| TCK | - | P2 | P207 | C4 | - |
| $V_{CCO}$ | 0 | P1 | P208 | $V_{CCO}$ Bank 0* | - |
| $V_{CCO}$ | 7 | P144 | P208 | $V_{CCO}$ Bank 7* | - |

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**Notes:**

1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. Pads labelled GND*, $V_{CCINT}$*, $V_{CCO}$ Bank 0*, $V_{CCO}$ Bank 1*, $V_{CCO}$ Bank 2*, $V_{CCO}$ Bank 3*, $V_{CCO}$ Bank 4*, $V_{CCO}$ Bank 5*, $V_{CCO}$ Bank 6*, $V_{CCO}$ Bank 7* are internally bonded to independent ground or power planes within the package.
3. See "VCCO Banks" for details on $V_{CCO}$ banking.

## Additional XC2S50 Package Pins

**TQ144**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P104 | P105 | - | - | - | - |

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## Additional XC2S50 Package Pins *(Continued)*

**PQ208**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P55 | P56 | - | - | - | - |

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**FG256**

| $V_{CCINT}$ Pins | | | | | |
|---|---|---|---|---|---|
| C3 | C14 | D4 | D13 | E5 | E12 |
| M5 | M12 | N4 | N13 | P3 | P14 |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |
| E8 | F8 | - | - | - | - |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| E9 | F9 | - | - | - | - |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| H11 | H12 | - | - | - | - |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| J11 | J12 | - | - | - | - |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| L9 | M9 | - | - | - | - |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| L8 | M8 | - | - | - | - |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| J5 | J6 | - | - | - | - |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |
| H5 | H6 | - | - | - | - |
| **GND Pins** | | | | | |
| A1 | A16 | B2 | B15 | F6 | F7 |
| F10 | F11 | G6 | G7 | G8 | G9 |
| G10 | G11 | H7 | H8 | H9 | H10 |
| J7 | J8 | J9 | J10 | K6 | K7 |
| K8 | K9 | K10 | K11 | L6 | L7 |
| L10 | L11 | R2 | R15 | T1 | T16 |
| **Not Connected Pins** | | | | | |
| P4 | R4 | - | - | - | - |

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## XC2S100 Device Pinouts

| XC2S100 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | FG456 | Bndry Scan |
| GND | - | P143 | P1 | GND* | GND* | - |
| TMS | - | P142 | P2 | D3 | D3 | - |
| I/O | 7 | P141 | P3 | C2 | B1 | 185 |
| I/O | 7 | - | - | A2 | F5 | 191 |
| I/O | 7 | P140 | P4 | B1 | D2 | 194 |
| I/O | 7 | - | - | - | E3 | 197 |
| I/O | 7 | - | - | E3 | G5 | 200 |
| I/O | 7 | - | P5 | D2 | F3 | 203 |
| GND | - | - | - | GND* | GND* | - |
| $V_{CCO}$ | 7 | - | - | $V_{CCO}$ Bank 7* | $V_{CCO}$ Bank 7* | - |
| I/O, $V_{REF}$ | 7 | P139 | P6 | C1 | E2 | 206 |

## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | FG456 | Bndry Scan |
| I/O | 7 | - | P7 | F3 | E1 | 209 |
| I/O | 7 | - | - | E2 | H5 | 215 |
| I/O | 7 | P138 | P8 | E4 | F2 | 218 |
| I/O | 7 | - | - | - | F1 | 221 |
| I/O, $V_{REF}$ | 7 | P137 | P9 | D1 | H4 | 224 |
| I/O | 7 | P136 | P10 | E1 | G1 | 227 |
| GND | - | P135 | P11 | GND* | GND* | - |
| $V_{CCO}$ | 7 | - | P12 | $V_{CCO}$ Bank 7* | $V_{CCO}$ Bank 7* | - |
| $V_{CCINT}$ | - | - | P13 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 7 | P134 | P14 | F2 | H3 | 230 |
| I/O | 7 | P133 | P15 | G3 | H2 | 233 |
| I/O | 7 | - | - | F1 | J5 | 236 |
| I/O | 7 | - | P16 | F4 | J2 | 239 |
| I/O | 7 | - | P17 | F5 | K5 | 245 |
| I/O | 7 | - | P18 | G2 | K1 | 248 |
| GND | - | - | P19 | GND* | GND* | - |
| I/O, $V_{REF}$ | 7 | P132 | P20 | H3 | K3 | 251 |
| I/O | 7 | P131 | P21 | G4 | K4 | 254 |
| I/O | 7 | - | - | H2 | L6 | 257 |
| I/O | 7 | P130 | P22 | G5 | L1 | 260 |
| I/O | 7 | - | P23 | H4 | L4 | 266 |
| I/O, IRDY(1) | 7 | P129 | P24 | G1 | L3 | 269 |
| GND | - | P128 | P25 | GND* | GND* | - |
| $V_{CCO}$ | 7 | P127 | P26 | $V_{CCO}$ Bank 7* | $V_{CCO}$ Bank 7* | - |
| $V_{CCO}$ | 6 | P127 | P26 | $V_{CCO}$ Bank 6* | $V_{CCO}$ Bank 6* | - |
| I/O, TRDY(1) | 6 | P126 | P27 | J2 | M1 | 272 |
| $V_{CCINT}$ | - | P125 | P28 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 6 | P124 | P29 | H1 | M3 | 281 |
| I/O | 6 | - | - | J4 | M4 | 284 |
| I/O | 6 | P123 | P30 | J1 | M5 | 287 |
| I/O, $V_{REF}$ | 6 | P122 | P31 | J3 | N2 | 290 |
| GND | - | - | P32 | GND* | GND* | - |
| I/O | 6 | - | P33 | K5 | N3 | 293 |
| I/O | 6 | - | P34 | K2 | N4 | 296 |
| I/O | 6 | - | P35 | K1 | P2 | 302 |
| I/O | 6 | - | - | K3 | P4 | 305 |
| I/O | 6 | P121 | P36 | L1 | P3 | 308 |
| I/O | 6 | P120 | P37 | L2 | R2 | 311 |

## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | TQ144 | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|---|
| Function | Bank | | | | | |
| $V_{CCINT}$ | - | - | P38 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 6 | - | P39 | $V_{CCO}$ Bank 6* | $V_{CCO}$ Bank 6* | - |
| GND | - | P119 | P40 | GND* | GND* | - |
| I/O | 6 | P118 | P41 | K4 | T1 | 314 |
| I/O, $V_{REF}$ | 6 | P117 | P42 | M1 | R4 | 317 |
| I/O | 6 | - | - | - | T2 | 320 |
| I/O | 6 | P116 | P43 | L4 | U1 | 323 |
| I/O | 6 | - | - | M2 | R5 | 326 |
| I/O | 6 | - | P44 | L3 | U2 | 332 |
| I/O, $V_{REF}$ | 6 | P115 | P45 | N1 | T3 | 335 |
| $V_{CCO}$ | 6 | - | - | $V_{CCO}$ Bank 6* | $V_{CCO}$ Bank 6* | - |
| GND | - | - | - | GND* | GND* | - |
| I/O | 6 | - | P46 | P1 | T4 | 338 |
| I/O | 6 | - | - | L5 | W1 | 341 |
| I/O | 6 | - | - | - | U4 | 344 |
| I/O | 6 | P114 | P47 | N2 | Y1 | 347 |
| I/O | 6 | - | - | M4 | W2 | 350 |
| I/O | 6 | P113 | P48 | R1 | Y2 | 356 |
| I/O | 6 | P112 | P49 | M3 | W3 | 359 |
| M1 | - | P111 | P50 | P2 | U5 | 362 |
| GND | - | P110 | P51 | GND* | GND* | - |
| M0 | - | P109 | P52 | N3 | AB2 | 363 |
| $V_{CCO}$ | 6 | P108 | P53 | $V_{CCO}$ Bank 6* | $V_{CCO}$ Bank 6* | - |
| $V_{CCO}$ | 5 | P107 | P53 | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| M2 | - | P106 | P54 | R3 | Y4 | 364 |
| I/O | 5 | - | - | N5 | V7 | 374 |
| I/O | 5 | P103 | P57 | T2 | Y6 | 377 |
| I/O | 5 | - | - | - | AA4 | 380 |
| I/O | 5 | - | - | P5 | W6 | 383 |
| I/O | 5 | - | P58 | T3 | Y7 | 386 |
| GND | - | - | - | GND* | GND* | - |
| $V_{CCO}$ | 5 | - | - | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| I/O, $V_{REF}$ | 5 | P102 | P59 | T4 | AA5 | 389 |
| I/O | 5 | - | P60 | M6 | AB5 | 392 |
| I/O | 5 | - | - | T5 | AB6 | 398 |
| I/O | 5 | P101 | P61 | N6 | AA7 | 401 |
| I/O | 5 | - | - | - | W7 | 404 |

## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | TQ144 | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|---|
| Function | Bank | | | | | |
| I/O, $V_{REF}$ | 5 | P100 | P62 | R5 | W8 | 407 |
| I/O | 5 | P99 | P63 | P6 | Y8 | 410 |
| GND | - | P98 | P64 | GND* | GND* | - |
| $V_{CCO}$ | 5 | - | P65 | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| $V_{CCINT}$ | - | P97 | P66 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 5 | P96 | P67 | R6 | AA8 | 413 |
| I/O | 5 | P95 | P68 | M7 | V9 | 416 |
| I/O | 5 | - | - | - | AB9 | 419 |
| I/O | 5 | - | P69 | N7 | Y9 | 422 |
| I/O | 5 | - | P70 | T6 | W10 | 428 |
| I/O | 5 | - | P71 | P7 | AB10 | 431 |
| GND | - | - | P72 | GND* | GND* | - |
| I/O, $V_{REF}$ | 5 | P94 | P73 | P8 | Y10 | 434 |
| I/O | 5 | - | P74 | R7 | V11 | 437 |
| I/O | 5 | - | - | T7 | W11 | 440 |
| I/O | 5 | P93 | P75 | T8 | AB11 | 443 |
| $V_{CCINT}$ | - | P92 | P76 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I, GCK1 | 5 | P91 | P77 | R8 | Y11 | 455 |
| $V_{CCO}$ | 5 | P90 | P78 | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| $V_{CCO}$ | 4 | P90 | P78 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | P89 | P79 | GND* | GND* | - |
| I, GCK0 | 4 | P88 | P80 | N8 | W12 | 456 |
| I/O | 4 | P87 | P81 | N9 | U12 | 460 |
| I/O | 4 | P86 | P82 | R9 | Y12 | 466 |
| I/O | 4 | - | - | N10 | AA12 | 469 |
| I/O | 4 | - | P83 | T9 | AB13 | 472 |
| I/O, $V_{REF}$ | 4 | P85 | P84 | P9 | AA13 | 475 |
| GND | - | - | P85 | GND* | GND* | - |
| I/O | 4 | - | P86 | M10 | Y13 | 478 |
| I/O | 4 | - | P87 | R10 | V13 | 481 |
| I/O | 4 | - | P88 | P10 | AA14 | 487 |
| I/O | 4 | - | - | - | V14 | 490 |
| I/O | 4 | P84 | P89 | T10 | AB15 | 493 |
| I/O | 4 | P83 | P90 | R11 | AA15 | 496 |
| $V_{CCINT}$ | - | P82 | P91 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 4 | - | P92 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | P81 | P93 | GND* | GND* | - |
| I/O | 4 | P80 | P94 | M11 | Y15 | 499 |

## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | TQ144 | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|---|
| Function | Bank | | | | | |
| I/O, $V_{REF}$ | 4 | P79 | P95 | T11 | AB16 | 502 |
| I/O | 4 | - | - | - | AB17 | 505 |
| I/O | 4 | P78 | P96 | N11 | V15 | 508 |
| I/O | 4 | - | - | R12 | Y16 | 511 |
| I/O | 4 | - | P97 | P11 | AB18 | 517 |
| I/O, $V_{REF}$ | 4 | P77 | P98 | T12 | AB19 | 520 |
| $V_{CCO}$ | 4 | - | - | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | - | - | GND* | GND* | - |
| I/O | 4 | - | P99 | T13 | Y17 | 523 |
| I/O | 4 | - | - | N12 | V16 | 526 |
| I/O | 4 | - | - | - | W17 | 529 |
| I/O | 4 | P76 | P100 | R13 | AB20 | 532 |
| I/O | 4 | - | - | P12 | AA19 | 535 |
| I/O | 4 | P75 | P101 | P13 | AA20 | 541 |
| I/O | 4 | P74 | P102 | T14 | W18 | 544 |
| GND | - | P73 | P103 | GND* | GND* | - |
| DONE | 3 | P72 | P104 | R14 | Y19 | 547 |
| $V_{CCO}$ | 4 | P71 | P105 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| $V_{CCO}$ | 3 | P70 | P105 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $\overline{PROGRAM}$ | - | P69 | P106 | P15 | W20 | 550 |
| I/O ($\overline{INIT}$) | 3 | P68 | P107 | N15 | V19 | 551 |
| I/O (D7) | 3 | P67 | P108 | N14 | Y21 | 554 |
| I/O | 3 | - | - | T15 | W21 | 560 |
| I/O | 3 | P66 | P109 | M13 | U20 | 563 |
| I/O | 3 | - | - | - | U19 | 566 |
| I/O | 3 | - | - | R16 | T18 | 569 |
| I/O | 3 | - | P110 | M14 | W22 | 572 |
| GND | - | - | - | GND* | GND* | - |
| $V_{CCO}$ | 3 | - | - | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| I/O, $V_{REF}$ | 3 | P65 | P111 | L14 | U21 | 575 |
| I/O | 3 | - | P112 | M15 | T20 | 578 |
| I/O | 3 | - | - | L12 | T21 | 584 |
| I/O | 3 | P64 | P113 | P16 | R18 | 587 |
| I/O | 3 | - | - | - | U22 | 590 |
| I/O, $V_{REF}$ | 3 | P63 | P114 | L13 | R19 | 593 |
| I/O (D6) | 3 | P62 | P115 | N16 | T22 | 596 |
| GND | - | P61 | P116 | GND* | GND* | - |

## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | TQ144 | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|---|
| Function | Bank | | | | | |
| $V_{CCO}$ | 3 | - | P117 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $V_{CCINT}$ | - | - | P118 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O (D5) | 3 | P60 | P119 | M16 | R21 | 599 |
| I/O | 3 | P59 | P120 | K14 | P18 | 602 |
| I/O | 3 | - | - | L16 | P20 | 605 |
| I/O | 3 | - | P121 | K13 | P21 | 608 |
| I/O | 3 | - | P122 | L15 | N18 | 614 |
| I/O | 3 | - | P123 | K12 | N20 | 617 |
| GND | - | - | P124 | GND* | GND* | - |
| I/O, $V_{REF}$ | 3 | P58 | P125 | K16 | N21 | 620 |
| I/O (D4) | 3 | P57 | P126 | J16 | N22 | 623 |
| I/O | 3 | - | - | J14 | M19 | 626 |
| I/O | 3 | P56 | P127 | K15 | M20 | 629 |
| $V_{CCINT}$ | - | P55 | P128 | E5 | $V_{CCINT}$* | - |
| I/O, TRDY(1) | 3 | P54 | P129 | J15 | M22 | 638 |
| $V_{CCO}$ | 3 | P53 | P130 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $V_{CCO}$ | 2 | P53 | P130 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P52 | P131 | GND* | GND* | - |
| I/O, IRDY(1) | 2 | P51 | P132 | H16 | L20 | 641 |
| I/O | 2 | - | P133 | H14 | L17 | 644 |
| I/O | 2 | P50 | P134 | H15 | L21 | 650 |
| I/O | 2 | - | - | J13 | L22 | 653 |
| I/O (D3) | 2 | P49 | P135 | G16 | K20 | 656 |
| I/O, $V_{REF}$ | 2 | P48 | P136 | H13 | K21 | 659 |
| GND | - | - | P137 | GND* | GND* | - |
| I/O | 2 | - | P138 | G14 | K22 | 662 |
| I/O | 2 | - | P139 | G15 | J21 | 665 |
| I/O | 2 | - | P140 | G12 | J18 | 671 |
| I/O | 2 | - | - | F16 | J22 | 674 |
| I/O | 2 | P47 | P141 | G13 | H19 | 677 |
| I/O (D2) | 2 | P46 | P142 | F15 | H20 | 680 |
| $V_{CCINT}$ | - | - | P143 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 2 | - | P144 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P45 | P145 | GND* | GND* | - |
| I/O (D1) | 2 | P44 | P146 | E16 | H22 | 683 |
| I/O, $V_{REF}$ | 2 | P43 | P147 | F14 | H18 | 686 |
| I/O | 2 | - | - | - | G21 | 689 |
| I/O | 2 | P42 | P148 | D16 | G18 | 692 |

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## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | TQ144 | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|---|
| Function | Bank | | | | | |
| I/O | 2 | - | - | F12 | G20 | 695 |
| I/O | 2 | - | P149 | E15 | F19 | 701 |
| I/O, $V_{REF}$ | 2 | P41 | P150 | F13 | F21 | 704 |
| $V_{CCO}$ | 2 | - | - | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | - | - | GND* | GND* | - |
| I/O | 2 | - | P151 | E14 | F20 | 707 |
| I/O | 2 | - | - | C16 | F18 | 710 |
| I/O | 2 | - | - | - | E21 | 713 |
| I/O | 2 | P40 | P152 | E13 | D22 | 716 |
| I/O | 2 | - | - | B16 | E20 | 719 |
| I/O (DIN, D0) | 2 | P39 | P153 | D14 | D20 | 725 |
| I/O (DOUT, BUSY) | 2 | P38 | P154 | C15 | C21 | 728 |
| CCLK | 2 | P37 | P155 | D15 | B22 | 731 |
| $V_{CCO}$ | 2 | P36 | P156 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| $V_{CCO}$ | 1 | P35 | P156 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| TDO | 2 | P34 | P157 | B14 | A21 | - |
| GND | - | P33 | P158 | GND* | GND* | - |
| TDI | - | P32 | P159 | A15 | B20 | - |
| I/O ($\overline{CS}$) | 1 | P31 | P160 | B13 | C19 | 0 |
| I/O ($\overline{WRITE}$) | 1 | P30 | P161 | C13 | A20 | 3 |
| I/O | 1 | - | - | C12 | D17 | 9 |
| I/O | 1 | P29 | P162 | A14 | A19 | 12 |
| I/O | 1 | - | - | - | B18 | 15 |
| I/O | 1 | - | - | D12 | C17 | 18 |
| I/O | 1 | - | P163 | B12 | D16 | 21 |
| GND | - | - | - | GND* | GND* | - |
| $V_{CCO}$ | 1 | - | - | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| I/O, $V_{REF}$ | 1 | P28 | P164 | C11 | A18 | 24 |
| I/O | 1 | - | P165 | A13 | B17 | 27 |
| I/O | 1 | - | - | D11 | D15 | 33 |
| I/O | 1 | - | P166 | A12 | C16 | 36 |
| I/O | 1 | - | - | - | D14 | 39 |
| I/O, $V_{REF}$ | 1 | P27 | P167 | E11 | E14 | 42 |
| I/O | 1 | P26 | P168 | B11 | A16 | 45 |
| GND | - | P25 | P169 | GND* | GND* | - |

## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | TQ144 | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|---|
| Function | Bank | | | | | |
| $V_{CCO}$ | 1 | - | P170 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| $V_{CCINT}$ | - | P24 | P171 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 1 | P23 | P172 | A11 | C15 | 48 |
| I/O | 1 | P22 | P173 | C10 | B15 | 51 |
| I/O | 1 | - | - | - | F12 | 54 |
| I/O | 1 | - | P174 | B10 | C14 | 57 |
| I/O | 1 | - | P175 | D10 | D13 | 63 |
| I/O | 1 | - | P176 | A10 | C13 | 66 |
| GND | - | - | P177 | GND* | GND* | - |
| I/O, $V_{REF}$ | 1 | P21 | P178 | B9 | B13 | 69 |
| I/O | 1 | - | P179 | E10 | E12 | 72 |
| I/O | 1 | - | - | A9 | B12 | 75 |
| I/O | 1 | P20 | P180 | D9 | D12 | 78 |
| I/O | 1 | P19 | P181 | A8 | D11 | 84 |
| I, GCK2 | 1 | P18 | P182 | C9 | A11 | 90 |
| GND | - | P17 | P183 | GND* | GND* | - |
| $V_{CCO}$ | 1 | P16 | P184 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| $V_{CCO}$ | 0 | P16 | P184 | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| I, GCK3 | 0 | P15 | P185 | B8 | C11 | 91 |
| $V_{CCINT}$ | - | P14 | P186 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 0 | P13 | P187 | A7 | A10 | 101 |
| I/O | 0 | - | - | D8 | B10 | 104 |

## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | FG456 | Bndry Scan |
| I/O | 0 | - | P188 | A6 | C10 | 107 |
| I/O, $V_{REF}$ | 0 | P12 | P189 | B7 | A9 | 110 |
| GND | - | - | P190 | GND* | GND* | - |
| I/O | 0 | - | P191 | C8 | B9 | 113 |
| I/O | 0 | - | P192 | D7 | E10 | 116 |
| I/O | 0 | - | P193 | E7 | A8 | 122 |
| I/O | 0 | - | - | - | D9 | 125 |
| I/O | 0 | P11 | P194 | C7 | E9 | 128 |
| I/O | 0 | P10 | P195 | B6 | A7 | 131 |
| $V_{CCINT}$ | - | P9 | P196 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 0 | - | P197 | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| GND | - | P8 | P198 | GND* | GND* | - |
| I/O | 0 | P7 | P199 | A5 | B7 | 134 |
| I/O, $V_{REF}$ | 0 | P6 | P200 | C6 | E8 | 137 |
| I/O | 0 | - | - | - | D8 | 140 |
| I/O | 0 | - | P201 | B5 | C7 | 143 |
| I/O | 0 | - | - | D6 | D7 | 146 |
| I/O | 0 | - | P202 | A4 | D6 | 152 |
| I/O, $V_{REF}$ | 0 | P5 | P203 | B4 | C6 | 155 |
| $V_{CCO}$ | 0 | - | - | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| GND | - | - | - | GND* | GND* | - |
| I/O | 0 | - | P204 | E6 | B5 | 158 |
| I/O | 0 | - | - | D5 | E7 | 161 |
| I/O | 0 | - | - | - | E6 | 164 |
| I/O | 0 | P4 | P205 | A3 | B4 | 167 |
| I/O | 0 | - | - | C5 | A3 | 170 |
| I/O | 0 | P3 | P206 | B3 | C5 | 176 |
| TCK | - | P2 | P207 | C4 | C4 | - |
| $V_{CCO}$ | 0 | P1 | P208 | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| $V_{CCO}$ | 7 | P144 | P208 | $V_{CCO}$ Bank 7* | $V_{CCO}$ Bank 7* | - |

04/18/01

**Notes:**

1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. Pads labelled GND*, $V_{CCINT}$*, $V_{CCO}$ Bank 0*, $V_{CCO}$ Bank 1*, $V_{CCO}$ Bank 2*, $V_{CCO}$ Bank 3*, $V_{CCO}$ Bank 4*, $V_{CCO}$ Bank 5*, $V_{CCO}$ Bank 6*, $V_{CCO}$ Bank 7* are internally bonded to independent ground or power planes within the package.
3. See "VCCO Banks" for details on $V_{CCO}$ banking.

XC2S200-5FG256I AMD IC FPGA 176 I/O 256FBGA



## Additional XC2S100 Package Pins

**TQ144**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P104 | P105 | - | - | - | - |

11/02/00

**PQ208**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P55 | P56 | - | - | - | - |

11/02/00

**FG256**

| $V_{CCINT}$ Pins | | | | | |
|---|---|---|---|---|---|
| C3 | C14 | D4 | D13 | E5 | E12 |
| M5 | M12 | N4 | N13 | P3 | P14 |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |
| E8 | F8 | - | - | - | - |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| E9 | F9 | - | - | - | - |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| H11 | H12 | - | - | - | - |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| J11 | J12 | - | - | - | - |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| L9 | M9 | - | - | - | - |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| L8 | M8 | - | - | - | - |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| J5 | J6 | - | - | - | - |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |
| H5 | H6 | - | - | - | - |
| **GND Pins** | | | | | |
| A1 | A16 | B2 | B15 | F6 | F7 |
| F10 | F11 | G6 | G7 | G8 | G9 |
| G10 | G11 | H7 | H8 | H9 | H10 |
| J7 | J8 | J9 | J10 | K6 | K7 |
| K8 | K9 | K10 | K11 | L6 | L7 |
| L10 | L11 | R2 | R15 | T1 | T16 |
| **Not Connected Pins** | | | | | |
| P4 | R4 | - | - | - | - |

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**FG456**

| $V_{CCINT}$ Pins | | | | | |
|---|---|---|---|---|---|
| E5 | E18 | F6 | F17 | G7 | G8 |
| G9 | G14 | G15 | G16 | H7 | H16 |
| J7 | J16 | P7 | P16 | R7 | R16 |
| T7 | T8 | T9 | T14 | T15 | T16 |
| U6 | U17 | V5 | V18 | - | - |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |

## Additional XC2S100 Package Pins *(Continued)*

| | | | | | |
|---|---|---|---|---|---|
| F10 | F7 | F8 | F9 | G10 | G11 |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| F13 | F14 | F15 | F16 | G12 | G13 |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| G17 | H17 | J17 | K16 | K17 | L16 |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| M16 | N16 | N17 | P17 | R17 | T17 |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| T12 | T13 | U13 | U14 | U15 | U16 |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| T10 | T11 | U10 | U7 | U8 | U9 |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| M7 | N6 | N7 | P6 | R6 | T6 |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |
| G6 | H6 | J6 | K6 | K7 | L7 |
| **GND Pins** | | | | | |
| A1 | A22 | B2 | B21 | C3 | C20 |
| J9 | J10 | J11 | J12 | J13 | J14 |
| K9 | K10 | K11 | K12 | K13 | K14 |
| L9 | L10 | L11 | L12 | L13 | L14 |
| M9 | M10 | M11 | M12 | M13 | M14 |
| N9 | N10 | N11 | N12 | N13 | N14 |
| P9 | P10 | P11 | P12 | P13 | P14 |
| Y3 | Y20 | AA2 | AA21 | AB1 | AB22 |
| **Not Connected Pins** | | | | | |
| A2 | A4 | A5 | A6 | A12 | A13 |
| A14 | A15 | A17 | B3 | B6 | B8 |
| B11 | B14 | B16 | B19 | C1 | C2 |
| C8 | C9 | C12 | C18 | C22 | D1 |
| D4 | D5 | D10 | D18 | D19 | D21 |
| E4 | E11 | E13 | E15 | E16 | E17 |
| E19 | E22 | F4 | F11 | F22 | G2 |
| G3 | G4 | G19 | G22 | H1 | H21 |
| J1 | J3 | J4 | J19 | J20 | K2 |
| K18 | K19 | L2 | L5 | L18 | L19 |
| M2 | M6 | M17 | M18 | M21 | N1 |
| N5 | N19 | P1 | P5 | P19 | P22 |
| R1 | R3 | R20 | R22 | T5 | T19 |
| U3 | U11 | U18 | V1 | V2 | V10 |
| V12 | V17 | V3 | V4 | V6 | V8 |
| V20 | V21 | V22 | W4 | W5 | W9 |
| W13 | W14 | W15 | W16 | W19 | Y5 |
| Y14 | Y18 | Y22 | AA1 | AA3 | AA6 |
| AA9 | AA10 | AA11 | AA16 | AA17 | AA18 |
| AA22 | AB3 | AB4 | AB7 | AB8 | AB12 |
| AB14 | AB21 | - | - | - | - |

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## XC2S150 Device Pinouts

| XC2S150 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| GND | - | P1 | GND* | GND* | - |
| TMS | - | P2 | D3 | D3 | - |
| I/O | 7 | P3 | C2 | B1 | 221 |
| I/O | 7 | - | - | E4 | 224 |
| I/O | 7 | - | - | C1 | 227 |
| I/O | 7 | - | A2 | F5 | 230 |
| GND | - | - | GND* | GND* | - |
| I/O | 7 | P4 | B1 | D2 | 233 |
| I/O | 7 | - | - | E3 | 236 |
| I/O | 7 | - | - | F4 | 239 |
| I/O | 7 | - | E3 | G5 | 242 |
| I/O | 7 | P5 | D2 | F3 | 245 |
| GND | - | - | GND* | GND* | - |
| $V_{CCO}$ | 7 | - | $V_{CCO}$ Bank 7* | $V_{CCO}$ Bank 7* | - |
| I/O, $V_{REF}$ | 7 | P6 | C1 | E2 | 248 |
| I/O | 7 | P7 | F3 | E1 | 251 |
| I/O | 7 | - | - | G4 | 254 |
| I/O | 7 | - | - | G3 | 257 |
| I/O | 7 | - | E2 | H5 | 260 |
| I/O | 7 | P8 | E4 | F2 | 263 |
| I/O | 7 | - | - | F1 | 266 |
| I/O, $V_{REF}$ | 7 | P9 | D1 | H4 | 269 |
| I/O | 7 | P10 | E1 | G1 | 272 |
| GND | - | P11 | GND* | GND* | - |
| $V_{CCO}$ | 7 | P12 | $V_{CCO}$ Bank 7* | $V_{CCO}$ Bank 7* | - |
| $V_{CCINT}$ | - | P13 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 7 | P14 | F2 | H3 | 275 |
| I/O | 7 | P15 | G3 | H2 | 278 |
| I/O | 7 | - | - | H1 | 284 |
| I/O | 7 | - | F1 | J5 | 287 |
| I/O | 7 | P16 | F4 | J2 | 290 |
| I/O | 7 | - | - | J3 | 293 |
| I/O | 7 | P17 | F5 | K5 | 299 |
| I/O | 7 | P18 | G2 | K1 | 302 |
| GND | - | P19 | GND* | GND* | - |
| $V_{CCO}$ | 7 | - | $V_{CCO}$ Bank 7* | $V_{CCO}$ Bank 7* | - |
| I/O, $V_{REF}$ | 7 | P20 | H3 | K3 | 305 |
| I/O | 7 | P21 | G4 | K4 | 308 |
| I/O | 7 | - | H2 | L6 | 311 |

## XC2S150 Device Pinouts *(Continued)*

| XC2S150 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| I/O | 7 | P22 | G5 | L1 | 314 |
| I/O | 7 | - | - | L5 | 317 |
| I/O | 7 | P23 | H4 | L4 | 320 |
| I/O, IRDY(1) | 7 | P24 | G1 | L3 | 323 |
| GND | - | P25 | GND* | GND* | - |
| $V_{CCO}$ | 7 | P26 | $V_{CCO}$ Bank 7* | $V_{CCO}$ Bank 7* | - |
| $V_{CCO}$ | 6 | P26 | $V_{CCO}$ Bank 6* | $V_{CCO}$ Bank 6* | - |
| I/O, TRDY(1) | 6 | P27 | J2 | M1 | 326 |
| $V_{CCINT}$ | - | P28 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 6 | - | - | M6 | 332 |
| I/O | 6 | P29 | H1 | M3 | 335 |
| I/O | 6 | - | J4 | M4 | 338 |
| I/O | 6 | P30 | J1 | M5 | 341 |
| I/O, $V_{REF}$ | 6 | P31 | J3 | N2 | 344 |
| $V_{CCO}$ | 6 | - | $V_{CCO}$ Bank 6* | $V_{CCO}$ Bank 6* | - |
| GND | - | P32 | GND* | GND* | - |
| I/O | 6 | P33 | K5 | N3 | 347 |
| I/O | 6 | P34 | K2 | N4 | 350 |
| I/O | 6 | - | - | N5 | 356 |
| I/O | 6 | P35 | K1 | P2 | 359 |
| I/O | 6 | - | K3 | P4 | 362 |
| I/O | 6 | - | - | R1 | 365 |
| I/O | 6 | P36 | L1 | P3 | 371 |
| I/O | 6 | P37 | L2 | R2 | 374 |
| $V_{CCINT}$ | - | P38 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 6 | P39 | $V_{CCO}$ Bank 6* | $V_{CCO}$ Bank 6* | - |
| GND | - | P40 | GND* | GND* | - |
| I/O | 6 | P41 | K4 | T1 | 377 |
| I/O, $V_{REF}$ | 6 | P42 | M1 | R4 | 380 |
| I/O | 6 | - | - | T2 | 383 |
| I/O | 6 | P43 | L4 | U1 | 386 |
| I/O | 6 | - | M2 | R5 | 389 |
| I/O | 6 | - | - | V1 | 392 |
| I/O | 6 | - | - | T5 | 395 |
| I/O | 6 | P44 | L3 | U2 | 398 |
| I/O, $V_{REF}$ | 6 | P45 | N1 | T3 | 401 |
| $V_{CCO}$ | 6 | - | $V_{CCO}$ Bank 6* | $V_{CCO}$ Bank 6* | - |
| GND | - | - | GND* | GND* | - |

## XC2S150 Device Pinouts *(Continued)*

| XC2S150 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| I/O | 6 | P46 | P1 | T4 | 404 |
| I/O | 6 | - | L5 | W1 | 407 |
| I/O | 6 | - | - | V2 | 410 |
| I/O | 6 | - | - | U4 | 413 |
| I/O | 6 | P47 | N2 | Y1 | 416 |
| GND | - | - | GND* | GND* | - |
| I/O | 6 | - | M4 | W2 | 419 |
| I/O | 6 | - | - | V3 | 422 |
| I/O | 6 | - | - | V4 | 425 |
| I/O | 6 | P48 | R1 | Y2 | 428 |
| I/O | 6 | P49 | M3 | W3 | 431 |
| M1 | - | P50 | P2 | U5 | 434 |
| GND | - | P51 | GND* | GND* | - |
| M0 | - | P52 | N3 | AB2 | 435 |
| $V_{CCO}$ | 6 | P53 | $V_{CCO}$ Bank 6* | $V_{CCO}$ Bank 6* | - |
| $V_{CCO}$ | 5 | P53 | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| M2 | - | P54 | R3 | Y4 | 436 |
| I/O | 5 | - | - | W5 | 443 |
| I/O | 5 | - | - | AB3 | 446 |
| I/O | 5 | - | N5 | V7 | 449 |
| GND | - | - | GND* | GND* | - |
| I/O | 5 | P57 | T2 | Y6 | 452 |
| I/O | 5 | - | - | AA4 | 455 |
| I/O | 5 | - | - | AB4 | 458 |
| I/O | 5 | - | P5 | W6 | 461 |
| I/O | 5 | P58 | T3 | Y7 | 464 |
| GND | - | - | GND* | GND* | - |
| $V_{CCO}$ | 5 | - | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| I/O, $V_{REF}$ | 5 | P59 | T4 | AA5 | 467 |
| I/O | 5 | P60 | M6 | AB5 | 470 |
| I/O | 5 | - | - | V8 | 473 |
| I/O | 5 | - | - | AA6 | 476 |
| I/O | 5 | - | T5 | AB6 | 479 |
| I/O | 5 | P61 | N6 | AA7 | 482 |
| I/O | 5 | - | - | W7 | 485 |
| I/O, $V_{REF}$ | 5 | P62 | R5 | W8 | 488 |
| I/O | 5 | P63 | P6 | Y8 | 491 |
| GND | - | P64 | GND* | GND* | - |

## XC2S150 Device Pinouts *(Continued)*

| XC2S150 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| $V_{CCO}$ | 5 | P65 | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| $V_{CCINT}$ | - | P66 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 5 | P67 | R6 | AA8 | 494 |
| I/O | 5 | P68 | M7 | V9 | 497 |
| I/O | 5 | - | - | W9 | 503 |
| I/O | 5 | - | - | AB9 | 506 |
| I/O | 5 | P69 | N7 | Y9 | 509 |
| I/O | 5 | - | - | V10 | 512 |
| I/O | 5 | P70 | T6 | W10 | 518 |
| I/O | 5 | P71 | P7 | AB10 | 521 |
| GND | - | P72 | GND* | GND* | - |
| $V_{CCO}$ | 5 | - | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| I/O, $V_{REF}$ | 5 | P73 | P8 | Y10 | 524 |
| I/O | 5 | P74 | R7 | V11 | 527 |
| I/O | 5 | - | T7 | W11 | 530 |
| I/O | 5 | P75 | T8 | AB11 | 533 |
| I/O | 5 | - | - | U11 | 536 |
| $V_{CCINT}$ | - | P76 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I, GCK1 | 5 | P77 | R8 | Y11 | 545 |
| $V_{CCO}$ | 5 | P78 | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| $V_{CCO}$ | 4 | P78 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | P79 | GND* | GND* | - |
| I, GCK0 | 4 | P80 | N8 | W12 | 546 |
| I/O | 4 | P81 | N9 | U12 | 550 |
| I/O | 4 | - | - | V12 | 553 |
| I/O | 4 | P82 | R9 | Y12 | 556 |
| I/O | 4 | - | N10 | AA12 | 559 |
| I/O | 4 | P83 | T9 | AB13 | 562 |
| I/O, $V_{REF}$ | 4 | P84 | P9 | AA13 | 565 |
| $V_{CCO}$ | 4 | - | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | P85 | GND* | GND* | - |
| I/O | 4 | P86 | M10 | Y13 | 568 |
| I/O | 4 | P87 | R10 | V13 | 571 |
| I/O | 4 | - | - | W14 | 577 |
| I/O | 4 | P88 | P10 | AA14 | 580 |
| I/O | 4 | - | - | V14 | 583 |
| I/O | 4 | - | - | Y14 | 586 |
| I/O | 4 | P89 | T10 | AB15 | 592 |

## XC2S150 Device Pinouts *(Continued)*

| XC2S150 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| I/O | 4 | P90 | R11 | AA15 | 595 |
| $V_{CCINT}$ | - | P91 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 4 | P92 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | P93 | GND* | GND* | - |
| I/O | 4 | P94 | M11 | Y15 | 598 |
| I/O, $V_{REF}$ | 4 | P95 | T11 | AB16 | 601 |
| I/O | 4 | - | - | AB17 | 604 |
| I/O | 4 | P96 | N11 | V15 | 607 |
| I/O | 4 | - | R12 | Y16 | 610 |
| I/O | 4 | - | - | AA17 | 613 |
| I/O | 4 | - | - | W16 | 616 |
| I/O | 4 | P97 | P11 | AB18 | 619 |
| I/O, $V_{REF}$ | 4 | P98 | T12 | AB19 | 622 |
| $V_{CCO}$ | 4 | - | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | P99 | T13 | Y17 | 625 |
| I/O | 4 | - | N12 | V16 | 628 |
| I/O | 4 | - | - | AA18 | 631 |
| I/O | 4 | - | - | W17 | 634 |
| I/O | 4 | P100 | R13 | AB20 | 637 |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | - | P12 | AA19 | 640 |
| I/O | 4 | - | - | V17 | 643 |
| I/O | 4 | - | - | Y18 | 646 |
| I/O | 4 | P101 | P13 | AA20 | 649 |
| I/O | 4 | P102 | T14 | W18 | 652 |
| GND | - | P103 | GND* | GND* | - |
| DONE | 3 | P104 | R14 | Y19 | 655 |
| $V_{CCO}$ | 4 | P105 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| $V_{CCO}$ | 3 | P105 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $\overline{PROGRAM}$ | - | P106 | P15 | W20 | 658 |
| I/O ($\overline{INIT}$) | 3 | P107 | N15 | V19 | 659 |
| I/O (D7) | 3 | P108 | N14 | Y21 | 662 |
| I/O | 3 | - | - | V20 | 665 |
| I/O | 3 | - | - | AA22 | 668 |
| I/O | 3 | - | T15 | W21 | 671 |
| GND | - | - | GND* | GND* | - |
| I/O | 3 | P109 | M13 | U20 | 674 |

## XC2S150 Device Pinouts *(Continued)*

| XC2S150 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| I/O | 3 | - | - | U19 | 677 |
| I/O | 3 | - | - | V21 | 680 |
| I/O | 3 | - | R16 | T18 | 683 |
| I/O | 3 | P110 | M14 | W22 | 686 |
| GND | - | - | GND* | GND* | - |
| $V_{CCO}$ | 3 | - | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| I/O, $V_{REF}$ | 3 | P111 | L14 | U21 | 689 |
| I/O | 3 | P112 | M15 | T20 | 692 |
| I/O | 3 | - | - | T19 | 695 |
| I/O | 3 | - | - | V22 | 698 |
| I/O | 3 | - | L12 | T21 | 701 |
| I/O | 3 | P113 | P16 | R18 | 704 |
| I/O | 3 | - | - | U22 | 707 |
| I/O, $V_{REF}$ | 3 | P114 | L13 | R19 | 710 |
| I/O (D6) | 3 | P115 | N16 | T22 | 713 |
| GND | - | P116 | GND* | GND* | - |
| $V_{CCO}$ | 3 | P117 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $V_{CCINT}$ | - | P118 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O (D5) | 3 | P119 | M16 | R21 | 716 |
| I/O | 3 | P120 | K14 | P18 | 719 |
| I/O | 3 | - | - | P19 | 725 |
| I/O | 3 | - | L16 | P20 | 728 |
| I/O | 3 | P121 | K13 | P21 | 731 |
| I/O | 3 | - | - | N19 | 734 |
| I/O | 3 | P122 | L15 | N18 | 740 |
| I/O | 3 | P123 | K12 | N20 | 743 |
| GND | - | P124 | GND* | GND* | - |
| $V_{CCO}$ | 3 | - | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| I/O, $V_{REF}$ | 3 | P125 | K16 | N21 | 746 |
| I/O (D4) | 3 | P126 | J16 | N22 | 749 |
| I/O | 3 | - | J14 | M19 | 752 |
| I/O | 3 | P127 | K15 | M20 | 755 |
| I/O | 3 | - | - | M18 | 758 |
| $V_{CCINT}$ | - | P128 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O, TRDY(1) | 3 | P129 | J15 | M22 | 764 |
| $V_{CCO}$ | 3 | P130 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $V_{CCO}$ | 2 | P130 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P131 | GND* | GND* | - |

## XC2S150 Device Pinouts *(Continued)*

| XC2S150 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| I/O, IRDY(1) | 2 | P132 | H16 | L20 | 767 |
| I/O | 2 | P133 | H14 | L17 | 770 |
| I/O | 2 | - | - | L18 | 773 |
| I/O | 2 | P134 | H15 | L21 | 776 |
| I/O | 2 | - | J13 | L22 | 779 |
| I/O (D3) | 2 | P135 | G16 | K20 | 782 |
| I/O, $V_{REF}$ | 2 | P136 | H13 | K21 | 785 |
| $V_{CCO}$ | 2 | - | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P137 | GND* | GND* | - |
| I/O | 2 | P138 | G14 | K22 | 788 |
| I/O | 2 | P139 | G15 | J21 | 791 |
| I/O | 2 | - | - | J20 | 797 |
| I/O | 2 | P140 | G12 | J18 | 800 |
| I/O | 2 | - | F16 | J22 | 803 |
| I/O | 2 | - | - | J19 | 806 |
| I/O | 2 | P141 | G13 | H19 | 812 |
| I/O (D2) | 2 | P142 | F15 | H20 | 815 |
| $V_{CCINT}$ | - | P143 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 2 | P144 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P145 | GND* | GND* | - |
| I/O (D1) | 2 | P146 | E16 | H22 | 818 |
| I/O, $V_{REF}$ | 2 | P147 | F14 | H18 | 821 |
| I/O | 2 | - | - | G21 | 824 |
| I/O | 2 | P148 | D16 | G18 | 827 |
| I/O | 2 | - | F12 | G20 | 830 |
| I/O | 2 | - | - | G19 | 833 |
| I/O | 2 | - | - | F22 | 836 |
| I/O | 2 | P149 | E15 | F19 | 839 |
| I/O, $V_{REF}$ | 2 | P150 | F13 | F21 | 842 |
| $V_{CCO}$ | 2 | - | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | - | GND* | GND* | - |
| I/O | 2 | P151 | E14 | F20 | 845 |
| I/O | 2 | - | C16 | F18 | 848 |
| I/O | 2 | - | - | E22 | 851 |
| I/O | 2 | - | - | E21 | 854 |
| I/O | 2 | P152 | E13 | D22 | 857 |
| GND | - | - | GND* | GND* | - |
| I/O | 2 | - | B16 | E20 | 860 |
| I/O | 2 | - | - | D21 | 863 |

## XC2S150 Device Pinouts *(Continued)*

| XC2S150 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| I/O | 2 | - | - | C22 | 866 |
| I/O (DIN, D0) | 2 | P153 | D14 | D20 | 869 |
| I/O (DOUT, BUSY) | 2 | P154 | C15 | C21 | 872 |
| CCLK | 2 | P155 | D15 | B22 | 875 |
| $V_{CCO}$ | 2 | P156 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| $V_{CCO}$ | 1 | P156 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| TDO | 2 | P157 | B14 | A21 | - |
| GND | - | P158 | GND* | GND* | - |
| TDI | - | P159 | A15 | B20 | - |
| I/O ($\overline{CS}$) | 1 | P160 | B13 | C19 | 0 |
| I/O ($\overline{WRITE}$) | 1 | P161 | C13 | A20 | 3 |
| I/O | 1 | - | - | B19 | 6 |
| I/O | 1 | - | - | C18 | 9 |
| I/O | 1 | - | C12 | D17 | 12 |
| GND | - | - | GND* | GND* | - |
| I/O | 1 | P162 | A14 | A19 | 15 |
| I/O | 1 | - | - | B18 | 18 |
| I/O | 1 | - | - | E16 | 21 |
| I/O | 1 | - | D12 | C17 | 24 |
| I/O | 1 | P163 | B12 | D16 | 27 |
| GND | - | - | GND* | GND* | - |
| $V_{CCO}$ | 1 | - | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| I/O, $V_{REF}$ | 1 | P164 | C11 | A18 | 30 |
| I/O | 1 | P165 | A13 | B17 | 33 |
| I/O | 1 | - | - | E15 | 36 |
| I/O | 1 | - | - | A17 | 39 |
| I/O | 1 | - | D11 | D15 | 42 |
| I/O | 1 | P166 | A12 | C16 | 45 |
| I/O | 1 | - | - | D14 | 48 |
| I/O, $V_{REF}$ | 1 | P167 | E11 | E14 | 51 |
| I/O | 1 | P168 | B11 | A16 | 54 |
| GND | - | P169 | GND* | GND* | - |
| $V_{CCO}$ | 1 | P170 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| $V_{CCINT}$ | - | P171 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 1 | P172 | A11 | C15 | 57 |
| I/O | 1 | P173 | C10 | B15 | 60 |
| I/O | 1 | - | - | A15 | 66 |
| I/O | 1 | - | - | F12 | 69 |

XC2S200-5FG256I AMD IC FPGA 176 I/O 256FBGA



## XC2S150 Device Pinouts *(Continued)*

| XC2S150 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| I/O | 1 | P174 | B10 | C14 | 72 |
| I/O | 1 | - | - | B14 | 75 |
| I/O | 1 | P175 | D10 | D13 | 81 |
| I/O | 1 | P176 | A10 | C13 | 84 |
| GND | - | P177 | GND* | GND* | - |
| $V_{CCO}$ | 1 | - | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| I/O, $V_{REF}$ | 1 | P178 | B9 | B13 | 87 |
| I/O | 1 | P179 | E10 | E12 | 90 |
| I/O | 1 | - | A9 | B12 | 93 |
| I/O | 1 | P180 | D9 | D12 | 96 |
| I/O | 1 | - | - | C12 | 99 |
| I/O | 1 | P181 | A8 | D11 | 102 |
| I, GCK2 | 1 | P182 | C9 | A11 | 108 |
| GND | - | P183 | GND* | GND* | - |
| $V_{CCO}$ | 1 | P184 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| $V_{CCO}$ | 0 | P184 | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| I, GCK3 | 0 | P185 | B8 | C11 | 109 |
| $V_{CCINT}$ | - | P186 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 0 | - | - | E11 | 116 |
| I/O | 0 | P187 | A7 | A10 | 119 |
| I/O | 0 | - | D8 | B10 | 122 |
| I/O | 0 | P188 | A6 | C10 | 125 |
| I/O, $V_{REF}$ | 0 | P189 | B7 | A9 | 128 |
| $V_{CCO}$ | 0 | - | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| GND | - | P190 | GND* | GND* | - |
| I/O | 0 | P191 | C8 | B9 | 131 |
| I/O | 0 | P192 | D7 | E10 | 134 |
| I/O | 0 | - | - | D10 | 140 |
| I/O | 0 | P193 | E7 | A8 | 143 |
| I/O | 0 | - | - | D9 | 146 |
| I/O | 0 | - | - | B8 | 149 |
| I/O | 0 | P194 | C7 | E9 | 155 |
| I/O | 0 | P195 | B6 | A7 | 158 |

## XC2S150 Device Pinouts *(Continued)*

| XC2S150 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| $V_{CCINT}$ | - | P196 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 0 | P197 | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| GND | - | P198 | GND* | GND* | - |
| I/O | 0 | P199 | A5 | B7 | 161 |
| I/O, $V_{REF}$ | 0 | P200 | C6 | E8 | 164 |
| I/O | 0 | - | - | D8 | 167 |
| I/O | 0 | P201 | B5 | C7 | 170 |
| I/O | 0 | - | D6 | D7 | 173 |
| I/O | 0 | - | - | B6 | 176 |
| I/O | 0 | - | - | A5 | 179 |
| I/O | 0 | P202 | A4 | D6 | 182 |
| I/O, $V_{REF}$ | 0 | P203 | B4 | C6 | 185 |
| $V_{CCO}$ | 0 | - | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| GND | - | - | GND* | GND* | - |
| I/O | 0 | P204 | E6 | B5 | 188 |
| I/O | 0 | - | D5 | E7 | 191 |
| I/O | 0 | - | - | A4 | 194 |
| I/O | 0 | - | - | E6 | 197 |
| I/O | 0 | P205 | A3 | B4 | 200 |
| GND | - | - | GND* | GND* | - |
| I/O | 0 | - | C5 | A3 | 203 |
| I/O | 0 | - | - | B3 | 206 |
| I/O | 0 | - | - | D5 | 209 |
| I/O | 0 | P206 | B3 | C5 | 212 |
| TCK | - | P207 | C4 | C4 | - |
| $V_{CCO}$ | 0 | P208 | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| $V_{CCO}$ | 7 | P208 | $V_{CCO}$ Bank 7* | $V_{CCO}$ Bank 7* | - |

04/18/01

**Notes:**

1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. Pads labelled GND*, $V_{CCINT}$*, $V_{CCO}$ Bank 0*, $V_{CCO}$ Bank 1*, $V_{CCO}$ Bank 2*, $V_{CCO}$ Bank 3*, $V_{CCO}$ Bank 4*, $V_{CCO}$ Bank 5*, $V_{CCO}$ Bank 6*, $V_{CCO}$ Bank 7* are internally bonded to independent ground or power planes within the package.
3. See "VCCO Banks" for details on $V_{CCO}$ banking.

XC2S200-5FG256I AMD IC FPGA 176 I/O 256FBGA



## Additional XC2S150 Package Pins

**PQ208**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P55 | P56 | - | - | - | - |

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**FG256**

| $V_{CCINT}$ Pins | | | | | |
|---|---|---|---|---|---|
| C3 | C14 | D4 | D13 | E5 | E12 |
| M5 | M12 | N4 | N13 | P3 | P14 |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |
| E8 | F8 | - | - | - | - |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| E9 | F9 | - | - | - | - |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| H11 | H12 | - | - | - | - |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| J11 | J12 | - | - | - | - |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| L9 | M9 | - | - | - | - |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| L8 | M8 | - | - | - | - |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| J5 | J6 | - | - | - | - |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |
| H5 | H6 | - | - | - | - |
| **GND Pins** | | | | | |
| A1 | A16 | B2 | B15 | F6 | F7 |
| F10 | F11 | G6 | G7 | G8 | G9 |
| G10 | G11 | H7 | H8 | H9 | H10 |
| J7 | J8 | J9 | J10 | K6 | K7 |
| K8 | K9 | K10 | K11 | L6 | L7 |
| L10 | L11 | R2 | R15 | T1 | T16 |
| **Not Connected Pins** | | | | | |
| P4 | R4 | - | - | - | - |

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## Additional XC2S150 Package Pins *(Continued)*

**FG456**

| $V_{CCINT}$ Pins | | | | | |
|---|---|---|---|---|---|
| E5 | E18 | F6 | F17 | G7 | G8 |
| G9 | G14 | G15 | G16 | H7 | H16 |
| J7 | J16 | P7 | P16 | R7 | R16 |
| T7 | T8 | T9 | T14 | T15 | T16 |
| U6 | U17 | V5 | V18 | - | - |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |
| F7 | F8 | F9 | F10 | G10 | G11 |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| F13 | F14 | F15 | F16 | G12 | G13 |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| G17 | H17 | J17 | K16 | K17 | L16 |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| M16 | N16 | N17 | P17 | R17 | T17 |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| T12 | T13 | U13 | U14 | U15 | U16 |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| T10 | T11 | U7 | U8 | U9 | U10 |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| M7 | N6 | N7 | P6 | R6 | T6 |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |
| G6 | H6 | J6 | K6 | K7 | L7 |
| **GND Pins** | | | | | |
| A1 | A22 | B2 | B21 | C3 | C20 |
| J9 | J10 | J11 | J12 | J13 | J14 |
| K9 | K10 | K11 | K12 | K13 | K14 |
| L9 | L10 | L11 | L12 | L13 | L14 |
| M9 | M10 | M11 | M12 | M13 | M14 |
| N9 | N10 | N11 | N12 | N13 | N14 |
| P9 | P10 | P11 | P12 | P13 | P14 |
| Y3 | Y20 | AA2 | AA21 | AB1 | AB22 |
| **Not Connected Pins** | | | | | |
| A2 | A6 | A12 | A13 | A14 | B11 |
| B16 | C2 | C8 | C9 | D1 | D4 |
| D18 | D19 | E13 | E17 | E19 | F11 |
| G2 | G22 | H21 | J1 | J4 | K2 |
| K18 | K19 | L2 | L19 | M2 | M17 |
| M21 | N1 | P1 | P5 | P22 | R3 |
| R20 | R22 | U3 | U18 | V6 | W4 |
| W13 | W15 | W19 | Y5 | Y22 | AA1 |
| AA3 | AA9 | AA10 | AA11 | AA16 | AB7 |
| AB8 | AB12 | AB14 | AB21 | - | - |

11/02/00

## XC2S200 Device Pinouts

| XC2S200 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| GND | - | P1 | GND* | GND* | - |
| TMS | - | P2 | D3 | D3 | - |
| I/O | 7 | P3 | C2 | B1 | 257 |
| I/O | 7 | - | - | E4 | 263 |
| I/O | 7 | - | - | C1 | 266 |
| I/O | 7 | - | A2 | F5 | 269 |
| GND | - | - | GND* | GND* | - |
| I/O, $V_{REF}$ | 7 | P4 | B1 | D2 | 272 |
| I/O | 7 | - | - | E3 | 275 |
| I/O | 7 | - | - | F4 | 281 |
| GND | - | - | GND* | GND* | - |
| I/O | 7 | - | E3 | G5 | 284 |
| I/O | 7 | P5 | D2 | F3 | 287 |
| GND | - | - | GND* | GND* | - |
| $V_{CCO}$ | 7 | - | $V_{CCO}$ Bank 7* | $V_{CCO}$ Bank 7* | - |
| I/O, $V_{REF}$ | 7 | P6 | C1 | E2 | 290 |
| I/O | 7 | P7 | F3 | E1 | 293 |
| I/O | 7 | - | - | G4 | 296 |
| I/O | 7 | - | - | G3 | 299 |
| I/O | 7 | - | E2 | H5 | 302 |
| GND | - | - | GND* | GND* | - |
| I/O | 7 | P8 | E4 | F2 | 305 |
| I/O | 7 | - | - | F1 | 308 |
| I/O, $V_{REF}$ | 7 | P9 | D1 | H4 | 314 |
| I/O | 7 | P10 | E1 | G1 | 317 |
| GND | - | P11 | GND* | GND* | - |
| $V_{CCO}$ | 7 | P12 | $V_{CCO}$ Bank 7* | $V_{CCO}$ Bank 7* | - |
| $V_{CCINT}$ | - | P13 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 7 | P14 | F2 | H3 | 320 |
| I/O | 7 | P15 | G3 | H2 | 323 |
| I/O | 7 | - | - | J4 | 326 |
| I/O | 7 | - | - | H1 | 329 |
| I/O | 7 | - | F1 | J5 | 332 |
| GND | - | - | GND* | GND* | - |
| I/O | 7 | P16 | F4 | J2 | 335 |
| I/O | 7 | - | - | J3 | 338 |
| I/O | 7 | - | - | J1 | 341 |
| I/O | 7 | P17 | F5 | K5 | 344 |
| I/O | 7 | P18 | G2 | K1 | 347 |
| GND | - | P19 | GND* | GND* | - |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| $V_{CCO}$ | 7 | - | $V_{CCO}$ Bank 7* | $V_{CCO}$ Bank 7* | - |
| I/O, $V_{REF}$ | 7 | P20 | H3 | K3 | 350 |
| I/O | 7 | P21 | G4 | K4 | 353 |
| I/O | 7 | - | - | K2 | 359 |
| I/O | 7 | - | H2 | L6 | 362 |
| I/O | 7 | P22 | G5 | L1 | 365 |
| I/O | 7 | - | - | L5 | 368 |
| I/O | 7 | P23 | H4 | L4 | 374 |
| I/O, IRDY(1) | 7 | P24 | G1 | L3 | 377 |
| GND | - | P25 | GND* | GND* | - |
| $V_{CCO}$ | 7 | P26 | $V_{CCO}$ Bank 7* | $V_{CCO}$ Bank 7* | - |
| $V_{CCO}$ | 6 | P26 | $V_{CCO}$ Bank 6* | $V_{CCO}$ Bank 6* | - |
| I/O, TRDY(1) | 6 | P27 | J2 | M1 | 380 |
| $V_{CCINT}$ | - | P28 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 6 | - | - | M6 | 389 |
| I/O | 6 | P29 | H1 | M3 | 392 |
| I/O | 6 | - | J4 | M4 | 395 |
| I/O | 6 | - | - | N1 | 398 |
| I/O | 6 | P30 | J1 | M5 | 404 |
| I/O, $V_{REF}$ | 6 | P31 | J3 | N2 | 407 |
| $V_{CCO}$ | 6 | - | $V_{CCO}$ Bank 6* | $V_{CCO}$ Bank 6* | - |
| GND | - | P32 | GND* | GND* | - |
| I/O | 6 | P33 | K5 | N3 | 410 |
| I/O | 6 | P34 | K2 | N4 | 413 |
| I/O | 6 | - | - | P1 | 416 |
| I/O | 6 | - | - | N5 | 419 |
| I/O | 6 | P35 | K1 | P2 | 422 |
| GND | - | - | GND* | GND* | - |
| I/O | 6 | - | K3 | P4 | 425 |
| I/O | 6 | - | - | R1 | 428 |
| I/O | 6 | - | - | P5 | 431 |
| I/O | 6 | P36 | L1 | P3 | 434 |
| I/O | 6 | P37 | L2 | R2 | 437 |
| $V_{CCINT}$ | - | P38 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 6 | P39 | $V_{CCO}$ Bank 6* | $V_{CCO}$ Bank 6* | - |
| GND | - | P40 | GND* | GND* | - |
| I/O | 6 | P41 | K4 | T1 | 440 |
| I/O, $V_{REF}$ | 6 | P42 | M1 | R4 | 443 |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| I/O | 6 | - | - | T2 | 449 |
| I/O | 6 | P43 | L4 | U1 | 452 |
| GND | - | - | GND* | GND* | - |
| I/O | 6 | - | M2 | R5 | 455 |
| I/O | 6 | - | - | V1 | 458 |
| I/O | 6 | - | - | T5 | 461 |
| I/O | 6 | P44 | L3 | U2 | 464 |
| I/O, $V_{REF}$ | 6 | P45 | N1 | T3 | 467 |
| $V_{CCO}$ | 6 | - | $V_{CCO}$ Bank 6* | $V_{CCO}$ Bank 6* | - |
| GND | - | - | GND* | GND* | - |
| I/O | 6 | P46 | P1 | T4 | 470 |
| I/O | 6 | - | L5 | W1 | 473 |
| GND | - | - | GND* | GND* | - |
| I/O | 6 | - | - | V2 | 476 |
| I/O | 6 | - | - | U4 | 482 |
| I/O, $V_{REF}$ | 6 | P47 | N2 | Y1 | 485 |
| GND | - | - | GND* | GND* | - |
| I/O | 6 | - | M4 | W2 | 488 |
| I/O | 6 | - | - | V3 | 491 |
| I/O | 6 | - | - | V4 | 494 |
| I/O | 6 | P48 | R1 | Y2 | 500 |
| I/O | 6 | P49 | M3 | W3 | 503 |
| M1 | - | P50 | P2 | U5 | 506 |
| GND | - | P51 | GND* | GND* | - |
| M0 | - | P52 | N3 | AB2 | 507 |
| $V_{CCO}$ | 6 | P53 | $V_{CCO}$ Bank 6* | $V_{CCO}$ Bank 6* | - |
| $V_{CCO}$ | 5 | P53 | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| M2 | - | P54 | R3 | Y4 | 508 |
| I/O | 5 | - | - | W5 | 518 |
| I/O | 5 | - | - | AB3 | 521 |
| I/O | 5 | - | N5 | V7 | 524 |
| GND | - | - | GND* | GND* | - |
| I/O, $V_{REF}$ | 5 | P57 | T2 | Y6 | 527 |
| I/O | 5 | - | - | AA4 | 530 |
| I/O | 5 | - | - | AB4 | 536 |
| I/O | 5 | - | P5 | W6 | 539 |
| I/O | 5 | P58 | T3 | Y7 | 542 |
| GND | - | - | GND* | GND* | - |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| $V_{CCO}$ | 5 | - | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| I/O, $V_{REF}$ | 5 | P59 | T4 | AA5 | 545 |
| I/O | 5 | P60 | M6 | AB5 | 548 |
| I/O | 5 | - | - | V8 | 551 |
| I/O | 5 | - | - | AA6 | 554 |
| I/O | 5 | - | T5 | AB6 | 557 |
| GND | - | - | GND* | GND* | - |
| I/O | 5 | P61 | N6 | AA7 | 560 |
| I/O | 5 | - | - | W7 | 563 |
| I/O, $V_{REF}$ | 5 | P62 | R5 | W8 | 569 |
| I/O | 5 | P63 | P6 | Y8 | 572 |
| GND | - | P64 | GND* | GND* | - |
| $V_{CCO}$ | 5 | P65 | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| $V_{CCINT}$ | - | P66 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 5 | P67 | R6 | AA8 | 575 |
| I/O | 5 | P68 | M7 | V9 | 578 |
| I/O | 5 | - | - | AB8 | 581 |
| I/O | 5 | - | - | W9 | 584 |
| I/O | 5 | - | - | AB9 | 587 |
| GND | - | - | GND* | GND* | - |
| I/O | 5 | P69 | N7 | Y9 | 590 |
| I/O | 5 | - | - | V10 | 593 |
| I/O | 5 | - | - | AA9 | 596 |
| I/O | 5 | P70 | T6 | W10 | 599 |
| I/O | 5 | P71 | P7 | AB10 | 602 |
| GND | - | P72 | GND* | GND* | - |
| $V_{CCO}$ | 5 | - | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| I/O, $V_{REF}$ | 5 | P73 | P8 | Y10 | 605 |
| I/O | 5 | P74 | R7 | V11 | 608 |
| I/O | 5 | - | - | AA10 | 614 |
| I/O | 5 | - | T7 | W11 | 617 |
| I/O | 5 | P75 | T8 | AB11 | 620 |
| I/O | 5 | - | - | U11 | 623 |
| $V_{CCINT}$ | - | P76 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I, GCK1 | 5 | P77 | R8 | Y11 | 635 |
| $V_{CCO}$ | 5 | P78 | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| $V_{CCO}$ | 4 | P78 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | P79 | GND* | GND* | - |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| I, GCK0 | 4 | P80 | N8 | W12 | 636 |
| I/O | 4 | P81 | N9 | U12 | 640 |
| I/O | 4 | - | - | V12 | 646 |
| I/O | 4 | P82 | R9 | Y12 | 649 |
| I/O | 4 | - | N10 | AA12 | 652 |
| I/O | 4 | - | - | W13 | 655 |
| I/O | 4 | P83 | T9 | AB13 | 661 |
| I/O, $V_{REF}$ | 4 | P84 | P9 | AA13 | 664 |
| $V_{CCO}$ | 4 | - | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | P85 | GND* | GND* | - |
| I/O | 4 | P86 | M10 | Y13 | 667 |
| I/O | 4 | P87 | R10 | V13 | 670 |
| I/O | 4 | - | - | AB14 | 673 |
| I/O | 4 | - | - | W14 | 676 |
| I/O | 4 | P88 | P10 | AA14 | 679 |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | - | - | V14 | 682 |
| I/O | 4 | - | - | Y14 | 685 |
| I/O | 4 | - | - | W15 | 688 |
| I/O | 4 | P89 | T10 | AB15 | 691 |
| I/O | 4 | P90 | R11 | AA15 | 694 |
| $V_{CCINT}$ | - | P91 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 4 | P92 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | P93 | GND* | GND* | - |
| I/O | 4 | P94 | M11 | Y15 | 697 |
| I/O, $V_{REF}$ | 4 | P95 | T11 | AB16 | 700 |
| I/O | 4 | - | - | AB17 | 706 |
| I/O | 4 | P96 | N11 | V15 | 709 |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | - | R12 | Y16 | 712 |
| I/O | 4 | - | - | AA17 | 715 |
| I/O | 4 | - | - | W16 | 718 |
| I/O | 4 | P97 | P11 | AB18 | 721 |
| I/O, $V_{REF}$ | 4 | P98 | T12 | AB19 | 724 |
| $V_{CCO}$ | 4 | - | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | P99 | T13 | Y17 | 727 |
| I/O | 4 | - | N12 | V16 | 730 |
| I/O | 4 | - | - | AA18 | 733 |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| I/O | 4 | - | - | W17 | 739 |
| I/O, $V_{REF}$ | 4 | P100 | R13 | AB20 | 742 |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | - | P12 | AA19 | 745 |
| I/O | 4 | - | - | V17 | 748 |
| I/O | 4 | - | - | Y18 | 751 |
| I/O | 4 | P101 | P13 | AA20 | 757 |
| I/O | 4 | P102 | T14 | W18 | 760 |
| GND | - | P103 | GND* | GND* | - |
| DONE | 3 | P104 | R14 | Y19 | 763 |
| $V_{CCO}$ | 4 | P105 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| $V_{CCO}$ | 3 | P105 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $\overline{PROGRAM}$ | - | P106 | P15 | W20 | 766 |
| I/O ($\overline{INIT}$) | 3 | P107 | N15 | V19 | 767 |
| I/O (D7) | 3 | P108 | N14 | Y21 | 770 |
| I/O | 3 | - | - | V20 | 776 |
| I/O | 3 | - | - | AA22 | 779 |
| I/O | 3 | - | T15 | W21 | 782 |
| GND | - | - | GND* | GND* | - |
| I/O, $V_{REF}$ | 3 | P109 | M13 | U20 | 785 |
| I/O | 3 | - | - | U19 | 788 |
| I/O | 3 | - | - | V21 | 794 |
| GND | - | - | GND* | GND* | - |
| I/O | 3 | - | R16 | T18 | 797 |
| I/O | 3 | P110 | M14 | W22 | 800 |
| GND | - | - | GND* | GND* | - |
| $V_{CCO}$ | 3 | - | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| I/O, $V_{REF}$ | 3 | P111 | L14 | U21 | 803 |
| I/O | 3 | P112 | M15 | T20 | 806 |
| I/O | 3 | - | - | T19 | 809 |
| I/O | 3 | - | - | V22 | 812 |
| I/O | 3 | - | L12 | T21 | 815 |
| GND | - | - | GND* | GND* | - |
| I/O | 3 | P113 | P16 | R18 | 818 |
| I/O | 3 | - | - | U22 | 821 |
| I/O, $V_{REF}$ | 3 | P114 | L13 | R19 | 827 |
| I/O (D6) | 3 | P115 | N16 | T22 | 830 |
| GND | - | P116 | GND* | GND* | - |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| $V_{CCO}$ | 3 | P117 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $V_{CCINT}$ | - | P118 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O (D5) | 3 | P119 | M16 | R21 | 833 |
| I/O | 3 | P120 | K14 | P18 | 836 |
| I/O | 3 | - | - | R22 | 839 |
| I/O | 3 | - | - | P19 | 842 |
| I/O | 3 | - | L16 | P20 | 845 |
| GND | - | - | GND* | GND* | - |
| I/O | 3 | P121 | K13 | P21 | 848 |
| I/O | 3 | - | - | N19 | 851 |
| I/O | 3 | - | - | P22 | 854 |
| I/O | 3 | P122 | L15 | N18 | 857 |
| I/O | 3 | P123 | K12 | N20 | 860 |
| GND | - | P124 | GND* | GND* | - |
| $V_{CCO}$ | 3 | - | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| I/O, $V_{REF}$ | 3 | P125 | K16 | N21 | 863 |
| I/O (D4) | 3 | P126 | J16 | N22 | 866 |
| I/O | 3 | - | - | M17 | 872 |
| I/O | 3 | - | J14 | M19 | 875 |
| I/O | 3 | P127 | K15 | M20 | 878 |
| I/O | 3 | - | - | M18 | 881 |
| $V_{CCINT}$ | - | P128 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O, TRDY(1) | 3 | P129 | J15 | M22 | 890 |
| $V_{CCO}$ | 3 | P130 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $V_{CCO}$ | 2 | P130 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P131 | GND* | GND* | - |
| I/O, IRDY(1) | 2 | P132 | H16 | L20 | 893 |
| I/O | 2 | P133 | H14 | L17 | 896 |
| I/O | 2 | - | - | L18 | 902 |
| I/O | 2 | P134 | H15 | L21 | 905 |
| I/O | 2 | - | J13 | L22 | 908 |
| I/O | 2 | - | - | K19 | 911 |
| I/O (D3) | 2 | P135 | G16 | K20 | 917 |
| I/O, $V_{REF}$ | 2 | P136 | H13 | K21 | 920 |
| $V_{CCO}$ | 2 | - | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P137 | GND* | GND* | - |
| I/O | 2 | P138 | G14 | K22 | 923 |
| I/O | 2 | P139 | G15 | J21 | 926 |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| I/O | 2 | - | - | K18 | 929 |
| I/O | 2 | - | - | J20 | 932 |
| I/O | 2 | P140 | G12 | J18 | 935 |
| GND | - | - | GND* | GND* | - |
| I/O | 2 | - | F16 | J22 | 938 |
| I/O | 2 | - | - | J19 | 941 |
| I/O | 2 | - | - | H21 | 944 |
| I/O | 2 | P141 | G13 | H19 | 947 |
| I/O (D2) | 2 | P142 | F15 | H20 | 950 |
| $V_{CCINT}$ | - | P143 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 2 | P144 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P145 | GND* | GND* | - |
| I/O (D1) | 2 | P146 | E16 | H22 | 953 |
| I/O, $V_{REF}$ | 2 | P147 | F14 | H18 | 956 |
| I/O | 2 | - | - | G21 | 962 |
| I/O | 2 | P148 | D16 | G18 | 965 |
| GND | - | - | GND* | GND* | - |
| I/O | 2 | - | F12 | G20 | 968 |
| I/O | 2 | - | - | G19 | 971 |
| I/O | 2 | - | - | F22 | 974 |
| I/O | 2 | P149 | E15 | F19 | 977 |
| I/O, $V_{REF}$ | 2 | P150 | F13 | F21 | 980 |
| $V_{CCO}$ | 2 | - | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | - | GND* | GND* | - |
| I/O | 2 | P151 | E14 | F20 | 983 |
| I/O | 2 | - | C16 | F18 | 986 |
| GND | - | - | GND* | GND* | - |
| I/O | 2 | - | - | E22 | 989 |
| I/O | 2 | - | - | E21 | 995 |
| I/O, $V_{REF}$ | 2 | P152 | E13 | D22 | 998 |
| GND | - | - | GND* | GND* | - |
| I/O | 2 | - | B16 | E20 | 1001 |
| I/O | 2 | - | - | D21 | 1004 |
| I/O | 2 | - | - | C22 | 1007 |
| I/O (DIN, D0) | 2 | P153 | D14 | D20 | 1013 |
| I/O (DOUT, BUSY) | 2 | P154 | C15 | C21 | 1016 |
| CCLK | 2 | P155 | D15 | B22 | 1019 |
| $V_{CCO}$ | 2 | P156 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| $V_{CCO}$ | 1 | P156 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| TDO | 2 | P157 | B14 | A21 | - |
| GND | - | P158 | GND* | GND* | - |
| TDI | - | P159 | A15 | B20 | - |
| I/O ($\overline{CS}$) | 1 | P160 | B13 | C19 | 0 |
| I/O ($\overline{WRITE}$) | 1 | P161 | C13 | A20 | 3 |
| I/O | 1 | - | - | B19 | 9 |
| I/O | 1 | - | - | C18 | 12 |
| I/O | 1 | - | C12 | D17 | 15 |
| GND | - | - | GND* | GND* | - |
| I/O, $V_{REF}$ | 1 | P162 | A14 | A19 | 18 |
| I/O | 1 | - | - | B18 | 21 |
| I/O | 1 | - | - | E16 | 27 |
| I/O | 1 | - | D12 | C17 | 30 |
| I/O | 1 | P163 | B12 | D16 | 33 |
| GND | - | - | GND* | GND* | - |
| $V_{CCO}$ | 1 | - | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| I/O, $V_{REF}$ | 1 | P164 | C11 | A18 | 36 |
| I/O | 1 | P165 | A13 | B17 | 39 |
| I/O | 1 | - | - | E15 | 42 |
| I/O | 1 | - | - | A17 | 45 |
| I/O | 1 | - | D11 | D15 | 48 |
| GND | - | - | GND* | GND* | - |
| I/O | 1 | P166 | A12 | C16 | 51 |
| I/O | 1 | - | - | D14 | 54 |
| I/O, $V_{REF}$ | 1 | P167 | E11 | E14 | 60 |
| I/O | 1 | P168 | B11 | A16 | 63 |
| GND | - | P169 | GND* | GND* | - |
| $V_{CCO}$ | 1 | P170 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| $V_{CCINT}$ | - | P171 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 1 | P172 | A11 | C15 | 66 |
| I/O | 1 | P173 | C10 | B15 | 69 |
| I/O | 1 | - | - | E13 | 72 |
| I/O | 1 | - | - | A15 | 75 |
| I/O | 1 | - | - | F12 | 78 |
| GND | - | - | GND* | GND* | - |
| I/O | 1 | P174 | B10 | C14 | 81 |
| I/O | 1 | - | - | B14 | 84 |
| I/O | 1 | - | - | A14 | 87 |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| I/O | 1 | P175 | D10 | D13 | 90 |
| I/O | 1 | P176 | A10 | C13 | 93 |
| GND | - | P177 | GND* | GND* | - |
| $V_{CCO}$ | 1 | - | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| I/O, $V_{REF}$ | 1 | P178 | B9 | B13 | 96 |
| I/O | 1 | P179 | E10 | E12 | 99 |
| I/O | 1 | - | - | A13 | 105 |
| I/O | 1 | - | A9 | B12 | 108 |
| I/O | 1 | P180 | D9 | D12 | 111 |
| I/O | 1 | - | - | C12 | 114 |
| I/O | 1 | P181 | A8 | D11 | 120 |
| I, GCK2 | 1 | P182 | C9 | A11 | 126 |
| GND | - | P183 | GND* | GND* | - |
| $V_{CCO}$ | 1 | P184 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| $V_{CCO}$ | 0 | P184 | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| I, GCK3 | 0 | P185 | B8 | C11 | 127 |
| $V_{CCINT}$ | - | P186 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 0 | - | - | E11 | 137 |
| I/O | 0 | P187 | A7 | A10 | 140 |
| I/O | 0 | - | D8 | B10 | 143 |
| I/O | 0 | - | - | F11 | 146 |
| I/O | 0 | P188 | A6 | C10 | 152 |
| I/O, $V_{REF}$ | 0 | P189 | B7 | A9 | 155 |
| $V_{CCO}$ | 0 | - | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| GND | - | P190 | GND* | GND* | - |
| I/O | 0 | P191 | C8 | B9 | 158 |
| I/O | 0 | P192 | D7 | E10 | 161 |
| I/O | 0 | - | - | C9 | 164 |
| I/O | 0 | - | - | D10 | 167 |
| I/O | 0 | P193 | E7 | A8 | 170 |
| GND | - | - | GND* | GND* | - |
| I/O | 0 | - | - | D9 | 173 |
| I/O | 0 | - | - | B8 | 176 |
| I/O | 0 | - | - | C8 | 179 |
| I/O | 0 | P194 | C7 | E9 | 182 |
| I/O | 0 | P195 | B6 | A7 | 185 |
| $V_{CCINT}$ | - | P196 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 0 | P197 | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| GND | - | P198 | GND* | GND* | - |
| I/O | 0 | P199 | A5 | B7 | 188 |
| I/O, $V_{REF}$ | 0 | P200 | C6 | E8 | 191 |
| I/O | 0 | - | - | D8 | 197 |
| I/O | 0 | P201 | B5 | C7 | 200 |
| GND | - | - | GND* | GND* | - |
| I/O | 0 | - | D6 | D7 | 203 |
| I/O | 0 | - | - | B6 | 206 |
| I/O | 0 | - | - | A5 | 209 |
| I/O | 0 | P202 | A4 | D6 | 212 |
| I/O, $V_{REF}$ | 0 | P203 | B4 | C6 | 215 |
| $V_{CCO}$ | 0 | - | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| GND | - | - | GND* | GND* | - |
| I/O | 0 | P204 | E6 | B5 | 218 |
| I/O | 0 | - | D5 | E7 | 221 |
| I/O | 0 | - | - | A4 | 224 |
| I/O | 0 | - | - | E6 | 230 |
| I/O, $V_{REF}$ | 0 | P205 | A3 | B4 | 233 |
| GND | - | - | GND* | GND* | - |
| I/O | 0 | - | C5 | A3 | 236 |
| I/O | 0 | - | - | B3 | 239 |
| I/O | 0 | - | - | D5 | 242 |
| I/O | 0 | P206 | B3 | C5 | 248 |
| TCK | - | P207 | C4 | C4 | - |
| $V_{CCO}$ | 0 | P208 | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| $V_{CCO}$ | 7 | P208 | $V_{CCO}$ Bank 7* | $V_{CCO}$ Bank 7* | - |

04/18/01

**Notes:**

1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. Pads labelled GND*, $V_{CCINT}$*, $V_{CCO}$ Bank 0*, $V_{CCO}$ Bank 1*, $V_{CCO}$ Bank 2*, $V_{CCO}$ Bank 3*, $V_{CCO}$ Bank 4*, $V_{CCO}$ Bank 5*, $V_{CCO}$ Bank 6*, $V_{CCO}$ Bank 7* are internally bonded to independent ground or power planes within the package.
3. See "VCCO Banks" for details on $V_{CCO}$ banking.

## Additional XC2S200 Package Pins

**PQ208**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P55 | P56 | - | - | - | - |

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**FG256**

| $V_{CCINT}$ Pins | | | | | |
|---|---|---|---|---|---|
| C3 | C14 | D4 | D13 | E5 | E12 |
| M5 | M12 | N4 | N13 | P3 | P14 |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |
| E8 | F8 | - | - | - | - |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| E9 | F9 | - | - | - | - |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| H11 | H12 | - | - | - | - |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| J11 | J12 | - | - | - | - |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| L9 | M9 | - | - | - | - |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| L8 | M8 | - | - | - | - |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| J5 | J6 | - | - | - | - |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |
| H5 | H6 | - | - | - | - |
| **GND Pins** | | | | | |
| A1 | A16 | B2 | B15 | F6 | F7 |
| F10 | F11 | G6 | G7 | G8 | G9 |
| G10 | G11 | H7 | H8 | H9 | H10 |
| J7 | J8 | J9 | J10 | K6 | K7 |
| K8 | K9 | K10 | K11 | L6 | L7 |
| L10 | L11 | R2 | R15 | T1 | T16 |
| **Not Connected Pins** | | | | | |
| P4 | R4 | - | - | - | - |

XC2S200-5FG256I AMD IC FPGA 176 I/O 256FBGA



## Additional XC2S200 Package Pins *(Continued)*

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**FG456**

| $V_{CCINT}$ Pins | | | | | |
|---|---|---|---|---|---|
| E5 | E18 | F6 | F17 | G7 | G8 |
| G9 | G14 | G15 | G16 | H7 | H16 |
| J7 | J16 | P7 | P16 | R7 | R16 |
| T7 | T8 | T9 | T14 | T15 | T16 |
| U6 | U17 | V5 | V18 | - | - |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |
| F7 | F8 | F9 | F10 | G10 | G11 |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| F13 | F14 | F15 | F16 | G12 | G13 |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| G17 | H17 | J17 | K16 | K17 | L16 |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| M16 | N16 | N17 | P17 | R17 | T17 |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| T12 | T13 | U13 | U14 | U15 | U16 |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| T10 | T11 | U7 | U8 | U9 | U10 |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| M7 | N6 | N7 | P6 | R6 | T6 |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |
| G6 | H6 | J6 | K6 | K7 | L7 |
| **GND Pins** | | | | | |
| A1 | A22 | B2 | B21 | C3 | C20 |
| J9 | J10 | J11 | J12 | J13 | J14 |
| K9 | K10 | K11 | K12 | K13 | K14 |
| L9 | L10 | L11 | L12 | L13 | L14 |
| M9 | M10 | M11 | M12 | M13 | M14 |
| N9 | N10 | N11 | N12 | N13 | N14 |
| P9 | P10 | P11 | P12 | P13 | P14 |
| Y3 | Y20 | AA2 | AA21 | AB1 | AB22 |
| **Not Connected Pins** | | | | | |
| A2 | A6 | A12 | B11 | B16 | C2 |
| D1 | D4 | D18 | D19 | E17 | E19 |
| G2 | G22 | L2 | L19 | M2 | M21 |
| R3 | R20 | U3 | U18 | V6 | W4 |
| W19 | Y5 | Y22 | AA1 | AA3 | AA11 |
| AA16 | AB7 | AB12 | AB21 | - | - |

11/02/00

# Revision History

| Version No. | Date | Description |
|---|---|---|
| 2.0 | 09/18/00 | Sectioned the Spartan-II Family data sheet into four modules. Corrected all known errors in the pinout tables. |
| 2.1 | 10/04/00 | Added notes requiring $\overline{PWDN}$ to be tied to $V_{CCINT}$ when unused. |
| 2.2 | 11/02/00 | Removed the Power Down feature. |
| 2.3 | 03/05/01 | Added notes on pinout tables for IRDY and TRDY. |
| 2.4 | 04/30/01 | Reinstated XC2S50 $V_{CCO}$ Bank 7, GND, and "not connected" pins missing in version 2.3. |
| 2.5 | 09/03/03 | Added caution about Not Connected Pins to XC2S30 pinout tables on page 76. |
| 2.8 | 06/13/08 | Added "Package Overview" section. Added notes to clarify shared $V_{CCO}$ banks. Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8. |
| 2.9 | 03/12/21 | Added note 3 to Table 2 (see XCN20012, *Product Discontinuation Notice for Spartan-II PQ(G)208 Package Pin Products*). |

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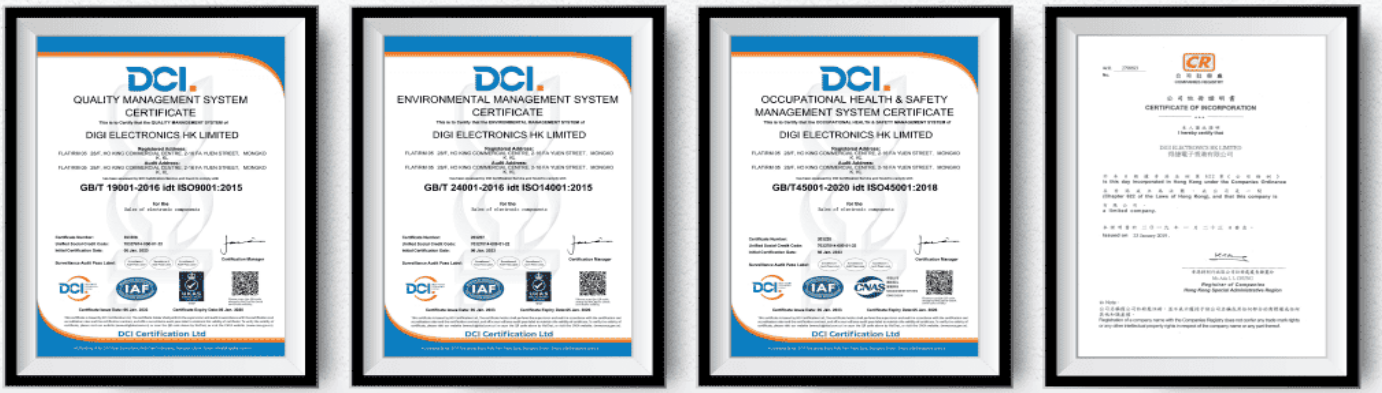

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