

XC6SLX4-2TQG144I Datasheet

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XC6SLX4-2TQG144I

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|------------------------------|--|
| DiGi Electronics Part Number | XC6SLX4-2TQG144I-DG |
| Manufacturer | AMD |
| Manufacturer Product Number | XC6SLX4-2TQG144I |
| Description | IC FPGA 102 I/O 144TQFP |
| Detailed Description | Spartan®-6 LX Field Programmable Gate Array (FPGA) IC 102 221184 3840 144-LQFP |



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Purchase and inquiry

Manufacturer Product Number:

XC6SLX4-2TQG144I

Series:

Spartan®-6 LX

DiGi-Electronics Programmable:

Not Verified

Number of Logic Elements/Cells:

3840

Number of I/O:

102

Mounting Type:

Surface Mount

Package / Case:

144-LQFP

Base Product Number:

XC6SLX4

Manufacturer:

AMD

Product Status:

Active

Number of LABs/CLBs:

300

Total RAM Bits:

221184

Voltage - Supply:

1.14V ~ 1.26V

Operating Temperature:

-40°C ~ 100°C (TJ)

Supplier Device Package:

144-TQFP (20x20)

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

3 (168 Hours)

ECCN:

EAR99



Spartan-6 FPGA Data Sheet: DC and Switching Characteristics

DS162 (v3.1.1) January 30, 2015

Product Specification

Spartan-6 FPGA Electrical Characteristics

Spartan®-6 LX and LXT FPGAs are available in various speed grades, with -3 having the highest performance. The DC and AC electrical parameters of the Automotive XA Spartan-6 FPGAs and Defense-grade Spartan-6Q FPGAs devices are equivalent to the commercial specifications except where noted. The timing characteristics of the commercial (XC) -2 speed grade industrial device are the same as for a -2 speed grade commercial device. The -2Q and -3Q speed grades are exclusively for the expanded (Q) temperature range. The timing characteristics are equivalent to those shown for the -2 and -3 speed grades for the Automotive and Defense-grade devices.

Spartan-6 FPGA DC and AC characteristics are specified for commercial (C), industrial (I), and expanded (Q) temperature ranges. Only selected speed grades and/or devices might be available in the industrial or expanded temperature ranges for Automotive and Defense-grade devices. References to device names refer to all available variations of that part number (for example, LX75 could denote XC6SLX75, XA6SLX75, or XQ6SLX75). The Spartan-6 FPGA -3N speed grade designates devices that do not support MCB functionality.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

Available device and package combinations can be found at:

- [DS160](#): *Spartan-6 Family Overview*
- [DS170](#): *Automotive XA Spartan-6 Family Overview*
- [DS172](#): *Defense-Grade Spartan-6Q Family Overview*

This Spartan-6 FPGA data sheet, part of an overall set of documentation on the Spartan-6 family of FPGAs, is available on the Xilinx website at <http://www.xilinx.com/support/documentation/spartan-6.htm>.

Spartan-6 FPGA DC Characteristics

Table 1: Absolute Maximum Ratings⁽¹⁾

| Symbol | Description | | Units |
|-------------|---|--------------|-------|
| V_{CCINT} | Internal supply voltage relative to GND | -0.5 to 1.32 | V |
| V_{CCAUX} | Auxiliary supply voltage relative to GND | -0.5 to 3.75 | V |
| V_{CCO} | Output drivers supply voltage relative to GND | -0.5 to 3.75 | V |
| V_{BATT} | Key memory battery backup supply (LX75, LX75T, LX100, LX100T, LX150, and LX150T only) | -0.5 to 4.05 | V |
| V_{FS} | External voltage supply for eFUSE programming (LX75, LX75T, LX100, LX100T, LX150, and LX150T only) ⁽²⁾ | -0.5 to 3.75 | V |
| V_{REF} | Input reference voltage | -0.5 to 3.75 | V |

Table 1: Absolute Maximum Ratings⁽¹⁾ (Cont'd)

| Symbol | Description | | | | Units | |
|--------------------------------------|--|--|--------------|---------------------------------------|---------------|----|
| V_{IN} and V_{TS} ⁽³⁾ | I/O input voltage or voltage applied to 3-state output, relative to GND ⁽⁴⁾ | All user and dedicated I/Os | Commercial | DC | -0.60 to 4.10 | V |
| | | | | 20% overshoot duration | -0.75 to 4.25 | V |
| | | | | 8% overshoot duration ⁽⁵⁾ | -0.75 to 4.40 | V |
| | | | Industrial | DC | -0.60 to 3.95 | V |
| | | | | 20% overshoot duration | -0.75 to 4.15 | V |
| | | | | 4% overshoot duration ⁽⁵⁾ | -0.75 to 4.40 | V |
| | | | Expanded (Q) | DC | -0.60 to 3.95 | V |
| | | | | 20% overshoot duration | -0.75 to 4.15 | V |
| | | | | 4% overshoot duration ⁽⁵⁾ | -0.75 to 4.40 | V |
| | | Restricted to maximum of 100 user I/Os | Commercial | 20% overshoot duration | -0.75 to 4.35 | V |
| | | | | 15% overshoot duration ⁽⁵⁾ | -0.75 to 4.40 | V |
| | | | | 10% overshoot duration | -0.75 to 4.45 | V |
| | | | Industrial | 20% overshoot duration | -0.75 to 4.25 | V |
| | | | | 10% overshoot duration | -0.75 to 4.35 | V |
| | | | | 8% overshoot duration ⁽⁵⁾ | -0.75 to 4.40 | V |
| Expanded (Q) | 20% overshoot duration | -0.75 to 4.25 | V | | | |
| | 10% overshoot duration | -0.75 to 4.35 | V | | | |
| | 8% overshoot duration ⁽⁵⁾ | -0.75 to 4.40 | V | | | |
| T_{STG} | Storage temperature (ambient) | | | | -65 to 150 | °C |
| T_{SOL} | Maximum soldering temperature ⁽⁶⁾ (TQG144, CPG196, CSG225, CSG324, CSG484, and FTG256) | | | | +260 | °C |
| | Maximum soldering temperature ⁽⁶⁾ (Pb-free packages: FGG484, FGG676, and FGG900) | | | | +250 | °C |
| | Maximum soldering temperature ⁽⁶⁾ (Pb packages: CS484, FT256, FG484, FG676, and FG900) | | | | +220 | °C |
| T_j | Maximum junction temperature ⁽⁶⁾ | | | | +125 | °C |

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- When programming eFUSE, $V_{FS} \leq V_{CCAUX}$. Requires up to 40 mA current. For read mode, V_{FS} can be between GND and 3.45 V.
- I/O absolute maximum limit applied to DC and AC signals. Overshoot duration is the percentage of a data period that the I/O is stressed beyond 3.45V.
- For I/O operation, refer to [UG381](#): *Spartan-6 FPGA SelectIO Resources User Guide*.
- Maximum percent overshoot duration to meet 4.40V maximum.
- T_{SOL} is the maximum soldering temperature for component bodies. For soldering guidelines and thermal considerations, see [UG385](#): *Spartan-6 FPGA Packaging and Pinout Specification*.

Table 2: Recommended Operating Conditions⁽¹⁾

| Symbol | Description | | Min | Typ | Max | Units | |
|--------------------------------|--|-----------------------------------|---|-------|-----------------|-------|------------------|
| V_{CCINT} | Internal supply voltage relative to GND | -3, -3N, -2 | Standard performance ⁽²⁾ | 1.14 | 1.2 | 1.26 | V |
| | | -3, -2 | Extended performance ⁽²⁾ | 1.2 | 1.23 | 1.26 | V |
| | | -1L | Standard performance ⁽²⁾ | 0.95 | 1.0 | 1.05 | V |
| V_{CCAUX} ⁽³⁾⁽⁴⁾ | Auxiliary supply voltage relative to GND | $V_{CCAUX} = 2.5V$ ⁽⁵⁾ | | 2.375 | 2.5 | 2.625 | V |
| | | $V_{CCAUX} = 3.3V$ | | 3.15 | 3.3 | 3.45 | V |
| V_{CCO} ⁽⁶⁾⁽⁷⁾⁽⁸⁾ | Output supply voltage relative to GND | | 1.1 | – | 3.45 | V | |
| V_{IN} | Input voltage relative to GND | All I/O standards (except PCI) | Commercial temperature (C) | –0.5 | – | 4.0 | V |
| | | | Industrial temperature (I) | –0.5 | – | 3.95 | V |
| | | | Expanded (Q) temperature | –0.5 | – | 3.95 | V |
| | | PCI I/O standard ⁽⁹⁾ | –0.5 | – | $V_{CCO} + 0.5$ | V | |
| I_{IN} ⁽¹⁰⁾ | Maximum current through pin using PCI I/O standard when forward biasing the clamp diode. ⁽⁹⁾ | | Commercial (C) and Industrial temperature (I) | – | – | 10 | mA |
| | | | Expanded (Q) temperature | – | – | 7 | mA |
| | Maximum current through pin when forward biasing the ground clamp diode. | | | – | – | 10 | mA |
| V_{BATT} ⁽¹¹⁾ | Battery voltage relative to GND, $T_j = 0^\circ\text{C}$ to $+85^\circ\text{C}$ (LX75, LX75T, LX100, LX100T, LX150, and LX150T only) | | 1.0 | – | 3.6 | V | |
| T_j | Junction temperature operating range | Commercial (C) range | | 0 | – | 85 | $^\circ\text{C}$ |
| | | Industrial temperature (I) range | | –40 | – | 100 | $^\circ\text{C}$ |
| | | Expanded (Q) temperature range | | –40 | – | 125 | $^\circ\text{C}$ |

Notes:

- All voltages are relative to ground.
- See *Interface Performances for Memory Interfaces* in Table 25. The extended performance range is specified for designs not using the standard V_{CCINT} voltage range. The standard V_{CCINT} voltage range is used for:
 - Designs that do not use an MCB
 - LX4 devices
 - Devices in the TQG144 or CPG196 packages
 - Devices with the -3N speed grade
- Recommended maximum voltage droop for V_{CCAUX} is 10 mV/ms.
- During configuration, if V_{CCO_2} is 1.8V, then V_{CCAUX} must be 2.5V.
- The -1L devices require $V_{CCAUX} = 2.5V$ when using the LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, RSDS_25, RSDS_33, PPDS_25, and PPDS_33 I/O standards on inputs. LVPECL_33 is not supported in the -1L devices.
- Configuration data is retained even if V_{CCO} drops to 0V.
- Includes V_{CCO} of 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
- For PCI systems, the transmitter and receiver should have common supplies for V_{CCO} .
- Devices with a -1L speed grade do not support Xilinx PCI IP.
- Do not exceed a total of 100 mA per bank.
- V_{BATT} is required to maintain the battery backed RAM (BBR) AES key when V_{CCAUX} is not applied. Once V_{CCAUX} is applied, V_{BATT} can be unconnected. When BBR is not used, Xilinx recommends connecting to V_{CCAUX} or GND. However, V_{BATT} can be unconnected.

Table 3: eFUSE Programming Conditions⁽¹⁾

| Symbol | Description | Min | Typ | Max | Units |
|------------------|--|------|------|------|--------------------|
| $V_{FS}^{(2)}$ | External voltage supply | 3.2 | 3.3 | 3.4 | V |
| I_{FS} | V_{FS} supply current | – | – | 40 | mA |
| V_{CCAUX} | Auxiliary supply voltage relative to GND | 3.2 | 3.3 | 3.45 | V |
| $R_{FUSE}^{(3)}$ | External resistor from R_{FUSE} pin to GND | 1129 | 1140 | 1151 | Ω |
| V_{CCINT} | Internal supply voltage relative to GND | 1.14 | 1.2 | 1.26 | V |
| t_j | Temperature range | 15 | – | 85 | $^{\circ}\text{C}$ |

Notes:

1. These specifications apply during programming of the eFUSE AES key. Programming is only supported through JTAG. The AES key is only supported in the following devices: LX75, LX75T, LX100, LX100T, LX150, and LX150T.
2. When programming eFUSE, V_{FS} must be less than or equal to V_{CCAUX} . When not programming or when eFUSE is not used, Xilinx recommends connecting V_{FS} to GND. However, V_{FS} can be between GND and 3.45 V.
3. An R_{FUSE} resistor is required when programming the eFUSE AES key. When not programming or when eFUSE is not used, Xilinx recommends connecting the R_{FUSE} pin to V_{CCAUX} or GND. However, R_{FUSE} can be unconnected.

Table 4: DC Characteristics Over Recommended Operating Conditions

| Symbol | Description | Min | Typ | Max | Units | |
|----------------------|--|---|---------------------------------|-----|----------|---------|
| V_{DRINT} | Data retention V_{CCINT} voltage (below which configuration data might be lost) | 0.8 | – | – | V | |
| V_{DRAUX} | Data retention V_{CCAUX} voltage (below which configuration data might be lost) | 2.0 | – | – | V | |
| I_{REF} | V_{REF} leakage current per pin for commercial (C) and industrial (I) devices | –10 | – | 10 | μ A | |
| | V_{REF} leakage current per pin for expanded (Q) devices | –15 | – | 15 | μ A | |
| I_L | Input or output leakage current per pin (sample-tested) for commercial (C) and industrial (I) devices | –10 | – | 10 | μ A | |
| | Input or output leakage current per pin (sample-tested) for expanded (Q) devices | –15 | – | 15 | μ A | |
| I_{HS} | Leakage current on pins during hot socketing with FPGA unpowered | All pins except PROGRAM_B, DONE, and JTAG pins when HSWAPEN = 1 | –20 | – | 20 | μ A |
| | | PROGRAM_B, DONE, and JTAG pins, or other pins when HSWAPEN = 0 | $I_{HS(HSWAPEN = 1)} + I_{RPU}$ | | μ A | |
| $C_{IN}^{(1)}$ | Die input capacitance at the pad | – | – | 10 | pF | |
| I_{RPU} | Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 3.3V$ or $V_{CCAUX} = 3.3V$ | 200 | – | 500 | μ A | |
| | Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 2.5V$ or $V_{CCAUX} = 2.5V$ | 120 | – | 350 | μ A | |
| | Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.8V$ | 60 | – | 200 | μ A | |
| | Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.5V$ | 40 | – | 150 | μ A | |
| | Pad pull-up (when selected) @ $V_{IN} = 0V$, $V_{CCO} = 1.2V$ | 12 | – | 100 | μ A | |
| I_{RPD} | Pad pull-down (when selected) @ $V_{IN} = V_{CCO}$, $V_{CCAUX} = 3.3V$ | 200 | – | 550 | μ A | |
| | Pad pull-down (when selected) @ $V_{IN} = V_{CCO}$, $V_{CCAUX} = 2.5V$ | 140 | – | 400 | μ A | |
| $I_{BATT}^{(2)}$ | Battery supply current | – | – | 150 | nA | |
| $R_{DT}^{(3)}$ | Resistance of optional input differential termination circuit, $V_{CCAUX} = 3.3V$ | – | 100 | – | Ω | |
| $R_{IN_TERM}^{(5)}$ | Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_25) for commercial (C) and industrial (I) devices | 23 | 25 | 55 | Ω | |
| | Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_25) for expanded (Q) devices | 20 | 25 | 55 | Ω | |
| | Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_50) for commercial (C) and industrial (I) devices | 39 | 50 | 72 | Ω | |
| | Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_50) for expanded (Q) devices | 32 | 50 | 74 | Ω | |
| | Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_75) for commercial (C) and industrial (I) devices | 56 | 75 | 109 | Ω | |
| | Thevenin equivalent resistance of programmable input termination to V_{CCO} (UNTUNED_SPLIT_75) for expanded (Q) devices | 47 | 75 | 115 | Ω | |
| R_{OUT_TERM} | Thevenin equivalent resistance of programmable output termination (UNTUNED_25) | 11 | 25 | 52 | Ω | |
| | Thevenin equivalent resistance of programmable output termination (UNTUNED_50) | 21 | 50 | 96 | Ω | |
| | Thevenin equivalent resistance of programmable output termination (UNTUNED_75) | 29 | 75 | 145 | Ω | |

Notes:

1. The C_{IN} measurement represents the die capacitance at the pad, not including the package.
2. Maximum value specified for worst case process at 25°C. LX75, LX75T, LX100, LX100T, LX150, and LX150T only.
3. Refer to IBIS models for R_{DT} variation and for values at $V_{CCAUX} = 2.5V$. IBIS values for R_{DT} are valid for all temperature ranges.
4. V_{CCO2} is not required for data retention. The minimum V_{CCO2} for power-on reset and configuration is 1.65V.
5. Termination resistance to a $V_{CCO}/2$ level.

Quiescent Current

Typical values for quiescent supply current are specified at nominal voltage, 25°C junction temperatures (T_j). Quiescent supply current is specified by speed grade for Spartan-6 devices. Xilinx recommends analyzing static power consumption using the Xilinx Power Estimator (XPE) tool (download at <http://www.xilinx.com/power>) for conditions other than those specified in Table 5.

Table 5: Typical Quiescent Supply Current

| Symbol | Description | Device | Speed Grade | | | | Units |
|---------------------|---|--------|-------------|------|------|------|-------|
| | | | -3 | -3N | -2 | -1L | |
| I _{CCINTQ} | Quiescent V _{CCINT} supply current | LX4 | 4.0 | 4.0 | 4.0 | 2.4 | mA |
| | | LX9 | 4.0 | 4.0 | 4.0 | 2.4 | mA |
| | | LX16 | 6.0 | 6.0 | 6.0 | 4.0 | mA |
| | | LX25 | 11.0 | 11.0 | 11.0 | 6.6 | mA |
| | | LX25T | 11.0 | 11.0 | 11.0 | N/A | mA |
| | | LX45 | 15.0 | 15.0 | 15.0 | 9.0 | mA |
| | | LX45T | 15.0 | 15.0 | 15.0 | N/A | mA |
| | | LX75 | 29.0 | 29.0 | 29.0 | 17.4 | mA |
| | | LX75T | 29.0 | 29.0 | 29.0 | N/A | mA |
| | | LX100 | 36.0 | 36.0 | 36.0 | 21.6 | mA |
| | | LX100T | 36.0 | 36.0 | 36.0 | N/A | mA |
| | | LX150 | 51.0 | 51.0 | 51.0 | 31.0 | mA |
| | | LX150T | 51.0 | 51.0 | 51.0 | N/A | mA |
| I _{CCOQ} | Quiescent V _{CCO} supply current | LX4 | 1.0 | 1.0 | 1.0 | 1.0 | mA |
| | | LX9 | 1.0 | 1.0 | 1.0 | 1.0 | mA |
| | | LX16 | 2.0 | 2.0 | 2.0 | 2.0 | mA |
| | | LX25 | 2.0 | 2.0 | 2.0 | 2.0 | mA |
| | | LX25T | 2.0 | 2.0 | 2.0 | N/A | mA |
| | | LX45 | 3.0 | 3.0 | 3.0 | 3.0 | mA |
| | | LX45T | 3.0 | 3.0 | 3.0 | N/A | mA |
| | | LX75 | 4.0 | 4.0 | 4.0 | 4.0 | mA |
| | | LX75T | 4.0 | 4.0 | 4.0 | N/A | mA |
| | | LX100 | 5.0 | 5.0 | 5.0 | 5.0 | mA |
| | | LX100T | 5.0 | 5.0 | 5.0 | N/A | mA |
| | | LX150 | 7.0 | 7.0 | 7.0 | 7.0 | mA |
| | | LX150T | 7.0 | 7.0 | 7.0 | N/A | mA |

Table 5: Typical Quiescent Supply Current (Cont'd)

| Symbol | Description | Device | Speed Grade | | | | Units |
|---------------------|---|--------|-------------|------|------|------|-------|
| | | | -3 | -3N | -2 | -1L | |
| I _{CCAUXQ} | Quiescent V _{CCAUX} supply current | LX4 | 2.5 | 2.5 | 2.5 | 2.5 | mA |
| | | LX9 | 2.5 | 2.5 | 2.5 | 2.5 | mA |
| | | LX16 | 3.0 | 3.0 | 3.0 | 3.0 | mA |
| | | LX25 | 4.0 | 4.0 | 4.0 | 4.0 | mA |
| | | LX25T | 4.0 | 4.0 | 4.0 | N/A | mA |
| | | LX45 | 5.0 | 5.0 | 5.0 | 5.0 | mA |
| | | LX45T | 5.0 | 5.0 | 5.0 | N/A | mA |
| | | LX75 | 7.0 | 7.0 | 7.0 | 7.0 | mA |
| | | LX75T | 7.0 | 7.0 | 7.0 | N/A | mA |
| | | LX100 | 9.0 | 9.0 | 9.0 | 9.0 | mA |
| | | LX100T | 9.0 | 9.0 | 9.0 | N/A | mA |
| | | LX150 | 12.0 | 12.0 | 12.0 | 12.0 | mA |
| | | LX150T | 12.0 | 12.0 | 12.0 | N/A | mA |

Notes:

1. Typical values are specified at nominal voltage, 25°C junction temperatures (T_j). Industrial (I) grade devices have the same typical values as commercial (C) grade devices at 25°C, but higher values at 100°C. Use the XPE tool to calculate 100°C values. Nominal V_{CCINT} is 1.20V; use the XPE tool to calculate 1.23V values for the nominal V_{CCINT} of the extended performance range.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. If differential signaling is used, more accurate quiescent current estimates can be obtained by using the Xilinx Power Estimator (XPE) or Xilinx Power Analyzer (XPA) tools.

Table 6: Power Supply Ramp Time

| Symbol | Description | Speed Grade | Ramp Time | Units |
|----------------------------------|--|-------------|--------------|-------|
| V _{CCINTR} | Internal supply voltage ramp time | -3, -3N, -2 | 0.20 to 50.0 | ms |
| | | -1L | 0.20 to 40.0 | ms |
| V _{CCO2} ⁽¹⁾ | Output drivers bank 2 supply voltage ramp time | All | 0.20 to 50.0 | ms |
| V _{CCAUXR} | Auxiliary supply voltage ramp time | All | 0.20 to 50.0 | ms |

Notes:

1. The minimum V_{CCO2} for power-on reset and configuration is 1.65V.
2. Spartan-6 FPGAs require a certain amount of supply current during power-on to insure proper device initialization. The actual current consumed depends on the power-on ramp rate of the power supply. Use the Xilinx Power Estimator (XPE) or Xilinx Power Analyzer (XPA) tools to estimate current drain on these supplies. Spartan-6 devices do not have a required power-on sequence.

SelectIO™ Interface DC Input and Output Levels

Table 7: Recommended Operating Conditions for User I/Os Using Single-Ended Standards

| I/O Standard | V _{CCO} for Drivers ⁽¹⁾ | | | V _{REF} for Inputs | | |
|------------------------|---|--------|--------|--|--------|--------|
| | V, Min | V, Nom | V, Max | V, Min | V, Nom | V, Max |
| LVTTTL | 3.0 | 3.3 | 3.45 | V _{REF} is not used for these I/O standards | | |
| LVC MOS33 | 3.0 | 3.3 | 3.45 | | | |
| LVC MOS25 | 2.3 | 2.5 | 2.7 | | | |
| LVC MOS18 | 1.65 | 1.8 | 1.95 | | | |
| LVC MOS18_JEDEC | 1.65 | 1.8 | 1.95 | | | |
| LVC MOS15 | 1.4 | 1.5 | 1.6 | | | |
| LVC MOS15_JEDEC | 1.4 | 1.5 | 1.6 | | | |
| LVC MOS12 | 1.1 | 1.2 | 1.3 | | | |
| LVC MOS12_JEDEC | 1.1 | 1.2 | 1.3 | | | |
| PCI33_3 ⁽²⁾ | 3.0 | 3.3 | 3.45 | | | |
| PCI66_3 ⁽²⁾ | 3.0 | 3.3 | 3.45 | | | |
| I2C | 2.7 | 3.0 | 3.45 | | | |
| SMBUS | 2.7 | 3.0 | 3.45 | | | |
| SDIO | 3.0 | 3.3 | 3.45 | | | |
| MOBILE_DDR | 1.7 | 1.8 | 1.9 | | | |
| HSTL_I | 1.4 | 1.5 | 1.6 | 0.68 | 0.75 | 0.9 |
| HSTL_II | 1.4 | 1.5 | 1.6 | 0.68 | 0.75 | 0.9 |
| HSTL_III | 1.4 | 1.5 | 1.6 | – | 0.9 | – |
| HSTL_I_18 | 1.7 | 1.8 | 1.9 | 0.8 | 0.9 | 1.1 |
| HSTL_II_18 | 1.7 | 1.8 | 1.9 | – | 0.9 | – |
| HSTL_III_18 | 1.7 | 1.8 | 1.9 | – | 1.1 | – |
| SSTL3_I | 3.0 | 3.3 | 3.45 | 1.3 | 1.5 | 1.7 |
| SSTL3_II | 3.0 | 3.3 | 3.45 | 1.3 | 1.5 | 1.7 |
| SSTL2_I | 2.3 | 2.5 | 2.7 | 1.13 | 1.25 | 1.38 |
| SSTL2_II | 2.3 | 2.5 | 2.7 | 1.13 | 1.25 | 1.38 |
| SSTL18_I | 1.7 | 1.8 | 1.9 | 0.833 | 0.9 | 0.969 |
| SSTL18_II | 1.7 | 1.8 | 1.9 | 0.833 | 0.9 | 0.969 |
| SSTL15_II | 1.425 | 1.5 | 1.575 | 0.69 | 0.75 | 0.81 |

Notes:

1. V_{CCO} range required when using I/O standard for an output. Also required for MOBILE_DDR, PCI33_3, LVC MOS18_JEDEC, LVC MOS15_JEDEC, and LVC MOS12_JEDEC inputs, and for LVC MOS25 inputs when V_{CCAUX} = 3.3V.
2. For PCI systems, the transmitter and receiver should have common supplies for V_{CCO}.

Table 8: Recommended Operating Conditions for User I/Os Using Differential Signal Standards

| I/O Standard | V _{CCO} for Drivers | | |
|--------------------------|------------------------------|--------|--------|
| | V, Min | V, Nom | V, Max |
| LVDS_33 | 3.0 | 3.3 | 3.45 |
| LVDS_25 | 2.25 | 2.5 | 2.75 |
| BLVDS_25 | 2.25 | 2.5 | 2.75 |
| MINI_LVDS_33 | 3.0 | 3.3 | 3.45 |
| MINI_LVDS_25 | 2.25 | 2.5 | 2.75 |
| LVPECL_33 ⁽¹⁾ | N/A—Inputs Only | | |
| LVPECL_25 | N/A—Inputs Only | | |
| RSDS_33 | 3.0 | 3.3 | 3.45 |
| RSDS_25 | 2.25 | 2.5 | 2.75 |
| TMDS_33 ⁽¹⁾ | 3.14 | 3.3 | 3.45 |
| PPDS_33 | 3.0 | 3.3 | 3.45 |
| PPDS_25 | 2.25 | 2.5 | 2.75 |
| DISPLAY_PORT | 2.3 | 2.5 | 2.7 |
| DIFF_MOBILE_DDR | 1.7 | 1.8 | 1.9 |
| DIFF_HSTL_I | 1.4 | 1.5 | 1.6 |
| DIFF_HSTL_II | 1.4 | 1.5 | 1.6 |
| DIFF_HSTL_III | 1.4 | 1.5 | 1.6 |
| DIFF_HSTL_I_18 | 1.7 | 1.8 | 1.9 |
| DIFF_HSTL_II_18 | 1.7 | 1.8 | 1.9 |
| DIFF_HSTL_III_18 | 1.7 | 1.8 | 1.9 |
| DIFF_SSTL3_I | 3.0 | 3.3 | 3.45 |
| DIFF_SSTL3_II | 3.0 | 3.3 | 3.45 |
| DIFF_SSTL2_I | 2.3 | 2.5 | 2.7 |
| DIFF_SSTL2_II | 2.3 | 2.5 | 2.7 |
| DIFF_SSTL18_I | 1.7 | 1.8 | 1.9 |
| DIFF_SSTL18_II | 1.7 | 1.8 | 1.9 |
| DIFF_SSTL15_II | 1.425 | 1.5 | 1.575 |

Notes:

1. LVPECL_33 and TMDS_33 inputs require V_{CCAUX} = 3.3V nominal.

In Table 9 and Table 10, values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Table 9: Single-Ended I/O Standard DC Input and Output Levels

| I/O Standard | V_{IL} | | V_{IH} | | V_{OL} | V_{OH} | I_{OL} | I_{OH} |
|-----------------|----------|-------------------|-------------------|-----------------|-----------------|------------------|----------|----------|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| LVTTTL | -0.5 | 0.8 | 2.0 | 4.1 | 0.4 | 2.4 | Note 2 | Note 2 |
| LVC MOS33 | -0.5 | 0.8 | 2.0 | 4.1 | 0.4 | $V_{CCO} - 0.4$ | Note 2 | Note 2 |
| LVC MOS25 | -0.5 | 0.7 | 1.7 | 4.1 | 0.4 | $V_{CCO} - 0.4$ | Note 2 | Note 2 |
| LVC MOS18 | -0.5 | 0.38 | 0.8 | 4.1 | 0.45 | $V_{CCO} - 0.45$ | Note 2 | Note 2 |
| LVC MOS18 (-1L) | -0.5 | 0.33 | 0.71 | 4.1 | 0.45 | $V_{CCO} - 0.45$ | Note 2 | Note 2 |
| LVC MOS18 JEDEC | -0.5 | 35% V_{CCO} | 65% V_{CCO} | 4.1 | 0.45 | $V_{CCO} - 0.45$ | Note 2 | Note 2 |
| LVC MOS15 | -0.5 | 0.38 | 0.8 | 4.1 | 25% V_{CCO} | 75% V_{CCO} | Note 3 | Note 3 |
| LVC MOS15 (-1L) | -0.5 | 0.33 | 0.71 | 4.1 | 25% V_{CCO} | 75% V_{CCO} | Note 3 | Note 3 |
| LVC MOS15 JEDEC | -0.5 | 35% V_{CCO} | 65% V_{CCO} | 4.1 | 25% V_{CCO} | 75% V_{CCO} | Note 3 | Note 3 |
| LVC MOS12 | -0.5 | 0.38 | 0.8 | 4.1 | 0.4 | $V_{CCO} - 0.4$ | Note 4 | Note 4 |
| LVC MOS12 (-1L) | -0.5 | 0.33 | 0.71 | 4.1 | 0.4 | $V_{CCO} - 0.4$ | Note 4 | Note 4 |
| LVC MOS12 JEDEC | -0.5 | 35% V_{CCO} | 65% V_{CCO} | 4.1 | 0.4 | $V_{CCO} - 0.4$ | Note 4 | Note 4 |
| PCI33_3 | -0.5 | 30% V_{CCO} | 50% V_{CCO} | $V_{CCO} + 0.5$ | 10% V_{CCO} | 90% V_{CCO} | 1.5 | -0.5 |
| PCI66_3 | -0.5 | 30% V_{CCO} | 50% V_{CCO} | $V_{CCO} + 0.5$ | 10% V_{CCO} | 90% V_{CCO} | 1.5 | -0.5 |
| I2C | -0.5 | 25% V_{CCO} | 70% V_{CCO} | 4.1 | 20% V_{CCO} | - | 3 | - |
| SMBUS | -0.5 | 0.8 | 2.1 | 4.1 | 0.4 | - | 4 | - |
| SDIO | -0.5 | 12.5% V_{CCO} | 75% V_{CCO} | 4.1 | 12.5% V_{CCO} | 75% V_{CCO} | 0.1 | -0.1 |
| MOBILE_DDR | -0.5 | 20% V_{CCO} | 80% V_{CCO} | 4.1 | 10% V_{CCO} | 90% V_{CCO} | 0.1 | -0.1 |
| HSTL_I | -0.5 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | 4.1 | 0.4 | $V_{CCO} - 0.4$ | 8 | -8 |
| HSTL_II | -0.5 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | 4.1 | 0.4 | $V_{CCO} - 0.4$ | 16 | -16 |
| HSTL_III | -0.5 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | 4.1 | 0.4 | $V_{CCO} - 0.4$ | 24 | -8 |
| HSTL_I_18 | -0.5 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | 4.1 | 0.4 | $V_{CCO} - 0.4$ | 11 | -11 |
| HSTL_II_18 | -0.5 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | 4.1 | 0.4 | $V_{CCO} - 0.4$ | 22 | -22 |
| HSTL_III_18 | -0.5 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | 4.1 | 0.4 | $V_{CCO} - 0.4$ | 30 | -11 |
| SSTL3_I | -0.5 | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 4.1 | $V_{TT} - 0.6$ | $V_{TT} + 0.6$ | 8 | -8 |
| SSTL3_II | -0.5 | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 4.1 | $V_{TT} - 0.8$ | $V_{TT} + 0.8$ | 16 | -16 |
| SSTL2_I | -0.5 | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | 4.1 | $V_{TT} - 0.61$ | $V_{TT} + 0.61$ | 8.1 | -8.1 |
| SSTL2_II | -0.5 | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | 4.1 | $V_{TT} - 0.81$ | $V_{TT} + 0.81$ | 16.2 | -16.2 |
| SSTL18_I | -0.5 | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | 4.1 | $V_{TT} - 0.47$ | $V_{TT} + 0.47$ | 6.7 | -6.7 |
| SSTL18_II | -0.5 | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | 4.1 | $V_{TT} - 0.60$ | $V_{TT} + 0.60$ | 13.4 | -13.4 |
| SSTL15_II | -0.5 | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | 4.1 | $V_{TT} - 0.4$ | $V_{TT} + 0.4$ | 13.4 | -13.4 |

Notes:

1. Tested according to relevant specifications.
2. Using drive strengths of 2, 4, 6, 8, 12, 16, or 24 mA.
3. Using drive strengths of 2, 4, 6, 8, 12, or 16 mA.
4. Using drive strengths of 2, 4, 6, 8, or 12 mA.
5. For more information, refer to [UG381](#): *Spartan-6 FPGA SelectIO Resources User Guide*.

Table 10: Differential I/O Standard DC Input and Output Levels

| I/O Standard | V _{ID} | | V _{ICM} | | V _{OD} | | V _{OCM} | | V _{OH} | V _{OL} |
|-----------------------------|-----------------|---------|------------------|---------------------|-----------------|---------|------------------------------|--------------------------|------------------------|------------------------|
| | mV, Min | mV, Max | V, Min | V, Max | mV, Min | mV, Max | V, Min | V, Max | V, Min | V, Max |
| LVDS_33 ⁽²⁾⁽³⁾ | 100 | 600 | 0.3 | 2.35 | 247 | 454 | 1.125 | 1.375 | – | – |
| LVDS_25 ⁽²⁾⁽³⁾ | 100 | 600 | 0.3 | 2.35 | 247 | 454 | 1.125 | 1.375 | – | – |
| BLVDS_25 ⁽²⁾⁽³⁾ | 100 | – | 0.3 | 2.35 | 240 | 460 | Typical 50% V _{CCO} | | – | – |
| MINI_LVDS_33 | 200 | 600 | 0.3 | 1.95 | 300 | 600 | 1.0 | 1.4 | – | – |
| MINI_LVDS_25 | 200 | 600 | 0.3 | 1.95 | 300 | 600 | 1.0 | 1.4 | – | – |
| LVPECL_33 ⁽²⁾⁽³⁾ | 100 | 1000 | 0.3 | 2.8 ⁽¹⁾ | Inputs only | | | | | |
| LVPECL_25 ⁽²⁾⁽³⁾ | 100 | 1000 | 0.3 | 1.95 | Inputs only | | | | | |
| RSDS_33 ⁽²⁾⁽³⁾ | 100 | – | 0.3 | 1.5 | 100 | 400 | 1.0 | 1.4 | – | – |
| RSDS_25 ⁽²⁾⁽³⁾ | 100 | – | 0.3 | 1.5 | 100 | 400 | 1.0 | 1.4 | – | – |
| TMDS_33 | 150 | 1200 | 2.7 | 3.23 ⁽¹⁾ | 400 | 800 | V _{CCO} – 0.405 | V _{CCO} – 0.190 | – | – |
| PPDS_33 ⁽²⁾⁽³⁾ | 100 | 400 | 0.2 | 2.3 | 100 | 400 | 0.5 | 1.4 | – | – |
| PPDS_25 ⁽²⁾⁽³⁾ | 100 | 400 | 0.2 | 2.3 | 100 | 400 | 0.5 | 1.4 | – | – |
| DISPLAY_PORT | 190 | 1260 | 0.3 | 2.35 | – | – | Typical 50% V _{CCO} | | – | – |
| DIFF_MOBILE_DDR | 100 | – | 0.78 | 1.02 | – | – | – | – | 90% V _{CCO} | 10% V _{CCO} |
| DIFF_HSTL_I | 100 | – | 0.68 | 0.9 | – | – | – | – | V _{CCO} – 0.4 | 0.4 |
| DIFF_HSTL_II | 100 | – | 0.68 | 0.9 | – | – | – | – | V _{CCO} – 0.4 | 0.4 |
| DIFF_HSTL_III | 100 | – | 0.68 | 0.9 | – | – | – | – | V _{CCO} – 0.4 | 0.4 |
| DIFF_HSTL_I_18 | 100 | – | 0.8 | 1.1 | – | – | – | – | V _{CCO} – 0.4 | 0.4 |
| DIFF_HSTL_II_18 | 100 | – | 0.8 | 1.1 | – | – | – | – | V _{CCO} – 0.4 | 0.4 |
| DIFF_HSTL_III_18 | 100 | – | 0.8 | 1.1 | – | – | – | – | V _{CCO} – 0.4 | 0.4 |
| DIFF_SSTL3_I | 100 | – | 1.0 | 1.9 | – | – | – | – | V _{TT} + 0.6 | V _{TT} – 0.6 |
| DIFF_SSTL3_II | 100 | – | 1.0 | 1.9 | – | – | – | – | V _{TT} + 0.8 | V _{TT} – 0.8 |
| DIFF_SSTL2_I | 100 | – | 1.0 | 1.5 | – | – | – | – | V _{TT} + 0.61 | V _{TT} – 0.61 |
| DIFF_SSTL2_II | 100 | – | 1.0 | 1.5 | – | – | – | – | V _{TT} + 0.81 | V _{TT} – 0.81 |
| DIFF_SSTL18_I | 100 | – | 0.7 | 1.1 | – | – | – | – | V _{TT} + 0.47 | V _{TT} – 0.47 |
| DIFF_SSTL18_II | 100 | – | 0.7 | 1.1 | – | – | – | – | V _{TT} + 0.6 | V _{TT} – 0.6 |
| DIFF_SSTL15_II | 100 | – | 0.55 | 0.95 | – | – | – | – | V _{TT} + 0.4 | V _{TT} – 0.4 |

Notes:

1. LVPECL_33 and TMDS_33 maximum V_{ICM} is the lower of V (maximum) or V_{CCAUX} – (V_{ID}/2)
2. When V_{CCAUX} = 3.3V, the DCD can be higher than 5% for V_{ICM} < 0.7V when using these I/O standards: LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, LVPECL_33, RSDS_25, RSDS_33, PPDS_25, and PPDS_33.
3. The -1L devices require V_{CCAUX} = 2.5V when using the LVDS_25, LVDS_33, BLVDS_25, LVPECL_25, RSDS_25, RSDS_33, PPDS_25, and PPDS_33 I/O standards on inputs. LVPECL_33 is not supported in the -1L devices.

eFUSE Read Endurance

Table 11 lists the minimum guaranteed number of read cycle operations for Device DNA and for the AES eFUSE key. For more information, see [UG380: Spartan-6 FPGA Configuration User Guide](#).

Table 11: eFUSE Read Endurance

| Symbol | Description | Speed Grade | | | | Units (Min) |
|------------|---|-------------|-----|----|-----|-------------|
| | | -3 | -3N | -2 | -1L | |
| DNA_CYCLES | Number of DNA_PORT READ operations or JTAG ISC_DNA read command operations. Unaffected by SHIFT operations. | 30,000,000 | | | | Read Cycles |
| AES_CYCLES | Number of JTAG FUSE_KEY or FUSE_CNTL read command operations. Unaffected by SHIFT operations. | 30,000,000 | | | | Read Cycles |

GTP Transceiver Specifications

GTP transceivers are available in the Spartan-6 LXT devices. See [DS160: Spartan-6 Family Overview](#) for more information.

GTP Transceiver DC Characteristics

Table 12: Absolute Maximum Ratings for GTP Transceivers⁽¹⁾

| Symbol | Description | Min | Max | Units |
|------------------------|--|------|------|-------|
| MGTAVCC | Analog supply voltage for the GTP transmitter and receiver circuits relative to GND | -0.5 | 1.32 | V |
| MGTAVTTTX | Analog supply voltage for the GTP transmitter termination circuit relative to GND | -0.5 | 1.32 | V |
| MGTAVTTRX | Analog supply voltage for the GTP receiver termination circuit relative to GND | -0.5 | 1.32 | V |
| MGTAVCCPLL | Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND | -0.5 | 1.32 | V |
| MGTAVTTRCAL | Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom) | -0.5 | 1.32 | V |
| V _{IN} | Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage | -0.5 | 1.32 | V |
| V _{MGTREFCLK} | Reference clock absolute input voltage | -0.5 | 1.32 | V |

Notes:

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Table 13: Recommended Operating Conditions for GTP Transceivers⁽¹⁾⁽²⁾⁽³⁾

| Symbol | Description | Min | Typ | Max | Units |
|-------------|--|------|------|------|-------|
| MGTAVCC | Analog supply voltage for the GTP transmitter and receiver circuits relative to GND | 1.14 | 1.20 | 1.26 | V |
| MGTAVTTTX | Analog supply voltage for the GTP transmitter termination circuit relative to GND | 1.14 | 1.20 | 1.26 | V |
| MGTAVTTRX | Analog supply voltage for the GTP receiver termination circuit relative to GND | 1.14 | 1.20 | 1.26 | V |
| MGTAVCCPLL | Analog supply voltage for the GTP transmitter and receiver PLL circuits relative to GND | 1.14 | 1.20 | 1.26 | V |
| MGTAVTTRCAL | Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank (top or bottom) | 1.14 | 1.20 | 1.26 | V |

Notes:

- Each voltage listed requires the filter circuit described in [UG386: Spartan-6 FPGA GTP Transceivers User Guide](#).
- Voltages are specified for the temperature range of T_j = -40°C to +125°C.
- The voltage level of MGTAVCCPLL must not exceed the voltage level of MGTAVCC +10mV. The voltage level of MGTAVCC must not exceed the voltage level of MGTAVCCPLL.

Table 14: GTP Transceiver Current Supply (per Lane)

| Symbol | Description | Typ ⁽¹⁾ | Max | Units |
|-------------------------|---|--------------------|---------------------|-------|
| I _{MGTAVCC} | GTP transceiver internal analog supply current | 40.4 | Note 2 | mA |
| I _{MGTAVTTTX} | GTP transmitter termination supply current | 27.4 | | mA |
| I _{MGTAVTTRX} | GTP receiver termination supply current | 13.6 | | mA |
| I _{MGTAVCCPLL} | GTP transmitter and receiver PLL supply current | 28.7 | | mA |
| R _{MGTRREF} | Precision reference resistor for internal calibration termination | | 50.0 ± 1% tolerance | Ω |

Notes:

1. Typical values are specified at nominal voltage, 25°C, with a 2.5 Gb/s line rate, with a shared PLL use mode.
2. Values for currents of other transceiver configurations and conditions can be obtained by using the Xilinx Power Estimator (XPE) or Xilinx Power Analyzer (XPA) tools.

Table 15: GTP Transceiver Quiescent Supply Current (per Lane)⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

| Symbol | Description | Typ ⁽⁵⁾ | Max | Units |
|--------------------------|-------------------------------------|--------------------|--------|-------|
| I _{MGTAVCCQ} | Quiescent MGTAVCC supply current | 1.7 | Note 2 | mA |
| I _{MGTAVTTTXQ} | Quiescent MGTAVTTTX supply current | 0.1 | | mA |
| I _{MGTAVTTRXQ} | Quiescent MGTAVTTRX supply current | 1.2 | | mA |
| I _{MGTAVCCPLLQ} | Quiescent MGTAVCCPLL supply current | 1.0 | | mA |

Notes:

1. Device powered and unconfigured.
2. Currents for conditions other than values specified in this table can be obtained by using the Xilinx Power Estimator (XPE) or Xilinx Power Analyzer (XPA) tools.
3. GTP transceiver quiescent supply current for an entire device can be calculated by multiplying the values in this table by the number of available GTP transceivers.
4. Does not include power-up MGTAVTTRCAL supply current during device configuration.
5. Typical values are specified at nominal voltage, 25°C.

GTP Transceiver DC Input and Output Levels

Table 16 summarizes the DC output specifications of the GTP transceivers in Spartan-6 FPGAs. Figure 1 shows the single-ended output voltage swing. Figure 2 shows the peak-to-peak differential output voltage.

Consult UG386: *Spartan-6 FPGA GTP Transceivers User Guide* for further details.

Table 16: GTP Transceiver DC Specifications

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|----------------------|---|--|-----------------------------------|------------------|-----------|-------|
| DV _{PPIN} | Differential peak-to-peak input voltage | External AC coupled | 140 | – | 2000 | mV |
| V _{IN} | Absolute input voltage | DC coupled MGTAVTTRX = 1.2V | –400 | – | MGTAVTTRX | mV |
| V _{CMIN} | Common mode input voltage | DC coupled MGTAVTTRX = 1.2V | – | 3/4 MGTAVTTRX | – | mV |
| DV _{PPOUT} | Differential peak-to-peak output voltage ⁽¹⁾ | Transmitter output swing is set to maximum setting | 1000 | – | – | mV |
| V _{SEOUT} | Single-ended output voltage swing ⁽¹⁾ | | – | – | 500 | mV |
| V _{CMOUTDC} | Common mode output voltage | Equation based | MGTAVTTTX – V _{SEOUT} /2 | | | mV |
| R _{IN} | Differential input resistance | | 80 | 100 | 130 | Ω |
| R _{OUT} | Differential output resistance | | 80 | 100 | 130 | Ω |
| T _{OSKEW} | Transmitter output skew | | – | – | 15 | ps |
| C _{EXT} | Recommended external AC coupling capacitor ⁽²⁾ | | 75 | 100 | 200 | nF |

Notes:

- The output swing and preemphasis levels are programmable using the attributes discussed in UG386: *Spartan-6 FPGA GTP Transceivers User Guide* and can result in values lower than reported in this table. DV_{PPOUT} is the minimum guaranteed value at the maximum setting. Refer to UG386: *Spartan-6 FPGA GTP Transceivers User Guide* for nominal values.
- Other values can be used as appropriate to conform to specific protocols and standards.



Figure 1: Single-Ended Peak-to-Peak Voltage



Figure 2: Differential Peak-to-Peak Voltage

Table 17 summarizes the DC specifications of the clock input of the GTP transceiver. Consult UG386: *Spartan-6 FPGA GTP Transceivers User Guide* for further details.

Table 17: GTP Transceiver Clock DC Input Level Specification

| Symbol | DC Parameter | Min | Typ | Max | Units |
|-------------|---|-----|-----|------|----------|
| V_{IDIFF} | Differential peak-to-peak input voltage | 200 | 800 | 2000 | mV |
| R_{IN} | Differential input resistance | 80 | 100 | 120 | Ω |
| C_{EXT} | Required external AC coupling capacitor | – | 100 | – | nF |

GTP Transceiver Switching Characteristics

Consult [UG386](#): *Spartan-6 FPGA GTP Transceivers User Guide* for further information.

Table 18: GTP Transceiver Performance

| Symbol | Description | Speed Grade | | | | Units |
|-----------------|---|--------------|--------------|--------------|-----|-------|
| | | -3 | -3N | -2 | -1L | |
| F_{GTPMAX} | Maximum GTP transceiver data rate | 3.2 | 3.2 | 2.7 | N/A | Gb/s |
| $F_{GTPRANGE1}$ | GTP transceiver data rate range when PLL_TXDIVSEL_OUT = 1 | 1.88 to 3.2 | 1.88 to 3.2 | 1.88 to 2.7 | N/A | Gb/s |
| $F_{GTPRANGE2}$ | GTP transceiver data rate range when PLL_TXDIVSEL_OUT = 2 | 0.94 to 1.62 | 0.94 to 1.62 | 0.94 to 1.62 | N/A | Gb/s |
| $F_{GTPRANGE3}$ | GTP transceiver data rate range when PLL_TXDIVSEL_OUT = 4 | 0.6 to 0.81 | 0.6 to 0.81 | 0.6 to 0.81 | N/A | Gb/s |
| $F_{GPLLMAX}$ | Maximum PLL frequency | 1.62 | 1.62 | 1.62 | N/A | GHz |
| $F_{GPLLMIN}$ | Minimum PLL frequency | 0.94 | 0.94 | 0.94 | N/A | GHz |

Table 19: GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|-----------------|--|-------------|-----|-----|-----|-------|
| | | -3 | -3N | -2 | -1L | |
| $F_{GTPDRPCLK}$ | GTP transceiver DCLK (DRP clock) maximum frequency | 125 | 125 | 100 | N/A | MHz |

Table 20: GTP Transceiver Reference Clock Switching Characteristics

| Symbol | Description | Conditions | All LXT Speed Grades | | | Units |
|-------------|---|--|----------------------|-----|-----|---------|
| | | | Min | Typ | Max | |
| F_{GCLK} | Reference clock frequency range | | 60 | – | 160 | MHz |
| T_{RCLK} | Reference clock rise time | 20% – 80% | – | 200 | – | ps |
| T_{FCLK} | Reference clock fall time | 80% – 20% | – | 200 | – | ps |
| T_{DCREF} | Reference clock duty cycle | Transceiver PLL only | 45 | 50 | 55 | % |
| T_{LOCK} | Clock recovery frequency acquisition time | Initial PLL lock | – | – | 1 | ms |
| T_{PHASE} | Clock recovery phase acquisition time | Lock to data after PLL has locked to the reference clock | – | – | 200 | μ s |



Figure 3: Reference Clock Timing Parameters

Table 21: GTP Transceiver User Clock Switching Characteristics⁽¹⁾

| Symbol | Description | Conditions | Speed Grade | | | | Units |
|--------------------|-----------------------------|------------------|-------------|--------|------|-----|-------|
| | | | -3 | -3N | -2 | -1L | |
| F _{TXOUT} | TXOUTCLK maximum frequency | | 320 | 320 | 270 | N/A | MHz |
| F _{RXREC} | RXRECCLK maximum frequency | | 320 | 320 | 270 | N/A | MHz |
| T _{RX} | RXUSRCLK maximum frequency | | 320 | 320 | 270 | N/A | MHz |
| T _{RX2} | RXUSRCLK2 maximum frequency | 1 byte interface | 156.25 | 156.25 | 125 | N/A | MHz |
| | | 2 byte interface | 160 | 160 | 125 | N/A | MHz |
| | | 4 byte interface | 80 | 80 | 67.5 | N/A | MHz |
| T _{TX} | TXUSRCLK maximum frequency | | 320 | 320 | 270 | N/A | MHz |
| T _{TX2} | TXUSRCLK2 maximum frequency | 1 byte interface | 156.25 | 156.25 | 125 | N/A | MHz |
| | | 2 byte interface | 160 | 160 | 125 | N/A | MHz |
| | | 4 byte interface | 80 | 80 | 67.5 | N/A | MHz |

Notes:

1. Clocking must be implemented as described in [UG386: Spartan-6 FPGA GTP Transceivers User Guide](#).

Table 22: GTP Transceiver Transmitter Switching Characteristics

| Symbol | Description | Condition | Min | Typ | Max | Units |
|------------------------------|-------------------------------------|------------|-----|-----|------|-------|
| T _{RTX} | TX Rise time | 20%–80% | – | 140 | – | ps |
| T _{FTX} | TX Fall time | 80%–20% | – | 120 | – | ps |
| T _{LLSKEW} | TX lane-to-lane skew ⁽¹⁾ | | – | – | 400 | ps |
| V _{TXOOBVDPP} | Electrical idle amplitude | | – | – | 20 | mV |
| T _{TXOOBTRANSITION} | Electrical idle transition time | | – | – | 50 | ns |
| T _{J3.125} | Total Jitter ⁽²⁾ | 3.125 Gb/s | – | – | 0.35 | UI |
| D _{J3.125} | Deterministic Jitter ⁽²⁾ | | – | – | 0.15 | UI |
| T _{J2.5} | Total Jitter ⁽²⁾ | 2.5 Gb/s | – | – | 0.33 | UI |
| D _{J2.5} | Deterministic Jitter ⁽²⁾ | | – | – | 0.15 | UI |
| T _{J1.62} | Total Jitter ⁽²⁾ | 1.62 Gb/s | – | – | 0.20 | UI |
| D _{J1.62} | Deterministic Jitter ⁽²⁾ | | – | – | 0.10 | UI |
| T _{J1.25} | Total Jitter ⁽²⁾ | 1.25 Gb/s | – | – | 0.20 | UI |
| D _{J1.25} | Deterministic Jitter ⁽²⁾ | | – | – | 0.10 | UI |
| T _{J614} | Total Jitter ⁽²⁾ | 614 Mb/s | – | – | 0.10 | UI |
| D _{J614} | Deterministic Jitter ⁽²⁾ | | – | – | 0.05 | UI |

Notes:

1. Using same REFCLK input with TXENPMAPHASEALIGN enabled for up to four consecutive GTP transceiver sites.
2. Using PLL_DIVSEL_FB = 2, INTDATAWIDTH = 1. These values are NOT intended for protocol specific compliance determinations.

Table 23: GTP Transceiver Receiver Switching Characteristics

| Symbol | Description | | Min | Typ | Max | Units | |
|---|---|--|----------------------|-------|------|-------|-----|
| T _{RXELECIDLE} | Time for RXELECIDLE to respond to loss or restoration of data | | – | 75 | – | ns | |
| R _{XOOBVDPP} | OOB detect threshold peak-to-peak | | 60 | – | 150 | mV | |
| R _{XSSST} | Receiver spread-spectrum tracking ⁽¹⁾ | Modulated @ 33 KHz | –5000 | – | 0 | ppm | |
| R _{XRL} | Run length (CID) | Internal AC capacitor bypassed | – | – | 150 | UI | |
| R _{XPPMTOL} | Data/REFCLK PPM offset tolerance | CDR 2 nd -order loop disabled | –200 | – | 200 | ppm | |
| | | CDR 2 nd -order loop enabled | PLL_RXDIVSEL_OUT = 1 | –2000 | – | 2000 | ppm |
| | | | PLL_RXDIVSEL_OUT = 2 | –2000 | – | 2000 | ppm |
| | | PLL_RXDIVSEL_OUT = 4 | –1000 | – | 1000 | ppm | |
| SJ Jitter Tolerance⁽²⁾ | | | | | | | |
| JT_SJ _{3.125} | Sinusoidal Jitter ⁽³⁾ | 3.125 Gb/s | 0.4 | – | – | UI | |
| JT_SJ _{2.5} | Sinusoidal Jitter ⁽³⁾ | 2.5 Gb/s | 0.4 | – | – | UI | |
| JT_SJ _{1.62} | Sinusoidal Jitter ⁽³⁾ | 1.62 Gb/s | 0.5 | – | – | UI | |
| JT_SJ _{1.25} | Sinusoidal Jitter ⁽³⁾ | 1.25 Gb/s | 0.5 | – | – | UI | |
| JT_SJ ₆₁₄ | Sinusoidal Jitter ⁽³⁾ | 614 Mb/s | 0.5 | – | – | UI | |
| SJ Jitter Tolerance with Stressed Eye⁽²⁾⁽⁵⁾ | | | | | | | |
| JT_TJSE _{3.125} | Total Jitter with stressed eye ⁽⁴⁾ | 3.125 Gb/s | 0.65 | – | – | UI | |
| JT_SJSE _{3.125} | Sinusoidal Jitter with stressed eye | 3.125 Gb/s | 0.1 | – | – | UI | |
| JT_TJSE _{2.7} | Total Jitter with stressed eye ⁽⁴⁾ | 2.7 Gb/s | 0.65 | – | – | UI | |
| JT_SJSE _{2.7} | Sinusoidal Jitter with stressed eye | 2.7 Gb/s | 0.1 | – | – | UI | |

Notes:

- Using PLL_RXDIVSEL_OUT = 1, 2, and 4.
- All jitter values are based on a Bit Error Ratio of 1e⁻¹².
- Using 80 MHz sinusoidal jitter only in the absence of deterministic and random jitter.
- Composed of 0.37 UI DJ in the form of ISI and 0.18 UI RJ.
- Measured using PRBS7 data pattern.

Endpoint Block for PCI Express Designs Switching Characteristics

The Endpoint block for PCI Express is available in the Spartan-6 LXT devices. Consult the [Spartan-6 FPGA Integrated Endpoint Block for PCI Express](#) for further information.

Table 24: Maximum Performance for PCI Express Designs

| Symbol | Description | Speed Grade | | | | Units |
|-----------------------|------------------------------|-------------|------|------|-----|-------|
| | | -3 | -3N | -2 | -1L | |
| F _{PCIEUSER} | User clock maximum frequency | 62.5 | 62.5 | 62.5 | N/A | MHz |

Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Spartan-6 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the [Switching Characteristics, page 19](#).

Table 25: Interface Performances

| Description | I/O Resource | Clock Buffer | Data Width | Speed Grade | | | | Units |
|---|--------------------------|--------------|------------|-------------|------------------------|-----|-----|-------|
| | | | | -3 | -3N | -2 | -1L | |
| Networking Applications⁽¹⁾ | | | | | | | | |
| SDR LVDS transmitter or receiver | IOB SDR register | BUFG | – | 400 | 400 | 375 | 250 | Mb/s |
| DDR LVDS transmitter or receiver | ODDR2/IDDR2 register | 2 BUFGs | – | 800 | 800 | 750 | 500 | Mb/s |
| SDR LVDS transmitter | OSERDES2 | BUFPLL | 2 | 500 | 500 | 500 | 250 | Mb/s |
| | | | 3 | 750 | 750 | 750 | 375 | Mb/s |
| | | | 4-8 | 1080 | 1050 | 950 | 500 | Mb/s |
| DDR LVDS transmitter | OSERDES2 | 2 BUFIO2s | 2 | 500 | 500 | 500 | 250 | Mb/s |
| | | | 3 | 750 | 750 | 750 | 375 | Mb/s |
| | | | 4-8 | 1080 | 1050 | 950 | 500 | Mb/s |
| SDR LVDS receiver | ISERDES2 in RETIMED mode | BUFPLL | 2 | 500 | 500 | 500 | — | Mb/s |
| | | | 3 | 750 | 750 | 750 | — | Mb/s |
| | | | 4-8 | 1080 | 1050 | 950 | — | Mb/s |
| DDR LVDS receiver | ISERDES2 in RETIMED mode | 2 BUFIO2s | 2 | 500 | 500 | 500 | — | Mb/s |
| | | | 3 | 750 | 750 | 750 | — | Mb/s |
| | | | 4-8 | 1080 | 1050 | 950 | — | Mb/s |
| Memory Interfaces (Implemented using the Spartan-6 FPGA Memory Controller Block)⁽²⁾ | | | | | | | | |
| Standard Performance (Standard V_{CCINT}) | | | | | | | | |
| DDR | | | | 400 | Note 4 | 400 | 350 | Mb/s |
| DDR2 | | | | 667 | Note 4 | 625 | 400 | Mb/s |
| DDR3 | | | | 800 | Note 4 | 667 | — | Mb/s |
| LPDDR (Mobile_DDR) | | | | 400 | Note 4 | 400 | 350 | Mb/s |
| Extended Performance (Requires Extended Performance V_{CCINT})⁽³⁾ | | | | | | | | |
| DDR2 | | | | 800 | Note 4 | 667 | — | Mb/s |

Notes:

1. Refer to [XAPP1064](#), *Source-Synchronous Serialization and Deserialization (up to 1050 Mb/s)* and [UG381](#), *Spartan-6 FPGA SelectIO Resources User Guide*.
2. Refer to [UG388](#), *Spartan-6 FPGA Memory Controller User Guide*.
3. Extended Memory Controller block performance for DDR2 can be achieved using the extended performance V_{CCINT} range from [Table 2](#).
4. The LX4 device, all devices in the TQG144 and CPG196 packages, and the -3N speed grade do not support a Memory Controller Block.

Switching Characteristics

All values represented in this data sheet are based on these speed specifications: v1.20 for -3, -3N, and -2; and v1.08 for -1L. Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

Advance

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

Production

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

All specifications are always representative of worst-case supply voltage and junction temperature conditions.

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device.

The -1L speed grade refers to the lower-power Spartan-6 devices. The -3N speed grade refers to the Spartan-6 devices that do not support MCB functionality.

[Table 26](#) correlates the current status of each Spartan-6 device on a per speed grade basis.

Testing of Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotated to the simulation net list. Unless otherwise noted, values apply to all Spartan-6 devices.

Table 26: Spartan-6 Device Speed Grade Designations

| Device | Speed Grade Designations | | |
|------------------------|--------------------------|-------------|------------------|
| | Advance | Preliminary | Production |
| XC6SLX4 ⁽¹⁾ | | | -3, -2, -1L |
| XC6SLX9 | | | -3, -3N, -2, -1L |
| XC6SLX16 | | | -3, -3N, -2, -1L |
| XC6SLX25 | | | -3, -3N, -2, -1L |
| XC6SLX25T | | | -3, -3N, -2 |
| XC6SLX45 | | | -3, -3N, -2, -1L |
| XC6SLX45T | | | -3, -3N, -2 |
| XC6SLX75 | | | -3, -3N, -2, -1L |
| XC6SLX75T | | | -3, -3N, -2 |
| XC6SLX100 | | | -3, -3N, -2, -1L |
| XC6SLX100T | | | -3, -3N, -2 |
| XC6SLX150 | | | -3, -3N, -2, -1L |
| XC6SLX150T | | | -3, -3N, -2 |
| XA6SLX4 | | | -3, -2 |
| XA6SLX9 | | | -3, -2 |
| XA6SLX16 | | | -3, -2 |
| XA6SLX25 | | | -3, -2 |
| XA6SLX25T | | | -3, -2 |
| XA6SLX45 | | | -3, -2 |
| XA6SLX45T | | | -3, -2 |
| XA6SLX75 | | | -3, -2 |
| XA6SLX75T | | | -3, -2 |
| XA6SLX100 | | | -2 |
| XQ6SLX75 | | | -2, -1L |
| XQ6SLX75T | | | -3, -2 |
| XQ6SLX150 | | | -2, -1L |
| XQ6SLX150T | | | -3, -2 |

Notes:

1. The XC6SLX4 is not available in the -3N speed grade.

Production Silicon and ISE Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases. [Table 27](#) lists the production released Spartan-6 family member, speed grade, and the minimum corresponding supported speed specification version and ISE® software revisions. The ISE software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

Table 27: Spartan-6 Device Production Software and Speed Specification Release⁽¹⁾

| Device | Speed Grade Designations ⁽²⁾ | | | |
|------------|---|--------------------------------------|-------------------------------|----------------|
| | -3 ⁽³⁾ | -3N | -2 ⁽⁴⁾ | -1L |
| XC6SLX4 | ISE 12.4 v1.15 | N/A | ISE 12.3 v1.12 ⁽⁵⁾ | ISE 13.2 v1.07 |
| XC6SLX9 | ISE 12.4 v1.15 | ISE 13.1 Update v1.18 ⁽⁷⁾ | ISE 12.3 v1.12 ⁽⁵⁾ | ISE 13.2 v1.07 |
| XC6SLX16 | ISE 12.1 v1.08 | ISE 13.1 Update v1.18 ⁽⁷⁾ | ISE 11.5 v1.06 | ISE 13.2 v1.07 |
| XC6SLX25 | ISE 12.2 v1.11 ⁽⁶⁾ | ISE 13.1 Update v1.18 ⁽⁷⁾ | ISE 12.2 v1.11 ⁽⁶⁾ | ISE 13.2 v1.07 |
| XC6SLX25T | ISE 12.2 v1.11 ⁽⁶⁾ | ISE 13.1 Update v1.18 ⁽⁷⁾ | ISE 12.2 v1.11 ⁽⁶⁾ | N/A |
| XC6SLX45 | ISE 12.1 v1.08 | ISE 13.1 Update v1.18 ⁽⁷⁾ | ISE 11.5 v1.07 | ISE 13.1 v1.06 |
| XC6SLX45T | ISE 12.1 v1.08 | ISE 13.1 Update v1.18 ⁽⁷⁾ | ISE 12.1 v1.08 | N/A |
| XC6SLX75 | ISE 12.2 v1.11 ⁽⁶⁾ | ISE 13.1 Update v1.18 ⁽⁷⁾ | ISE 12.2 v1.11 ⁽⁶⁾ | ISE 13.2 v1.07 |
| XC6SLX75T | ISE 12.2 v1.11 ⁽⁶⁾ | ISE 13.1 Update v1.18 ⁽⁷⁾ | ISE 12.2 v1.11 ⁽⁶⁾ | N/A |
| XC6SLX100 | ISE 12.2 v1.11 ⁽⁶⁾ | ISE 13.1 Update v1.18 ⁽⁷⁾ | ISE 12.2 v1.11 ⁽⁶⁾ | ISE 13.1 v1.06 |
| XC6SLX100T | ISE 12.2 v1.11 ⁽⁶⁾ | ISE 13.1 Update v1.18 ⁽⁷⁾ | ISE 12.2 v1.11 ⁽⁶⁾ | N/A |
| XC6SLX150 | ISE 12.2 v1.11 ⁽⁶⁾ | ISE 13.1 Update v1.18 ⁽⁷⁾ | ISE 12.2 v1.11 ⁽⁶⁾ | ISE 13.1 v1.06 |
| XC6SLX150T | ISE 12.2 v1.11 ⁽⁶⁾ | ISE 13.1 Update v1.18 ⁽⁷⁾ | ISE 12.2 v1.11 ⁽⁶⁾ | N/A |
| XA6SLX4 | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX9 | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX16 | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX25 | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX25T | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX45 | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX45T | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX75 | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX75T | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XA6SLX100 | N/A | N/A | ISE 13.3 v1.20 | N/A |

Table 27: Spartan-6 Device Production Software and Speed Specification Release⁽¹⁾ (Cont'd)

| Device | Speed Grade Designations ⁽²⁾ | | | |
|------------|---|-----|-------------------|----------------|
| | -3 ⁽³⁾ | -3N | -2 ⁽⁴⁾ | -1L |
| XQ6SLX75 | N/A | N/A | ISE 13.2 v1.19 | ISE 13.2 v1.07 |
| XQ6SLX75T | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |
| XQ6SLX150 | N/A | N/A | ISE 13.2 v1.19 | ISE 13.2 v1.07 |
| XQ6SLX150T | ISE 13.2 v1.19 | N/A | ISE 13.2 v1.19 | N/A |

Notes:

1. ISE 13.3 software with v1.20 for -3, -3N, and -2; and v1.08 for -1L speed specification reflects the changes outlined in [XCN11028: Spartan-6 FPGA Speed File Changes](#).
2. As marked with an N/A, LXT devices and all XA devices are not available with a -1L speed grade; LX4 devices and all XA and XQ devices are not available with a -3N speed grade.
3. Improved -3 specifications reflected in this data sheet require ISE 12.4 software with v1.15 speed specification.
4. Improved -2 specifications reflected in this data sheet require ISE 12.4 software and the *12.4 Speed Files Patch* which contains the v1.17 speed specification available on the [Xilinx Download Center](#).
5. ISE 12.3 software with v1.12 speed specification is available using ISE 12.3 software and the *12.3 Speed Files Patch* available on the [Xilinx Download Center](#).
6. ISE 12.2 software with v1.11 speed specification is available using ISE 12.2 software and the *12.2 Speed Files Patch* available on the [Xilinx Download Center](#).
7. ISE 13.1 software with v1.18 speed specification is available using ISE 13.1 software and the *13.1 Update* available on the [Xilinx Download Center](#). See [XCN11012: Speed File Change for -3N Devices](#).

IOB Pad Input/Output/3-State Switching Characteristics

Table 28 (for commercial (XC) Spartan-6 devices) and Table 29 (for Automotive XA Spartan-6 and Defense-grade Spartan-6Q devices) summarizes the values of standard-specific data input delays, output delays terminating at pads (based on standard), and 3-state delays.

- T_{IOPI} is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- T_{IOOP} is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- T_{IOTP} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer.

See the TRACE report for further information on delays when using an I/O standard with UNTUNED termination on inputs or outputs.

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices

| I/O Standard | T_{IOPI} | | | | T_{IOOP} | | | | T_{IOTP} | | | | Units |
|--------------------------|-------------|------|------|--------------------|-------------|------|------|--------------------|-------------|------|------|--------------------|-------|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -3N | -2 | -1L ⁽¹⁾ | -3 | -3N | -2 | -1L ⁽¹⁾ | -3 | -3N | -2 | -1L ⁽¹⁾ | |
| LVDS_33 | 1.17 | 1.29 | 1.42 | 1.68 | 1.55 | 1.69 | 1.89 | 2.42 | 3000 | 3000 | 3000 | 3000 | ns |
| LVDS_25 | 1.01 | 1.13 | 1.26 | 1.57 | 1.65 | 1.79 | 1.99 | 2.47 | 3000 | 3000 | 3000 | 3000 | ns |
| BLVDS_25 | 1.02 | 1.14 | 1.27 | 1.57 | 1.72 | 1.86 | 2.06 | 2.68 | 1.72 | 1.86 | 2.06 | 2.68 | ns |
| MINI_LVDS_33 | 1.17 | 1.29 | 1.42 | 1.68 | 1.57 | 1.71 | 1.91 | 2.41 | 3000 | 3000 | 3000 | 3000 | ns |
| MINI_LVDS_25 | 1.01 | 1.13 | 1.26 | 1.57 | 1.65 | 1.79 | 1.99 | 2.47 | 3000 | 3000 | 3000 | 3000 | ns |
| LVPECL_33 | 1.18 | 1.30 | 1.43 | 1.68 | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | ns |
| LVPECL_25 | 1.02 | 1.14 | 1.27 | 1.57 | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A | ns |
| RSDS_33 (point to point) | 1.17 | 1.29 | 1.42 | 1.68 | 1.57 | 1.71 | 1.91 | 2.42 | 3000 | 3000 | 3000 | 3000 | ns |
| RSDS_25 (point to point) | 1.01 | 1.13 | 1.26 | 1.56 | 1.65 | 1.79 | 1.99 | 2.47 | 3000 | 3000 | 3000 | 3000 | ns |
| TMDS_33 | 1.21 | 1.33 | 1.46 | 1.71 | 1.54 | 1.68 | 1.88 | 2.50 | 3000 | 3000 | 3000 | 3000 | ns |

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

| I/O Standard | T _{IOPI} | | | | T _{IOOP} | | | | T _{IOTP} | | | | Units |
|------------------|-------------------|------|------|---------------------|-------------------|-------|-------|---------------------|-------------------|-------|-------|---------------------|-------|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -3N | -2 | -1L ⁽¹⁾ | -3 | -3N | -2 | -1L ⁽¹⁾ | -3 | -3N | -2 | -1L ⁽¹⁾ | |
| PPDS_33 | 1.17 | 1.29 | 1.42 | 1.68 | 1.57 | 1.71 | 1.91 | 2.43 | 3000 | 3000 | 3000 | 3000 | ns |
| PPDS_25 | 1.01 | 1.13 | 1.26 | 1.56 | 1.68 | 1.82 | 2.02 | 2.47 | 3000 | 3000 | 3000 | 3000 | ns |
| PCI33_3 | 1.07 | 1.19 | 1.32 | 1.57 ⁽²⁾ | 3.51 | 3.65 | 3.85 | 4.38 ⁽²⁾ | 3.51 | 3.65 | 3.85 | 4.38 ⁽¹⁾ | ns |
| PCI66_3 | 1.07 | 1.19 | 1.32 | 1.57 ⁽²⁾ | 3.53 | 3.67 | 3.87 | 4.39 ⁽²⁾ | 3.53 | 3.67 | 3.87 | 4.39 ⁽¹⁾ | ns |
| DISPLAY_PORT | 1.02 | 1.14 | 1.27 | 1.56 | 3.15 | 3.29 | 3.49 | 4.08 | 3.15 | 3.29 | 3.49 | 4.08 | ns |
| I2C | 1.33 | 1.45 | 1.58 | 1.82 | 11.56 | 11.70 | 11.90 | 12.52 | 11.56 | 11.70 | 11.90 | 12.52 | ns |
| SMBUS | 1.33 | 1.45 | 1.58 | 1.82 | 11.56 | 11.70 | 11.90 | 12.52 | 11.56 | 11.70 | 11.90 | 12.52 | ns |
| SDIO | 1.36 | 1.48 | 1.61 | 1.84 | 2.64 | 2.78 | 2.98 | 3.60 | 2.64 | 2.78 | 2.98 | 3.60 | ns |
| MOBILE_DDR | 0.94 | 1.06 | 1.19 | 1.43 | 2.35 | 2.49 | 2.69 | 3.31 | 2.35 | 2.49 | 2.69 | 3.31 | ns |
| HSTL_I | 0.90 | 1.02 | 1.15 | 1.39 | 1.66 | 1.80 | 2.00 | 2.62 | 1.66 | 1.80 | 2.00 | 2.62 | ns |
| HSTL_II | 0.91 | 1.03 | 1.16 | 1.40 | 1.72 | 1.86 | 2.06 | 2.68 | 1.72 | 1.86 | 2.06 | 2.68 | ns |
| HSTL_III | 0.95 | 1.07 | 1.20 | 1.44 | 1.67 | 1.81 | 2.01 | 2.61 | 1.67 | 1.81 | 2.01 | 2.61 | ns |
| HSTL_I_18 | 0.94 | 1.06 | 1.19 | 1.43 | 1.77 | 1.91 | 2.11 | 2.73 | 1.77 | 1.91 | 2.11 | 2.73 | ns |
| HSTL_II_18 | 0.94 | 1.06 | 1.19 | 1.43 | 1.85 | 1.99 | 2.19 | 2.81 | 1.85 | 1.99 | 2.19 | 2.81 | ns |
| HSTL_III_18 | 0.99 | 1.11 | 1.24 | 1.47 | 1.79 | 1.93 | 2.13 | 2.72 | 1.79 | 1.93 | 2.13 | 2.72 | ns |
| SSTL3_I | 1.58 | 1.70 | 1.83 | 2.16 | 1.83 | 1.97 | 2.17 | 2.72 | 1.83 | 1.97 | 2.17 | 2.72 | ns |
| SSTL3_II | 1.58 | 1.70 | 1.83 | 2.16 | 2.01 | 2.15 | 2.35 | 2.94 | 2.01 | 2.15 | 2.35 | 2.94 | ns |
| SSTL2_I | 1.30 | 1.42 | 1.55 | 1.87 | 1.77 | 1.91 | 2.11 | 2.69 | 1.77 | 1.91 | 2.11 | 2.69 | ns |
| SSTL2_II | 1.30 | 1.42 | 1.55 | 1.88 | 1.86 | 2.00 | 2.20 | 2.82 | 1.86 | 2.00 | 2.20 | 2.82 | ns |
| SSTL18_I | 0.92 | 1.04 | 1.17 | 1.41 | 1.63 | 1.77 | 1.97 | 2.59 | 1.63 | 1.77 | 1.97 | 2.59 | ns |
| SSTL18_II | 0.92 | 1.04 | 1.17 | 1.41 | 1.66 | 1.80 | 2.00 | 2.62 | 1.66 | 1.80 | 2.00 | 2.62 | ns |
| SSTL15_II | 0.92 | 1.04 | 1.17 | 1.41 | 1.67 | 1.81 | 2.01 | 2.63 | 1.67 | 1.81 | 2.01 | 2.63 | ns |
| DIFF_HSTL_I | 0.94 | 1.06 | 1.19 | 1.46 | 1.77 | 1.91 | 2.11 | 2.62 | 1.77 | 1.91 | 2.11 | 2.62 | ns |
| DIFF_HSTL_II | 0.93 | 1.05 | 1.18 | 1.45 | 1.72 | 1.86 | 2.06 | 2.54 | 1.72 | 1.86 | 2.06 | 2.54 | ns |
| DIFF_HSTL_III | 0.93 | 1.05 | 1.18 | 1.46 | 1.69 | 1.83 | 2.03 | 2.53 | 1.69 | 1.83 | 2.03 | 2.53 | ns |
| DIFF_HSTL_I_18 | 0.97 | 1.09 | 1.22 | 1.50 | 1.79 | 1.93 | 2.13 | 2.63 | 1.79 | 1.93 | 2.13 | 2.63 | ns |
| DIFF_HSTL_II_18 | 0.97 | 1.09 | 1.22 | 1.49 | 1.69 | 1.83 | 2.03 | 2.51 | 1.69 | 1.83 | 2.03 | 2.51 | ns |
| DIFF_HSTL_III_18 | 0.97 | 1.09 | 1.22 | 1.50 | 1.69 | 1.83 | 2.03 | 2.53 | 1.69 | 1.83 | 2.03 | 2.53 | ns |
| DIFF_SSTL3_I | 1.18 | 1.30 | 1.43 | 1.68 | 1.81 | 1.95 | 2.15 | 2.64 | 1.81 | 1.95 | 2.15 | 2.64 | ns |
| DIFF_SSTL3_II | 1.19 | 1.31 | 1.44 | 1.68 | 1.80 | 1.94 | 2.14 | 2.63 | 1.80 | 1.94 | 2.14 | 2.63 | ns |
| DIFF_SSTL2_I | 1.02 | 1.14 | 1.27 | 1.57 | 1.80 | 1.94 | 2.14 | 2.62 | 1.80 | 1.94 | 2.14 | 2.62 | ns |
| DIFF_SSTL2_II | 1.02 | 1.14 | 1.27 | 1.57 | 1.76 | 1.90 | 2.10 | 2.57 | 1.76 | 1.90 | 2.10 | 2.57 | ns |
| DIFF_SSTL18_I | 0.97 | 1.09 | 1.22 | 1.51 | 1.72 | 1.86 | 2.06 | 2.56 | 1.72 | 1.86 | 2.06 | 2.56 | ns |
| DIFF_SSTL18_II | 0.98 | 1.10 | 1.23 | 1.50 | 1.68 | 1.82 | 2.02 | 2.52 | 1.68 | 1.82 | 2.02 | 2.52 | ns |
| DIFF_SSTL15_II | 0.94 | 1.06 | 1.19 | 1.46 | 1.67 | 1.81 | 2.01 | 2.50 | 1.67 | 1.81 | 2.01 | 2.50 | ns |
| DIFF_MOBILE_DDR | 0.97 | 1.09 | 1.22 | 1.51 | 1.75 | 1.89 | 2.09 | 2.57 | 1.75 | 1.89 | 2.09 | 2.57 | ns |

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

| I/O Standard | T_{IOPI} | | | | T_{IOOP} | | | | T_{IOTP} | | | | Units |
|---------------------------|-------------|------|------|--------------------|-------------|------|------|--------------------|-------------|------|------|--------------------|-------|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -3N | -2 | -1L ⁽¹⁾ | -3 | -3N | -2 | -1L ⁽¹⁾ | -3 | -3N | -2 | -1L ⁽¹⁾ | |
| LVTTTL, QUIETIO, 2 mA | 1.35 | 1.47 | 1.60 | 1.82 | 5.39 | 5.53 | 5.73 | 6.37 | 5.39 | 5.53 | 5.73 | 6.37 | ns |
| LVTTTL, QUIETIO, 4 mA | 1.35 | 1.47 | 1.60 | 1.82 | 4.29 | 4.43 | 4.63 | 5.22 | 4.29 | 4.43 | 4.63 | 5.22 | ns |
| LVTTTL, QUIETIO, 6 mA | 1.35 | 1.47 | 1.60 | 1.82 | 3.75 | 3.89 | 4.09 | 4.69 | 3.75 | 3.89 | 4.09 | 4.69 | ns |
| LVTTTL, QUIETIO, 8 mA | 1.35 | 1.47 | 1.60 | 1.82 | 3.23 | 3.37 | 3.57 | 4.20 | 3.23 | 3.37 | 3.57 | 4.20 | ns |
| LVTTTL, QUIETIO, 12 mA | 1.35 | 1.47 | 1.60 | 1.82 | 3.28 | 3.42 | 3.62 | 4.22 | 3.28 | 3.42 | 3.62 | 4.22 | ns |
| LVTTTL, QUIETIO, 16 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.94 | 3.08 | 3.28 | 3.92 | 2.94 | 3.08 | 3.28 | 3.92 | ns |
| LVTTTL, QUIETIO, 24 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.69 | 2.83 | 3.03 | 3.67 | 2.69 | 2.83 | 3.03 | 3.67 | ns |
| LVTTTL, Slow, 2 mA | 1.35 | 1.47 | 1.60 | 1.82 | 4.36 | 4.50 | 4.70 | 5.30 | 4.36 | 4.50 | 4.70 | 5.30 | ns |
| LVTTTL, Slow, 4 mA | 1.35 | 1.47 | 1.60 | 1.82 | 3.17 | 3.31 | 3.51 | 4.16 | 3.17 | 3.31 | 3.51 | 4.16 | ns |
| LVTTTL, Slow, 6 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.76 | 2.90 | 3.10 | 3.75 | 2.76 | 2.90 | 3.10 | 3.75 | ns |
| LVTTTL, Slow, 8 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.59 | 2.73 | 2.93 | 3.55 | 2.59 | 2.73 | 2.93 | 3.55 | ns |
| LVTTTL, Slow, 12 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.58 | 2.72 | 2.92 | 3.54 | 2.58 | 2.72 | 2.92 | 3.54 | ns |
| LVTTTL, Slow, 16 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.39 | 2.53 | 2.73 | 3.40 | 2.39 | 2.53 | 2.73 | 3.40 | ns |
| LVTTTL, Slow, 24 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.28 | 2.42 | 2.62 | 3.24 | 2.28 | 2.42 | 2.62 | 3.24 | ns |
| LVTTTL, Fast, 2 mA | 1.35 | 1.47 | 1.60 | 1.82 | 3.78 | 3.92 | 4.12 | 4.74 | 3.78 | 3.92 | 4.12 | 4.74 | ns |
| LVTTTL, Fast, 4 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.49 | 2.63 | 2.83 | 3.45 | 2.49 | 2.63 | 2.83 | 3.45 | ns |
| LVTTTL, Fast, 6 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.44 | 2.58 | 2.78 | 3.40 | 2.44 | 2.58 | 2.78 | 3.40 | ns |
| LVTTTL, Fast, 8 mA | 1.35 | 1.47 | 1.60 | 1.82 | 2.32 | 2.46 | 2.66 | 3.28 | 2.32 | 2.46 | 2.66 | 3.28 | ns |
| LVTTTL, Fast, 12 mA | 1.35 | 1.47 | 1.60 | 1.82 | 1.83 | 1.97 | 2.17 | 2.79 | 1.83 | 1.97 | 2.17 | 2.79 | ns |
| LVTTTL, Fast, 16 mA | 1.35 | 1.47 | 1.60 | 1.82 | 1.83 | 1.97 | 2.17 | 2.79 | 1.83 | 1.97 | 2.17 | 2.79 | ns |
| LVTTTL, Fast, 24 mA | 1.35 | 1.47 | 1.60 | 1.82 | 1.83 | 1.97 | 2.17 | 2.79 | 1.83 | 1.97 | 2.17 | 2.79 | ns |
| LVC MOS33, QUIETIO, 2 mA | 1.34 | 1.46 | 1.59 | 1.82 | 5.40 | 5.54 | 5.74 | 6.37 | 5.40 | 5.54 | 5.74 | 6.37 | ns |
| LVC MOS33, QUIETIO, 4 mA | 1.34 | 1.46 | 1.59 | 1.82 | 4.03 | 4.17 | 4.37 | 5.01 | 4.03 | 4.17 | 4.37 | 5.01 | ns |
| LVC MOS33, QUIETIO, 6 mA | 1.34 | 1.46 | 1.59 | 1.82 | 3.51 | 3.65 | 3.85 | 4.47 | 3.51 | 3.65 | 3.85 | 4.47 | ns |
| LVC MOS33, QUIETIO, 8 mA | 1.34 | 1.46 | 1.59 | 1.82 | 3.37 | 3.51 | 3.71 | 4.33 | 3.37 | 3.51 | 3.71 | 4.33 | ns |
| LVC MOS33, QUIETIO, 12 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.94 | 3.08 | 3.28 | 3.93 | 2.94 | 3.08 | 3.28 | 3.93 | ns |
| LVC MOS33, QUIETIO, 16 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.77 | 2.91 | 3.11 | 3.78 | 2.77 | 2.91 | 3.11 | 3.78 | ns |
| LVC MOS33, QUIETIO, 24 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.59 | 2.73 | 2.93 | 3.58 | 2.59 | 2.73 | 2.93 | 3.58 | ns |
| LVC MOS33, Slow, 2 mA | 1.34 | 1.46 | 1.59 | 1.82 | 4.37 | 4.51 | 4.71 | 5.28 | 4.37 | 4.51 | 4.71 | 5.28 | ns |
| LVC MOS33, Slow, 4 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.98 | 3.12 | 3.32 | 3.94 | 2.98 | 3.12 | 3.32 | 3.94 | ns |
| LVC MOS33, Slow, 6 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.58 | 2.72 | 2.92 | 3.61 | 2.58 | 2.72 | 2.92 | 3.61 | ns |
| LVC MOS33, Slow, 8 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.65 | 2.79 | 2.99 | 3.61 | 2.65 | 2.79 | 2.99 | 3.61 | ns |
| LVC MOS33, Slow, 12 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.39 | 2.53 | 2.73 | 3.31 | 2.39 | 2.53 | 2.73 | 3.31 | ns |
| LVC MOS33, Slow, 16 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.31 | 2.45 | 2.65 | 3.27 | 2.31 | 2.45 | 2.65 | 3.27 | ns |
| LVC MOS33, Slow, 24 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.28 | 2.42 | 2.62 | 3.24 | 2.28 | 2.42 | 2.62 | 3.24 | ns |
| LVC MOS33, Fast, 2 mA | 1.34 | 1.46 | 1.59 | 1.82 | 3.76 | 3.90 | 4.10 | 4.70 | 3.76 | 3.90 | 4.10 | 4.70 | ns |
| LVC MOS33, Fast, 4 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.48 | 2.62 | 2.82 | 3.44 | 2.48 | 2.62 | 2.82 | 3.44 | ns |
| LVC MOS33, Fast, 6 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.32 | 2.46 | 2.66 | 3.28 | 2.32 | 2.46 | 2.66 | 3.28 | ns |

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

| I/O Standard | T _{IOPI} | | | | T _{IOOP} | | | | T _{IOTP} | | | | Units |
|---------------------------|-------------------|------|------|--------------------|-------------------|------|------|--------------------|-------------------|------|------|--------------------|-------|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -3N | -2 | -1L ⁽¹⁾ | -3 | -3N | -2 | -1L ⁽¹⁾ | -3 | -3N | -2 | -1L ⁽¹⁾ | |
| LVC MOS33, Fast, 8 mA | 1.34 | 1.46 | 1.59 | 1.82 | 2.07 | 2.21 | 2.41 | 3.03 | 2.07 | 2.21 | 2.41 | 3.03 | ns |
| LVC MOS33, Fast, 12 mA | 1.34 | 1.46 | 1.59 | 1.82 | 1.65 | 1.79 | 1.99 | 2.62 | 1.65 | 1.79 | 1.99 | 2.62 | ns |
| LVC MOS33, Fast, 16 mA | 1.34 | 1.46 | 1.59 | 1.82 | 1.65 | 1.79 | 1.99 | 2.62 | 1.65 | 1.79 | 1.99 | 2.62 | ns |
| LVC MOS33, Fast, 24 mA | 1.34 | 1.46 | 1.59 | 1.82 | 1.65 | 1.79 | 1.99 | 2.62 | 1.65 | 1.79 | 1.99 | 2.62 | ns |
| LVC MOS25, QUIETIO, 2 mA | 0.82 | 0.94 | 1.07 | 1.31 | 4.81 | 4.95 | 5.15 | 5.79 | 4.81 | 4.95 | 5.15 | 5.79 | ns |
| LVC MOS25, QUIETIO, 4 mA | 0.82 | 0.94 | 1.07 | 1.31 | 3.70 | 3.84 | 4.04 | 4.66 | 3.70 | 3.84 | 4.04 | 4.66 | ns |
| LVC MOS25, QUIETIO, 6 mA | 0.82 | 0.94 | 1.07 | 1.31 | 3.46 | 3.60 | 3.80 | 4.38 | 3.46 | 3.60 | 3.80 | 4.38 | ns |
| LVC MOS25, QUIETIO, 8 mA | 0.82 | 0.94 | 1.07 | 1.31 | 3.20 | 3.34 | 3.54 | 4.12 | 3.20 | 3.34 | 3.54 | 4.12 | ns |
| LVC MOS25, QUIETIO, 12 mA | 0.82 | 0.94 | 1.07 | 1.31 | 2.83 | 2.97 | 3.17 | 3.75 | 2.83 | 2.97 | 3.17 | 3.75 | ns |
| LVC MOS25, QUIETIO, 16 mA | 0.82 | 0.94 | 1.07 | 1.31 | 2.64 | 2.78 | 2.98 | 3.64 | 2.64 | 2.78 | 2.98 | 3.64 | ns |
| LVC MOS25, QUIETIO, 24 mA | 0.82 | 0.94 | 1.07 | 1.31 | 2.45 | 2.59 | 2.79 | 3.42 | 2.45 | 2.59 | 2.79 | 3.42 | ns |
| LVC MOS25, Slow, 2 mA | 0.82 | 0.94 | 1.07 | 1.31 | 3.78 | 3.92 | 4.12 | 4.76 | 3.78 | 3.92 | 4.12 | 4.76 | ns |
| LVC MOS25, Slow, 4 mA | 0.82 | 0.94 | 1.07 | 1.31 | 2.79 | 2.93 | 3.13 | 3.73 | 2.79 | 2.93 | 3.13 | 3.73 | ns |
| LVC MOS25, Slow, 6 mA | 0.82 | 0.94 | 1.07 | 1.31 | 2.73 | 2.87 | 3.07 | 3.66 | 2.73 | 2.87 | 3.07 | 3.66 | ns |
| LVC MOS25, Slow, 8 mA | 0.82 | 0.94 | 1.07 | 1.31 | 2.48 | 2.62 | 2.82 | 3.42 | 2.48 | 2.62 | 2.82 | 3.42 | ns |
| LVC MOS25, Slow, 12 mA | 0.82 | 0.94 | 1.07 | 1.31 | 2.01 | 2.15 | 2.35 | 2.95 | 2.01 | 2.15 | 2.35 | 2.95 | ns |
| LVC MOS25, Slow, 16 mA | 0.82 | 0.94 | 1.07 | 1.31 | 2.01 | 2.15 | 2.35 | 2.95 | 2.01 | 2.15 | 2.35 | 2.95 | ns |
| LVC MOS25, Slow, 24 mA | 0.82 | 0.94 | 1.07 | 1.31 | 2.01 | 2.15 | 2.35 | 2.94 | 2.01 | 2.15 | 2.35 | 2.94 | ns |
| LVC MOS25, Fast, 2 mA | 0.82 | 0.94 | 1.07 | 1.31 | 3.35 | 3.49 | 3.69 | 4.31 | 3.35 | 3.49 | 3.69 | 4.31 | ns |
| LVC MOS25, Fast, 4 mA | 0.82 | 0.94 | 1.07 | 1.31 | 2.25 | 2.39 | 2.59 | 3.22 | 2.25 | 2.39 | 2.59 | 3.22 | ns |
| LVC MOS25, Fast, 6 mA | 0.82 | 0.94 | 1.07 | 1.31 | 2.09 | 2.23 | 2.43 | 3.05 | 2.09 | 2.23 | 2.43 | 3.05 | ns |
| LVC MOS25, Fast, 8 mA | 0.82 | 0.94 | 1.07 | 1.31 | 2.02 | 2.16 | 2.36 | 2.98 | 2.02 | 2.16 | 2.36 | 2.98 | ns |
| LVC MOS25, Fast, 12 mA | 0.82 | 0.94 | 1.07 | 1.31 | 1.56 | 1.70 | 1.90 | 2.52 | 1.56 | 1.70 | 1.90 | 2.52 | ns |
| LVC MOS25, Fast, 16 mA | 0.82 | 0.94 | 1.07 | 1.31 | 1.56 | 1.70 | 1.90 | 2.52 | 1.56 | 1.70 | 1.90 | 2.52 | ns |
| LVC MOS25, Fast, 24 mA | 0.82 | 0.94 | 1.07 | 1.31 | 1.56 | 1.70 | 1.90 | 2.52 | 1.56 | 1.70 | 1.90 | 2.52 | ns |
| LVC MOS18, QUIETIO, 2 mA | 1.18 | 1.30 | 1.43 | 2.04 | 5.92 | 6.06 | 6.26 | 6.80 | 5.92 | 6.06 | 6.26 | 6.80 | ns |
| LVC MOS18, QUIETIO, 4 mA | 1.18 | 1.30 | 1.43 | 2.04 | 4.74 | 4.88 | 5.08 | 5.63 | 4.74 | 4.88 | 5.08 | 5.63 | ns |
| LVC MOS18, QUIETIO, 6 mA | 1.18 | 1.30 | 1.43 | 2.04 | 4.05 | 4.19 | 4.39 | 4.96 | 4.05 | 4.19 | 4.39 | 4.96 | ns |
| LVC MOS18, QUIETIO, 8 mA | 1.18 | 1.30 | 1.43 | 2.04 | 3.71 | 3.85 | 4.05 | 4.63 | 3.71 | 3.85 | 4.05 | 4.63 | ns |
| LVC MOS18, QUIETIO, 12 mA | 1.18 | 1.30 | 1.43 | 2.04 | 3.35 | 3.49 | 3.69 | 4.27 | 3.35 | 3.49 | 3.69 | 4.27 | ns |
| LVC MOS18, QUIETIO, 16 mA | 1.18 | 1.30 | 1.43 | 2.04 | 3.20 | 3.34 | 3.54 | 4.14 | 3.20 | 3.34 | 3.54 | 4.14 | ns |
| LVC MOS18, QUIETIO, 24 mA | 1.18 | 1.30 | 1.43 | 2.04 | 2.96 | 3.10 | 3.30 | 3.98 | 2.96 | 3.10 | 3.30 | 3.98 | ns |
| LVC MOS18, Slow, 2 mA | 1.18 | 1.30 | 1.43 | 2.04 | 4.62 | 4.76 | 4.96 | 5.54 | 4.62 | 4.76 | 4.96 | 5.54 | ns |
| LVC MOS18, Slow, 4 mA | 1.18 | 1.30 | 1.43 | 2.04 | 3.69 | 3.83 | 4.03 | 4.60 | 3.69 | 3.83 | 4.03 | 4.60 | ns |
| LVC MOS18, Slow, 6 mA | 1.18 | 1.30 | 1.43 | 2.04 | 3.00 | 3.14 | 3.34 | 3.94 | 3.00 | 3.14 | 3.34 | 3.94 | ns |
| LVC MOS18, Slow, 8 mA | 1.18 | 1.30 | 1.43 | 2.04 | 2.19 | 2.33 | 2.53 | 3.17 | 2.19 | 2.33 | 2.53 | 3.17 | ns |
| LVC MOS18, Slow, 12 mA | 1.18 | 1.30 | 1.43 | 2.04 | 1.99 | 2.13 | 2.33 | 2.95 | 1.99 | 2.13 | 2.33 | 2.95 | ns |
| LVC MOS18, Slow, 16 mA | 1.18 | 1.30 | 1.43 | 2.04 | 1.99 | 2.13 | 2.33 | 2.95 | 1.99 | 2.13 | 2.33 | 2.95 | ns |

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

| I/O Standard | T_{IOPI} | | | | T_{IOOP} | | | | T_{IOTP} | | | | Units |
|---------------------------------|-------------|------|------|--------------------|-------------|------|------|--------------------|-------------|------|------|--------------------|-------|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -3N | -2 | -1L ⁽¹⁾ | -3 | -3N | -2 | -1L ⁽¹⁾ | -3 | -3N | -2 | -1L ⁽¹⁾ | |
| LVC MOS18, Slow, 24 mA | 1.18 | 1.30 | 1.43 | 2.04 | 1.99 | 2.13 | 2.33 | 2.95 | 1.99 | 2.13 | 2.33 | 2.95 | ns |
| LVC MOS18, Fast, 2 mA | 1.18 | 1.30 | 1.43 | 2.04 | 3.59 | 3.73 | 3.93 | 4.53 | 3.59 | 3.73 | 3.93 | 4.53 | ns |
| LVC MOS18, Fast, 4 mA | 1.18 | 1.30 | 1.43 | 2.04 | 2.39 | 2.53 | 2.73 | 3.35 | 2.39 | 2.53 | 2.73 | 3.35 | ns |
| LVC MOS18, Fast, 6 mA | 1.18 | 1.30 | 1.43 | 2.04 | 1.88 | 2.02 | 2.22 | 2.84 | 1.88 | 2.02 | 2.22 | 2.84 | ns |
| LVC MOS18, Fast, 8 mA | 1.18 | 1.30 | 1.43 | 2.04 | 1.81 | 1.95 | 2.15 | 2.77 | 1.81 | 1.95 | 2.15 | 2.77 | ns |
| LVC MOS18, Fast, 12 mA | 1.18 | 1.30 | 1.43 | 2.04 | 1.71 | 1.85 | 2.05 | 2.67 | 1.71 | 1.85 | 2.05 | 2.67 | ns |
| LVC MOS18, Fast, 16 mA | 1.18 | 1.30 | 1.43 | 2.04 | 1.71 | 1.85 | 2.05 | 2.67 | 1.71 | 1.85 | 2.05 | 2.67 | ns |
| LVC MOS18, Fast, 24 mA | 1.18 | 1.30 | 1.43 | 2.04 | 1.71 | 1.85 | 2.05 | 2.67 | 1.71 | 1.85 | 2.05 | 2.67 | ns |
| LVC MOS18_JEDEC, QUIETIO, 2 mA | 0.94 | 1.06 | 1.19 | 1.41 | 5.91 | 6.05 | 6.25 | 6.79 | 5.91 | 6.05 | 6.25 | 6.79 | ns |
| LVC MOS18_JEDEC, QUIETIO, 4 mA | 0.94 | 1.06 | 1.19 | 1.41 | 4.75 | 4.89 | 5.09 | 5.64 | 4.75 | 4.89 | 5.09 | 5.64 | ns |
| LVC MOS18_JEDEC, QUIETIO, 6 mA | 0.94 | 1.06 | 1.19 | 1.41 | 4.04 | 4.18 | 4.38 | 4.96 | 4.04 | 4.18 | 4.38 | 4.96 | ns |
| LVC MOS18_JEDEC, QUIETIO, 8 mA | 0.94 | 1.06 | 1.19 | 1.41 | 3.71 | 3.85 | 4.05 | 4.62 | 3.71 | 3.85 | 4.05 | 4.62 | ns |
| LVC MOS18_JEDEC, QUIETIO, 12 mA | 0.94 | 1.06 | 1.19 | 1.41 | 3.35 | 3.49 | 3.69 | 4.28 | 3.35 | 3.49 | 3.69 | 4.28 | ns |
| LVC MOS18_JEDEC, QUIETIO, 16 mA | 0.94 | 1.06 | 1.19 | 1.41 | 3.20 | 3.34 | 3.54 | 4.13 | 3.20 | 3.34 | 3.54 | 4.13 | ns |
| LVC MOS18_JEDEC, QUIETIO, 24 mA | 0.94 | 1.06 | 1.19 | 1.41 | 2.96 | 3.10 | 3.30 | 3.98 | 2.96 | 3.10 | 3.30 | 3.98 | ns |
| LVC MOS18_JEDEC, Slow, 2 mA | 0.94 | 1.06 | 1.19 | 1.41 | 4.59 | 4.73 | 4.93 | 5.54 | 4.59 | 4.73 | 4.93 | 5.54 | ns |
| LVC MOS18_JEDEC, Slow, 4 mA | 0.94 | 1.06 | 1.19 | 1.41 | 3.69 | 3.83 | 4.03 | 4.60 | 3.69 | 3.83 | 4.03 | 4.60 | ns |
| LVC MOS18_JEDEC, Slow, 6 mA | 0.94 | 1.06 | 1.19 | 1.41 | 3.00 | 3.14 | 3.34 | 3.94 | 3.00 | 3.14 | 3.34 | 3.94 | ns |
| LVC MOS18_JEDEC, Slow, 8 mA | 0.94 | 1.06 | 1.19 | 1.41 | 2.19 | 2.33 | 2.53 | 3.18 | 2.19 | 2.33 | 2.53 | 3.18 | ns |
| LVC MOS18_JEDEC, Slow, 12 mA | 0.94 | 1.06 | 1.19 | 1.41 | 1.99 | 2.13 | 2.33 | 2.95 | 1.99 | 2.13 | 2.33 | 2.95 | ns |
| LVC MOS18_JEDEC, Slow, 16 mA | 0.94 | 1.06 | 1.19 | 1.41 | 1.99 | 2.13 | 2.33 | 2.95 | 1.99 | 2.13 | 2.33 | 2.95 | ns |
| LVC MOS18_JEDEC, Slow, 24 mA | 0.94 | 1.06 | 1.19 | 1.41 | 1.99 | 2.13 | 2.33 | 2.95 | 1.99 | 2.13 | 2.33 | 2.95 | ns |
| LVC MOS18_JEDEC, Fast, 2 mA | 0.94 | 1.06 | 1.19 | 1.41 | 3.57 | 3.71 | 3.91 | 4.52 | 3.57 | 3.71 | 3.91 | 4.52 | ns |
| LVC MOS18_JEDEC, Fast, 4 mA | 0.94 | 1.06 | 1.19 | 1.41 | 2.39 | 2.53 | 2.73 | 3.35 | 2.39 | 2.53 | 2.73 | 3.35 | ns |
| LVC MOS18_JEDEC, Fast, 6 mA | 0.94 | 1.06 | 1.19 | 1.41 | 1.88 | 2.02 | 2.22 | 2.84 | 1.88 | 2.02 | 2.22 | 2.84 | ns |
| LVC MOS18_JEDEC, Fast, 8 mA | 0.94 | 1.06 | 1.19 | 1.41 | 1.80 | 1.94 | 2.14 | 2.76 | 1.80 | 1.94 | 2.14 | 2.76 | ns |
| LVC MOS18_JEDEC, Fast, 12 mA | 0.94 | 1.06 | 1.19 | 1.41 | 1.72 | 1.86 | 2.06 | 2.68 | 1.72 | 1.86 | 2.06 | 2.68 | ns |
| LVC MOS18_JEDEC, Fast, 16 mA | 0.94 | 1.06 | 1.19 | 1.41 | 1.72 | 1.86 | 2.06 | 2.68 | 1.72 | 1.86 | 2.06 | 2.68 | ns |
| LVC MOS18_JEDEC, Fast, 24 mA | 0.94 | 1.06 | 1.19 | 1.41 | 1.72 | 1.86 | 2.06 | 2.68 | 1.72 | 1.86 | 2.06 | 2.68 | ns |
| LVC MOS15, QUIETIO, 2 mA | 0.98 | 1.10 | 1.23 | 1.79 | 5.47 | 5.61 | 5.81 | 6.38 | 5.47 | 5.61 | 5.81 | 6.38 | ns |
| LVC MOS15, QUIETIO, 4 mA | 0.98 | 1.10 | 1.23 | 1.79 | 4.61 | 4.75 | 4.95 | 5.51 | 4.61 | 4.75 | 4.95 | 5.51 | ns |
| LVC MOS15, QUIETIO, 6 mA | 0.98 | 1.10 | 1.23 | 1.79 | 4.07 | 4.21 | 4.41 | 4.97 | 4.07 | 4.21 | 4.41 | 4.97 | ns |
| LVC MOS15, QUIETIO, 8 mA | 0.98 | 1.10 | 1.23 | 1.79 | 3.91 | 4.05 | 4.25 | 4.81 | 3.91 | 4.05 | 4.25 | 4.81 | ns |
| LVC MOS15, QUIETIO, 12 mA | 0.98 | 1.10 | 1.23 | 1.79 | 3.53 | 3.67 | 3.87 | 4.51 | 3.53 | 3.67 | 3.87 | 4.51 | ns |
| LVC MOS15, QUIETIO, 16 mA | 0.98 | 1.10 | 1.23 | 1.79 | 3.32 | 3.46 | 3.66 | 4.31 | 3.32 | 3.46 | 3.66 | 4.31 | ns |
| LVC MOS15, Slow, 2 mA | 0.98 | 1.10 | 1.23 | 1.79 | 4.18 | 4.32 | 4.52 | 5.11 | 4.18 | 4.32 | 4.52 | 5.11 | ns |
| LVC MOS15, Slow, 4 mA | 0.98 | 1.10 | 1.23 | 1.79 | 3.42 | 3.56 | 3.76 | 4.34 | 3.42 | 3.56 | 3.76 | 4.34 | ns |
| LVC MOS15, Slow, 6 mA | 0.98 | 1.10 | 1.23 | 1.79 | 2.29 | 2.43 | 2.63 | 3.24 | 2.29 | 2.43 | 2.63 | 3.24 | ns |

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

| I/O Standard | T_{IOPI} | | | | T_{IOOP} | | | | T_{IOTP} | | | | Units |
|---------------------------------|-------------|------|------|--------------------|-------------|------|------|--------------------|-------------|------|------|--------------------|-------|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -3N | -2 | -1L ⁽¹⁾ | -3 | -3N | -2 | -1L ⁽¹⁾ | -3 | -3N | -2 | -1L ⁽¹⁾ | |
| LVC MOS15, Slow, 8 mA | 0.98 | 1.10 | 1.23 | 1.79 | 2.30 | 2.44 | 2.64 | 3.25 | 2.30 | 2.44 | 2.64 | 3.25 | ns |
| LVC MOS15, Slow, 12 mA | 0.98 | 1.10 | 1.23 | 1.79 | 2.03 | 2.17 | 2.37 | 2.99 | 2.03 | 2.17 | 2.37 | 2.99 | ns |
| LVC MOS15, Slow, 16 mA | 0.98 | 1.10 | 1.23 | 1.79 | 2.01 | 2.15 | 2.35 | 2.97 | 2.01 | 2.15 | 2.35 | 2.97 | ns |
| LVC MOS15, Fast, 2 mA | 0.98 | 1.10 | 1.23 | 1.79 | 3.29 | 3.43 | 3.63 | 4.24 | 3.29 | 3.43 | 3.63 | 4.24 | ns |
| LVC MOS15, Fast, 4 mA | 0.98 | 1.10 | 1.23 | 1.79 | 2.27 | 2.41 | 2.61 | 3.22 | 2.27 | 2.41 | 2.61 | 3.22 | ns |
| LVC MOS15, Fast, 6 mA | 0.98 | 1.10 | 1.23 | 1.79 | 1.78 | 1.92 | 2.12 | 2.74 | 1.78 | 1.92 | 2.12 | 2.74 | ns |
| LVC MOS15, Fast, 8 mA | 0.98 | 1.10 | 1.23 | 1.79 | 1.73 | 1.87 | 2.07 | 2.69 | 1.73 | 1.87 | 2.07 | 2.69 | ns |
| LVC MOS15, Fast, 12 mA | 0.98 | 1.10 | 1.23 | 1.79 | 1.73 | 1.87 | 2.07 | 2.64 | 1.73 | 1.87 | 2.07 | 2.64 | ns |
| LVC MOS15, Fast, 16 mA | 0.98 | 1.10 | 1.23 | 1.79 | 1.73 | 1.87 | 2.07 | 2.64 | 1.73 | 1.87 | 2.07 | 2.64 | ns |
| LVC MOS15_JEDEC, QUIETIO, 2 mA | 1.03 | 1.15 | 1.28 | 1.49 | 5.49 | 5.63 | 5.83 | 6.37 | 5.49 | 5.63 | 5.83 | 6.37 | ns |
| LVC MOS15_JEDEC, QUIETIO, 4 mA | 1.03 | 1.15 | 1.28 | 1.49 | 4.61 | 4.75 | 4.95 | 5.51 | 4.61 | 4.75 | 4.95 | 5.51 | ns |
| LVC MOS15_JEDEC, QUIETIO, 6 mA | 1.03 | 1.15 | 1.28 | 1.49 | 4.07 | 4.21 | 4.41 | 4.97 | 4.07 | 4.21 | 4.41 | 4.97 | ns |
| LVC MOS15_JEDEC, QUIETIO, 8 mA | 1.03 | 1.15 | 1.28 | 1.49 | 3.92 | 4.06 | 4.26 | 4.81 | 3.92 | 4.06 | 4.26 | 4.81 | ns |
| LVC MOS15_JEDEC, QUIETIO, 12 mA | 1.03 | 1.15 | 1.28 | 1.49 | 3.54 | 3.68 | 3.88 | 4.51 | 3.54 | 3.68 | 3.88 | 4.51 | ns |
| LVC MOS15_JEDEC, QUIETIO, 16 mA | 1.03 | 1.15 | 1.28 | 1.49 | 3.33 | 3.47 | 3.67 | 4.31 | 3.33 | 3.47 | 3.67 | 4.31 | ns |
| LVC MOS15_JEDEC, Slow, 2 mA | 1.03 | 1.15 | 1.28 | 1.49 | 4.18 | 4.32 | 4.52 | 5.13 | 4.18 | 4.32 | 4.52 | 5.13 | ns |
| LVC MOS15_JEDEC, Slow, 4 mA | 1.03 | 1.15 | 1.28 | 1.49 | 3.42 | 3.56 | 3.76 | 4.35 | 3.42 | 3.56 | 3.76 | 4.35 | ns |
| LVC MOS15_JEDEC, Slow, 6 mA | 1.03 | 1.15 | 1.28 | 1.49 | 2.29 | 2.43 | 2.63 | 3.25 | 2.29 | 2.43 | 2.63 | 3.25 | ns |
| LVC MOS15_JEDEC, Slow, 8 mA | 1.03 | 1.15 | 1.28 | 1.49 | 2.30 | 2.44 | 2.64 | 3.26 | 2.30 | 2.44 | 2.64 | 3.26 | ns |
| LVC MOS15_JEDEC, Slow, 12 mA | 1.03 | 1.15 | 1.28 | 1.49 | 2.01 | 2.15 | 2.35 | 2.97 | 2.01 | 2.15 | 2.35 | 2.97 | ns |
| LVC MOS15_JEDEC, Slow, 16 mA | 1.03 | 1.15 | 1.28 | 1.49 | 2.01 | 2.15 | 2.35 | 2.97 | 2.01 | 2.15 | 2.35 | 2.97 | ns |
| LVC MOS15_JEDEC, Fast, 2 mA | 1.03 | 1.15 | 1.28 | 1.49 | 3.28 | 3.42 | 3.62 | 4.22 | 3.28 | 3.42 | 3.62 | 4.22 | ns |
| LVC MOS15_JEDEC, Fast, 4 mA | 1.03 | 1.15 | 1.28 | 1.49 | 2.27 | 2.41 | 2.61 | 3.23 | 2.27 | 2.41 | 2.61 | 3.23 | ns |
| LVC MOS15_JEDEC, Fast, 6 mA | 1.03 | 1.15 | 1.28 | 1.49 | 1.78 | 1.92 | 2.12 | 2.74 | 1.78 | 1.92 | 2.12 | 2.74 | ns |
| LVC MOS15_JEDEC, Fast, 8 mA | 1.03 | 1.15 | 1.28 | 1.49 | 1.73 | 1.87 | 2.07 | 2.69 | 1.73 | 1.87 | 2.07 | 2.69 | ns |
| LVC MOS15_JEDEC, Fast, 12 mA | 1.03 | 1.15 | 1.28 | 1.49 | 1.73 | 1.87 | 2.07 | 2.63 | 1.73 | 1.87 | 2.07 | 2.63 | ns |
| LVC MOS15_JEDEC, Fast, 16 mA | 1.03 | 1.15 | 1.28 | 1.49 | 1.73 | 1.87 | 2.07 | 2.63 | 1.73 | 1.87 | 2.07 | 2.63 | ns |
| LVC MOS12, QUIETIO, 2 mA | 0.91 | 1.03 | 1.16 | 1.51 | 6.40 | 6.54 | 6.74 | 7.30 | 6.40 | 6.54 | 6.74 | 7.30 | ns |
| LVC MOS12, QUIETIO, 4 mA | 0.91 | 1.03 | 1.16 | 1.51 | 4.98 | 5.12 | 5.32 | 5.90 | 4.98 | 5.12 | 5.32 | 5.90 | ns |
| LVC MOS12, QUIETIO, 6 mA | 0.91 | 1.03 | 1.16 | 1.51 | 4.65 | 4.79 | 4.99 | 5.55 | 4.65 | 4.79 | 4.99 | 5.55 | ns |
| LVC MOS12, QUIETIO, 8 mA | 0.91 | 1.03 | 1.16 | 1.51 | 4.23 | 4.37 | 4.57 | 5.21 | 4.23 | 4.37 | 4.57 | 5.21 | ns |
| LVC MOS12, QUIETIO, 12 mA | 0.91 | 1.03 | 1.16 | 1.51 | 3.98 | 4.12 | 4.32 | 4.94 | 3.98 | 4.12 | 4.32 | 4.94 | ns |
| LVC MOS12, Slow, 2 mA | 0.91 | 1.03 | 1.16 | 1.51 | 4.98 | 5.12 | 5.32 | 5.91 | 4.98 | 5.12 | 5.32 | 5.91 | ns |
| LVC MOS12, Slow, 4 mA | 0.91 | 1.03 | 1.16 | 1.51 | 2.84 | 2.98 | 3.18 | 3.81 | 2.84 | 2.98 | 3.18 | 3.81 | ns |
| LVC MOS12, Slow, 6 mA | 0.91 | 1.03 | 1.16 | 1.51 | 2.77 | 2.91 | 3.11 | 3.72 | 2.77 | 2.91 | 3.11 | 3.72 | ns |
| LVC MOS12, Slow, 8 mA | 0.91 | 1.03 | 1.16 | 1.51 | 2.34 | 2.48 | 2.68 | 3.31 | 2.34 | 2.48 | 2.68 | 3.31 | ns |
| LVC MOS12, Slow, 12 mA | 0.91 | 1.03 | 1.16 | 1.51 | 2.08 | 2.22 | 2.42 | 3.06 | 2.08 | 2.22 | 2.42 | 3.06 | ns |

Table 28: IOB Switching Characteristics for the Commercial (XC) Spartan-6 Devices (Cont'd)

| I/O Standard | T_{IOPI} | | | | T_{IOOP} | | | | T_{IOTP} | | | | Units |
|---------------------------------|-------------|------|------|--------------------|-------------|------|------|--------------------|-------------|------|------|--------------------|-------|
| | Speed Grade | | | | Speed Grade | | | | Speed Grade | | | | |
| | -3 | -3N | -2 | -1L ⁽¹⁾ | -3 | -3N | -2 | -1L ⁽¹⁾ | -3 | -3N | -2 | -1L ⁽¹⁾ | |
| LVC MOS12, Fast, 2 mA | 0.91 | 1.03 | 1.16 | 1.51 | 3.46 | 3.60 | 3.80 | 4.44 | 3.46 | 3.60 | 3.80 | 4.44 | ns |
| LVC MOS12, Fast, 4 mA | 0.91 | 1.03 | 1.16 | 1.51 | 2.35 | 2.49 | 2.69 | 3.30 | 2.35 | 2.49 | 2.69 | 3.30 | ns |
| LVC MOS12, Fast, 6 mA | 0.91 | 1.03 | 1.16 | 1.51 | 1.79 | 1.93 | 2.13 | 2.75 | 1.79 | 1.93 | 2.13 | 2.75 | ns |
| LVC MOS12, Fast, 8 mA | 0.91 | 1.03 | 1.16 | 1.51 | 1.68 | 1.82 | 2.02 | 2.64 | 1.68 | 1.82 | 2.02 | 2.64 | ns |
| LVC MOS12, Fast, 12 mA | 0.91 | 1.03 | 1.16 | 1.51 | 1.66 | 1.80 | 2.00 | 2.62 | 1.66 | 1.80 | 2.00 | 2.62 | ns |
| LVC MOS12_JEDEC, QUIETIO, 2 mA | 1.50 | 1.62 | 1.75 | 1.88 | 6.39 | 6.53 | 6.73 | 7.31 | 6.39 | 6.53 | 6.73 | 7.31 | ns |
| LVC MOS12_JEDEC, QUIETIO, 4 mA | 1.50 | 1.62 | 1.75 | 1.88 | 4.98 | 5.12 | 5.32 | 5.88 | 4.98 | 5.12 | 5.32 | 5.88 | ns |
| LVC MOS12_JEDEC, QUIETIO, 6 mA | 1.50 | 1.62 | 1.75 | 1.88 | 4.67 | 4.81 | 5.01 | 5.54 | 4.67 | 4.81 | 5.01 | 5.54 | ns |
| LVC MOS12_JEDEC, QUIETIO, 8 mA | 1.50 | 1.62 | 1.75 | 1.88 | 4.23 | 4.37 | 4.57 | 5.22 | 4.23 | 4.37 | 4.57 | 5.22 | ns |
| LVC MOS12_JEDEC, QUIETIO, 12 mA | 1.50 | 1.62 | 1.75 | 1.88 | 3.99 | 4.13 | 4.33 | 4.94 | 3.99 | 4.13 | 4.33 | 4.94 | ns |
| LVC MOS12_JEDEC, Slow, 2 mA | 1.50 | 1.62 | 1.75 | 1.88 | 5.00 | 5.14 | 5.34 | 5.90 | 5.00 | 5.14 | 5.34 | 5.90 | ns |
| LVC MOS12_JEDEC, Slow, 4 mA | 1.50 | 1.62 | 1.75 | 1.88 | 2.85 | 2.99 | 3.19 | 3.80 | 2.85 | 2.99 | 3.19 | 3.80 | ns |
| LVC MOS12_JEDEC, Slow, 6 mA | 1.50 | 1.62 | 1.75 | 1.88 | 2.76 | 2.90 | 3.10 | 3.72 | 2.76 | 2.90 | 3.10 | 3.72 | ns |
| LVC MOS12_JEDEC, Slow, 8 mA | 1.50 | 1.62 | 1.75 | 1.88 | 2.35 | 2.49 | 2.69 | 3.30 | 2.35 | 2.49 | 2.69 | 3.30 | ns |
| LVC MOS12_JEDEC, Slow, 12 mA | 1.50 | 1.62 | 1.75 | 1.88 | 2.09 | 2.23 | 2.43 | 3.05 | 2.09 | 2.23 | 2.43 | 3.05 | ns |
| LVC MOS12_JEDEC, Fast, 2 mA | 1.50 | 1.62 | 1.75 | 1.88 | 3.46 | 3.60 | 3.80 | 4.42 | 3.46 | 3.60 | 3.80 | 4.42 | ns |
| LVC MOS12_JEDEC, Fast, 4 mA | 1.50 | 1.62 | 1.75 | 1.88 | 2.35 | 2.49 | 2.69 | 3.31 | 2.35 | 2.49 | 2.69 | 3.31 | ns |
| LVC MOS12_JEDEC, Fast, 6 mA | 1.50 | 1.62 | 1.75 | 1.88 | 1.79 | 1.93 | 2.13 | 2.76 | 1.79 | 1.93 | 2.13 | 2.76 | ns |
| LVC MOS12_JEDEC, Fast, 8 mA | 1.50 | 1.62 | 1.75 | 1.88 | 1.69 | 1.83 | 2.03 | 2.65 | 1.69 | 1.83 | 2.03 | 2.65 | ns |
| LVC MOS12_JEDEC, Fast, 12 mA | 1.50 | 1.62 | 1.75 | 1.88 | 1.66 | 1.80 | 2.00 | 2.62 | 1.66 | 1.80 | 2.00 | 2.62 | ns |

Notes:

1. The -1L values listed in this table are also applicable to the Spartan-6Q devices.
2. Devices with a -1L speed grade do not support Xilinx PCI IP.

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices⁽¹⁾

| I/O Standard | T_{IOPI} | | T_{IOOP} | | T_{IOTP} | | Units |
|--------------------------|-------------|------|-------------|-------|-------------|-------|-------|
| | Speed Grade | | Speed Grade | | Speed Grade | | |
| | -3 | -2 | -3 | -2 | -3 | -2 | |
| LVDS_33 | 1.24 | 1.42 | 1.69 | 1.89 | 3000 | 3000 | ns |
| LVDS_25 | 1.08 | 1.26 | 1.79 | 1.99 | 3000 | 3000 | ns |
| BLVDS_25 | 1.09 | 1.27 | 1.86 | 2.06 | 1.86 | 2.06 | ns |
| MINI_LVDS_33 | 1.25 | 1.43 | 1.71 | 1.91 | 3000 | 3000 | ns |
| MINI_LVDS_25 | 1.08 | 1.26 | 1.79 | 1.99 | 3000 | 3000 | ns |
| LVPECL_33 | 1.25 | 1.43 | N/A | N/A | N/A | N/A | ns |
| LVPECL_25 | 1.09 | 1.27 | N/A | N/A | N/A | N/A | ns |
| RSDS_33 (point to point) | 1.24 | 1.42 | 1.71 | 1.91 | 3000 | 3000 | ns |
| RSDS_25 (point to point) | 1.08 | 1.26 | 1.79 | 1.99 | 3000 | 3000 | ns |
| TMDS_33 | 1.29 | 1.47 | 1.68 | 1.88 | 3000 | 3000 | ns |
| PPDS_33 | 1.25 | 1.43 | 1.71 | 1.91 | 3000 | 3000 | ns |
| PPDS_25 | 1.08 | 1.26 | 1.82 | 2.02 | 3000 | 3000 | ns |
| PCI33_3 | 1.14 | 1.32 | 3.81 | 4.01 | 3.81 | 4.01 | ns |
| PCI66_3 | 1.14 | 1.32 | 3.81 | 4.01 | 3.81 | 4.01 | ns |
| DISPLAY_PORT | 1.09 | 1.27 | 3.29 | 3.49 | 3.29 | 3.49 | ns |
| I2C | 1.40 | 1.58 | 11.70 | 11.90 | 11.70 | 11.90 | ns |
| SMBUS | 1.40 | 1.58 | 11.70 | 11.90 | 11.70 | 11.90 | ns |
| SDIO | 1.43 | 1.61 | 2.78 | 2.98 | 2.78 | 2.98 | ns |
| MOBILE_DDR | 1.01 | 1.19 | 2.50 | 2.70 | 2.50 | 2.70 | ns |
| HSTL_I | 1.01 | 1.19 | 1.80 | 2.00 | 1.80 | 2.00 | ns |
| HSTL_II | 1.01 | 1.19 | 1.86 | 2.06 | 1.86 | 2.06 | ns |
| HSTL_III | 1.07 | 1.25 | 1.81 | 2.01 | 1.81 | 2.01 | ns |
| HSTL_I_18 | 1.05 | 1.23 | 1.91 | 2.11 | 1.91 | 2.11 | ns |
| HSTL_II_18 | 1.05 | 1.23 | 1.99 | 2.19 | 1.99 | 2.19 | ns |
| HSTL_III_18 | 1.13 | 1.31 | 1.93 | 2.13 | 1.93 | 2.13 | ns |
| SSTL3_I | 1.65 | 1.83 | 1.97 | 2.17 | 1.97 | 2.17 | ns |
| SSTL3_II | 1.65 | 1.83 | 2.15 | 2.35 | 2.15 | 2.35 | ns |
| SSTL2_I | 1.37 | 1.55 | 1.91 | 2.11 | 1.91 | 2.11 | ns |
| SSTL2_II | 1.37 | 1.55 | 2.00 | 2.20 | 2.00 | 2.20 | ns |
| SSTL18_I | 0.99 | 1.17 | 1.77 | 1.97 | 1.77 | 1.97 | ns |
| SSTL18_II | 1.00 | 1.18 | 1.80 | 2.00 | 1.80 | 2.00 | ns |
| SSTL15_II | 1.00 | 1.18 | 1.81 | 2.01 | 1.81 | 2.01 | ns |
| DIFF_HSTL_I | 1.01 | 1.19 | 1.91 | 2.11 | 1.91 | 2.11 | ns |
| DIFF_HSTL_II | 1.00 | 1.18 | 1.86 | 2.06 | 1.86 | 2.06 | ns |
| DIFF_HSTL_III | 1.00 | 1.18 | 1.83 | 2.03 | 1.83 | 2.03 | ns |
| DIFF_HSTL_I_18 | 1.04 | 1.22 | 1.93 | 2.13 | 1.93 | 2.13 | ns |
| DIFF_HSTL_II_18 | 1.04 | 1.22 | 1.83 | 2.03 | 1.83 | 2.03 | ns |
| DIFF_HSTL_III_18 | 1.04 | 1.22 | 1.83 | 2.03 | 1.83 | 2.03 | ns |

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices⁽¹⁾ (Cont'd)

| I/O Standard | T _{IOPI} | | T _{IOOP} | | T _{IOTP} | | Units |
|---------------------------|-------------------|------|-------------------|------|-------------------|------|-------|
| | Speed Grade | | Speed Grade | | Speed Grade | | |
| | -3 | -2 | -3 | -2 | -3 | -2 | |
| DIFF_SSTL3_I | 1.26 | 1.44 | 1.95 | 2.15 | 1.95 | 2.15 | ns |
| DIFF_SSTL3_II | 1.26 | 1.44 | 1.94 | 2.14 | 1.94 | 2.14 | ns |
| DIFF_SSTL2_I | 1.09 | 1.27 | 1.94 | 2.14 | 1.94 | 2.14 | ns |
| DIFF_SSTL2_II | 1.09 | 1.27 | 1.90 | 2.10 | 1.90 | 2.10 | ns |
| DIFF_SSTL18_I | 1.04 | 1.22 | 1.86 | 2.06 | 1.86 | 2.06 | ns |
| DIFF_SSTL18_II | 1.05 | 1.23 | 1.82 | 2.02 | 1.82 | 2.02 | ns |
| DIFF_SSTL15_II | 1.01 | 1.19 | 1.81 | 2.01 | 1.81 | 2.01 | ns |
| DIFF_MOBILE_DDR | 1.04 | 1.22 | 1.89 | 2.09 | 1.89 | 2.09 | ns |
| LVTTL, QUIETIO, 2 mA | 1.42 | 1.60 | 5.64 | 5.84 | 5.64 | 5.84 | ns |
| LVTTL, QUIETIO, 4 mA | 1.42 | 1.60 | 4.46 | 4.66 | 4.46 | 4.66 | ns |
| LVTTL, QUIETIO, 6 mA | 1.42 | 1.60 | 3.92 | 4.12 | 3.92 | 4.12 | ns |
| LVTTL, QUIETIO, 8 mA | 1.42 | 1.60 | 3.37 | 3.57 | 3.37 | 3.57 | ns |
| LVTTL, QUIETIO, 12 mA | 1.42 | 1.60 | 3.42 | 3.62 | 3.42 | 3.62 | ns |
| LVTTL, QUIETIO, 16 mA | 1.42 | 1.60 | 3.09 | 3.29 | 3.09 | 3.29 | ns |
| LVTTL, QUIETIO, 24 mA | 1.42 | 1.60 | 2.83 | 3.03 | 2.83 | 3.03 | ns |
| LVTTL, Slow, 2 mA | 1.42 | 1.60 | 4.58 | 4.78 | 4.58 | 4.78 | ns |
| LVTTL, Slow, 4 mA | 1.42 | 1.60 | 3.38 | 3.58 | 3.38 | 3.58 | ns |
| LVTTL, Slow, 6 mA | 1.42 | 1.60 | 2.95 | 3.15 | 2.95 | 3.15 | ns |
| LVTTL, Slow, 8 mA | 1.42 | 1.60 | 2.73 | 2.93 | 2.73 | 2.93 | ns |
| LVTTL, Slow, 12 mA | 1.42 | 1.60 | 2.72 | 2.92 | 2.72 | 2.92 | ns |
| LVTTL, Slow, 16 mA | 1.42 | 1.60 | 2.53 | 2.73 | 2.53 | 2.73 | ns |
| LVTTL, Slow, 24 mA | 1.42 | 1.60 | 2.42 | 2.62 | 2.42 | 2.62 | ns |
| LVTTL, Fast, 2 mA | 1.42 | 1.60 | 4.04 | 4.24 | 4.04 | 4.24 | ns |
| LVTTL, Fast, 4 mA | 1.42 | 1.60 | 2.66 | 2.86 | 2.66 | 2.86 | ns |
| LVTTL, Fast, 6 mA | 1.42 | 1.60 | 2.58 | 2.78 | 2.58 | 2.78 | ns |
| LVTTL, Fast, 8 mA | 1.42 | 1.60 | 2.46 | 2.66 | 2.46 | 2.66 | ns |
| LVTTL, Fast, 12 mA | 1.42 | 1.60 | 1.97 | 2.17 | 1.97 | 2.17 | ns |
| LVTTL, Fast, 16 mA | 1.42 | 1.60 | 1.97 | 2.17 | 1.97 | 2.17 | ns |
| LVTTL, Fast, 24 mA | 1.42 | 1.60 | 1.97 | 2.17 | 1.97 | 2.17 | ns |
| LVC MOS33, QUIETIO, 2 mA | 1.41 | 1.59 | 5.65 | 5.85 | 5.65 | 5.85 | ns |
| LVC MOS33, QUIETIO, 4 mA | 1.41 | 1.59 | 4.20 | 4.40 | 4.20 | 4.40 | ns |
| LVC MOS33, QUIETIO, 6 mA | 1.41 | 1.59 | 3.65 | 3.85 | 3.65 | 3.85 | ns |
| LVC MOS33, QUIETIO, 8 mA | 1.41 | 1.59 | 3.51 | 3.71 | 3.51 | 3.71 | ns |
| LVC MOS33, QUIETIO, 12 mA | 1.41 | 1.59 | 3.09 | 3.29 | 3.09 | 3.29 | ns |
| LVC MOS33, QUIETIO, 16 mA | 1.41 | 1.59 | 2.91 | 3.11 | 2.91 | 3.11 | ns |
| LVC MOS33, QUIETIO, 24 mA | 1.41 | 1.59 | 2.73 | 2.93 | 2.73 | 2.93 | ns |
| LVC MOS33, Slow, 2 mA | 1.41 | 1.59 | 4.59 | 4.79 | 4.59 | 4.79 | ns |
| LVC MOS33, Slow, 4 mA | 1.41 | 1.59 | 3.14 | 3.34 | 3.14 | 3.34 | ns |

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices⁽¹⁾ (Cont'd)

| I/O Standard | T _{IOPI} | | T _{IOOP} | | T _{IOTP} | | Units |
|---------------------------|-------------------|------|-------------------|------|-------------------|------|-------|
| | Speed Grade | | Speed Grade | | Speed Grade | | |
| | -3 | -2 | -3 | -2 | -3 | -2 | |
| LVC MOS33, Slow, 6 mA | 1.41 | 1.59 | 2.79 | 2.99 | 2.79 | 2.99 | ns |
| LVC MOS33, Slow, 8 mA | 1.41 | 1.59 | 2.79 | 2.99 | 2.79 | 2.99 | ns |
| LVC MOS33, Slow, 12 mA | 1.41 | 1.59 | 2.53 | 2.73 | 2.53 | 2.73 | ns |
| LVC MOS33, Slow, 16 mA | 1.41 | 1.59 | 2.45 | 2.65 | 2.45 | 2.65 | ns |
| LVC MOS33, Slow, 24 mA | 1.41 | 1.59 | 2.42 | 2.62 | 2.42 | 2.62 | ns |
| LVC MOS33, Fast, 2 mA | 1.41 | 1.59 | 4.05 | 4.25 | 4.05 | 4.25 | ns |
| LVC MOS33, Fast, 4 mA | 1.41 | 1.59 | 2.66 | 2.86 | 2.66 | 2.86 | ns |
| LVC MOS33, Fast, 6 mA | 1.41 | 1.59 | 2.46 | 2.66 | 2.46 | 2.66 | ns |
| LVC MOS33, Fast, 8 mA | 1.41 | 1.59 | 2.21 | 2.41 | 2.21 | 2.41 | ns |
| LVC MOS33, Fast, 12 mA | 1.41 | 1.59 | 1.80 | 2.00 | 1.80 | 2.00 | ns |
| LVC MOS33, Fast, 16 mA | 1.41 | 1.59 | 1.80 | 2.00 | 1.80 | 2.00 | ns |
| LVC MOS33, Fast, 24 mA | 1.41 | 1.59 | 1.80 | 2.00 | 1.80 | 2.00 | ns |
| LVC MOS25, QUIETIO, 2 mA | 0.89 | 1.07 | 5.00 | 5.20 | 5.00 | 5.20 | ns |
| LVC MOS25, QUIETIO, 4 mA | 0.89 | 1.07 | 3.85 | 4.05 | 3.85 | 4.05 | ns |
| LVC MOS25, QUIETIO, 6 mA | 0.89 | 1.07 | 3.60 | 3.80 | 3.60 | 3.80 | ns |
| LVC MOS25, QUIETIO, 8 mA | 0.89 | 1.07 | 3.34 | 3.54 | 3.34 | 3.54 | ns |
| LVC MOS25, QUIETIO, 12 mA | 0.89 | 1.07 | 2.98 | 3.18 | 2.98 | 3.18 | ns |
| LVC MOS25, QUIETIO, 16 mA | 0.89 | 1.07 | 2.79 | 2.99 | 2.79 | 2.99 | ns |
| LVC MOS25, QUIETIO, 24 mA | 0.89 | 1.07 | 2.64 | 2.84 | 2.64 | 2.84 | ns |
| LVC MOS25, Slow, 2 mA | 0.89 | 1.07 | 3.96 | 4.16 | 3.96 | 4.16 | ns |
| LVC MOS25, Slow, 4 mA | 0.89 | 1.07 | 2.96 | 3.16 | 2.96 | 3.16 | ns |
| LVC MOS25, Slow, 6 mA | 0.89 | 1.07 | 2.88 | 3.08 | 2.88 | 3.08 | ns |
| LVC MOS25, Slow, 8 mA | 0.89 | 1.07 | 2.63 | 2.83 | 2.63 | 2.83 | ns |
| LVC MOS25, Slow, 12 mA | 0.89 | 1.07 | 2.15 | 2.35 | 2.15 | 2.35 | ns |
| LVC MOS25, Slow, 16 mA | 0.89 | 1.07 | 2.15 | 2.35 | 2.15 | 2.35 | ns |
| LVC MOS25, Slow, 24 mA | 0.89 | 1.07 | 2.15 | 2.35 | 2.15 | 2.35 | ns |
| LVC MOS25, Fast, 2 mA | 0.89 | 1.07 | 3.52 | 3.72 | 3.52 | 3.72 | ns |
| LVC MOS25, Fast, 4 mA | 0.89 | 1.07 | 2.43 | 2.63 | 2.43 | 2.63 | ns |
| LVC MOS25, Fast, 6 mA | 0.89 | 1.07 | 2.23 | 2.43 | 2.23 | 2.43 | ns |
| LVC MOS25, Fast, 8 mA | 0.89 | 1.07 | 2.16 | 2.36 | 2.16 | 2.36 | ns |
| LVC MOS25, Fast, 12 mA | 0.89 | 1.07 | 1.70 | 1.90 | 1.70 | 1.90 | ns |
| LVC MOS25, Fast, 16 mA | 0.89 | 1.07 | 1.70 | 1.90 | 1.70 | 1.90 | ns |
| LVC MOS25, Fast, 24 mA | 0.89 | 1.07 | 1.70 | 1.90 | 1.70 | 1.90 | ns |
| LVC MOS18, QUIETIO, 2 mA | 1.25 | 1.43 | 6.11 | 6.31 | 6.11 | 6.31 | ns |
| LVC MOS18, QUIETIO, 4 mA | 1.25 | 1.43 | 4.88 | 5.08 | 4.88 | 5.08 | ns |
| LVC MOS18, QUIETIO, 6 mA | 1.25 | 1.43 | 4.20 | 4.40 | 4.20 | 4.40 | ns |
| LVC MOS18, QUIETIO, 8 mA | 1.25 | 1.43 | 3.86 | 4.06 | 3.86 | 4.06 | ns |
| LVC MOS18, QUIETIO, 12 mA | 1.25 | 1.43 | 3.49 | 3.69 | 3.49 | 3.69 | ns |

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices⁽¹⁾ (Cont'd)

| I/O Standard | T _{IOPI} | | T _{IOOP} | | T _{IO TP} | | Units |
|---------------------------------|-------------------|------|-------------------|------|--------------------|------|-------|
| | Speed Grade | | Speed Grade | | Speed Grade | | |
| | -3 | -2 | -3 | -2 | -3 | -2 | |
| LVC MOS18, QUIETIO, 16 mA | 1.25 | 1.43 | 3.34 | 3.54 | 3.34 | 3.54 | ns |
| LVC MOS18, QUIETIO, 24 mA | 1.25 | 1.43 | 3.18 | 3.38 | 3.18 | 3.38 | ns |
| LVC MOS18, Slow, 2 mA | 1.25 | 1.43 | 4.79 | 4.99 | 4.79 | 4.99 | ns |
| LVC MOS18, Slow, 4 mA | 1.25 | 1.43 | 3.84 | 4.04 | 3.84 | 4.04 | ns |
| LVC MOS18, Slow, 6 mA | 1.25 | 1.43 | 3.17 | 3.37 | 3.17 | 3.37 | ns |
| LVC MOS18, Slow, 8 mA | 1.25 | 1.43 | 2.37 | 2.57 | 2.37 | 2.57 | ns |
| LVC MOS18, Slow, 12 mA | 1.25 | 1.43 | 2.13 | 2.33 | 2.13 | 2.33 | ns |
| LVC MOS18, Slow, 16 mA | 1.25 | 1.43 | 2.13 | 2.33 | 2.13 | 2.33 | ns |
| LVC MOS18, Slow, 24 mA | 1.25 | 1.43 | 2.13 | 2.33 | 2.13 | 2.33 | ns |
| LVC MOS18, Fast, 2 mA | 1.25 | 1.43 | 3.78 | 3.98 | 3.78 | 3.98 | ns |
| LVC MOS18, Fast, 4 mA | 1.25 | 1.43 | 2.54 | 2.74 | 2.54 | 2.74 | ns |
| LVC MOS18, Fast, 6 mA | 1.25 | 1.43 | 2.02 | 2.22 | 2.02 | 2.22 | ns |
| LVC MOS18, Fast, 8 mA | 1.25 | 1.43 | 1.95 | 2.15 | 1.95 | 2.15 | ns |
| LVC MOS18, Fast, 12 mA | 1.25 | 1.43 | 1.85 | 2.05 | 1.85 | 2.05 | ns |
| LVC MOS18, Fast, 16 mA | 1.25 | 1.43 | 1.85 | 2.05 | 1.85 | 2.05 | ns |
| LVC MOS18, Fast, 24 mA | 1.25 | 1.43 | 1.85 | 2.05 | 1.85 | 2.05 | ns |
| LVC MOS18_JEDEC, QUIETIO, 2 mA | 1.01 | 1.19 | 6.09 | 6.29 | 6.09 | 6.29 | ns |
| LVC MOS18_JEDEC, QUIETIO, 4 mA | 1.01 | 1.19 | 4.89 | 5.09 | 4.89 | 5.09 | ns |
| LVC MOS18_JEDEC, QUIETIO, 6 mA | 1.01 | 1.19 | 4.20 | 4.40 | 4.20 | 4.40 | ns |
| LVC MOS18_JEDEC, QUIETIO, 8 mA | 1.01 | 1.19 | 3.87 | 4.07 | 3.87 | 4.07 | ns |
| LVC MOS18_JEDEC, QUIETIO, 12 mA | 1.01 | 1.19 | 3.49 | 3.69 | 3.49 | 3.69 | ns |
| LVC MOS18_JEDEC, QUIETIO, 16 mA | 1.01 | 1.19 | 3.34 | 3.54 | 3.34 | 3.54 | ns |
| LVC MOS18_JEDEC, QUIETIO, 24 mA | 1.01 | 1.19 | 3.17 | 3.37 | 3.17 | 3.37 | ns |
| LVC MOS18_JEDEC, Slow, 2 mA | 1.01 | 1.19 | 4.79 | 4.99 | 4.79 | 4.99 | ns |
| LVC MOS18_JEDEC, Slow, 4 mA | 1.01 | 1.19 | 3.84 | 4.04 | 3.84 | 4.04 | ns |
| LVC MOS18_JEDEC, Slow, 6 mA | 1.01 | 1.19 | 3.18 | 3.38 | 3.18 | 3.38 | ns |
| LVC MOS18_JEDEC, Slow, 8 mA | 1.01 | 1.19 | 2.37 | 2.57 | 2.37 | 2.57 | ns |
| LVC MOS18_JEDEC, Slow, 12 mA | 1.01 | 1.19 | 2.13 | 2.33 | 2.13 | 2.33 | ns |
| LVC MOS18_JEDEC, Slow, 16 mA | 1.01 | 1.19 | 2.13 | 2.33 | 2.13 | 2.33 | ns |
| LVC MOS18_JEDEC, Slow, 24 mA | 1.01 | 1.19 | 2.13 | 2.33 | 2.13 | 2.33 | ns |
| LVC MOS18_JEDEC, Fast, 2 mA | 1.01 | 1.19 | 3.75 | 3.95 | 3.75 | 3.95 | ns |
| LVC MOS18_JEDEC, Fast, 4 mA | 1.01 | 1.19 | 2.54 | 2.74 | 2.54 | 2.74 | ns |
| LVC MOS18_JEDEC, Fast, 6 mA | 1.01 | 1.19 | 2.02 | 2.22 | 2.02 | 2.22 | ns |
| LVC MOS18_JEDEC, Fast, 8 mA | 1.01 | 1.19 | 1.94 | 2.14 | 1.94 | 2.14 | ns |
| LVC MOS18_JEDEC, Fast, 12 mA | 1.01 | 1.19 | 1.86 | 2.06 | 1.86 | 2.06 | ns |
| LVC MOS18_JEDEC, Fast, 16 mA | 1.01 | 1.19 | 1.86 | 2.06 | 1.86 | 2.06 | ns |
| LVC MOS18_JEDEC, Fast, 24 mA | 1.01 | 1.19 | 1.86 | 2.06 | 1.86 | 2.06 | ns |

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices⁽¹⁾ (Cont'd)

| I/O Standard | T _{IOPI} | | T _{IOOP} | | T _{IOTP} | | Units |
|---------------------------------|-------------------|------|-------------------|------|-------------------|------|-------|
| | Speed Grade | | Speed Grade | | Speed Grade | | |
| | -3 | -2 | -3 | -2 | -3 | -2 | |
| LVC MOS15, QUIETIO, 2 mA | 1.05 | 1.23 | 5.63 | 5.83 | 5.63 | 5.83 | ns |
| LVC MOS15, QUIETIO, 4 mA | 1.05 | 1.23 | 4.75 | 4.95 | 4.75 | 4.95 | ns |
| LVC MOS15, QUIETIO, 6 mA | 1.05 | 1.23 | 4.21 | 4.41 | 4.21 | 4.41 | ns |
| LVC MOS15, QUIETIO, 8 mA | 1.05 | 1.23 | 4.05 | 4.25 | 4.05 | 4.25 | ns |
| LVC MOS15, QUIETIO, 12 mA | 1.05 | 1.23 | 3.74 | 3.94 | 3.74 | 3.94 | ns |
| LVC MOS15, QUIETIO, 16 mA | 1.05 | 1.23 | 3.52 | 3.72 | 3.52 | 3.72 | ns |
| LVC MOS15, Slow, 2 mA | 1.05 | 1.23 | 4.32 | 4.52 | 4.32 | 4.52 | ns |
| LVC MOS15, Slow, 4 mA | 1.05 | 1.23 | 3.58 | 3.78 | 3.58 | 3.78 | ns |
| LVC MOS15, Slow, 6 mA | 1.05 | 1.23 | 2.45 | 2.65 | 2.45 | 2.65 | ns |
| LVC MOS15, Slow, 8 mA | 1.05 | 1.23 | 2.46 | 2.66 | 2.46 | 2.66 | ns |
| LVC MOS15, Slow, 12 mA | 1.05 | 1.23 | 2.17 | 2.37 | 2.17 | 2.37 | ns |
| LVC MOS15, Slow, 16 mA | 1.05 | 1.23 | 2.15 | 2.35 | 2.15 | 2.35 | ns |
| LVC MOS15, Fast, 2 mA | 1.05 | 1.23 | 3.43 | 3.63 | 3.43 | 3.63 | ns |
| LVC MOS15, Fast, 4 mA | 1.05 | 1.23 | 2.42 | 2.62 | 2.42 | 2.62 | ns |
| LVC MOS15, Fast, 6 mA | 1.05 | 1.23 | 1.92 | 2.12 | 1.92 | 2.12 | ns |
| LVC MOS15, Fast, 8 mA | 1.05 | 1.23 | 1.87 | 2.07 | 1.87 | 2.07 | ns |
| LVC MOS15, Fast, 12 mA | 1.05 | 1.23 | 1.87 | 2.07 | 1.87 | 2.07 | ns |
| LVC MOS15, Fast, 16 mA | 1.05 | 1.23 | 1.87 | 2.07 | 1.87 | 2.07 | ns |
| LVC MOS15_JEDEC, QUIETIO, 2 mA | 1.10 | 1.28 | 5.64 | 5.84 | 5.64 | 5.84 | ns |
| LVC MOS15_JEDEC, QUIETIO, 4 mA | 1.10 | 1.28 | 4.75 | 4.95 | 4.75 | 4.95 | ns |
| LVC MOS15_JEDEC, QUIETIO, 6 mA | 1.10 | 1.28 | 4.21 | 4.41 | 4.21 | 4.41 | ns |
| LVC MOS15_JEDEC, QUIETIO, 8 mA | 1.10 | 1.28 | 4.06 | 4.26 | 4.06 | 4.26 | ns |
| LVC MOS15_JEDEC, QUIETIO, 12 mA | 1.10 | 1.28 | 3.75 | 3.95 | 3.75 | 3.95 | ns |
| LVC MOS15_JEDEC, QUIETIO, 16 mA | 1.10 | 1.28 | 3.53 | 3.73 | 3.53 | 3.73 | ns |
| LVC MOS15_JEDEC, Slow, 2 mA | 1.10 | 1.28 | 4.32 | 4.52 | 4.32 | 4.52 | ns |
| LVC MOS15_JEDEC, Slow, 4 mA | 1.10 | 1.28 | 3.56 | 3.76 | 3.56 | 3.76 | ns |
| LVC MOS15_JEDEC, Slow, 6 mA | 1.10 | 1.28 | 2.44 | 2.64 | 2.44 | 2.64 | ns |
| LVC MOS15_JEDEC, Slow, 8 mA | 1.10 | 1.28 | 2.47 | 2.67 | 2.47 | 2.67 | ns |
| LVC MOS15_JEDEC, Slow, 12 mA | 1.10 | 1.28 | 2.15 | 2.35 | 2.15 | 2.35 | ns |
| LVC MOS15_JEDEC, Slow, 16 mA | 1.10 | 1.28 | 2.15 | 2.35 | 2.15 | 2.35 | ns |
| LVC MOS15_JEDEC, Fast, 2 mA | 1.10 | 1.28 | 3.43 | 3.63 | 3.43 | 3.63 | ns |
| LVC MOS15_JEDEC, Fast, 4 mA | 1.10 | 1.28 | 2.42 | 2.62 | 2.42 | 2.62 | ns |
| LVC MOS15_JEDEC, Fast, 6 mA | 1.10 | 1.28 | 1.92 | 2.12 | 1.92 | 2.12 | ns |
| LVC MOS15_JEDEC, Fast, 8 mA | 1.10 | 1.28 | 1.87 | 2.07 | 1.87 | 2.07 | ns |
| LVC MOS15_JEDEC, Fast, 12 mA | 1.10 | 1.28 | 1.87 | 2.07 | 1.87 | 2.07 | ns |
| LVC MOS15_JEDEC, Fast, 16 mA | 1.10 | 1.28 | 1.87 | 2.07 | 1.87 | 2.07 | ns |
| LVC MOS12, QUIETIO, 2 mA | 0.98 | 1.16 | 6.54 | 6.74 | 6.54 | 6.74 | ns |
| LVC MOS12, QUIETIO, 4 mA | 0.98 | 1.16 | 5.12 | 5.32 | 5.12 | 5.32 | ns |

Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices⁽¹⁾ (Cont'd)

| I/O Standard | T _{IOPI} | | T _{IOOP} | | T _{IOTP} | | Units |
|---------------------------------|-------------------|------|-------------------|------|-------------------|------|-------|
| | Speed Grade | | Speed Grade | | Speed Grade | | |
| | -3 | -2 | -3 | -2 | -3 | -2 | |
| LVC MOS12, QUIETIO, 6 mA | 0.98 | 1.16 | 4.79 | 4.99 | 4.79 | 4.99 | ns |
| LVC MOS12, QUIETIO, 8 mA | 0.98 | 1.16 | 4.43 | 4.63 | 4.43 | 4.63 | ns |
| LVC MOS12, QUIETIO, 12 mA | 0.98 | 1.16 | 4.18 | 4.38 | 4.18 | 4.38 | ns |
| LVC MOS12, Slow, 2 mA | 0.98 | 1.16 | 5.12 | 5.32 | 5.12 | 5.32 | ns |
| LVC MOS12, Slow, 4 mA | 0.98 | 1.16 | 3.00 | 3.20 | 3.00 | 3.20 | ns |
| LVC MOS12, Slow, 6 mA | 0.98 | 1.16 | 2.91 | 3.11 | 2.91 | 3.11 | ns |
| LVC MOS12, Slow, 8 mA | 0.98 | 1.16 | 2.51 | 2.71 | 2.51 | 2.71 | ns |
| LVC MOS12, Slow, 12 mA | 0.98 | 1.16 | 2.25 | 2.45 | 2.25 | 2.45 | ns |
| LVC MOS12, Fast, 2 mA | 0.98 | 1.16 | 3.60 | 3.80 | 3.60 | 3.80 | ns |
| LVC MOS12, Fast, 4 mA | 0.98 | 1.16 | 2.49 | 2.69 | 2.49 | 2.69 | ns |
| LVC MOS12, Fast, 6 mA | 0.98 | 1.16 | 1.94 | 2.14 | 1.94 | 2.14 | ns |
| LVC MOS12, Fast, 8 mA | 0.98 | 1.16 | 1.82 | 2.02 | 1.82 | 2.02 | ns |
| LVC MOS12, Fast, 12 mA | 0.98 | 1.16 | 1.80 | 2.00 | 1.80 | 2.00 | ns |
| LVC MOS12_JEDEC, QUIETIO, 2 mA | 1.57 | 1.75 | 6.53 | 6.73 | 6.53 | 6.73 | ns |
| LVC MOS12_JEDEC, QUIETIO, 4 mA | 1.57 | 1.75 | 5.12 | 5.32 | 5.12 | 5.32 | ns |
| LVC MOS12_JEDEC, QUIETIO, 6 mA | 1.57 | 1.75 | 4.81 | 5.01 | 4.81 | 5.01 | ns |
| LVC MOS12_JEDEC, QUIETIO, 8 mA | 1.57 | 1.75 | 4.44 | 4.64 | 4.44 | 4.64 | ns |
| LVC MOS12_JEDEC, QUIETIO, 12 mA | 1.57 | 1.75 | 4.20 | 4.40 | 4.20 | 4.40 | ns |
| LVC MOS12_JEDEC, Slow, 2 mA | 1.57 | 1.75 | 5.14 | 5.34 | 5.14 | 5.34 | ns |
| LVC MOS12_JEDEC, Slow, 4 mA | 1.57 | 1.75 | 2.99 | 3.19 | 2.99 | 3.19 | ns |
| LVC MOS12_JEDEC, Slow, 6 mA | 1.57 | 1.75 | 2.90 | 3.10 | 2.90 | 3.10 | ns |
| LVC MOS12_JEDEC, Slow, 8 mA | 1.57 | 1.75 | 2.50 | 2.70 | 2.50 | 2.70 | ns |
| LVC MOS12_JEDEC, Slow, 12 mA | 1.57 | 1.75 | 2.26 | 2.46 | 2.26 | 2.46 | ns |
| LVC MOS12_JEDEC, Fast, 2 mA | 1.57 | 1.75 | 3.60 | 3.80 | 3.60 | 3.80 | ns |
| LVC MOS12_JEDEC, Fast, 4 mA | 1.57 | 1.75 | 2.49 | 2.69 | 2.49 | 2.69 | ns |
| LVC MOS12_JEDEC, Fast, 6 mA | 1.57 | 1.75 | 1.94 | 2.14 | 1.94 | 2.14 | ns |
| LVC MOS12_JEDEC, Fast, 8 mA | 1.57 | 1.75 | 1.83 | 2.03 | 1.83 | 2.03 | ns |
| LVC MOS12_JEDEC, Fast, 12 mA | 1.57 | 1.75 | 1.80 | 2.00 | 1.80 | 2.00 | ns |

Notes:

1. The Spartan-6Q FPGA -1L values are listed in Table 28.

Table 30 summarizes the value of T_{IOTPHZ}. T_{IOTPHZ} is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). These delays are measured using LVC MOS25, Fast, 12 mA.

Table 30: IOB 3-state ON Output Switching Characteristics (T_{IOTPHZ})

| Symbol | Description | Speed Grade | | | | Units |
|---------------------|-------------------------------|-------------|------|------|------|-------|
| | | -3 | -3N | -2 | -1L | |
| T _{IOTPHZ} | T input to Pad high-impedance | 1.39 | 1.59 | 1.59 | 1.91 | ns |

I/O Standard Measurement Methodology

Input Delay Measurements

Table 31 shows the test setup parameters used for measuring input delay.

Table 31: Input Delay Measurement Methodology

| Description | I/O Standard Attribute | $V_L^{(1)}$ | $V_H^{(1)}$ | $V_{MEAS}^{(3)(4)}$ | $V_{REF}^{(2)(4)}$ |
|--|----------------------------|-----------------------|------------------|---------------------|--------------------|
| LVTTTL (Low-Voltage Transistor-Transistor Logic) | LVTTTL | 0 | 3.0 | 1.4 | – |
| LVC MOS (Low-Voltage CMOS), 3.3V | LVC MOS33 | 0 | 3.3 | 1.65 | – |
| LVC MOS, 2.5V | LVC MOS25 | 0 | 2.5 | 1.25 | – |
| LVC MOS, 1.8V | LVC MOS18 | 0 | 1.8 | 0.9 | – |
| LVC MOS, 1.5V | LVC MOS15 | 0 | 1.5 | 0.75 | – |
| LVC MOS, 1.2V | LVC MOS12 | 0 | 1.2 | 0.6 | – |
| PCI (Peripheral Component Interface), 33 MHz and 66 MHz, 3.3V | PCI33_3, PCI66_3 | Per PCI Specification | | | – |
| HSTL (High-Speed Transceiver Logic), Class I & II | HSTL_I, HSTL_II | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | V_{REF} | 0.75 |
| HSTL, Class III | HSTL_III | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | V_{REF} | 0.90 |
| HSTL, Class I & II, 1.8V | HSTL_I_18, HSTL_II_18 | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | V_{REF} | 0.90 |
| HSTL, Class III 1.8V | HSTL_III_18 | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | V_{REF} | 1.1 |
| SSTL (Stub Terminated Transceiver Logic), Class I & II, 3.3V | SSTL3_I, SSTL3_II | $V_{REF} - 0.75$ | $V_{REF} + 0.75$ | V_{REF} | 1.5 |
| SSTL, Class I & II, 2.5V | SSTL2_I, SSTL2_II | $V_{REF} - 0.75$ | $V_{REF} + 0.75$ | V_{REF} | 1.25 |
| SSTL, Class I & II, 1.8V | SSTL18_I, SSTL18_II | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | V_{REF} | 0.90 |
| SSTL, Class II, 1.5V | SSTL15_II | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | V_{REF} | 0.75 |
| LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V | LVDS_25, LVDS_33 | $1.25 - 0.125$ | $1.25 + 0.125$ | 0 ⁽⁵⁾ | – |
| LVPECL (Low-Voltage Positive Emitter-Coupled Logic), 2.5V & 3.3V | LVPECL_25, LVPECL_33 | $1.2 - 0.3$ | $1.2 + 0.3$ | 0 ⁽⁵⁾ | – |
| BLVDS (Bus LVDS), 2.5V | BLVDS_25 | $1.3 - 0.125$ | $1.3 + 0.125$ | 0 ⁽⁵⁾ | – |
| Mini-LVDS, 2.5V & 3.3V | MINI_LVDS_25, MINI_LVDS_33 | $1.2 - 0.125$ | $1.2 + 0.125$ | 0 ⁽⁵⁾ | – |
| RS DS (Reduced Swing Differential Signaling), 2.5V & 3.3V | RS DS_25, RS DS_33 | $1.2 - 0.1$ | $1.2 + 0.1$ | 0 ⁽⁵⁾ | – |
| TMDS (Transition Minimized Differential Signaling), 3.3V | TMDS_33 | $3.0 - 0.1$ | $3.0 + 0.1$ | 0 ⁽⁵⁾ | – |
| PPDS (Point-to-Point Differential Signaling), 2.5V & 3.3V | PPDS_25, PPDS_33 | $1.25 - 0.1$ | $1.25 + 0.1$ | 0 ⁽⁵⁾ | – |

Notes:

1. Input waveform switches between V_L and V_H .
2. Measurements are made at typical, minimum, and maximum V_{REF} values. Reported delays reflect worst case of these measurements. V_{REF} values listed are typical.
3. Input voltage level from which measurement starts.
4. This is an input voltage reference that bears no relation to the V_{REF} / V_{MEAS} parameters found in IBIS models and/or noted in Figure 4.
5. The value given is the differential input voltage.

Output Delay Measurements

Output delays are measured using a Tektronix P6245 TDS500/600 probe (< 1 pF) across approximately 4" of FR4 microstrip trace. Standard termination was used for all testing. The propagation delay of the 4" trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 4 and Figure 5.



Figure 4: Single-Ended Test Setup



ds162_07_011309

Figure 5: Differential Test Setup

Measurements and test conditions are reflected in the IBIS models except where the IBIS format precludes it. Parameters V_{REF} , R_{REF} , C_{REF} , and V_{MEAS} fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using the following method:

1. Simulate the output driver of choice into the generalized test setup, using values from Table 32.
2. Record the time to V_{MEAS} .
3. Simulate the output driver of choice into the actual PCB trace and load, using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to V_{MEAS} .
5. Compare the results of steps 2 and 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 32: Output Delay Measurement Methodology

| Description | I/O Standard Attribute | R_{REF} (Ω) | C_{REF} ⁽¹⁾ (pF) | V_{MEAS} (V) | V_{REF} (V) |
|---|---------------------------------|------------------------|-------------------------------|----------------|---------------|
| LVTTTL (Low-Voltage Transistor-Transistor Logic) | LVTTTL (all) | 1M | 0 | 1.4 | 0 |
| LVC MOS (Low-Voltage CMOS), 3.3V | LVC MOS33 | 1M | 0 | 1.65 | 0 |
| LVC MOS, 2.5V | LVC MOS25 | 1M | 0 | 1.25 | 0 |
| LVC MOS, 1.8V | LVC MOS18 | 1M | 0 | 0.9 | 0 |
| LVC MOS, 1.5V | LVC MOS15 | 1M | 0 | 0.75 | 0 |
| LVC MOS, 1.2V | LVC MOS12 | 1M | 0 | 0.6 | 0 |
| PCI (Peripheral Component Interface) 33 MHz and 66 MHz, 3.3V | PCI33_3, PCI66_3 (rising edge) | 25 | 10 ⁽²⁾ | 0.94 | 0 |
| | PCI33_3, PCI66_3 (falling edge) | 25 | 10 ⁽²⁾ | 2.03 | 3.3 |
| HSTL (High-Speed Transceiver Logic), Class I | HSTL_I | 50 | 0 | V_{REF} | 0.75 |
| HSTL, Class II | HSTL_II | 25 | 0 | V_{REF} | 0.75 |
| HSTL, Class III | HSTL_III | 50 | 0 | 0.9 | 1.5 |
| HSTL, Class I, 1.8V | HSTL_I_18 | 50 | 0 | V_{REF} | 0.9 |
| HSTL, Class II, 1.8V | HSTL_II_18 | 25 | 0 | V_{REF} | 0.9 |
| HSTL, Class III, 1.8V | HSTL_III_18 | 50 | 0 | 1.1 | 1.8 |
| SSTL (Stub Series Terminated Logic), Class I, 1.8V | SSTL18_I | 50 | 0 | V_{REF} | 0.9 |
| SSTL, Class II, 1.8V | SSTL18_II | 25 | 0 | V_{REF} | 0.9 |
| SSTL, Class I, 2.5V | SSTL2_I | 50 | 0 | V_{REF} | 1.25 |

Table 32: Output Delay Measurement Methodology (Cont'd)

| Description | I/O Standard Attribute | R _{REF} (Ω) | C _{REF} ⁽¹⁾ (pF) | V _{MEAS} (V) | V _{REF} (V) |
|---|----------------------------|----------------------|--------------------------------------|-----------------------|----------------------|
| SSTL, Class II, 2.5V | SSTL2_II | 25 | 0 | V _{REF} | 1.25 |
| SSTL, Class II, 1.5V | SSTL15_II | 25 | 0 | V _{REF} | 0.75 |
| LVDS (Low-Voltage Differential Signaling), 2.5V & 3.3V | LVDS_25, LVDS_33 | 100 | 0 | 0 ⁽³⁾ | – |
| BLVDS (Bus LVDS), 2.5V | BLVDS_25 | Note 4 | 0 | 0 ⁽³⁾ | – |
| Mini-LVDS, 2.5V & 3.3V | MINI_LVDS_25, MINI_LVDS_33 | 100 | 0 | 0 ⁽³⁾ | – |
| RSDS (Reduced Swing Differential Signaling), 2.5V & 3.3V | RSDS_25, RSDS_33 | 100 | 0 | 0 ⁽³⁾ | – |
| TMDS (Transition Minimized Differential Signaling), 3.3V | TMDS_33 | Note 5 | 0 | 0 ⁽³⁾ | – |
| PPDS (Point-to-Point Differential Signaling, 2.5V & 3.3V) | PPDS_25, PPDS_33 | 100 | 0 | 0 ⁽³⁾ | – |

Notes:

1. C_{REF} is the capacitance of the probe, nominally 0 pF.
2. Per PCI specifications.
3. The value given is the differential output voltage.
4. See the *BLVDS Output Termination* section in [UG381](#), *Spartan-6 FPGA SelectIO Resources User Guide*.
5. See the *TMDS_33 Termination* section in [UG381](#), *Spartan-6 FPGA SelectIO Resources User Guide*.

Simultaneously Switching Outputs

Due to package electrical parasitics, a given package supports a limited number of simultaneous switching outputs (SSOs) when using fast, high-drive outputs. [Table 33](#) and [Table 34](#) provide guidelines for the recommended maximum allowable number of SSOs. These guidelines describe the maximum number of user I/O pins of an output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise for that particular signal standard. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of GND and power bounce.

For each device/package combination, [Table 33](#) provides the number of equivalent V_{CCO}/GND pairs per bank. For each output signal standard and drive strength, [Table 34](#) recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The guidelines are categorized by package style, slew rate, and output drive current. The number of SSOs are also specified by I/O bank. Multiply the appropriate numbers from each table to calculate the maximum number of SSOs allowed within an I/O bank. The guidelines assume that all pins within a bank use the same I/O standard. Although in general lower DRIVE settings improve SSO characteristics, in some instances higher DRIVE settings improve SSO values because they also improve noise margin. Analysis using the PlanAhead tool supports mixed standards within a bank. Exceeding these SSO guidelines can result in increased power or GND bounce, degraded signal integrity, or increased system jitter. For a given I/O standard, if the SSO limit per pair in [Table 34](#) is greater than the maximum I/O per pair in [Table 33](#), then there is no SSO limit for the exclusive use of that I/O standard.

The recommended maximum SSO values assume that the FPGA is soldered on a printed circuit board and that the board uses sound design practices. Due to the additional inductance introduced by the socket, the SSO values do not apply for FPGAs mounted in sockets. The SSO values assume that the V_{CCAUX} is powered at 3.3V. Setting V_{CCAUX} to 2.5V provides better SSO characteristics. For more detail, see [UG381](#): *Spartan-6 FPGA SelectIO Resources User Guide*.

SSO analysis does not take relative pin locations into account. The PlanAhead tool supports simultaneous switching noise (SSN) analysis, which is based on relative pin locations, allowing the optimal choice of package pins. For more information, see [UG792](#): *Pin Planning Methodology Guide*.

There are also restrictions on using SelectIO resources in proximity to GTP transceivers. For more information, see [UG386](#): *Spartan-6 FPGA GTP Transceivers User Guide*.

Table 33: Spartan-6 FPGA V_{CCO}/GND Pairs per Bank

| Package | Devices | Description | Bank 0 | Bank 1 | Bank 2 | Bank 3 | Bank 4 | Bank 5 |
|----------|--------------------|-----------------------------|--------|--------|--------|--------|--------|--------|
| TQG144 | LX | V _{CCO} /GND Pairs | 3 | 3 | 2 | 3 | N/A | N/A |
| | | Maximum I/O per Pair | 8 | 8 | 13 | 8 | N/A | N/A |
| CPG196 | LX | V _{CCO} /GND Pairs | 4 | 6 | 4 | 6 | N/A | N/A |
| | | Maximum I/O per Pair | 6 | 4 | 7 | 4 | N/A | N/A |
| CSG225 | LX | V _{CCO} /GND Pairs | 4 | 4 | 4 | 4 | N/A | N/A |
| | | Maximum I/O per Pair | 10 | 10 | 9 | 10 | N/A | N/A |
| FT(G)256 | LX | V _{CCO} /GND Pairs | 5 | 6 | 4 | 5 | N/A | N/A |
| | | Maximum I/O per Pair | 8 | 9 | 9 | 10 | N/A | N/A |
| CSG324 | LX | V _{CCO} /GND Pairs | 6 | 6 | 6 | 6 | N/A | N/A |
| | | Maximum I/O per Pair | 10 | 9 | 10 | 9 | N/A | N/A |
| | LXT | V _{CCO} /GND Pairs | 4 | 6 | 6 | 6 | N/A | N/A |
| | | Maximum I/O per Pair | 4 | 9 | 10 | 9 | N/A | N/A |
| CS(G)484 | LX | V _{CCO} /GND Pairs | 8 | 13 | 8 | 13 | N/A | N/A |
| | | Maximum I/O per Pair | 7 | 8 | 7 | 8 | N/A | N/A |
| | LXT | V _{CCO} /GND Pairs | 7 | 12 | 8 | 13 | N/A | N/A |
| | | Maximum I/O per Pair | 5 | 8 | 6 | 8 | N/A | N/A |
| FG(G)484 | LX | V _{CCO} /GND Pairs | 10 | 10 | 11 | 11 | N/A | N/A |
| | | Maximum I/O per Pair | 6 | 8 | 9 | 8 | N/A | N/A |
| | LXT | V _{CCO} /GND Pairs | 6 | 10 | 11 | 10 | N/A | N/A |
| | | Maximum I/O per Pair | 7 | 8 | 7 | 8 | N/A | N/A |
| FG(G)676 | LX45 | V _{CCO} /GND Pairs | 12 | 15 | 10 | 16 | N/A | N/A |
| | | Maximum I/O per Pair | 3 | 7 | 8 | 7 | N/A | N/A |
| | LX75, LX100, LX150 | V _{CCO} /GND Pairs | 12 | 9 | 10 | 10 | 6 | 6 |
| | | Maximum I/O per Pair | 9 | 10 | 9 | 9 | 8 | 9 |
| | LXT | V _{CCO} /GND Pairs | 10 | 8 | 10 | 8 | 7 | 7 |
| | | Maximum I/O per Pair | 8 | 7 | 8 | 8 | 7 | 7 |
| FG(G)900 | LX | V _{CCO} /GND Pairs | 17 | 14 | 17 | 14 | 7 | 8 |
| | | Maximum I/O per Pair | 7 | 6 | 7 | 8 | 7 | 6 |
| | LXT | V _{CCO} /GND Pairs | 15 | 14 | 13 | 14 | 7 | 8 |
| | | Maximum I/O per Pair | 7 | 6 | 8 | 8 | 7 | 6 |

Table 34: SSO Limit per V_{CCO}/GND Pair

| V _{CCO} | I/O Standard | Drive | Slew | SSO Limit per V _{CCO} /GND Pair | | | |
|------------------|--------------------------|-------|---------|--|----------|---|--------------|
| | | | | All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324 | | All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324 | |
| | | | | Bank 0/2 | Bank 1/3 | Bank 0/2 | Bank 1/3/4/5 |
| 1.2V | LVCMOS12, LVCMOS12_JEDEC | 2 | Fast | 30 ⁽¹⁾ | 35 | 30 | 35 |
| | | | Slow | 51 | 55 | 51 | 52 |
| | | | QuietIO | 71 | 58 | 71 | 70 |
| | | 4 | Fast | 17 | 17 | 17 | 19 |
| | | | Slow | 23 | 25 | 23 | 22 |
| | | | QuietIO | 35 | 32 | 35 | 32 |
| | | 6 | Fast | 13 | 15 | 13 | 14 |
| | | | Slow | 19 | 20 | 19 | 17 |
| | | | QuietIO | 26 | 24 | 26 | 24 |
| | | 8 | Fast | N/A | 12 | N/A | 12 |
| | | | Slow | N/A | 15 | N/A | 13 |
| | | | QuietIO | N/A | 20 | N/A | 19 |
| | | 12 | Fast | N/A | 5 | N/A | 4 |
| | | | Slow | N/A | 8 | N/A | 5 |
| | | | QuietIO | N/A | 11 | N/A | 10 |

Table 34: SSO Limit per V_{CC0}/GND Pair (Cont'd)

| V _{CC0} | I/O Standard | Drive | Slew | SSO Limit per V _{CC0} /GND Pair | | | | | |
|--------------------------------|--------------------------|---------|---------|--|----------|---|--------------|-----|----|
| | | | | All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324 | | All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324 | | | |
| | | | | Bank 0/2 | Bank 1/3 | Bank 0/2 | Bank 1/3/4/5 | | |
| 1.5V | LVCMOS15, LVCMOS15_JEDEC | 2 | Fast | 33 | 40 | 33 | 41 | | |
| | | | Slow | 57 | 62 | 57 | 56 | | |
| | | | QuietIO | 70 | 67 | 70 | 66 | | |
| | | 4 | Fast | 19 | 21 | 19 | 21 | | |
| | | | Slow | 30 | 30 | 30 | 24 | | |
| | | | QuietIO | 38 | 33 | 38 | 30 | | |
| | | 6 | Fast | 14 | 16 | 14 | 16 | | |
| | | | Slow | 18 | 19 | 18 | 17 | | |
| | | | QuietIO | 27 | 24 | 27 | 21 | | |
| | | 8 | Fast | 11 | 13 | 11 | 12 | | |
| | | | Slow | 16 | 16 | 16 | 14 | | |
| | | | QuietIO | 23 | 20 | 23 | 17 | | |
| | | 12 | Fast | N/A | 5 | N/A | 4 | | |
| | | | Slow | N/A | 8 | N/A | 5 | | |
| | | | QuietIO | N/A | 10 | N/A | 9 | | |
| | | 16 | Fast | N/A | 5 | N/A | 4 | | |
| | | | Slow | N/A | 8 | N/A | 8 | | |
| | | | QuietIO | N/A | 10 | N/A | 9 | | |
| | | HSTL_I | | | | 9 | 10 | 9 | 10 |
| | | HSTL_II | | | | N/A | 5 | N/A | 6 |
| HSTL_III | | | | 7 | 9 | 7 | 9 | | |
| DIFF_HSTL_I | | | | 27 | 30 | 27 | 30 | | |
| DIFF_HSTL_II | | | | N/A | 15 | N/A | 18 | | |
| DIFF_HSTL_III | | | | 21 | 27 | 21 | 27 | | |
| SSTL_15_II ⁽³⁾ | | | | N/A | 5 | N/A | 4 | | |
| DIFF_SSTL_15_II ⁽³⁾ | | | | N/A | 15 | N/A | 12 | | |

Table 34: SSO Limit per V_{CCO}/GND Pair (Cont'd)

| V _{CCO} | I/O Standard | Drive | Slew | SSO Limit per V _{CCO} /GND Pair | | | | | |
|--------------------------------|--------------------------|------------------|---------|--|----------|---|--------------|-----|----|
| | | | | All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324 | | All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324 | | | |
| | | | | Bank 0/2 | Bank 1/3 | Bank 0/2 | Bank 1/3/4/5 | | |
| 1.8V | LVCMOS18, LVCMOS18_JEDEC | 2 | Fast | 39 | 46 | 39 | 47 | | |
| | | | Slow | 65 | 75 | 65 | 74 | | |
| | | | QuietIO | 80 | 80 | 80 | 85 | | |
| | | 4 | Fast | 22 | 25 | 22 | 25 | | |
| | | | Slow | 38 | 36 | 38 | 29 | | |
| | | | QuietIO | 45 | 40 | 45 | 35 | | |
| | | 6 | Fast | 16 | 18 | 16 | 17 | | |
| | | | Slow | 27 | 25 | 27 | 19 | | |
| | | | QuietIO | 30 | 28 | 30 | 23 | | |
| | | 8 | Fast | 13 | 15 | 13 | 14 | | |
| | | | Slow | 16 | 18 | 16 | 16 | | |
| | | | QuietIO | 25 | 22 | 25 | 18 | | |
| | | 12 | Fast | 5 | 7 | 5 | 5 | | |
| | | | Slow | 7 | 8 | 7 | 6 | | |
| | | | QuietIO | 11 | 10 | 11 | 8 | | |
| | | 16 | Fast | 4 | 5 | 4 | 4 | | |
| | | | Slow | 7 | 8 | 7 | 5 | | |
| | | | QuietIO | 11 | 10 | 11 | 8 | | |
| | | 24 | Fast | N/A | 5 | N/A | 3 | | |
| | | | Slow | N/A | 8 | N/A | 8 | | |
| | | | QuietIO | N/A | 10 | N/A | 8 | | |
| | | HSTL_I_18 | | | | 9 | 10 | 9 | 9 |
| | | HSTL_II_18 | | | | N/A | 5 | N/A | 6 |
| | | HSTL_III_18 | | | | 9 | 10 | 9 | 11 |
| | | DIFF_HSTL_I_18 | | | | 27 | 30 | 27 | 27 |
| | | DIFF_HSTL_II_18 | | | | N/A | 15 | N/A | 18 |
| | | DIFF_HSTL_III_18 | | | | 27 | 30 | 27 | 33 |
| MOBILE_DDR ⁽³⁾ | | | | 12 | 14 | 12 | 14 | | |
| DIFF_MOBILE_DDR ⁽³⁾ | | | | 36 | 42 | 36 | 42 | | |
| SSTL_18_I ⁽³⁾ | | | | 9 | 10 | 9 | 10 | | |
| SSTL_18_II ⁽³⁾ | | | | N/A | 5 | N/A | 4 | | |
| DIFF_SSTL_18_I ⁽³⁾ | | | | 27 | 30 | 27 | 30 | | |
| DIFF_SSTL_18_II ⁽³⁾ | | | | N/A | 15 | N/A | 12 | | |

Table 34: SSO Limit per V_{CCO}/GND Pair (Cont'd)

| V _{CCO} | I/O Standard | Drive | Slew | SSO Limit per V _{CCO} /GND Pair | | | |
|------------------|-------------------------------|-------|---------|--|----------|---|--------------|
| | | | | All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324 | | All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324 | |
| | | | | Bank 0/2 | Bank 1/3 | Bank 0/2 | Bank 1/3/4/5 |
| 2.5V | LVCMOS25 | 2 | Fast | 38 | 43 | 38 | 43 |
| | | | Slow | 46 | 52 | 46 | 48 |
| | | | QuietIO | 57 | 64 | 57 | 59 |
| | | 4 | Fast | 21 | 24 | 21 | 23 |
| | | | Slow | 26 | 31 | 26 | 27 |
| | | | QuietIO | 33 | 32 | 33 | 30 |
| | | 6 | Fast | 15 | 17 | 15 | 16 |
| | | | Slow | 19 | 22 | 19 | 19 |
| | | | QuietIO | 25 | 23 | 25 | 19 |
| | | 8 | Fast | 12 | 15 | 12 | 14 |
| | | | Slow | 15 | 18 | 15 | 16 |
| | | | QuietIO | 21 | 19 | 21 | 16 |
| | | 12 | Fast | 1 | 3 | 1 | 1 |
| | | | Slow | 2 | 7 | 2 | 4 |
| | | | QuietIO | 3 | 8 | 3 | 8 |
| | | 16 | Fast | 1 | 3 | 1 | 1 |
| | | | Slow | 3 | 7 | 3 | 3 |
| | | | QuietIO | 4 | 9 | 4 | 8 |
| | | 24 | Fast | N/A | 3 | N/A | 1 |
| | | | Slow | N/A | 5 | N/A | 2 |
| QuietIO | N/A | | 8 | N/A | 6 | | |
| | SSTL_2_I ⁽³⁾ | | | 10 | 11 | 10 | 11 |
| | SSTL_2_II ⁽³⁾ | | | N/A | 7 | N/A | 7 |
| | DIFF_SSTL_2_I ⁽³⁾ | | | 30 | 33 | 30 | 33 |
| | DIFF_SSTL_2_II ⁽³⁾ | | | N/A | 21 | N/A | 24 |

Table 34: SSO Limit per V_{CC0}/GND Pair (Cont'd)

| V _{CC0} | I/O Standard | Drive | Slew | SSO Limit per V _{CC0} /GND Pair | | | |
|------------------|--------------|-------|---------|--|----------|---|--------------|
| | | | | All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324 | | All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324 | |
| | | | | Bank 0/2 | Bank 1/3 | Bank 0/2 | Bank 1/3/4/5 |
| 3.3V | LVCMOS33 | 2 | Fast | 42 | 46 | 42 | 44 |
| | | | Slow | 50 | 55 | 50 | 49 |
| | | | QuietIO | 60 | 68 | 60 | 60 |
| | | 4 | Fast | 21 | 27 | 21 | 25 |
| | | | Slow | 32 | 37 | 32 | 32 |
| | | | QuietIO | 39 | 42 | 39 | 37 |
| | | 6 | Fast | 14 | 19 | 14 | 17 |
| | | | Slow | 19 | 25 | 19 | 22 |
| | | | QuietIO | 29 | 30 | 29 | 25 |
| | | 8 | Fast | 11 | 15 | 11 | 14 |
| | | | Slow | 15 | 20 | 15 | 18 |
| | | | QuietIO | 25 | 24 | 25 | 20 |
| | | 12 | Fast | 1 | 3 | 1 | 1 |
| | | | Slow | 2 | 5 | 2 | 2 |
| | | | QuietIO | 4 | 9 | 4 | 7 |
| | | 16 | Fast | 1 | 2 | 1 | 1 |
| | | | Slow | 1 | 5 | 1 | 1 |
| | | | QuietIO | 3 | 10 | 3 | 8 |
| | | 24 | Fast | 1 | 2 | 1 | 1 |
| | | | Slow | 2 | 5 | 2 | 1 |
| | | | QuietIO | 7 | 9 | 7 | 7 |

Table 34: SSO Limit per V_{CCO}/GND Pair (Cont'd)

| V _{CCO} | I/O Standard | Drive | Slew | SSO Limit per V _{CCO} /GND Pair | | | | | |
|------------------|--------------|-------|----------------|--|----------|---|--------------|----|----|
| | | | | All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324 | | All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324 | | | |
| | | | | Bank 0/2 | Bank 1/3 | Bank 0/2 | Bank 1/3/4/5 | | |
| 3.3V | LVTTTL | 2 | Fast | 53 | 65 | 53 | 62 | | |
| | | | Slow | 70 | 80 | 70 | 73 | | |
| | | | QuietIO | 79 | 89 | 79 | 91 | | |
| | | 4 | Fast | 23 | 30 | 23 | 27 | | |
| | | | Slow | 34 | 41 | 34 | 37 | | |
| | | | QuietIO | 44 | 49 | 44 | 46 | | |
| | | 6 | Fast | 16 | 21 | 16 | 20 | | |
| | | | Slow | 21 | 28 | 21 | 25 | | |
| | | | QuietIO | 34 | 39 | 34 | 34 | | |
| | | 8 | Fast | 12 | 16 | 12 | 15 | | |
| | | | Slow | 16 | 22 | 16 | 19 | | |
| | | | QuietIO | 27 | 28 | 27 | 24 | | |
| | | 12 | Fast | 1 | 3 | 1 | 1 | | |
| | | | Slow | 2 | 5 | 2 | 4 | | |
| | | | QuietIO | 2 | 10 | 2 | 8 | | |
| | | 16 | Fast | 1 | 3 | 1 | 1 | | |
| | | | Slow | 1 | 7 | 1 | 2 | | |
| | | | QuietIO | 3 | 11 | 3 | 8 | | |
| | | 24 | Fast | 1 | 2 | 1 | 1 | | |
| | | | Slow | 2 | 5 | 2 | 2 | | |
| | | | QuietIO | 8 | 9 | 8 | 8 | | |
| | | | PCI33_3 | | | 18 | 19 | 18 | 19 |
| | | | PCI66_3 | | | 18 | 19 | 18 | 19 |
| | | | SSTL_3_I | | | 5 | 8 | 5 | 8 |
| | | | SSTL_3_II | | | 3 | 5 | 3 | 3 |
| | | | DIFF_SSTL_3_I | | | 15 | 24 | 15 | 24 |
| | | | DIFF_SSTL_3_II | | | 9 | 15 | 9 | 9 |
| | SDIO | | | 17 | 18 | 17 | 15 | | |

Table 34: SSO Limit per V_{CCO}/GND Pair (Cont'd)

| V_{CCO} | I/O Standard | Drive | Slew | SSO Limit per V_{CCO}/GND Pair | | | |
|-----------|--------------|-------|------|--|----------|---|--------------|
| | | | | All TQG144, CPG196, CSG225, FT(G)256, and LX devices in CSG324 | | All CS(G)484, FG(G)484, FG(G)676, FG(G)900, and LXT devices in CSG324 | |
| | | | | Bank 0/2 | Bank 1/3 | Bank 0/2 | Bank 1/3/4/5 |
| Various | LVDS_33 | | | 16 | N/A | 16 | N/A |
| | LVDS_25 | | | 20 | N/A | 20 | N/A |
| | BLVDS_25 | | | 20 | 48 | 20 | 20 |
| | MINI_LVDS_33 | | | 13 | N/A | 13 | N/A |
| | MINI_LVDS_25 | | | 18 | N/A | 18 | N/A |
| | RSDS_33 | | | 12 | N/A | 12 | N/A |
| | RSDS_25 | | | 15 | N/A | 15 | N/A |
| | TMDS_33 | | | 83 | N/A | 83 | N/A |
| | PPDS_33 | | | 12 | N/A | 12 | N/A |
| | PPDS_25 | | | 16 | N/A | 16 | N/A |
| | DISPLAY_PORT | | | 42 | 40 | 42 | 30 |
| | I2C | | | 47 | 55 | 47 | 42 |
| | SMBUS | | | 44 | 52 | 44 | 40 |

Notes:

1. SSO limits greater than the number of I/O per V_{CCO}/GND pair (Table 33) indicate No Limit for the given I/O standard. They are provided in this table to calculate limits when using multiple I/O standards in a bank.
2. Not available (N/A) indicates that the I/O standard is not available in the given bank.
3. When used with the MCB, these signals are exempt from SSO analysis due to the known activity of the MCB switching patterns. SSO performance is validated for all MCB instances. MCB outputs can, in some cases, exceed the SSO limits.

Input/Output Logic Switching Characteristics

Table 35: ILOGIC2 Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|--------------------------|--|----------------|----------------|----------------|----------------|-------|
| | | -3 | -3N | -2 | -1L | |
| Setup/Hold | | | | | | |
| T_{ICE0CK}/T_{ICKCE0} | CE0 pin Setup/Hold with respect to CLK | 0.56/ -0.30 | 0.56/ -0.25 | 0.79/ -0.22 | 1.21/ -0.52 | ns |
| T_{ISRCK}/T_{ICKSR} | SR pin Setup/Hold with respect to CLK | 0.74/ -0.23 | 0.74/ -0.22 | 0.98/ -0.20 | 1.31/ -0.45 | ns |
| T_{IDOCK}/T_{IOCKD} | D pin Setup/Hold with respect to CLK without Delay | 1.19/ -0.83 | 1.36/ -0.83 | 1.73/ -0.83 | 2.18/ -1.77 | ns |
| T_{IDOCKD}/T_{IOCKDD} | DDLY pin Setup/Hold with respect to CLK (using IODELAY2) | 0.31/ 0.00 | 0.47/ 0.00 | 0.54/ 0.00 | 0.63/ -0.39 | ns |
| Combinatorial | | | | | | |
| T_{IDI} | D pin to O pin propagation delay, no Delay | 0.95 | 1.28 | 1.53 | 2.25 | ns |
| T_{IDID} | DDLY pin to O pin propagation delay (using IODELAY2) | 0.23 | 0.39 | 0.44 | 0.74 | ns |
| Sequential Delays | | | | | | |
| T_{IDLO} | D pin to Q pin using flip-flop as a latch without Delay | 1.56 | 1.86 | 2.39 | 3.49 | ns |
| T_{IDLOD} | DDLY pin to Q1 pin using flip-flop as a latch (using IODELAY2) | 0.68 | 0.97 | 1.20 | 1.94 | ns |
| T_{ICKQ} | CLK to Q outputs for XC devices ⁽¹⁾ | 1.03 | 1.24 | 1.43 | 2.11 | ns |
| | CLK to Q outputs for XA and XQ devices | 1.38 | N/A | 1.78 | 2.11 | ns |
| $T_{RQ_ILOGIC2}$ | SR pin to Q outputs | 1.81 | 1.81 | 2.50 | 3.05 | ns |

Notes:

- For IDDR2 configuration; see TRACE reports for SDR timing.

Table 36: OLOGIC2 Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|--------------------------|--|----------------|----------------|----------------|----------------|-------|
| | | -3 | -3N | -2 | -1L | |
| Setup/Hold | | | | | | |
| T_{ODCK}/T_{OOCKD} | D1/D2 pins Setup/Hold with respect to CLK | 0.81/ -0.05 | 0.86/ -0.05 | 1.18/ 0.00 | 1.73/ -0.27 | ns |
| $T_{OOCECK}/T_{OOCKOCE}$ | OCE pin Setup/Hold with respect to CLK | 0.75/ -0.10 | 0.75/ -0.10 | 1.01/ -0.05 | 1.66/ -0.23 | ns |
| T_{OSRCK}/T_{OOCKSR} | SR pin Setup/Hold with respect to CLK | 0.70/ -0.28 | 0.79/ -0.28 | 1.03/ -0.23 | 1.39/ -0.47 | ns |
| T_{OTCK}/T_{OOCKT} | T1/T2 pins Setup/Hold with respect to CLK | 0.24/ -0.08 | 0.56/ -0.06 | 0.83/ -0.01 | 0.99/ -0.19 | ns |
| $T_{OTCECK}/T_{OOCKTCE}$ | TCE pin Setup/Hold with respect to CLK | 0.58/ -0.06 | 0.72/ -0.06 | 1.18/ -0.01 | 1.51/ -0.13 | ns |
| Sequential Delays | | | | | | |
| T_{OOCKQ} | CLK to OQ/TQ out for XC devices ⁽¹⁾ | 0.48 | 0.51 | 0.74 | 0.74 | ns |
| | CLK to OQ/TQ out for XA and XQ devices | 0.85 | N/A | 1.16 | 0.74 | ns |
| $T_{RQ_OLOGIC2}$ | SR pin to OQ/TQ out | 1.81 | 1.81 | 2.50 | 3.05 | ns |

Notes:

- For ODDR2 configuration; see TRACE reports for SDR timing.

Input Serializer/Deserializer Switching Characteristics

Table 37: ISERDES2 Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|---|---|----------------|----------------|----------------|----------------|-------|
| | | -3 | -3N | -2 | -1L | |
| Setup/Hold for Control Lines | | | | | | |
| $T_{ISCK_BITSLIP} / T_{ISCKC_BITSLIP}$ | BITSLIP pin Setup/Hold with respect to CLKDIV | 0.16/ -0.09 | 0.20/ -0.09 | 0.31/ -0.09 | 0.34/ -0.14 | ns |
| $T_{ISCK_CE} / T_{ISCKC_CE}$ | CE pin Setup/Hold with respect to CLK | 0.71/ -0.47 | 0.71/ -0.42 | 0.97/ -0.42 | 1.39/ -0.71 | ns |
| Setup/Hold for Data Lines | | | | | | |
| $T_{ISDCK_D} / T_{ISCKD_D}$ | D pin Setup/Hold with respect to CLK | 0.24/ -0.15 | 0.25/ -0.05 | 0.29/ -0.05 | 0.09/ -0.05 | ns |
| $T_{ISDCK_DDLY} / T_{ISCKD_DDLY}$ | DDLY pin Setup/Hold with respect to CLK (using IODELAY2) | -0.25/ 0.30 | -0.25/ 0.42 | -0.25/ 0.56 | -0.54/ 0.67 | ns |
| $T_{ISDCK_D_DDR} / T_{ISCKD_D_DDR}$ | D pin Setup/Hold with respect to CLK at DDR mode | -0.03/ 0.04 | -0.03/ 0.16 | -0.03/ 0.18 | -0.05/ 0.12 | ns |
| $T_{ISDCK_DDLY_DDR} / T_{ISCKD_DDLY_DDR}$ | D pin Setup/Hold with respect to CLK at DDR mode (using IODELAY2) | -0.40/ 0.48 | -0.40/ 0.53 | -0.40/ 0.71 | -0.71/ 0.86 | ns |
| Sequential Delays | | | | | | |
| T_{ISCKO_Q} | CLKDIV to out at Q pin | 1.30 | 1.44 | 2.02 | 2.22 | ns |
| F_{CLKDIV} | CLKDIV maximum frequency | 270 | 262.5 | 250 | 125 | MHz |

Output Serializer/Deserializer Switching Characteristics

Table 38: OSERDES2 Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|-------------------------------------|---|----------------|----------------|----------------|----------------|-------|
| | | -3 | -3N | -2 | -1L | |
| Setup/Hold | | | | | | |
| $T_{OSDCK_D} / T_{OSCKD_D}$ | D input Setup/Hold with respect to CLKDIV | -0.03/ 1.02 | -0.03/ 1.17 | -0.03/ 1.27 | -0.02/ 0.23 | ns |
| $T_{OSDCK_T} / T_{OSCKD_T}^{(1)}$ | T input Setup/Hold with respect to CLK | -0.05/ 1.03 | -0.05/ 1.13 | -0.05/ 1.23 | -0.05/ 0.24 | ns |
| $T_{OSCCK_OCE} / T_{OSCKC_OCE}$ | OCE input Setup/Hold with respect to CLK | 0.12/ -0.03 | 0.15/ -0.03 | 0.24/ -0.03 | 0.28/ -0.17 | ns |
| $T_{OSCCK_TCE} / T_{OSCKC_TCE}$ | TCE input Setup/Hold with respect to CLK | 0.14/ -0.08 | 0.17/ -0.08 | 0.27/ -0.08 | 0.31/ -0.16 | ns |
| Sequential Delays | | | | | | |
| T_{OSCKO_OQ} | Clock to out from CLK to OQ | 0.94 | 1.11 | 1.51 | 1.89 | ns |
| T_{OSCKO_TQ} | Clock to out from CLK to TQ | 0.94 | 1.11 | 1.51 | 1.91 | ns |
| F_{CLKDIV} | CLKDIV maximum frequency | 270 | 262.5 | 250 | 125 | MHz |

Notes:

- $T_{OSDCK_T2} / T_{OSCKD_T2}$ (T input setup/hold with respect to CLKDIV) are reported as $T_{OSDCK_T} / T_{OSCKD_T}$ in TRACE report.

Input/Output Delay Switching Characteristics

Table 39: IODELAY2 Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|-------------------------------------|---|----------------|----------------|----------------|--------------------|-------|
| | | -3 | -3N | -2 | -1L ⁽³⁾ | |
| $T_{IODCCK_CAL} / T_{IODCKC_CAL}$ | CAL pin Setup/Hold with respect to CK | 0.28/ -0.13 | 0.33/ -0.13 | 0.48/ -0.13 | N/A | ns |
| $T_{IODCCK_CE} / T_{IODCKC_CE}$ | CE pin Setup/Hold with respect to CK | 0.17/ -0.03 | 0.17/ -0.03 | 0.25/ -0.02 | N/A | ns |
| $T_{IODCCK_INC} / T_{IODCKC_INC}$ | INC pin Setup/Hold with respect to CK | 0.10/ 0.02 | 0.12/ 0.03 | 0.18/ 0.06 | N/A | ns |
| $T_{IODCCK_RST} / T_{IODCKC_RST}$ | RST pin Setup/Hold with respect to CK | 0.12/ -0.02 | 0.15/ -0.02 | 0.22/ -0.01 | N/A | ns |
| $T_{TAP1}^{(2)}$ | Maximum tap 1 delay | 8 | 14 | 16 | N/A | ps |
| T_{TAP2} | Maximum tap 2 delay | 40 | 66 | 77 | N/A | ps |
| T_{TAP3} | Maximum tap 3 delay | 95 | 120 | 140 | N/A | ps |
| T_{TAP4} | Maximum tap 4 delay | 108 | 141 | 166 | N/A | ps |
| T_{TAP5} | Maximum tap 5 delay | 171 | 194 | 231 | N/A | ps |
| T_{TAP6} | Maximum tap 6 delay | 207 | 249 | 292 | N/A | ps |
| T_{TAP7} | Maximum tap 7 delay | 212 | 276 | 343 | N/A | ps |
| T_{TAP8} | Maximum tap 8 delay | 322 | 341 | 424 | N/A | ps |
| F_{MINCAL} | Minimum allowed bit rate for calibration in variable mode: VARIABLE_FROM_ZERO, VARIABLE_FROM_HALF_MAX, and DIFF_PHASE_DETECTOR. | 188 | 188 | 188 | N/A | Mb/s |
| $T_{IODDO_IDATAIN}$ | Propagation delay through IODELAY2 | Note 1 | Note 1 | Note 1 | Note 3 | – |
| $T_{IODDO_ODATAIN}$ | Propagation delay through IODELAY2 | Note 1 | Note 1 | Note 1 | Note 3 | – |

Notes:

1. Delay depends on IODELAY2 tap setting. See TRACE report for actual values.
2. Maximum tap delay = integer (number of taps/8) \times T_{TAP8} + T_{TAPn} (where n equals the remainder). For minimum delay consult the TRACE setup and hold report. Minimum delay is typically greater than 30% of the maximum delay. Tap delays can vary by device and overall conditions. See TRACE report for actual values.
3. Spartan-6 -1L devices only support tap 0. See TRACE report for actual values.

CLB Switching Characteristics (SLICEM Only)

Table 40: CLB Switching Characteristics (SLICEM Only)

| Symbol | Description | Speed Grade | | | | Units |
|--|--|----------------|----------------|----------------|----------------|---------|
| | | -3 | -3N | -2 | -1L | |
| Combinatorial Delays | | | | | | |
| T _{ILO} | An – Dn LUT inputs to A to D outputs | 0.21 | 0.26 | 0.26 | 0.46 | ns, Max |
| | An – Dn LUT inputs through F7AMUX/F7BMUX to AMUX/CMUX output | 0.37 | 0.43 | 0.43 | 0.77 | ns, Max |
| T _{OPAB} | An – Dn LUT inputs through F7AMUX or F7BMUX and F8MUX to BMUX output | 0.37 | 0.46 | 0.46 | 0.84 | ns, Max |
| T _{ITO} | An – Dn LUT inputs through latch to AQ – DQ outputs | 0.82 | 0.95 | 0.95 | 1.64 | ns, Max |
| T _{TITO_LOGIC} | An – Dn LUT inputs to AQ – DQ outputs (latch as logic) | 0.82 | 0.95 | 0.95 | 1.64 | ns, Max |
| T _{OPCYA} | An LUT inputs to COUT output | 0.38 | 0.48 | 0.48 | 0.69 | ns, Max |
| T _{OPCYB} | Bn LUT inputs to COUT output | 0.38 | 0.49 | 0.49 | 0.71 | ns, Max |
| T _{OPCYC} | Cn LUT inputs to COUT output | 0.28 | 0.33 | 0.33 | 0.55 | ns, Max |
| T _{OPCYD} | Dn LUT inputs to COUT output | 0.28 | 0.35 | 0.35 | 0.52 | ns, Max |
| T _{AXCY} | AX input to COUT output | 0.21 | 0.26 | 0.26 | 0.36 | ns, Max |
| T _{BXCY} | BX input to COUT output | 0.13 | 0.16 | 0.16 | 0.18 | ns, Max |
| T _{CXCY} | CX input to COUT output | 0.10 | 0.12 | 0.12 | 0.09 | ns, Max |
| T _{DXCY} | DX input to COUT output | 0.09 | 0.11 | 0.11 | 0.09 | ns, Max |
| T _{BYP} | CIN input to COUT output | 0.08 | 0.10 | 0.10 | 0.06 | ns, Max |
| T _{CINA} | CIN input to AMUX output | 0.21 | 0.22 | 0.22 | 0.47 | ns, Max |
| T _{CINB} | CIN input to BMUX output | 0.30 | 0.31 | 0.31 | 0.57 | ns, Max |
| T _{CINC} | CIN input to CMUX output | 0.29 | 0.31 | 0.31 | 0.58 | ns, Max |
| T _{CIND} | CIN input to DMUX output | 0.31 | 0.32 | 0.32 | 0.68 | ns, Max |
| Sequential Delays | | | | | | |
| T _{CKO} | Clock to AQ – DQ outputs | 0.45 | 0.53 | 0.53 | 0.74 | ns, Max |
| Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK | | | | | | |
| T _{DICK} /T _{CKDI} | AX – DX input to CLK on A – D flip-flops | 0.42/ 0.28 | 0.47/ 0.39 | 0.47/ 0.39 | 0.90/ 0.56 | ns, Min |
| T _{CECK} /T _{CKCE} | CE input to CLK on A – D flip-flops | 0.31/ –0.07 | 0.37/ –0.07 | 0.37/ –0.07 | 0.59/ –0.27 | ns, Min |
| T _{SRCK} /T _{CKSR} | SR input to CLK on A – D flip-flops for XC devices | 0.41/ 0.02 | 0.42/ 0.02 | 0.42/ 0.02 | 0.68/ –0.29 | ns, Min |
| | SR input to CLK on A – D flip-flops for XA and XQ devices | 0.41/ 0.02 | N/A | 0.44/ 0.02 | 0.68/ –0.29 | ns, Min |
| T _{CINCK} /T _{CKCIN} | CIN input to CLK on A – D flip-flops | 0.31/ –0.17 | 0.31/ –0.13 | 0.31/ –0.13 | 0.81/ –0.42 | ns, Min |
| Set/Reset | | | | | | |
| T _{RPW} | SR input minimum pulse width | 0.41 | 0.48 | 0.48 | 1.37 | ns, Min |
| T _{RQ} | Delay from SR input to AQ – DQ flip-flops | 0.60 | 0.70 | 0.70 | 0.88 | ns, Max |
| T _{CEO} | Delay from CE input to AQ – DQ flip-flops | 0.60 | 0.65 | 0.65 | 0.90 | ns, Max |
| F _{TOG} | Toggle frequency (for export control) | 862 | 806 | 667 | 500 | MHz |

CLB Distributed RAM Switching Characteristics (SLICEM Only)

Table 41: CLB Distributed RAM Switching Characteristics (SLICEM Only)

| Symbol | Description | Speed Grade | | | | Units |
|--|--|----------------|----------------|----------------|----------------|---------|
| | | -3 | -3N | -2 | -1L | |
| Sequential Delays | | | | | | |
| T_{SHCKO} | Clock to A – D outputs | 1.26 | 1.55 | 1.55 | 2.35 | ns, Max |
| | Clock to A – D outputs (direct output path) | 0.96 | 1.20 | 1.20 | 1.87 | ns, Max |
| Setup and Hold Times Before/After Clock CLK | | | | | | |
| T_{DS}/T_{DH} | AX – DX or AI – DI inputs to CLK | 0.59/ 0.17 | 0.73/ 0.22 | 0.73/ 0.22 | 1.17/ 0.33 | ns, Min |
| T_{AS}/T_{AH} | Address An inputs to clock for XC devices | 0.28/ 0.35 | 0.32/ 0.42 | 0.32/ 0.42 | 0.26/ 0.71 | ns, Min |
| | Address An inputs to clock for XA and XQ devices | 0.28/ 0.51 | N/A | 0.32/ 0.51 | 0.26/ 0.71 | ns, Min |
| T_{WS}/T_{WH} | WE input to clock | 0.31/ –0.08 | 0.37/ –0.08 | 0.37/ –0.08 | 0.59/ –0.27 | ns, Min |
| T_{CECK}/T_{CKCE} | CE input to CLK | 0.31/ –0.08 | 0.37/ –0.08 | 0.37/ –0.08 | 0.59/ –0.27 | ns, Min |

CLB Shift Register Switching Characteristics (SLICEM Only)

Table 42: CLB Shift Register Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|--|---|----------------|----------------|----------------|----------------|---------|
| | | -3 | -3N | -2 | -1L | |
| Sequential Delays | | | | | | |
| T_{REG} | Clock to A – D outputs | 1.35 | 1.78 | 1.78 | 2.74 | ns, Max |
| | Clock to A – D outputs (direct output path) | 1.24 | 1.65 | 1.65 | 2.48 | ns, Max |
| Setup and Hold Times Before/After Clock CLK | | | | | | |
| T_{WS}/T_{WH} | WE input to CLK | 0.20/ –0.07 | 0.24/ –0.07 | 0.24/ –0.07 | 0.29/ –0.27 | ns, Min |
| T_{CECK}/T_{CKCE} | CE input to CLK for XC devices | 0.30/ 0.30 | 0.30/ 0.38 | 0.30/ 0.38 | 0.82/ –0.41 | ns, Min |
| | CE input to CLK for XA and XQ devices | 0.32/ 0.30 | N/A | 0.40/ 0.38 | 0.82/ –0.41 | ns, Min |
| T_{DS}/T_{DH} | AX – DX or AI – DI inputs to CLK | 0.07/ 0.11 | 0.09/ 0.14 | 0.09/ 0.14 | 0.11/ 0.23 | ns, Min |

Block RAM Switching Characteristics

Table 43: Block RAM Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|--|---|---------------|---------------|---------------|---------------|---------|
| | | -3 | -3N | -2 | -1L | |
| Block RAM Clock to Out Delays | | | | | | |
| T_{RCKO_DO} | Clock CLK to DOUT output (without output register) ⁽¹⁾ | 1.85 | 2.10 | 2.10 | 3.50 | ns, Max |
| $T_{RCKO_DO_REG}$ | Clock CLK to DOUT output (with output register) ⁽²⁾ | 1.60 | 1.75 | 1.75 | 2.30 | ns, Max |
| Setup and Hold Times Before/After Clock CLK | | | | | | |
| $T_{RCKC_ADDR}/T_{RCKC_ADDR}$ | ADDR inputs for XC devices ⁽³⁾ | 0.35/ 0.10 | 0.40/ 0.12 | 0.40/ 0.12 | 0.50/ 0.15 | ns, Min |
| | ADDR inputs for XA and XQ devices ⁽³⁾ | 0.35/ 0.17 | N/A | 0.40/ 0.17 | 0.50/ 0.15 | ns, Min |
| T_{RDCK_DI}/T_{RCKD_DI} | DIN inputs ⁽⁴⁾ | 0.30/ 0.10 | 0.30/ 0.10 | 0.30/ 0.10 | 0.40/ 0.15 | ns, Min |
| T_{RCKC_EN}/T_{RCKC_EN} | Block RAM Enable (EN) input | 0.22/ 0.05 | 0.25/ 0.06 | 0.25/ 0.06 | 0.44/ 0.10 | ns, Min |
| $T_{RCKC_REGCE}/T_{RCKC_REGCE}$ | CE input of output register | 0.20/ 0.10 | 0.20/ 0.10 | 0.20/ 0.10 | 0.28/ 0.15 | ns, Min |
| T_{RCKC_WE}/T_{RCKC_WE} | Write Enable (WE) input | 0.25/ 0.10 | 0.33/ 0.10 | 0.33/ 0.10 | 0.28/ 0.15 | ns, Min |
| Maximum Frequency | | | | | | |
| F_{MAX} | Block RAM in all modes | 320 | 280 | 280 | 150 | MHz |

Notes:

- T_{RCKO_DO} includes T_{RCKO_DOA} and T_{RCKO_DOPA} as well as the B port equivalent timing parameters.
- $T_{RCKO_DO_REG}$ includes $T_{RCKO_DOA_REG}$ and $T_{RCKO_DOPA_REG}$ as well as the B port equivalent timing parameters.
- The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
- T_{RDCK_DI} includes both A and B inputs as well as the parity inputs of A and B.

DSP48A1 Switching Characteristics

Table 44: DSP48A1 Switching Characteristics

| Symbol | Description | Pre-adder | Multiplier | Post-adder | Speed Grade | | | | Units |
|---|---|-----------|------------|------------|----------------|----------------|----------------|-----------------|-------|
| | | | | | -3 | -3N | -2 | -1L | |
| Setup and Hold Times of Data/Control Pins to the Input Register Clock | | | | | | | | | |
| $T_{DSPDCK_A_A1REG}/$ $T_{DSPCKD_A_A1REG}$ | A input to A1 register CLK | N/A | N/A | N/A | 0.15/ 0.09 | 0.17/ 0.09 | 0.17/ 0.09 | 0.32/ 0.09 | ns |
| $T_{DSPDCK_D_B1REG}/$ $T_{DSPCKD_D_B1REG}$ | D input to B1 register CLK | Yes | N/A | N/A | 1.90/ -0.07 | 1.95/ -0.07 | 1.95/ -0.07 | 2.82/ -0.07 | ns |
| $T_{DSPDCK_C_CREG}/$ $T_{DSPCKD_C_CREG}$ | C input to C register CLK for XC devices | N/A | N/A | N/A | 0.11/ 0.15 | 0.13/ 0.15 | 0.13/ 0.15 | 0.24/ 0.09 | ns |
| | C input to C register CLK for XA and XQ devices | | | | 0.11/ 0.19 | N/A | 0.13/ 0.23 | 0.24/ 0.09 | |
| $T_{DSPDCK_D_DREG}/$ $T_{DSPCKD_D_DREG}$ | D input to D register CLK for XC devices | N/A | N/A | N/A | 0.09/ 0.15 | 0.10/ 0.15 | 0.10/ 0.15 | 0.19/ 0.12 | ns |
| | D input to D register CLK for XA and XQ devices | | | | 0.09/ 0.23 | N/A | 0.10/ 0.27 | 0.19/ 0.12 | |
| $T_{DSPDCK_OPMODE_B1REG}/$ $T_{DSPCKD_OPMODE_B1REG}$ | OPMODE input to B1 register CLK | Yes | N/A | N/A | 1.97/ 0.01 | 2.00/ 0.01 | 2.00/ 0.01 | 2.85/ 0.01 | ns |
| $T_{DSPDCK_OPMODE_OPMODEREG}/$ $T_{DSPCKD_OPMODE_OPMODEREG}$ | OPMODE input to OPMODE register CLK for XC devices | N/A | N/A | N/A | 0.18/ 0.12 | 0.21/ 0.12 | 0.21/ 0.12 | 0.40/ 0.12 | ns |
| | OPMODE input to OPMODE register CLK for XA and XQ devices | | | | 0.18/ 0.16 | N/A | 0.21/ 0.22 | 0.40/ 0.12 | |
| Setup and Hold Times of Data Pins to the Pipeline Register Clock | | | | | | | | | |
| $T_{DSPDCK_A_MREG}/$ $T_{DSPCKD_A_MREG}$ | A input to M register CLK | N/A | Yes | N/A | 3.06/ -0.40 | 3.51/ -0.40 | 3.51/ -0.40 | 3.97/ -0.40 | ns |
| $T_{DSPDCK_B_MREG}/$ $T_{DSPCKD_B_MREG}$ | B input to M register CLK | Yes | Yes | N/A | 3.96/ -0.68 | 4.58/ -0.68 | 4.58/ -0.68 | 7.00/ -0.68 | ns |
| $T_{DSPDCK_D_MREG}/$ $T_{DSPCKD_D_MREG}$ | D input to M register CLK | Yes | Yes | N/A | 4.23/ -0.56 | 4.80/ -0.56 | 4.80/ -0.56 | 6.84/ -0.56 | ns |
| $T_{DSPDCK_OPMODE_MREG}/$ $T_{DSPCKD_OPMODE_MREG}$ | OPMODE to M register CLK | Yes | Yes | N/A | 4.18/ -0.48 | 4.80/ -0.48 | 4.80/ -0.48 | 6.88/ -0.48 | ns |
| | | No | Yes | N/A | 2.37/ -0.48 | 2.70/ -0.48 | 2.70/ -0.48 | 4.28/ -0.48 | ns |
| Setup and Hold Times of Data/Control Pins to the Output Register Clock | | | | | | | | | |
| $T_{DSPDCK_A_PREG}/$ $T_{DSPCKD_A_PREG}$ | A input to P register CLK | N/A | Yes | Yes | 4.32/ -0.76 | 5.06/ -0.76 | 5.06/ -0.76 | 7.52/ -0.76 | ns |
| $T_{DSPDCK_B_PREG}/$ $T_{DSPCKD_B_PREG}$ | B input to P register CLK | Yes | Yes | Yes | 5.87/ -0.59 | 6.87/ -0.59 | 6.87/ -0.59 | 10.55/ -0.59 | ns |
| | | No | Yes | Yes | 4.14/ -0.93 | 4.68/ -0.93 | 4.68/ -0.93 | 8.12/ -0.93 | ns |
| $T_{DSPDCK_C_PREG}/$ $T_{DSPCKD_C_PREG}$ | C input to P register CLK | N/A | N/A | Yes | 2.20/ -0.23 | 2.25/ -0.23 | 2.25/ -0.23 | 3.27/ -0.23 | ns |
| $T_{DSPDCK_D_PREG}/$ $T_{DSPCKD_D_PREG}$ | D input to P register CLK | Yes | Yes | Yes | 5.90/ -0.92 | 6.91/ -0.92 | 6.91/ -0.92 | 10.39/ -0.92 | ns |

Table 44: DSP48A1 Switching Characteristics (Cont'd)

| Symbol | Description | Pre-adder | Multiplier | Post-adder | Speed Grade | | | | Units |
|--|--------------------------------|-----------|------------|-------------------|----------------|----------------|----------------|-----------------|-------|
| | | | | | -3 | -3N | -2 | -1L | |
| T _{DSPDCK_OPMODE_PREG} / T _{DSPCKD_OPMODE_PREG} | OPMODE input to P register CLK | Yes | Yes | Yes | 6.21/ -0.84 | 7.27/ -0.84 | 7.27/ -0.84 | 10.43/ -0.84 | ns |
| | | No | Yes | Yes | 1.69/ -0.87 | 1.98/ -0.87 | 1.98/ -0.87 | 3.62/ -0.87 | ns |
| | | No | No | Yes | 2.09/ -0.22 | 2.30/ -0.22 | 2.30/ -0.22 | 3.79/ -0.22 | ns |
| Clock to Out from Output Register Clock to Output Pin | | | | | | | | | |
| T _{DSPCKO_P_PREG} | CLK (PREG) to P output | N/A | N/A | N/A | 1.20 | 1.34 | 1.34 | 1.90 | ns |
| Clock to Out from Pipeline Register Clock to Output Pins | | | | | | | | | |
| T _{DSPCKO_P_MREG} | CLK (MREG) to P output | N/A | N/A | Yes | 3.38 | 3.95 | 3.95 | 5.83 | ns |
| Clock to Out from Input Register Clock to Output Pins | | | | | | | | | |
| T _{DSPCKO_P_A1REG} | CLK (A1REG) to P output | N/A | Yes | Yes | 5.02 | 5.87 | 5.87 | 9.65 | ns |
| T _{DSPCKO_P_B1REG} | CLK (B1REG) to P output | N/A | Yes | Yes | 5.02 | 5.87 | 5.87 | 9.63 | ns |
| T _{DSPCKO_P_CREG} | CLK (CREG) to P output | N/A | N/A | Yes | 3.12 | 3.64 | 3.64 | 5.24 | ns |
| T _{DSPCKO_P_DREG} | CLK (DREG) to P output | Yes | Yes | Yes | 6.77 | 7.92 | 7.92 | 12.53 | ns |
| Combinatorial Delays from Input Pins to Output Pins | | | | | | | | | |
| T _{DSPDO_A_P} | A input to P output | N/A | No | Yes | 2.85 | 3.33 | 3.33 | 4.73 | ns |
| | | N/A | Yes | No ⁽²⁾ | 3.35 | 3.93 | 3.93 | 6.74 | ns |
| | | N/A | Yes | Yes | 4.56 | 5.22 | 5.22 | 8.94 | ns |
| T _{DSPDO_B_P} | B input to P output | Yes | No | No ⁽²⁾ | 3.22 | 3.76 | 3.76 | 5.55 | ns |
| | | Yes | Yes | No ⁽²⁾ | 6.01 | 6.54 | 6.54 | 9.76 | ns |
| | | Yes | Yes | Yes | 6.27 | 7.34 | 7.34 | 11.96 | ns |
| T _{DSPDO_C_P} | C input to P output | N/A | N/A | Yes | 2.69 | 3.15 | 3.15 | 4.68 | ns |
| T _{DSPDO_D_P} | D input to P output | Yes | Yes | Yes | 6.31 | 7.38 | 7.38 | 11.81 | ns |
| T _{DSPDO_OPMODE_P} | OPMODE input to P output | Yes | Yes | Yes | 6.43 | 7.52 | 7.52 | 11.84 | ns |
| | | No | Yes | Yes | 4.84 | 5.66 | 5.66 | 9.25 | ns |
| | | No | No | Yes | 3.11 | 3.49 | 3.49 | 5.03 | ns |
| Maximum Frequency | | | | | | | | | |
| F _{MAX} | All registers used | Yes | Yes | Yes | 390 | 333 | 333 | 213 | MHz |

Notes:

1. A Yes signifies that the component is in the path. A No signifies that the component is being bypassed. N/A signifies not applicable because no path exists.
2. Implemented in the post-adder by adding to zero.

Table 45: Device DNA Interface Port Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|---|--|-------------|-----|----|-----|----------|
| | | -3 | -3N | -2 | -1L | |
| T _{DNASSU} (T _{DNADCK_SHIFT}) | Setup time on SHIFT before the rising edge of CLK | 7 | | | | ns, Min |
| T _{DNASH} (T _{DNACKD_SHIFT}) | Hold time on SHIFT after the rising edge of CLK | 1 | | | | ns, Min |
| T _{DNADSU} (T _{DNADCK_DIN}) | Setup time on DIN before the rising edge of CLK | 7 | | | | ns, Min |
| T _{DNADH} (T _{DNACKD_DIN}) | Hold time on DIN after the rising edge of CLK | 1 | | | | ns, Min |
| T _{DNARSU} (T _{DNADCK_READ}) | Setup time on READ before the rising edge of CLK | 7 | | | | ns, Min |
| | | 1,000 | | | | ns, Max |
| T _{DNARH} (T _{DNACKD_READ}) | Hold time on READ after the rising edge of CLK | 1 | | | | ns, Min |
| T _{DNADCKO} (T _{DNACKO_DOUT}) | Clock-to-output delay on DOUT after rising edge of CLK | 0.5 | | | | ns, Min |
| | | 6 | | | | ns, Max |
| T _{DNACLKF} ⁽²⁾ | CLK frequency | 2 | | | | MHz, Max |
| T _{DNACLKL} | CLK Low time | 50 | | | | ns, Min |
| T _{DNACLKH} | CLK High time | 50 | | | | ns, Min |

Notes:

1. The minimum READ pulse width is 8 ns, the maximum READ pulse width is 1 μs.
2. Also applies to TCK when reading DNA through the boundary-scan port.

Table 46: Suspend Mode Switching Characteristics

| Symbol | Description | Min | Max | Units |
|--------------------------------|--|-----|------|-------|
| Entering Suspend Mode | | | | |
| T _{SUSPENDHIGH_AWAKE} | Rising edge of SUSPEND pin to falling edge of AWAKE pin without glitch filter | 2.5 | 14 | ns |
| T _{SUSPENDFILTER} | Adjustment to SUSPEND pin rising edge parameters when glitch filter enabled | 31 | 430 | ns |
| T _{SUSPEND_GWE} | Rising edge of SUSPEND pin until FPGA output pins drive their defined SUSPEND constraint behavior (without glitch filter) | – | 15 | ns |
| T _{SUSPEND_GTS} | Rising edge of SUSPEND pin to write-protect lock on all writable clocked elements (without glitch filter) | – | 15 | ns |
| T _{SUSPEND_DISABLE} | Rising edge of the SUSPEND pin to FPGA input pins and interconnect disabled (without glitch filter) | – | 1500 | ns |
| Exiting Suspend Mode | | | | |
| T _{SUSPENDLOW_AWAKE} | Falling edge of the SUSPEND pin to rising edge of the AWAKE pin. Does not include DCM or PLL lock time. | 7 | 75 | μs |
| T _{SUSPEND_ENABLE} | Falling edge of the SUSPEND pin to FPGA input pins and interconnect re-enabled | 7 | 41 | μs |
| T _{AWAKE_GWE1} | Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using sw_clk:InternalClock and sw_gwe_cycle:1 . | – | 80 | ns |
| T _{AWAKE_GWE512} | Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using sw_clk:InternalClock and sw_gwe_cycle:512 . | – | 20.5 | μs |
| T _{AWAKE_GTS1} | Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using sw_clk:InternalClock and sw_gts_cycle:1 . | – | 80 | ns |
| T _{AWAKE_GTS512} | Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using sw_clk:InternalClock and sw_gts_cycle:512 . | – | 20.5 | μs |
| T _{SCP_AWAKE} | Rising edge of SCP pins to rising edge of AWAKE pin | 7 | 75 | μs |

Configuration Switching Characteristics

Table 47: Configuration Switching Characteristics⁽¹⁾

| Symbol | Description | Speed Grade | | | | Units |
|---|---|-------------|----------|----------|----------|-------------|
| | | -3 | -3N | -2 | -1L | |
| Power-up Timing Characteristics | | | | | | |
| T _{PL} ⁽²⁾ | PROGRAM_B Latency | 4 | 4 | 4 | 5 | ms, Max |
| T _{POR} ⁽²⁾ | Power-on reset (50 ms ramp time) ⁽³⁾ | 5/30 | 5/34 | 5/40 | 5/40 | ms, Min/Max |
| | Power-on reset (10 ms ramp time) | 5/25 | 5/29 | 5/35 | 5/40 | ms, Min/Max |
| T _{PROGRAM} | PROGRAM_B Pulse Width | 500 | 500 | 500 | 500 | ns, Min |
| Slave Serial Mode Programming Switching | | | | | | |
| T _{DCCK} /T _{CCKD} | DIN Setup/Hold, slave mode | 6.0/1.0 | 6.0/1.0 | 6.0/1.0 | 8.0/2.0 | ns, Min |
| T _{CCO} | CCLK to DOUT | 12 | 12 | 12 | 17 | ns, Max |
| F _{SCCK} | Slave mode external CCLK | 80 | 80 | 80 | 50 | MHz, Max |
| Slave SelectMAP Mode Programming Switching | | | | | | |
| T _{SMDCCK} /T _{SMCCKD} | SelectMAP Data Setup/Hold | 6.0/1.0 | 6.0/1.0 | 6.0/1.0 | 8.0/2.0 | ns, Min |
| T _{SMCSCCK} /T _{SMCCKCS} | CSI_B Setup/Hold | 7.0/0.0 | 7.0/0.0 | 7.0/0.0 | 9.0/2.0 | ns, Min |
| T _{SMWCCK} /T _{SMCCKW} | RDWR_B Setup/Hold | 17.0/1.0 | 17.0/1.0 | 17.0/1.0 | 27.0/2.0 | ns, Min |
| T _{SMCKCSO} | CSO_B clock to out | 16 | 16 | 16 | 26 | ns, Max |
| T _{SMCO} | CCLK to DATA out in readback | 13 | 13 | 13 | 25 | ns, Max |
| T _{SMCKBY} | CCLK to BUSY out in readback | 12 | 12 | 12 | 17 | ns, Max |
| F _{SMCCK} | Maximum CCLK frequency (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only) | 50 | 50 | 50 | 25 | MHz, Max |
| | Maximum CCLK frequency (LX100 and LX100T in x8 mode, LX150, and LX150T only) | 40 | 40 | 40 | 20 | MHz, Max |
| | Maximum CCLK frequency (LX100 and LX100T in x16 mode only) | 35 | 35 | 35 | 20 | MHz, Max |
| F _{RBCK} | Maximum Readback CCLK frequency, including block RAM (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only) | 20 | 20 | 20 | 4 | MHz, Max |
| | Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX4, LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T only) | 50 | 50 | 50 | 30 | MHz, Max |
| | Maximum Readback CCLK frequency, including block RAM (LX100, LX100T, LX150, and LX150T only) | 12 | 12 | 12 | 4 | MHz, Max |
| | Maximum Readback CCLK frequency, ignoring block RAM (POST_CRC) (LX100, LX100T, LX150, and LX150T only) | 35 | 35 | 35 | 20 | MHz, Max |
| Boundary-Scan Port Timing Specifications | | | | | | |
| T _{TAPTCK} | TMS and TDI Setup time before TCK | 10 | 10 | 10 | 17 | ns, Min |
| T _{TCKTAP} | TMS and TDI Hold time after TCK | 5.5 | 5.5 | 5.5 | 5.5 | ns, Min |
| T _{TCKTDO} | TCK falling edge to TDO output valid | 6.5 | 6.5 | 6.5 | 8 | ns, Max |
| T _{TCKH} | TCK clock minimum High time | 12 | 12 | 12 | 21 | ns, Min |
| T _{TCKL} | TCK clock minimum Low time | 12 | 12 | 12 | 21 | ns, Min |
| F _{TCK} | Maximum configuration TCK clock frequency | 33 | 33 | 33 | 18 | MHz, Max |
| F _{TCKB} | Maximum boundary-scan TCK clock frequency | 33 | 33 | 33 | 18 | MHz, Max |
| F _{TCKAES} | Maximum AES key TCK clock frequency | 2 | 2 | 2 | 2 | MHz, Max |

Table 47: Configuration Switching Characteristics⁽¹⁾ (Cont'd)

| Symbol | Description | Speed Grade | | | | Units |
|--|--|-------------|---------|---------|----------|-------------|
| | | -3 | -3N | -2 | -1L | |
| BPI Master Flash Mode Programming Switching⁽⁴⁾ | | | | | | |
| T _{BPICCO} ⁽⁵⁾ | A[25:0], FCS_B, FOE_B, FWE_B, LDC outputs valid after CCLK falling edge | 15 | 15 | 15 | 20 | ns, Max |
| T _{BPIICCK} | Master BPI CCLK (output) delay | 10/100 | 10/100 | 10/100 | 10/130 | μs, Min/Max |
| T _{BPIDCC} /T _{BPICCD} | Setup/Hold on D[15:0] data input pins | 5.0/1.0 | 5.0/1.0 | 5.0/1.0 | 6.0/2.0 | ns, Min |
| SPI Master Flash Mode Programming Switching⁽⁶⁾ | | | | | | |
| T _{SPIDCC} /T _{SPIDCCD} | DIN, MISO0, MISO1, MISO2, MISO3, Setup/Hold before/after the rising CCLK edge | 5.0/1.0 | 5.0/1.0 | 5.0/1.0 | 7.0/1.0 | ns, Min |
| T _{SPIICCK} | Master SPI CCLK (output) delay | 0.4/7.0 | 0.4/7.0 | 0.4/7.0 | 0.4/10.0 | μs, Min/Max |
| T _{SPICCM} | MOSI clock to out | 13 | 13 | 13 | 19 | ns, Max |
| T _{SPICFC} | CSO_B clock to out | 16 | 16 | 16 | 26 | ns, Max |
| CCLK Output (Master Modes) | | | | | | |
| T _{MCCKL} | Master CCLK clock duty cycle Low | 40/60 | | | | %, Min/Max |
| T _{MCCKH} | Master CCLK clock duty cycle High | 40/60 | | | | %, Min/Max |
| F _{MCCK} | Maximum frequency, serial mode (Master Serial/SPI) All devices | 40 | 40 | 40 | 30 | MHz, Max |
| | Maximum frequency, parallel mode (Master SelectMAP/BPI) LX9, LX16, LX25, LX25T, LX45, LX45T, LX75, and LX75T | 40 | 40 | 40 | 25 | MHz, Max |
| | Maximum frequency, parallel mode (Master SelectMAP/BPI) LX100 and LX100T in x8 mode, LX150, and LX150T | 40 | 40 | 40 | 20 | MHz, Max |
| | Maximum frequency, parallel mode (Master SelectMAP/BPI) LX100 and LX100T in x16 mode | 35 | 35 | 35 | 20 | MHz, Max |
| F _{MCCKTOL} | Frequency Tolerance, master mode | ±50 | ±50 | ±50 | ±50 | % |
| CCLK Input (Slave Modes) | | | | | | |
| T _{SCCKL} | Slave CCLK clock minimum Low time | 5 | 5 | 5 | 8 | ns, Min |
| T _{SCCKH} | Slave CCLK clock minimum High time | 5 | 5 | 5 | 8 | ns, Min |
| USERCCLK Input | | | | | | |
| T _{USERCCKL} | USERCCLK clock minimum Low time | 12 | 12 | 12 | 16 | ns, Min |
| T _{USERCCKH} | USERCCLK clock minimum High time | 12 | 12 | 12 | 16 | ns, Min |
| F _{USERCCLK} | Maximum USERCCLK frequency | 40 | 40 | 40 | 30 | MHz, Max |

Notes:

- Maximum frequency and setup/hold timing parameters are for 3.3V and 2.5V configuration voltages.
- To support longer delays in configuration, use the design solutions described in [UG380: Spartan-6 FPGA Configuration User Guide](#).
- [Table 6](#) specifies the power supply ramp time.
- BPI mode is not supported in:
 - LX4, LX25, or LX25T devices
 - LX9 devices in the TQG144 package
 - LX9 or LX16 devices in the CPG196 package.
- Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.
- Defense-grade Spartan-6Q -2Q devices configure in single default SPI Master (x1) mode at T_j = -55°C. During operation and when using all other configuration functions, the minimum operating temperature is -40°C.

Clock Buffers and Networks

Table 48: Global Clock Switching Characteristics (BUFGMUX)

| Symbol | Description | Devices | Speed Grade | | | | Units |
|---------------------------------------|--|-------------|-------------|------|------|------|-------|
| | | | -3 | -3N | -2 | -1L | |
| T_{GSI} (T_{GSI0} , T_{GSI1}) | S pin Setup to I0/I1 inputs | LX devices | 0.25 | 0.31 | 0.48 | 0.48 | ns |
| | | LXT devices | 0.25 | 0.31 | 0.48 | N/A | ns |
| T_{GIO} (T_{GIO0} , T_{GIO1}) | BUFGMUX delay from I0/I1 to O | LX devices | 0.21 | 0.21 | 0.21 | 0.21 | ns |
| | | LXT devices | 0.21 | 0.21 | 0.21 | N/A | ns |
| Maximum Frequency | | | | | | | |
| F_{MAX} | Global clock tree (BUFGMUX) ⁽¹⁾ | LX devices | 400 | 400 | 375 | 250 | MHz |
| | | LXT devices | 400 | 400 | 375 | N/A | MHz |

Notes:

- The BUFGMUX F_{MAX} values also apply to BUFH.

Table 49: Input/Output Clock Switching Characteristics (BUFIO2)

| Symbol | Description | Devices | Speed Grade | | | | Units |
|--------------------------------|--------------------------------|-------------|-------------|------|------|------|-------|
| | | | -3 | -3N | -2 | -1L | |
| T_{BUFCKO_O} ⁽¹⁾ | Clock to out delay from I to O | LX devices | 0.67 | 0.82 | 1.09 | 1.50 | ns |
| | | LXT devices | 0.67 | 0.82 | 1.09 | N/A | ns |
| Maximum Frequency | | | | | | | |
| F_{MAX} | I/O clock tree (BUFIO2) | LX devices | 540 | 525 | 500 | 300 | MHz |
| | | LXT devices | 540 | 525 | 500 | N/A | MHz |

Notes:

- T_{BUFCKO_O} reflects the longest delay of T_{BUFCKO_IOCLK} , T_{BUFCKO_DIVCLK} , and $T_{BUFCKO_SSTROBE}$. See TRACE reports for specific values.

Table 50: Input/Output Clock Switching Characteristics (BUFIO2FB)

| Symbol | Description | Devices | Speed Grade | | | | Units |
|--------------------------|---------------------------|-------------|-------------|------|-----|-----|-------|
| | | | -3 | -3N | -2 | -1L | |
| Maximum Frequency | | | | | | | |
| F_{MAX} | I/O clock tree (BUFIO2FB) | LX devices | 1080 | 1050 | 950 | 500 | MHz |
| | | LXT devices | 1080 | 1050 | 950 | N/A | MHz |

Table 51: Input/Output Clock Switching Characteristics (BUFPLL)

| Symbol | Description | Devices | Speed Grade | | | | Units |
|--------------------------|----------------------------|-------------|-------------|------|-----|-----|-------|
| | | | -3 | -3N | -2 | -1L | |
| Maximum Frequency | | | | | | | |
| F_{MAX} | BUFPLL clock tree (BUFPLL) | LX devices | 1080 | 1050 | 950 | 500 | MHz |
| | | LXT devices | 1080 | 1050 | 950 | N/A | MHz |

PLL Switching Characteristics

Table 52: PLL Specification

| Symbol | Description | Device ⁽¹⁾ | Speed Grade | | | | Units |
|------------------------------------|--|-----------------------|-------------------------------------|-------|-------|-------|-------|
| | | | -3 | -3N | -2 | -1L | |
| F _{INMAX} | Maximum Input Clock Frequency from I/O Clock (BUFIO2) | LX devices | 540 | 525 | 450 | 300 | MHz |
| | | LXT devices | 540 | 525 | 450 | N/A | MHz |
| | Maximum Input Clock Frequency from Global Clock Buffer (BUFGMUX) | LX devices | 400 | 400 | 375 | 250 | MHz |
| | | LXT devices | 400 | 400 | 375 | N/A | MHz |
| F _{INMIN} | Minimum Input Clock Frequency | LX devices | 19 | 19 | 19 | 19 | MHz |
| | | LXT devices | 19 | 19 | 19 | N/A | MHz |
| F _{INJITTER} | Maximum Input Clock Period Jitter: 19–200 MHz | All | 1 ns Maximum | | | | |
| | Maximum Input Clock Period Jitter: > 200 MHz | All | <20% of clock input period Maximum | | | | |
| F _{INDUTY} | Allowable Input Duty Cycle: 19—199 MHz | All | 25/75 | | | | % |
| | Allowable Input Duty Cycle: 200—299 MHz | All | 35/65 | | | | % |
| | Allowable Input Duty Cycle: > 300 MHz | All | 45/55 | | | | % |
| F _{VCOMIN} | Minimum PLL VCO Frequency | LX devices | 400 | 400 | 400 | 400 | MHz |
| | | LXT devices | 400 | 400 | 400 | N/A | MHz |
| F _{VCOMAX} | Maximum PLL VCO Frequency | LX devices | 1080 | 1050 | 1000 | 1000 | MHz |
| | | LXT devices | 1080 | 1050 | 1000 | N/A | MHz |
| F _{BANDWIDTH} | Low PLL Bandwidth at Typical ⁽³⁾ | All | 1 | 1 | 1 | 1 | MHz |
| | High PLL Bandwidth at Typical ⁽³⁾ | All | 4 | 4 | 4 | 4 | MHz |
| T _{STAPHAOFFSET} | Static Phase Offset of the PLL Outputs | All | 0.12 | 0.12 | 0.12 | 0.15 | ns |
| T _{OUTJITTER} | PLL Output Jitter ⁽³⁾ | All | Note 2 | | | | |
| T _{OUTDUTY} | PLL Output Clock Duty Cycle Precision ⁽⁴⁾ | All | 0.15 | 0.15 | 0.20 | 0.25 | ns |
| T _{LOCKMAX} | PLL Maximum Lock Time | All | 100 | 100 | 100 | 100 | µs |
| F _{OUTMAX} | PLL Maximum Output Frequency for BUFGMUX | LX devices | 400 | 400 | 375 | 250 | MHz |
| | | LXT devices | 400 | 400 | 375 | N/A | MHz |
| | PLL Maximum Output Frequency for BUFPLL | LX devices | 1080 | 1050 | 950 | 500 | MHz |
| | | LXT devices | 1080 | 1050 | 950 | N/A | MHz |
| F _{OUTMIN} | PLL Minimum Output Frequency ⁽⁵⁾ | All | 3.125 | 3.125 | 3.125 | 3.125 | MHz |
| T _{EXTFDVAR} | External Clock Feedback Variation: 19–200 MHz | All | 1 ns Maximum | | | | |
| | External Clock Feedback Variation: > 200 MHz | All | < 20% of clock input period Maximum | | | | |
| RST _{MINPULSE} | Minimum Reset Pulse Width | All | 5 | 5 | 5 | 5 | ns |
| F _{PFDMAX} ⁽⁶⁾ | Maximum Frequency at the Phase Frequency Detector | LX devices | 500 | 500 | 400 | 300 | MHz |
| | | LXT devices | 500 | 500 | 400 | N/A | MHz |
| F _{PFDMIN} | Minimum Frequency at the Phase Frequency Detector | LX devices | 19 | 19 | 19 | 19 | MHz |
| | | LXT devices | 19 | 19 | 19 | N/A | MHz |

Table 52: PLL Specification (Cont'd)

| Symbol | Description | Device ⁽¹⁾ | Speed Grade | | | | Units |
|---------------|------------------------------------|-----------------------|-----------------------------|-----|----|-----|-------|
| | | | -3 | -3N | -2 | -1L | |
| $T_{FBDELAY}$ | Maximum Delay in the Feedback Path | All | 3 ns Max or one CLKIN cycle | | | | |

Notes:

1. LXT devices are not available with a -1L speed grade.
2. Values for this parameter are available in the Clocking Wizard.
3. The PLL does not filter typical spread spectrum input clocks because they are usually far below the bandwidth filter frequencies.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.
6. When using $CLK_FEEDBACK = CLKOUT0$ with $BUFIO2$ feedback, the feedback frequency will be higher than the phase frequency detector frequency. $F_{PFDMAX} = F_{CLKFB} / CLKFBOUT_MULT$

DCM Switching Characteristics

Table 53: Operating Frequency Ranges and Conditions for the Delay-Locked Loop (DLL)⁽¹⁾

| Symbol | Description | Speed Grade | | | | | | | | Units |
|--|--|------------------|--------------------|------------------|--------------------|------------------|--------------------|------------------|--------------------|-------|
| | | -3 | | -3N | | -2 | | -1L | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Input Frequency Ranges | | | | | | | | | | |
| CLKIN_FREQ_DLL | Frequency of the CLKIN clock input when the CLKDV output is not used. | 5 ⁽²⁾ | 280 ⁽³⁾ | 5 ⁽²⁾ | 280 ⁽³⁾ | 5 ⁽²⁾ | 250 ⁽³⁾ | 5 ⁽²⁾ | 175 ⁽³⁾ | MHz |
| | Frequency of the CLKIN clock input when using the CLKDV output. | 5 ⁽²⁾ | 280 ⁽³⁾ | 5 ⁽²⁾ | 280 ⁽³⁾ | 5 ⁽²⁾ | 250 ⁽³⁾ | 5 ⁽²⁾ | 133 ⁽³⁾ | MHz |
| Input Pulse Requirements | | | | | | | | | | |
| CLKIN_PULSE | CLKIN pulse width as a percentage of the CLKIN period for CLKIN_FREQ_DLL < 150 MHz | 40 | 60 | 40 | 60 | 40 | 60 | 40 | 60 | % |
| | CLKIN pulse width as a percentage of the CLKIN period for CLKIN_FREQ_DLL > 150 MHz | 45 | 55 | 45 | 55 | 45 | 55 | 45 | 55 | % |
| Input Clock Jitter Tolerance and Delay Path Variation⁽⁴⁾ | | | | | | | | | | |
| CLKIN_CYC_JITT_DLL_LF | Cycle-to-cycle jitter at the CLKIN input for CLKIN_FREQ_DLL < 150 MHz | – | ±300 | – | ±300 | – | ±300 | – | ±300 | ps |
| CLKIN_CYC_JITT_DLL_HF | Cycle-to-cycle jitter at the CLKIN input for CLKIN_FREQ_DLL > 150 MHz. | – | ±150 | – | ±150 | – | ±150 | – | ±150 | ps |
| CLKIN_PER_JITT_DLL | Period jitter at the CLKIN input. | – | ±1 | – | ±1 | – | ±1 | – | ±1 | ns |
| CLKFB_DELAY_VAR_EXT | Allowable variation of the off-chip feedback delay from the DCM output to the CLKFB input. | – | ±1 | – | ±1 | – | ±1 | – | ±1 | ns |

Notes:

- DLL specifications apply when using any of the DLL outputs: CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV.
- When operating independently of the DLL, the DFS supports lower CLKIN_FREQ_DLL frequencies. See [Table 55](#).
- The CLKIN_DIVIDE_BY_2 attribute increases the effective input frequency range. When set to TRUE, the input clock frequency is divided by two as it enters the DCM. Input clock frequencies for the clock buffer being used can be increased up to the F_{MAX} (see [Table 48](#) and [Table 49](#) for BUFGMUX and BUFIO2 limits). When used with CLK_FEEDBACK=2X, the input clock frequency matches the frequency for CLK2X, and is limited to CLKOUT_FREQ_2X.
- CLKIN_FREQ_DLL input jitter beyond these limits can cause the DCM to lose LOCK, indicated by the LOCKED output deasserting. The user must then reset the DCM.
- When using both DCMs in a CMT, both DCMs must be LOCKED.

Table 54: Switching Characteristics for the Delay-Locked Loop (DLL)⁽¹⁾

| Symbol | Description | Speed Grade | | | | | | | | Units |
|--|---|---|------|--------|------|--------|------|---------------------------------------|------|-------|
| | | -3 | | -3N | | -2 | | -1L | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Output Frequency Ranges | | | | | | | | | | |
| CLKOUT_FREQ_CLK0 | Frequency for the CLK0 and CLK180 outputs. | 5 | 280 | 5 | 280 | 5 | 250 | 5 | 175 | MHz |
| CLKOUT_FREQ_CLK90 | Frequency for the CLK90 and CLK270 outputs. | 5 | 200 | 5 | 200 | 5 | 200 | 5 | 175 | MHz |
| CLKOUT_FREQ_2X | Frequency for the CLK2X and CLK2X180 outputs. | 10 | 375 | 10 | 375 | 10 | 334 | 10 | 250 | MHz |
| CLKOUT_FREQ_DV | Frequency for the CLKDV output. | 0.3125 | 186 | 0.3125 | 186 | 0.3125 | 166 | 0.3125 | 88.6 | MHz |
| Output Clock Jitter⁽²⁾⁽³⁾⁽⁴⁾ | | | | | | | | | | |
| CLKOUT_PER_JITT_0 | Period jitter at the CLK0 output. | – | ±100 | – | ±100 | – | ±100 | – | ±100 | ps |
| CLKOUT_PER_JITT_90 | Period jitter at the CLK90 output. | – | ±150 | – | ±150 | – | ±150 | – | ±150 | ps |
| CLKOUT_PER_JITT_180 | Period jitter at the CLK180 output. | – | ±150 | – | ±150 | – | ±150 | – | ±150 | ps |
| CLKOUT_PER_JITT_270 | Period jitter at the CLK270 output. | – | ±150 | – | ±150 | – | ±150 | – | ±150 | ps |
| CLKOUT_PER_JITT_2X | Period jitter at the CLK2X and CLK2X180 outputs. | Maximum = ±[0.5% of CLKIN period + 100] | | | | | | | | ps |
| CLKOUT_PER_JITT_DV1 | Period jitter at the CLKDV output when performing integer division. | – | ±150 | – | ±150 | – | ±150 | – | ±150 | ps |
| CLKOUT_PER_JITT_DV2 | Period jitter at the CLKDV output when performing non-integer division. | Maximum = ±[0.5% of CLKIN period + 100] | | | | | | | | ps |
| Duty Cycle⁽⁴⁾ | | | | | | | | | | |
| CLKOUT_DUTY_CYCLE_DLL | Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion. | Typical = ±[1% of CLKIN period + 350] | | | | | | | | ps |
| Phase Alignment⁽⁴⁾ | | | | | | | | | | |
| CLKIN_CLKFB_PHASE | Phase offset between the CLKIN and CLKFB inputs (CLK_FEEDBACK = 1X). | – | ±150 | – | ±150 | – | ±150 | – | ±250 | ps |
| | Phase offset between the CLKIN and CLKFB inputs (CLK_FEEDBACK = 2X). ⁽⁶⁾ | – | ±250 | – | ±250 | – | ±250 | – | ±350 | |
| CLKOUT_PHASE_DLL | Phase offset between DLL outputs for CLK0 to CLK2X (not CLK2X180). | Maximum = ±[1% of CLKIN period + 100] | | | | | | | | ps |
| | Phase offset between DLL outputs for all others. | Maximum = ±[1% of CLKIN period + 150] | | | | | | Maximum = ±[1% of CLKIN period + 200] | | ps |

Table 54: Switching Characteristics for the Delay-Locked Loop (DLL)⁽¹⁾ (Cont'd)

| Symbol | Description | Speed Grade | | | | | | | | Units |
|-------------------------------|--|-------------|------|-----|------|-----|------|-----|------|-------|
| | | -3 | | -3N | | -2 | | -1L | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| LOCK_DLL ⁽³⁾ | When using the DLL alone: The time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase. CLKIN_FREQ_DLL < 50 MHz. | - | 5 | - | 5 | - | 5 | - | 5 | ms |
| | When using the DLL alone: The time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase. CLKIN_FREQ_DLL > 50 MHz | - | 0.60 | - | 0.60 | - | 0.60 | - | 0.60 | ms |
| Delay Lines | | | | | | | | | | |
| DCM_DELAY_STEP ⁽⁵⁾ | Finest delay resolution, averaged over all steps. | 10 | 40 | 10 | 40 | 10 | 40 | 10 | 40 | ps |

Notes:

1. The values in this table are based on the operating conditions described in Table 2 and Table 53.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster LOCK time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, this data sheet specifies a maximum jitter of ±(1% of CLKIN period + 150 ps). Assuming that the CLKIN frequency is 100 MHz, the equivalent CLKIN period is 10 ns. Since 1% of 10 ns is 0.1 ns or 100 ps, the maximum jitter is ±(100 ps + 150 ps) = ±250 ps.
5. A typical delay step size is 23 ps.
6. The timing analysis tools use the CLK_FEEDBACK = 1X condition for the CLKIN_CLKFB_PHASE value (reported as phase error). When using CLK_FEEDBACK = 2X, add 100 ps to the phase error for the CLKIN_CLKFB_PHASE value (as shown in this table).

Table 55: Recommended Operating Conditions for the Digital Frequency Synthesizer (DFS)⁽¹⁾

| Symbol | Description | Speed Grade | | | | | | | | Units |
|---|--|-------------|--------------------|-----|--------------------|-----|--------------------|-----|--------------------|-------|
| | | -3 | | -3N | | -2 | | -1L | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Input Frequency Ranges⁽²⁾ | | | | | | | | | | |
| CLKIN_FREQ_FX | Frequency for the CLKIN input. Also described as F _{CLKIN} . | 0.5 | 375 ⁽³⁾ | 0.5 | 375 ⁽³⁾ | 0.5 | 333 ⁽³⁾ | 0.5 | 200 ⁽³⁾ | MHz |
| Input Clock Jitter Tolerance⁽⁴⁾ | | | | | | | | | | |
| CLKIN_CYC_JITT_FX_LF | Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency: F _{CLKFX} < 150 MHz. | - | ±300 | - | ±300 | - | ±300 | - | ±300 | ps |
| CLKIN_CYC_JITT_FX_HF | Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency: F _{CLKFX} > 150 MHz. | - | ±150 | - | ±150 | - | ±150 | - | ±150 | ps |
| CLKIN_PER_JITT_FX | Period jitter at the CLKIN input. | - | ±1 | - | ±1 | - | ±1 | - | ±1 | ns |

Notes:

1. DFS specifications apply when using either of the DFS outputs (CLKFX or CLKFX180).
2. When using both DFS and DLL outputs on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 53.
3. The CLKIN_DIVIDE_BY_2 attribute increases the effective input frequency range. When set to TRUE, the input clock frequency is divided by two as it enters the DCM. Input clock frequencies for the clock buffer being used can be increased up to the F_{MAX} (see Table 48 and Table 49 for BUFGMUX and BUFIO2 limits).
4. CLKIN input jitter beyond these limits can cause the DCM to lose LOCK.

Table 56: Switching Characteristics for the Digital Frequency Synthesizer (DFS) for DCM_SP⁽¹⁾

| Symbol | Description | Speed Grade | | | | | | | | Units |
|--|---|---------------------------------------|------|-----|------|-----|------|-----|------|-------|
| | | -3 | | -3N | | -2 | | -1L | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Output Frequency Ranges | | | | | | | | | | |
| CLKOUT_FREQ_FX | Frequency for the CLKFX and CLKFX180 outputs | 5 | 375 | 5 | 375 | 5 | 333 | 5 | 200 | MHz |
| Output Clock Jitter⁽²⁾⁽³⁾ | | | | | | | | | | |
| CLKOUT_PER_JITT_FX | Period jitter at the CLKFX and CLKFX180 outputs. When CLKIN < 20 MHz | Use the Clocking Wizard | | | | | | | | ps |
| | Period jitter at the CLKFX and CLKFX180 outputs. When CLKIN > 20 MHz | Typical = ±(1% of CLKFX period + 100) | | | | | | | | ps |
| Duty Cycle⁽⁴⁾⁽⁵⁾ | | | | | | | | | | |
| CLKOUT_DUTY_CYCLE_FX | Duty cycle precision for the CLKFX and CLKFX180 outputs including the BUFGMUX and clock tree duty-cycle distortion | Maximum = ±(1% of CLKFX period + 350) | | | | | | | | ps |
| Phase Alignment (Phase Error)⁽⁵⁾ | | | | | | | | | | |
| CLKOUT_PHASE_FX | Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used | - | ±200 | - | ±200 | - | ±200 | - | ±250 | ps |
| CLKOUT_PHASE_FX180 | Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used | Maximum = ±(1% of CLKFX period + 200) | | | | | | | | ps |
| LOCKED Time | | | | | | | | | | |
| LOCK_FX ⁽²⁾ | When FCLKIN < 50 MHz, the time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. When using both the DLL and the DFS, use the longer locking time. | - | 5 | - | 5 | - | 5 | - | 5 | ms |
| | When FCLKIN > 50 MHz, the time from deassertion at the DCM's reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. When using both the DLL and the DFS, use the longer locking time. | - | 0.45 | - | 0.45 | - | 0.45 | - | 0.60 | ms |

Notes:

1. The values in this table are based on the operating conditions described in Table 2 and Table 55.
2. For optimal jitter tolerance and a faster LOCK time, use the CLKIN_PERIOD attribute.
3. Output jitter is characterized with no input jitter. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply, and PCB design. The actual maximum output jitter depends on the system application.
4. The CLKFX, CLKFXDV, and CLKFX180 outputs have a duty cycle of approximately 50%.
5. Some duty cycle and alignment specifications include a percentage of the CLKFX output period. For example, this data sheet specifies a maximum CLKFX jitter of ±(1% of CLKFX period + 200 ps). Assuming that the CLKFX output frequency is 100 MHz, the equivalent CLKFX period is 10 ns, and 1% of 10 ns is 0.1 ns or 100 ps. Accordingly, the maximum jitter is ±(100 ps + 200 ps) = ±300 ps.

Table 57: Switching Characteristics for the Digital Frequency Synthesizer DFS (DCM_CLKGEN)⁽¹⁾

| Symbol | Description | Speed Grade | | | | | | | | Units |
|---|---|--|-------|---------|-------|---------|-------|---------|-----|-------|
| | | -3 | | -3N | | -2 | | -1L | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Output Frequency Ranges (DCM_CLKGEN) | | | | | | | | | | |
| CLKOUT_FREQ_FX | Frequency for the CLKFX and CLKFX180 outputs | 5 | 375 | 5 | 375 | 5 | 333 | 5 | 200 | MHz |
| CLKOUT_FREQ_FXDV | Frequency for the CLKFXDV output | 0.15625 | 187.5 | 0.15625 | 187.5 | 0.15625 | 166.5 | 0.15625 | 100 | MHz |
| Output Clock Jitter⁽²⁾⁽³⁾ | | | | | | | | | | |
| CLKOUT_PER_JITT_FX | Period jitter at the CLKFX and CLKFX180 outputs. | Typical = $\pm[0.2\% \text{ of CLKFX period} + 100]$ | | | | | | | | ps |
| CLKOUT_PER_JITT_FXDV | Period jitter at the CLKFXDV output. | Typical = $\pm[0.2\% \text{ of CLKFX period} + 100]$ | | | | | | | | ps |
| CLKFX_FREEZE_VAR | CLKFX period change in free running oscillator mode at the same temperature. FCLKFX > 50 MHz | Maximum = $\pm 3\%$ of CLKFX period | | | | | | | | ps |
| | CLKFX period change in free running oscillator mode at the same temperature. FCLKFX < 50 MHz | Maximum = $\pm 5\%$ of CLKFX period | | | | | | | | ps |
| CLKFX_FREEZE_TEMP_SLOPE | CLKFX period will change in free_oscillator mode over temperature. Add to CLKFX_FREEZE_VAR to determine total CLKFX period change. Percentage change for CLKFX period over 1°C. | Maximum = 0.1 | | | | | | | | %/°C |
| Duty Cycle⁽⁴⁾⁽⁵⁾ | | | | | | | | | | |
| CLKOUT_DUTY_CYCLE_FX | Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion | Maximum = $\pm[1\% \text{ of CLKFX period} + 350]$ | | | | | | | | ps |
| CLKOUT_DUTY_CYCLE_FXDV | Duty cycle precision for the CLKFXDV outputs, including the BUFGMUX and clock tree duty-cycle distortion | Maximum = $\pm[1\% \text{ of CLKFX period} + 350]$ | | | | | | | | ps |
| Lock Time | | | | | | | | | | |
| LOCK_FX ⁽²⁾⁽⁷⁾ | The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX, CLKFX180, and CLKFXDV signals are valid. Lock time requires CLKFX_DIVIDE < F _{IN} /(0.50 MHz) | – | 50 | – | 50 | – | 50 | – | 50 | ms |
| | when: F _{CLKIN} > 50 MHz | – | 5 | – | 5 | – | 5 | – | 5 | ms |

Table 57: Switching Characteristics for the Digital Frequency Synthesizer DFS (DCM_CLKGEN)⁽¹⁾ (Cont'd)

| Symbol | Description | Speed Grade | | | | | | | | Units |
|---|--|---|-----|-----|-----|-----|-----|-----|-----|-------|
| | | -3 | | -3N | | -2 | | -1L | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Spread Spectrum | | | | | | | | | | |
| F _{CLKIN_FIXED_SPREAD_SPECTRUM} | Frequency of the CLKIN input for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD/ CENTER_HIGH_SPREAD) | 30 | 200 | 30 | 200 | 30 | 200 | 30 | 200 | MHz |
| T _{CENTER_LOW_SPREAD} ⁽⁶⁾ | Spread at the CLKFX output for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD) | Typical = $\frac{100}{\text{CLKFX_DIVIDE}}$ Maximum = 250 | | | | | | | | ps |
| T _{CENTER_HIGH_SPREAD} ⁽⁶⁾ | Spread at the CLKFX output for fixed spread spectrum (SPREAD_SPECTRUM = CENTER_HIGH_SPREAD) | Typical = $\frac{240}{\text{CLKFX_DIVIDE}}$ Maximum = 400 | | | | | | | | ps |
| F _{MOD_FIXED_SPREAD_SPECTRUM} ⁽⁶⁾ | Average modulation frequency when using fixed spread spectrum (SPREAD_SPECTRUM = CENTER_LOW_SPREAD / CENTER_HIGH_SPREAD) | Typical = F _{IN} /1024 | | | | | | | | MHz |

Notes:

- The values in this table are based on the operating conditions described in Table 2 and Table 55.
- For optimal jitter tolerance and a faster LOCK time, use the CLKIN_PERIOD attribute.
- Output jitter is characterized with no input jitter. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply, and PCB design. The actual maximum output jitter depends on the system application.
- The CLKFX, CLKFXDV, and CLKFX180 outputs have a duty cycle of approximately 50%.
- Some duty-cycle and alignment specifications include a percentage of the CLKFX output period. For example, this data sheet specifies a maximum CLKFX jitter of ±(1% of CLKFX period + 200 ps). Assuming that the CLKFX output frequency is 100 MHz, the equivalent CLKFX period is 10 ns, and 1% of 10 ns is 0.1 ns or 100 ps. Accordingly, the maximum jitter is ±(100 ps + 200 ps) = ±300 ps.
- When using CENTER_LOW_SPREAD, CENTER_HIGH_SPREAD, the valid values for CLKFX_MULTIPLY are limited to 2 through 32, and the valid values for CLKFX_DIVIDE are limited to 1 through 4, with the resulting CLKFX or CLKFX180 output frequency limited to a minimum of 50 MHz.
- When using dynamic frequency synthesis, LOCK_FX does not apply.

Table 58: Recommended Operating Conditions for the Phase-Shift Clock in Variable Phase Mode (DCM_SP) or Dynamic Frequency Synthesis (DCM_CLKGEN)

| Symbol | Description | Speed Grade | | | | | | | | Units |
|-----------------------------------|---|-------------|-----|-----|-----|-----|-----|-----|-----|-------|
| | | -3 | | -3N | | -2 | | -1L | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Operating Frequency Ranges | | | | | | | | | | |
| PSCLK_FREQ | Frequency for the PSCLK (DCM_SP) or PROGCLK (DCM_CLKGEN) input. | 1 | 167 | 1 | 167 | 1 | 167 | 1 | 100 | MHz |
| Input Pulse Requirements | | | | | | | | | | |
| PSCLK_PULSE | PSCLK (DCM_SP) or PROGCLK (DCM_CLKGEN) pulse width as a percentage of the clock period. | 40 | 60 | 40 | 60 | 40 | 60 | 40 | 60 | % |

Table 59: Switching Characteristics for the Phase-Shift Clock in Variable Phase Mode⁽¹⁾

| Symbol | Description | Amount of Phase Shift | Units |
|-----------------------------|---|-----------------------------------|-------|
| Phase Shifting Range | | | |
| MAX_STEPS ⁽²⁾ | When CLKIN < 60 MHz, the maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. When using CLKIN_DIVIDE_BY_2 = TRUE, double the clock-effective clock period. | ±(INTEGER(10 x (TCLKIN – 3 ns))) | steps |
| | When CLKIN ≥ 60 MHz, the maximum allowed number of DCM_DELAY_STEP steps for a given CLKIN clock period, where T = CLKIN clock period in ns. When using CLKIN_DIVIDE_BY_2 = TRUE, double the clock-effective clock period. | ±(INTEGER(15 x (TCLKIN – 3 ns))) | steps |
| FINE_SHIFT_RANGE_MIN | Minimum guaranteed delay for variable phase shifting. | ±(MAX_STEPS x DCM_DELAY_STEP_MIN) | ps |
| FINE_SHIFT_RANGE_MAX | Maximum guaranteed delay for variable phase shifting | ±(MAX_STEPS x DCM_DELAY_STEP_MAX) | ps |

Notes:

1. The values in this table are based on the operating conditions described in Table 53 and Table 58.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM has no initial fixed-phase shifting, that is, the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the end of Table 54.

Table 60: Miscellaneous DCM Timing Parameters⁽¹⁾

| Symbol | Description | Min | Max | Units |
|----------------|---------------------------------------|-----|-----|--------------|
| DCM_RST_PW_MIN | Minimum duration of a RST pulse width | 3 | – | CLKIN cycles |

Notes:

1. This limit only applies to applications that use the DCM DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV). The DCM DFS outputs (CLKFX, CLKFXDV, CLKFX180) are unaffected.

Table 61: Frequency Synthesis

| Attribute | Min | Max |
|-----------------------------|-----|-----|
| CLKFX_MULTIPLY (DCM_SP) | 2 | 32 |
| CLKFX_DIVIDE (DCM_SP) | 1 | 32 |
| CLKDV_DIVIDE (DCM_SP) | 1.5 | 16 |
| CLKFX_MULTIPLY (DCM_CLKGEN) | 2 | 256 |
| CLKFX_DIVIDE (DCM_CLKGEN) | 1 | 256 |
| CLKFXDV_DIVIDE (DCM_CLKGEN) | 2 | 32 |

Table 62: DCM Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|---|------------------------|---------------|---------------|---------------|---------------|-------|
| | | -3 | -3N | -2 | -1L | |
| T _{DMCK_PSEN} /T _{DMCKC_PSEN} | PSEN Setup/Hold | 1.50/ 0.00 | 1.50/ 0.00 | 1.50/ 0.00 | 1.50/ 0.00 | ns |
| T _{DMCK_PSINCDEC} /T _{DMCKC_PSINCDEC} | PSINCDEC Setup/Hold | 1.50/ 0.00 | 1.50/ 0.00 | 1.50/ 0.00 | 1.50/ 0.00 | ns |
| T _{DMCKO_PSDONE} | Clock to out of PSDONE | 1.50 | 1.50 | 1.50 | 1.50 | ns |

Spartan-6 Device Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in [Table 63](#) through [Table 69](#). Values are expressed in nanoseconds unless otherwise noted.

Table 63: Global Clock Input to Output Delay Without DCM or PLL

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|--|------------|-------------|-------|------|-------|-------|
| | | | -3 | -3N | -2 | -1L | |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>without</i> DCM or PLL | | | | | | | |
| T _{ICKOF} | Global Clock and OUTFF <i>without</i> DCM or PLL | XC6SLX4 | 6.12 | N/A | 7.68 | 9.41 | ns |
| | | XC6SLX9 | 6.12 | 6.51 | 7.68 | 9.41 | ns |
| | | XC6SLX16 | 5.98 | 6.42 | 7.48 | 9.10 | ns |
| | | XC6SLX25 | 6.20 | 6.69 | 7.84 | 9.44 | ns |
| | | XC6SLX25T | 6.20 | 6.69 | 7.84 | N/A | ns |
| | | XC6SLX45 | 6.37 | 6.88 | 8.10 | 9.61 | ns |
| | | XC6SLX45T | 6.37 | 6.88 | 8.10 | N/A | ns |
| | | XC6SLX75 | 6.39 | 6.99 | 8.16 | 10.18 | ns |
| | | XC6SLX75T | 6.39 | 6.99 | 8.16 | N/A | ns |
| | | XC6SLX100 | 6.59 | 7.18 | 8.41 | 10.31 | ns |
| | | XC6SLX100T | 6.59 | 7.18 | 8.41 | N/A | ns |
| | | XC6SLX150 | 6.98 | 7.68 | 8.80 | 10.62 | ns |
| | | XC6SLX150T | 6.98 | 7.68 | 8.80 | N/A | ns |
| | | XA6SLX4 | 6.44 | N/A | 7.68 | N/A | ns |
| | | XA6SLX9 | 6.44 | N/A | 7.68 | N/A | ns |
| | | XA6SLX16 | 6.30 | N/A | 7.48 | N/A | ns |
| | | XA6SLX25 | 6.52 | N/A | 7.84 | N/A | ns |
| | | XA6SLX25T | 6.52 | N/A | 7.84 | N/A | ns |
| | | XA6SLX45 | 6.69 | N/A | 8.12 | N/A | ns |
| | | XA6SLX45T | 6.69 | N/A | 8.12 | N/A | ns |
| | | XA6SLX75 | 6.89 | N/A | 8.16 | N/A | ns |
| | | XA6SLX75T | 6.89 | N/A | 8.16 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 8.36 | N/A | ns |
| XQ6SLX75 | N/A | N/A | 8.16 | 10.18 | ns | | |
| XQ6SLX75T | 6.89 | N/A | 8.16 | N/A | ns | | |
| XQ6SLX150 | N/A | N/A | 8.80 | 10.62 | ns | | |
| XQ6SLX150T | 7.61 | N/A | 8.80 | N/A | ns | | |

Notes:

- Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Table 64: Global Clock Input to Output Delay With DCM in System-Synchronous Mode

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|--|------------|-------------|------|------|------|-------|
| | | | -3 | -3N | -2 | -1L | |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in System-Synchronous Mode. | | | | | | | |
| T _{ICKOFDCM} | Global Clock and OUTFF <i>with</i> DCM | XC6SLX4 | 4.23 | N/A | 6.11 | 6.60 | ns |
| | | XC6SLX9 | 4.23 | 5.17 | 6.11 | 6.60 | ns |
| | | XC6SLX16 | 4.28 | 4.57 | 5.34 | 6.36 | ns |
| | | XC6SLX25 | 3.95 | 4.18 | 4.59 | 6.91 | ns |
| | | XC6SLX25T | 3.95 | 4.18 | 4.59 | N/A | ns |
| | | XC6SLX45 | 4.37 | 4.70 | 5.50 | 6.85 | ns |
| | | XC6SLX45T | 4.37 | 4.70 | 5.50 | N/A | ns |
| | | XC6SLX75 | 3.90 | 4.23 | 4.77 | 6.31 | ns |
| | | XC6SLX75T | 3.90 | 4.23 | 4.77 | N/A | ns |
| | | XC6SLX100 | 3.86 | 4.16 | 4.66 | 7.25 | ns |
| | | XC6SLX100T | 3.90 | 4.16 | 4.66 | N/A | ns |
| | | XC6SLX150 | 4.03 | 4.33 | 4.83 | 6.63 | ns |
| | | XC6SLX150T | 4.03 | 4.33 | 4.83 | N/A | ns |
| | | XA6SLX4 | 4.55 | N/A | 6.11 | N/A | ns |
| | | XA6SLX9 | 4.55 | N/A | 6.11 | N/A | ns |
| | | XA6SLX16 | 4.62 | N/A | 5.33 | N/A | ns |
| | | XA6SLX25 | 4.27 | N/A | 4.59 | N/A | ns |
| | | XA6SLX25T | 4.27 | N/A | 4.69 | N/A | ns |
| | | XA6SLX45 | 4.69 | N/A | 5.50 | N/A | ns |
| | | XA6SLX45T | 4.69 | N/A | 5.50 | N/A | ns |
| | | XA6SLX75 | 4.22 | N/A | 4.77 | N/A | ns |
| | | XA6SLX75T | 4.22 | N/A | 4.77 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 5.34 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 4.77 | 6.31 | ns |
| | | XQ6SLX75T | 4.22 | N/A | 4.77 | N/A | ns |
| | | XQ6SLX150 | N/A | N/A | 4.96 | 6.63 | ns |
| | | XQ6SLX150T | 4.62 | N/A | 4.96 | N/A | ns |

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Table 65: Global Clock Input to Output Delay With DCM in Source-Synchronous Mode

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|--|------------|-------------|------|------|------|-------|
| | | | -3 | -3N | -2 | -1L | |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in Source-Synchronous Mode. | | | | | | | |
| T _{ICKOFDCM_0} | Global Clock and OUTFF <i>with</i> DCM | XC6SLX4 | 5.03 | N/A | 7.21 | 8.05 | ns |
| | | XC6SLX9 | 5.03 | 6.13 | 7.21 | 8.05 | ns |
| | | XC6SLX16 | 5.08 | 5.51 | 6.44 | 7.96 | ns |
| | | XC6SLX25 | 4.81 | 5.13 | 5.69 | 7.94 | ns |
| | | XC6SLX25T | 4.81 | 5.13 | 5.69 | N/A | ns |
| | | XC6SLX45 | 5.26 | 5.69 | 6.63 | 7.92 | ns |
| | | XC6SLX45T | 5.26 | 5.69 | 6.63 | N/A | ns |
| | | XC6SLX75 | 4.77 | 5.18 | 5.88 | 7.95 | ns |
| | | XC6SLX75T | 4.77 | 5.18 | 5.88 | N/A | ns |
| | | XC6SLX100 | 4.72 | 5.11 | 5.76 | 8.59 | ns |
| | | XC6SLX100T | 4.76 | 5.11 | 5.76 | N/A | ns |
| | | XC6SLX150 | 4.90 | 5.30 | 5.93 | 7.93 | ns |
| | | XC6SLX150T | 4.90 | 5.30 | 5.93 | N/A | ns |
| | | XA6SLX4 | 5.35 | N/A | 7.21 | N/A | ns |
| | | XA6SLX9 | 5.35 | N/A | 7.21 | N/A | ns |
| | | XA6SLX16 | 5.42 | N/A | 6.44 | N/A | ns |
| | | XA6SLX25 | 5.13 | N/A | 5.69 | N/A | ns |
| | | XA6SLX25T | 5.13 | N/A | 5.79 | N/A | ns |
| | | XA6SLX45 | 5.58 | N/A | 6.63 | N/A | ns |
| | | XA6SLX45T | 5.58 | N/A | 6.63 | N/A | ns |
| | | XA6SLX75 | 5.09 | N/A | 5.87 | N/A | ns |
| | | XA6SLX75T | 5.09 | N/A | 5.87 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 6.44 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 5.87 | 7.95 | ns |
| XQ6SLX75T | 5.09 | N/A | 5.87 | N/A | ns | | |
| XQ6SLX150 | N/A | N/A | 6.06 | 7.93 | ns | | |
| XQ6SLX150T | 5.50 | N/A | 6.06 | N/A | ns | | |

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM output jitter is already included in the timing calculation.

Table 66: Global Clock Input to Output Delay With PLL in System-Synchronous Mode

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|--|------------|-------------|------|------|------|-------|
| | | | -3 | -3N | -2 | -1L | |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> PLL in System-Synchronous Mode. | | | | | | | |
| T _{ICKOFFPLL} | Global Clock and OUTFF <i>with</i> PLL | XC6SLX4 | 4.57 | N/A | 6.25 | 7.34 | ns |
| | | XC6SLX9 | 4.57 | 5.25 | 6.25 | 7.34 | ns |
| | | XC6SLX16 | 4.41 | 4.64 | 5.39 | 6.92 | ns |
| | | XC6SLX25 | 4.03 | 4.32 | 4.91 | 7.64 | ns |
| | | XC6SLX25T | 4.03 | 4.32 | 4.91 | N/A | ns |
| | | XC6SLX45 | 4.63 | 4.96 | 5.75 | 7.36 | ns |
| | | XC6SLX45T | 4.63 | 4.96 | 5.75 | N/A | ns |
| | | XC6SLX75 | 4.01 | 4.30 | 4.88 | 7.15 | ns |
| | | XC6SLX75T | 4.01 | 4.30 | 4.88 | N/A | ns |
| | | XC6SLX100 | 4.02 | 4.33 | 4.90 | 7.37 | ns |
| | | XC6SLX100T | 4.06 | 4.33 | 4.90 | N/A | ns |
| | | XC6SLX150 | 3.65 | 3.98 | 4.58 | 6.94 | ns |
| | | XC6SLX150T | 3.65 | 3.98 | 4.58 | N/A | ns |
| | | XA6SLX4 | 4.88 | N/A | 6.13 | N/A | ns |
| | | XA6SLX9 | 4.88 | N/A | 6.13 | N/A | ns |
| | | XA6SLX16 | 4.74 | N/A | 5.27 | N/A | ns |
| | | XA6SLX25 | 4.43 | N/A | 4.78 | N/A | ns |
| | | XA6SLX25T | 4.43 | N/A | 4.88 | N/A | ns |
| | | XA6SLX45 | 4.94 | N/A | 5.62 | N/A | ns |
| | | XA6SLX45T | 4.94 | N/A | 5.62 | N/A | ns |
| | | XA6SLX75 | 4.32 | N/A | 4.77 | N/A | ns |
| | | XA6SLX75T | 4.32 | N/A | 4.77 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 5.41 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 4.77 | 7.15 | ns |
| XQ6SLX75T | 4.32 | N/A | 4.77 | N/A | ns | | |
| XQ6SLX150 | N/A | N/A | 4.60 | 6.94 | ns | | |
| XQ6SLX150T | 4.35 | N/A | 4.60 | N/A | ns | | |

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

Table 67: Global Clock Input to Output Delay With PLL in Source-Synchronous Mode

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|--|------------|-------------|------|------|------|-------|
| | | | -3 | -3N | -2 | -1L | |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> PLL in Source-Synchronous Mode. | | | | | | | |
| T _{ICKOFFLL_0} | Global Clock and OUTFF <i>with</i> PLL | XC6SLX4 | 5.49 | N/A | 7.44 | 8.55 | ns |
| | | XC6SLX9 | 5.49 | 6.29 | 7.44 | 8.55 | ns |
| | | XC6SLX16 | 5.23 | 5.77 | 6.79 | 8.21 | ns |
| | | XC6SLX25 | 5.00 | 5.35 | 6.10 | 8.54 | ns |
| | | XC6SLX25T | 5.00 | 5.35 | 6.10 | N/A | ns |
| | | XC6SLX45 | 5.59 | 6.03 | 7.02 | 8.39 | ns |
| | | XC6SLX45T | 5.59 | 6.03 | 7.02 | N/A | ns |
| | | XC6SLX75 | 4.96 | 5.41 | 6.22 | 8.32 | ns |
| | | XC6SLX75T | 4.96 | 5.41 | 6.22 | N/A | ns |
| | | XC6SLX100 | 4.97 | 5.42 | 6.21 | 9.08 | ns |
| | | XC6SLX100T | 5.01 | 5.42 | 6.21 | N/A | ns |
| | | XC6SLX150 | 4.59 | 5.06 | 5.86 | 8.13 | ns |
| | | XC6SLX150T | 4.59 | 5.06 | 5.86 | N/A | ns |
| | | XA6SLX4 | 5.79 | N/A | 7.32 | N/A | ns |
| | | XA6SLX9 | 5.79 | N/A | 7.32 | N/A | ns |
| | | XA6SLX16 | 5.56 | N/A | 6.66 | N/A | ns |
| | | XA6SLX25 | 5.40 | N/A | 5.97 | N/A | ns |
| | | XA6SLX25T | 5.40 | N/A | 6.07 | N/A | ns |
| | | XA6SLX45 | 5.89 | N/A | 6.90 | N/A | ns |
| | | XA6SLX45T | 5.89 | N/A | 6.90 | N/A | ns |
| | | XA6SLX75 | 5.27 | N/A | 6.12 | N/A | ns |
| | | XA6SLX75T | 5.27 | N/A | 6.12 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 6.80 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 6.12 | 8.32 | ns |
| | | XQ6SLX75T | 5.27 | N/A | 6.12 | N/A | ns |
| | | XQ6SLX150 | N/A | N/A | 5.88 | 8.13 | ns |
| | | XQ6SLX150T | 5.21 | N/A | 5.88 | N/A | ns |

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is included in the timing calculation.

Table 68: Global Clock Input to Output Delay With DCM and PLL in System-Synchronous Mode

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|------------|-------------|------|------|------|-------|
| | | | -3 | -3N | -2 | -1L | |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in System-Synchronous Mode and PLL in DCM2PLL Mode. | | | | | | | |
| T _{ICKOFDCM_PLL} | Global Clock and OUTFF with DCM and PLL | XC6SLX4 | 4.78 | N/A | 6.32 | 7.09 | ns |
| | | XC6SLX9 | 4.78 | 5.24 | 6.32 | 7.09 | ns |
| | | XC6SLX16 | 4.70 | 5.12 | 5.94 | 6.63 | ns |
| | | XC6SLX25 | 4.70 | 5.09 | 5.92 | 7.30 | ns |
| | | XC6SLX25T | 4.70 | 5.09 | 5.92 | N/A | ns |
| | | XC6SLX45 | 4.63 | 4.98 | 5.83 | 7.26 | ns |
| | | XC6SLX45T | 4.63 | 4.98 | 5.83 | N/A | ns |
| | | XC6SLX75 | 4.68 | 5.04 | 5.88 | 6.90 | ns |
| | | XC6SLX75T | 4.68 | 5.04 | 5.88 | N/A | ns |
| | | XC6SLX100 | 4.72 | 5.07 | 5.92 | 7.77 | ns |
| | | XC6SLX100T | 4.76 | 5.07 | 5.92 | N/A | ns |
| | | XC6SLX150 | 4.44 | 4.73 | 5.31 | 6.96 | ns |
| | | XC6SLX150T | 4.44 | 4.73 | 5.31 | N/A | ns |
| | | XA6SLX4 | 5.07 | N/A | 6.18 | N/A | ns |
| | | XA6SLX9 | 5.07 | N/A | 6.18 | N/A | ns |
| | | XA6SLX16 | 5.22 | N/A | 5.77 | N/A | ns |
| | | XA6SLX25 | 5.01 | N/A | 5.80 | N/A | ns |
| | | XA6SLX25T | 5.01 | N/A | 5.90 | N/A | ns |
| | | XA6SLX45 | 4.93 | N/A | 5.67 | N/A | ns |
| | | XA6SLX45T | 4.93 | N/A | 5.67 | N/A | ns |
| | | XA6SLX75 | 4.94 | N/A | 5.70 | N/A | ns |
| | | XA6SLX75T | 4.94 | N/A | 5.70 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 5.77 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 5.70 | 6.90 | ns |
| XQ6SLX75T | 4.94 | N/A | 5.70 | N/A | ns | | |
| XQ6SLX150 | N/A | N/A | 5.31 | 6.96 | ns | | |
| XQ6SLX150T | 5.02 | N/A | 5.31 | N/A | ns | | |

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Table 69: Global Clock Input to Output Delay With DCM and PLL in Source-Synchronous Mode

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|------------|-------------|------|------|------|-------|
| | | | -3 | -3N | -2 | -1L | |
| LVCMOS25 Global Clock Input to Output Delay using Output Flip-Flop, 12mA, Fast Slew Rate, <i>with</i> DCM in Source-Synchronous Mode and PLL in DCM2PLL Mode. | | | | | | | |
| T _{ICKOFDCM0_PLL} | Global Clock and OUTFF with DCM and PLL | XC6SLX4 | 5.58 | N/A | 7.42 | 8.54 | ns |
| | | XC6SLX9 | 5.58 | 6.19 | 7.42 | 8.54 | ns |
| | | XC6SLX16 | 5.50 | 6.06 | 7.05 | 8.24 | ns |
| | | XC6SLX25 | 5.57 | 6.04 | 7.02 | 8.33 | ns |
| | | XC6SLX25T | 5.57 | 6.04 | 7.02 | N/A | ns |
| | | XC6SLX45 | 5.53 | 5.97 | 6.96 | 8.32 | ns |
| | | XC6SLX45T | 5.53 | 5.97 | 6.96 | N/A | ns |
| | | XC6SLX75 | 5.55 | 6.00 | 6.99 | 8.54 | ns |
| | | XC6SLX75T | 5.55 | 6.00 | 6.99 | N/A | ns |
| | | XC6SLX100 | 5.58 | 6.03 | 7.02 | 9.11 | ns |
| | | XC6SLX100T | 5.62 | 6.03 | 7.02 | N/A | ns |
| | | XC6SLX150 | 5.32 | 5.70 | 6.41 | 8.26 | ns |
| | | XC6SLX150T | 5.32 | 5.70 | 6.41 | N/A | ns |
| | | XA6SLX4 | 5.87 | N/A | 7.28 | N/A | ns |
| | | XA6SLX9 | 5.87 | N/A | 7.28 | N/A | ns |
| | | XA6SLX16 | 6.02 | N/A | 6.87 | N/A | ns |
| | | XA6SLX25 | 5.88 | N/A | 6.90 | N/A | ns |
| | | XA6SLX25T | 5.88 | N/A | 7.00 | N/A | ns |
| | | XA6SLX45 | 5.82 | N/A | 6.81 | N/A | ns |
| | | XA6SLX45T | 5.82 | N/A | 6.81 | N/A | ns |
| | | XA6SLX75 | 5.81 | N/A | 6.80 | N/A | ns |
| | | XA6SLX75T | 5.81 | N/A | 6.80 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 6.88 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 6.80 | 8.54 | ns |
| XQ6SLX75T | 5.81 | N/A | 6.80 | N/A | ns | | |
| XQ6SLX150 | N/A | N/A | 6.41 | 8.26 | ns | | |
| XQ6SLX150T | 5.90 | N/A | 6.41 | N/A | ns | | |

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. DCM and PLL output jitter are already included in the timing calculation.

Spartan-6 Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. The representative values for typical pin locations and normal clock loading are listed in Table 70 through Table 77. Values are expressed in nanoseconds unless otherwise noted.

Table 70: Global Clock Setup and Hold Without DCM or PLL (No Delay)

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|------------|-------------|------------|------------|------------|-------|
| | | | -3 | -3N | -2 | -1L | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.(1) | | | | | | | |
| T _{PSND} / T _{PHND} | No Delay Global Clock and IFF ⁽³⁾ without DCM or PLL | XC6SLX4 | 0.10/1.56 | N/A | 0.10/1.83 | 0.07/2.54 | ns |
| | | XC6SLX9 | 0.10/1.56 | 0.10/1.57 | 0.10/1.84 | 0.07/2.54 | ns |
| | | XC6SLX16 | 0.12/1.42 | 0.12/1.48 | 0.12/1.64 | 0.13/2.19 | ns |
| | | XC6SLX25 | 0.18/1.64 | 0.18/1.75 | 0.18/1.99 | 0.11/2.57 | ns |
| | | XC6SLX25T | 0.18/1.64 | 0.18/1.75 | 0.18/1.99 | N/A | ns |
| | | XC6SLX45 | -0.08/1.80 | -0.08/1.95 | -0.08/2.27 | -0.17/2.74 | ns |
| | | XC6SLX45T | -0.08/1.80 | -0.08/1.95 | -0.08/2.27 | N/A | ns |
| | | XC6SLX75 | 0.13/1.81 | 0.13/2.06 | 0.13/2.27 | -0.12/3.30 | ns |
| | | XC6SLX75T | 0.13/1.81 | 0.13/2.06 | 0.13/2.27 | N/A | ns |
| | | XC6SLX100 | -0.14/2.03 | -0.14/2.24 | -0.14/2.56 | -0.17/3.44 | ns |
| | | XC6SLX100T | -0.14/2.03 | -0.14/2.24 | -0.14/2.56 | N/A | ns |
| | | XC6SLX150 | -0.24/2.42 | -0.24/2.74 | -0.24/2.95 | -0.60/3.75 | ns |
| | | XC6SLX150T | -0.24/2.42 | -0.24/2.74 | -0.24/2.95 | N/A | ns |
| | | XA6SLX4 | 0.10/1.57 | N/A | 0.10/1.84 | N/A | ns |
| | | XA6SLX9 | 0.10/1.57 | N/A | 0.10/1.84 | N/A | ns |
| | | XA6SLX16 | 0.12/1.43 | N/A | 0.12/1.64 | N/A | ns |
| | | XA6SLX25 | 0.18/1.65 | N/A | 0.18/1.99 | N/A | ns |
| | | XA6SLX25T | 0.18/1.65 | N/A | 0.18/1.99 | N/A | ns |
| | | XA6SLX45 | -0.08/1.82 | N/A | -0.08/2.27 | N/A | ns |
| | | XA6SLX45T | -0.08/1.82 | N/A | -0.08/2.27 | N/A | ns |
| | | XA6SLX75 | 0.13/2.02 | N/A | 0.13/2.32 | N/A | ns |
| | | XA6SLX75T | 0.13/2.02 | N/A | 0.13/2.32 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 0.10/2.51 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 0.13/2.32 | -0.12/3.30 | ns |
| XQ6SLX75T | 0.13/2.02 | N/A | 0.13/2.32 | N/A | ns | | |
| XQ6SLX150 | N/A | N/A | -0.24/2.95 | -0.60/3.75 | ns | | |
| XQ6SLX150T | -0.24/2.74 | N/A | -0.24/2.95 | N/A | ns | | |

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input Flip-Flop or Latch.

Table 71: Global Clock Setup and Hold Without DCM or PLL (Default Delay)

| Symbol | Description | Device | Speed Grade | | | | Units |
|--|---|------------|-------------|-----------|-----------|-----------|-------|
| | | | -3 | -3N | -2 | -1L | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.⁽¹⁾ | | | | | | | |
| T _{PSFD} / T _{PHFD} | Default Delay ⁽²⁾ Global Clock and IFF ⁽³⁾ without DCM or PLL | XC6SLX4 | 0.66/1.17 | N/A | 1.05/0.79 | 2.09/1.05 | ns |
| | | XC6SLX9 | 0.66/1.17 | 0.75/1.17 | 1.05/1.17 | 2.09/1.05 | ns |
| | | XC6SLX16 | 0.87/1.16 | 0.93/1.16 | 0.96/1.16 | 1.86/1.06 | ns |
| | | XC6SLX25 | 0.68/0.77 | 0.81/0.81 | 0.87/0.82 | 2.21/1.33 | ns |
| | | XC6SLX25T | 0.68/0.77 | 0.81/0.81 | 0.87/0.82 | N/A | ns |
| | | XC6SLX45 | 0.40/1.05 | 0.42/1.17 | 0.64/1.20 | 1.61/1.67 | ns |
| | | XC6SLX45T | 0.40/1.05 | 0.42/1.17 | 0.64/1.20 | N/A | ns |
| | | XC6SLX75 | 0.41/1.11 | 0.41/1.13 | 0.80/1.14 | 1.23/1.82 | ns |
| | | XC6SLX75T | 0.41/1.11 | 0.41/1.13 | 0.80/1.14 | N/A | ns |
| | | XC6SLX100 | 0.39/1.12 | 0.39/1.23 | 0.39/1.28 | 1.13/1.94 | ns |
| | | XC6SLX100T | 0.39/1.12 | 0.39/1.23 | 0.39/1.28 | N/A | ns |
| | | XC6SLX150 | 0.23/1.54 | 0.23/1.62 | 0.23/1.62 | 1.14/2.05 | ns |
| | | XC6SLX150T | 0.23/1.54 | 0.23/1.62 | 0.23/1.62 | N/A | ns |
| | | XA6SLX4 | 0.73/1.18 | N/A | 1.05/0.80 | N/A | ns |
| | | XA6SLX9 | 0.73/1.18 | N/A | 1.05/0.80 | N/A | ns |
| | | XA6SLX16 | 0.90/1.20 | N/A | 0.96/0.75 | N/A | ns |
| | | XA6SLX25 | 0.70/0.81 | N/A | 0.87/0.91 | N/A | ns |
| | | XA6SLX25T | 0.76/0.81 | N/A | 1.03/0.91 | N/A | ns |
| | | XA6SLX45 | 0.40/1.06 | N/A | 0.64/1.20 | N/A | ns |
| | | XA6SLX45T | 0.40/1.06 | N/A | 0.64/1.20 | N/A | ns |
| | | XA6SLX75 | 0.41/1.24 | N/A | 0.80/1.18 | N/A | ns |
| | | XA6SLX75T | 0.41/1.24 | N/A | 0.80/1.18 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 0.86/1.55 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 0.80/1.18 | 1.23/1.82 | ns |
| XQ6SLX75T | 0.41/1.24 | N/A | 0.80/1.18 | N/A | ns | | |
| XQ6SLX150 | N/A | N/A | 0.28/1.57 | 1.14/2.05 | ns | | |
| XQ6SLX150T | 0.28/1.78 | N/A | 0.28/1.57 | N/A | ns | | |

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage.
- Default delay uses IODELAY2 tap 0.
- IFF = Input Flip-Flop or Latch.

Table 72: Global Clock Setup and Hold With DCM in System-Synchronous Mode

| Symbol | Description | Device | Speed Grade | | | | Units |
|--|--|------------|-------------|------------|------------|-----------|-------|
| | | | -3 | -3N | -2 | -1L | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.⁽¹⁾ | | | | | | | |
| T _{PSDCM} / T _{PHDCM} | No Delay Global Clock and IFF ⁽²⁾ with DCM in System-Synchronous Mode | XC6SLX4 | 1.54/0.06 | N/A | 1.75/0.12 | 2.84/0.27 | ns |
| | | XC6SLX9 | 1.54/0.06 | 1.63/0.12 | 1.75/0.12 | 2.84/0.27 | ns |
| | | XC6SLX16 | 1.72/-0.18 | 1.87/-0.17 | 2.13/-0.17 | 2.31/0.26 | ns |
| | | XC6SLX25 | 1.70/-0.03 | 1.78/-0.02 | 2.00/-0.02 | 2.88/0.20 | ns |
| | | XC6SLX25T | 1.70/0.07 | 1.78/0.08 | 2.00/0.08 | N/A | ns |
| | | XC6SLX45 | 1.74/-0.03 | 1.84/-0.02 | 2.02/-0.02 | 2.64/0.52 | ns |
| | | XC6SLX45T | 1.74/-0.01 | 1.84/0.00 | 2.02/0.00 | N/A | ns |
| | | XC6SLX75 | 1.86/0.11 | 1.98/0.12 | 2.20/0.12 | 2.96/0.58 | ns |
| | | XC6SLX75T | 1.86/0.11 | 1.98/0.12 | 2.20/0.12 | N/A | ns |
| | | XC6SLX100 | 1.64/0.07 | 1.72/0.08 | 1.97/0.08 | 2.70/0.99 | ns |
| | | XC6SLX100T | 1.64/0.09 | 1.72/0.10 | 1.97/0.10 | N/A | ns |
| | | XC6SLX150 | 1.53/0.39 | 1.62/0.40 | 1.82/0.40 | 2.75/1.00 | ns |
| | | XC6SLX150T | 1.53/0.39 | 1.62/0.40 | 1.82/0.40 | N/A | ns |
| | | XA6SLX4 | 1.65/0.16 | N/A | 1.75/0.26 | N/A | ns |
| | | XA6SLX9 | 1.65/0.16 | N/A | 1.75/0.26 | N/A | ns |
| | | XA6SLX16 | 1.88/0.02 | N/A | 2.13/0.03 | N/A | ns |
| | | XA6SLX25 | 1.80/0.16 | N/A | 2.05/0.17 | N/A | ns |
| | | XA6SLX25T | 1.80/0.16 | N/A | 2.13/0.17 | N/A | ns |
| | | XA6SLX45 | 1.75/0.12 | N/A | 2.02/0.13 | N/A | ns |
| | | XA6SLX45T | 1.75/0.12 | N/A | 2.02/0.13 | N/A | ns |
| | | XA6SLX75 | 1.87/0.11 | N/A | 2.20/0.12 | N/A | ns |
| | | XA6SLX75T | 1.87/0.11 | N/A | 2.20/0.12 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 2.46/0.24 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 2.20/0.12 | 2.96/0.58 | ns |
| | | XQ6SLX75T | 1.87/0.11 | N/A | 2.20/0.12 | N/A | ns |
| | | XQ6SLX150 | N/A | N/A | 1.82/0.56 | 2.75/1.00 | ns |
| XQ6SLX150T | 1.65/0.55 | N/A | 1.82/0.56 | N/A | ns | | |

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 73: Global Clock Setup and Hold With DCM in Source-Synchronous Mode

| Symbol | Description | Device | Speed Grade | | | | Units |
|--|--|------------|-------------|-----------|-----------|-----------|-------|
| | | | -3 | -3N | -2 | -1L | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.⁽¹⁾ | | | | | | | |
| T_{PSDCMO}/T_{PHDCMO} | No Delay Global Clock and IFF ⁽²⁾ with DCM in Source-Synchronous Mode | XC6SLX4 | 0.71/0.65 | N/A | 0.72/1.22 | 1.58/1.18 | ns |
| | | XC6SLX9 | 0.71/0.69 | 0.71/1.19 | 0.72/1.36 | 1.58/1.18 | ns |
| | | XC6SLX16 | 0.86/0.52 | 0.92/0.57 | 1.04/0.60 | 1.02/1.06 | ns |
| | | XC6SLX25 | 0.84/0.58 | 0.90/0.59 | 1.01/0.59 | 1.58/1.07 | ns |
| | | XC6SLX25T | 0.84/0.58 | 0.90/0.59 | 1.01/0.59 | N/A | ns |
| | | XC6SLX45 | 0.85/0.70 | 0.90/0.76 | 0.98/0.79 | 1.34/1.34 | ns |
| | | XC6SLX45T | 0.85/0.70 | 0.90/0.76 | 0.98/0.79 | N/A | ns |
| | | XC6SLX75 | 1.00/0.62 | 1.06/0.63 | 1.15/0.63 | 1.65/1.46 | ns |
| | | XC6SLX75T | 1.00/0.71 | 1.06/0.72 | 1.15/0.72 | N/A | ns |
| | | XC6SLX100 | 0.81/0.68 | 0.81/0.69 | 0.94/0.69 | 1.42/2.07 | ns |
| | | XC6SLX100T | 0.81/0.68 | 0.81/0.69 | 0.94/0.69 | N/A | ns |
| | | XC6SLX150 | 0.68/0.98 | 0.69/0.99 | 0.79/0.99 | 1.45/1.60 | ns |
| | | XC6SLX150T | 0.68/0.98 | 0.69/0.99 | 0.79/0.99 | N/A | ns |
| | | XA6SLX4 | 0.81/0.74 | N/A | 0.72/1.36 | N/A | ns |
| | | XA6SLX9 | 0.81/0.74 | N/A | 0.72/1.36 | N/A | ns |
| | | XA6SLX16 | 1.01/0.56 | N/A | 1.04/0.60 | N/A | ns |
| | | XA6SLX25 | 0.94/0.76 | N/A | 1.06/0.77 | N/A | ns |
| | | XA6SLX25T | 0.94/0.76 | N/A | 1.14/0.77 | N/A | ns |
| | | XA6SLX45 | 0.86/0.74 | N/A | 0.98/0.78 | N/A | ns |
| | | XA6SLX45T | 0.86/0.74 | N/A | 0.98/0.78 | N/A | ns |
| | | XA6SLX75 | 1.02/0.71 | N/A | 1.15/0.72 | N/A | ns |
| | | XA6SLX75T | 1.02/0.71 | N/A | 1.15/0.72 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 1.37/0.75 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 1.15/0.72 | 1.65/1.46 | ns |
| | | XQ6SLX75T | 1.02/0.71 | N/A | 1.15/0.72 | N/A | ns |
| | | XQ6SLX150 | N/A | N/A | 0.79/1.15 | 1.45/1.60 | ns |
| XQ6SLX150T | 0.73/1.15 | N/A | 0.79/1.15 | N/A | ns | | |

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include DCM CLK0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 74: Global Clock Setup and Hold With PLL in System-Synchronous Mode

| Symbol | Description | Device | Speed Grade | | | | Units |
|--|--|------------|-------------|------------|------------|-----------|-------|
| | | | -3 | -3N | -2 | -1L | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.⁽¹⁾ | | | | | | | |
| T _{PSPLL} / T _{PHPLL} | No Delay Global Clock and IFF ⁽²⁾ with PLL in System-Synchronous Mode | XC6SLX4 | 1.37/0.25 | N/A | 1.52/0.41 | 2.07/0.69 | ns |
| | | XC6SLX9 | 1.37/0.21 | 1.48/0.21 | 1.52/0.26 | 2.07/0.69 | ns |
| | | XC6SLX16 | 1.33/-0.03 | 1.53/-0.02 | 1.60/-0.02 | 1.57/0.48 | ns |
| | | XC6SLX25 | 1.65/0.28 | 1.71/0.28 | 1.91/0.28 | 2.44/0.76 | ns |
| | | XC6SLX25T | 1.65/0.28 | 1.71/0.28 | 1.91/0.28 | N/A | ns |
| | | XC6SLX45 | 1.55/0.18 | 1.64/0.18 | 1.75/0.18 | 2.02/0.90 | ns |
| | | XC6SLX45T | 1.55/0.18 | 1.64/0.18 | 1.75/0.18 | N/A | ns |
| | | XC6SLX75 | 1.77/0.21 | 1.89/0.21 | 2.13/0.21 | 2.46/0.53 | ns |
| | | XC6SLX75T | 1.77/0.21 | 1.89/0.21 | 2.13/0.21 | N/A | ns |
| | | XC6SLX100 | 1.44/0.32 | 1.52/0.32 | 1.70/0.32 | 1.78/0.86 | ns |
| | | XC6SLX100T | 1.44/0.32 | 1.52/0.32 | 1.70/0.32 | N/A | ns |
| | | XC6SLX150 | 1.39/0.49 | 1.48/0.49 | 1.67/0.49 | 1.94/0.94 | ns |
| | | XC6SLX150T | 1.39/0.49 | 1.48/0.49 | 1.67/0.49 | N/A | ns |
| | | XA6SLX4 | 1.61/0.10 | N/A | 1.64/0.28 | N/A | ns |
| | | XA6SLX9 | 1.61/0.10 | N/A | 1.64/0.28 | N/A | ns |
| | | XA6SLX16 | 1.89/-0.08 | N/A | 1.72/-0.08 | N/A | ns |
| | | XA6SLX25 | 1.85/0.16 | N/A | 2.08/0.16 | N/A | ns |
| | | XA6SLX25T | 1.85/0.16 | N/A | 2.17/0.16 | N/A | ns |
| | | XA6SLX45 | 1.58/0.07 | N/A | 1.87/0.03 | N/A | ns |
| | | XA6SLX45T | 1.58/0.07 | N/A | 1.87/0.03 | N/A | ns |
| | | XA6SLX75 | 1.80/0.06 | N/A | 2.25/0.06 | N/A | ns |
| | | XA6SLX75T | 1.80/0.06 | N/A | 2.25/0.06 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 2.34/0.14 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 2.25/0.06 | 2.46/0.53 | ns |
| XQ6SLX75T | 1.80/0.06 | N/A | 2.25/0.06 | N/A | ns | | |
| XQ6SLX150 | N/A | N/A | 1.79/0.37 | 1.94/0.94 | ns | | |
| XQ6SLX150T | 1.43/0.37 | N/A | 1.79/0.37 | N/A | ns | | |

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 75: Global Clock Setup and Hold With PLL in Source-Synchronous Mode

| Symbol | Description | Device | Speed Grade | | | | Units |
|--|--|------------|-------------|-----------|-----------|-----------|-------|
| | | | -3 | -3N | -2 | -1L | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.⁽¹⁾ | | | | | | | |
| T_{PSPLL0} / T_{PHPLL0} | No Delay Global Clock and IFF ⁽²⁾ with PLL in Source-Synchronous Mode | XC6SLX4 | 0.47/1.08 | N/A | 0.47/1.60 | 1.15/1.68 | ns |
| | | XC6SLX9 | 0.47/1.08 | 0.47/1.35 | 0.47/1.60 | 1.15/1.68 | ns |
| | | XC6SLX16 | 0.37/0.75 | 0.37/0.82 | 0.51/0.94 | 0.57/1.31 | ns |
| | | XC6SLX25 | 0.69/1.06 | 0.69/1.06 | 0.69/1.06 | 1.86/1.67 | ns |
| | | XC6SLX25T | 0.69/1.06 | 0.69/1.06 | 0.69/1.06 | N/A | ns |
| | | XC6SLX45 | 0.57/1.05 | 0.65/1.10 | 0.65/1.18 | 1.02/1.65 | ns |
| | | XC6SLX45T | 0.57/1.06 | 0.65/1.10 | 0.65/1.18 | N/A | ns |
| | | XC6SLX75 | 0.86/1.04 | 0.87/1.04 | 0.90/1.04 | 1.34/1.55 | ns |
| | | XC6SLX75T | 0.86/1.04 | 0.87/1.04 | 0.90/1.04 | N/A | ns |
| | | XC6SLX100 | 0.53/1.13 | 0.54/1.13 | 0.55/1.13 | 0.89/2.39 | ns |
| | | XC6SLX100T | 0.53/1.13 | 0.54/1.13 | 0.55/1.13 | N/A | ns |
| | | XC6SLX150 | 0.50/1.31 | 0.51/1.31 | 0.52/1.31 | 1.02/1.72 | ns |
| | | XC6SLX150T | 0.50/1.31 | 0.51/1.31 | 0.52/1.31 | N/A | ns |
| | | XA6SLX4 | 0.71/0.93 | N/A | 0.62/1.47 | N/A | ns |
| | | XA6SLX9 | 0.71/0.93 | N/A | 0.62/1.47 | N/A | ns |
| | | XA6SLX16 | 0.92/0.69 | N/A | 0.63/0.82 | N/A | ns |
| | | XA6SLX25 | 0.99/0.94 | N/A | 0.96/0.94 | N/A | ns |
| | | XA6SLX25T | 0.99/0.94 | N/A | 1.04/0.94 | N/A | ns |
| | | XA6SLX45 | 0.63/1.02 | N/A | 0.72/1.05 | N/A | ns |
| | | XA6SLX45T | 0.63/1.02 | N/A | 0.72/1.05 | N/A | ns |
| | | XA6SLX75 | 0.88/0.89 | N/A | 1.02/0.89 | N/A | ns |
| | | XA6SLX75T | 0.88/0.89 | N/A | 1.02/0.89 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 1.25/0.96 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 1.02/0.89 | 1.34/1.55 | ns |
| XQ6SLX75T | 0.88/0.89 | N/A | 1.02/0.89 | N/A | ns | | |
| XQ6SLX150 | N/A | N/A | 0.63/1.19 | 1.02/1.72 | ns | | |
| XQ6SLX150T | 0.60/1.19 | N/A | 0.63/1.19 | N/A | ns | | |

Notes:

1. Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include PLL CLKOUT0 jitter.
2. IFF = Input Flip-Flop or Latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 76: Global Clock Setup and Hold With DCM and PLL in System-Synchronous Mode

| Symbol | Description | Device | Speed Grade | | | | Units |
|--|---|------------|-------------|------------|------------|-----------|-------|
| | | | -3 | -3N | -2 | -1L | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVC MOS25 Standard.⁽¹⁾ | | | | | | | |
| T _{PSDCMPLL} / T _{PHDCMPLL} | No Delay Global Clock and IFF ⁽²⁾ with DCM in System-Synchronous Mode and PLL in DCM2PLL Mode. | XC6SLX4 | 1.16/0.49 | N/A | 1.39/0.49 | 2.36/0.59 | ns |
| | | XC6SLX9 | 1.16/0.44 | 1.37/0.44 | 1.39/0.44 | 2.36/0.59 | ns |
| | | XC6SLX16 | 1.44/-0.08 | 1.49/-0.04 | 1.62/-0.04 | 2.06/0.55 | ns |
| | | XC6SLX25 | 1.52/0.42 | 1.65/0.42 | 1.83/0.42 | 2.52/0.43 | ns |
| | | XC6SLX25T | 1.52/0.42 | 1.65/0.42 | 1.83/0.42 | N/A | ns |
| | | XC6SLX45 | 1.54/0.39 | 1.59/0.39 | 1.75/0.39 | 2.48/0.76 | ns |
| | | XC6SLX45T | 1.54/0.39 | 1.59/0.39 | 1.75/0.39 | N/A | ns |
| | | XC6SLX75 | 1.72/0.41 | 1.80/0.41 | 1.99/0.41 | 2.60/0.75 | ns |
| | | XC6SLX75T | 1.72/0.41 | 1.80/0.41 | 1.99/0.41 | N/A | ns |
| | | XC6SLX100 | 1.34/0.51 | 1.46/0.51 | 1.64/0.51 | 2.12/0.90 | ns |
| | | XC6SLX100T | 1.34/0.51 | 1.46/0.51 | 1.64/0.51 | N/A | ns |
| | | XC6SLX150 | 1.30/0.60 | 1.40/0.60 | 1.55/0.60 | 2.57/0.97 | ns |
| | | XC6SLX150T | 1.30/0.60 | 1.40/0.60 | 1.55/0.60 | N/A | ns |
| | | XA6SLX4 | 1.58/0.37 | N/A | 1.58/0.37 | N/A | ns |
| | | XA6SLX9 | 1.58/0.37 | N/A | 1.58/0.37 | N/A | ns |
| | | XA6SLX16 | 2.67/0.35 | N/A | 2.67/0.17 | N/A | ns |
| | | XA6SLX25 | 1.74/0.27 | N/A | 1.95/0.27 | N/A | ns |
| | | XA6SLX25T | 1.74/0.27 | N/A | 2.03/0.27 | N/A | ns |
| | | XA6SLX45 | 1.58/0.29 | N/A | 1.87/0.29 | N/A | ns |
| | | XA6SLX45T | 1.58/0.29 | N/A | 1.87/0.29 | N/A | ns |
| | | XA6SLX75 | 1.74/0.24 | N/A | 2.11/0.24 | N/A | ns |
| | | XA6SLX75T | 1.74/0.24 | N/A | 2.11/0.24 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 2.64/0.82 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 2.11/0.24 | 2.60/0.75 | ns |
| | | XQ6SLX75T | 1.74/0.24 | N/A | 2.11/0.24 | N/A | ns |
| | | XQ6SLX150 | N/A | N/A | 1.67/0.70 | 2.57/0.97 | ns |
| XQ6SLX150T | 1.50/0.70 | N/A | 1.67/0.70 | N/A | ns | | |

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG.
- IFF = Input Flip-Flop or Latch
- Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 77: Global Clock Setup and Hold With DCM and PLL in Source-Synchronous Mode

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|------------|-------------|-----------|-----------|-----------|-------|
| | | | -3 | -3N | -2 | -1L | |
| Example Data Input Set-Up and Hold Times Relative to a Forwarded Clock Input Pin, ⁽¹⁾ Using DCM, PLL, and Global Clock Buffer for the LVCMOS25 standard. | | | | | | | |
| T _{PSDCMPLL_0} / T _{PHDCMPLL_0} | No Delay Global Clock and IFF ⁽²⁾ with DCM in Source-Synchronous Mode and PLL in DCM2PLL Mode. | XC6SLX4 | 0.43/1.07 | N/A | 0.43/1.43 | 1.10/1.67 | ns |
| | | XC6SLX9 | 0.43/1.03 | 0.45/1.14 | 0.45/1.43 | 1.10/1.67 | ns |
| | | XC6SLX16 | 0.74/0.93 | 0.74/1.12 | 0.74/1.21 | 0.77/1.35 | ns |
| | | XC6SLX25 | 0.67/1.02 | 0.76/1.11 | 0.84/1.18 | 1.23/1.46 | ns |
| | | XC6SLX25T | 0.67/1.02 | 0.76/1.11 | 0.84/1.18 | N/A | ns |
| | | XC6SLX45 | 0.65/0.99 | 0.65/1.04 | 0.71/1.12 | 1.18/1.58 | ns |
| | | XC6SLX45T | 0.65/1.00 | 0.65/1.04 | 0.71/1.12 | N/A | ns |
| | | XC6SLX75 | 0.86/1.01 | 0.88/1.06 | 0.94/1.14 | 1.29/1.67 | ns |
| | | XC6SLX75T | 0.86/1.01 | 0.88/1.06 | 0.94/1.14 | N/A | ns |
| | | XC6SLX100 | 0.50/1.10 | 0.56/1.10 | 0.61/1.17 | 0.84/2.24 | ns |
| | | XC6SLX100T | 0.50/1.10 | 0.56/1.10 | 0.61/1.17 | N/A | ns |
| | | XC6SLX150 | 0.45/1.28 | 0.47/1.28 | 0.52/1.28 | 1.27/1.56 | ns |
| | | XC6SLX150T | 0.45/1.28 | 0.47/1.28 | 0.52/1.28 | N/A | ns |
| | | XA6SLX4 | 0.74/1.00 | N/A | 0.74/1.43 | N/A | ns |
| | | XA6SLX9 | 0.74/1.00 | N/A | 0.74/1.43 | N/A | ns |
| | | XA6SLX16 | 1.81/1.15 | N/A | 1.81/1.03 | N/A | ns |
| | | XA6SLX25 | 0.89/1.01 | N/A | 0.96/1.05 | N/A | ns |
| | | XA6SLX25T | 0.89/1.01 | N/A | 1.04/1.15 | N/A | ns |
| | | XA6SLX45 | 0.69/0.95 | N/A | 0.83/0.96 | N/A | ns |
| | | XA6SLX45T | 0.69/0.95 | N/A | 0.83/0.96 | N/A | ns |
| | | XA6SLX75 | 0.88/0.94 | N/A | 1.06/0.96 | N/A | ns |
| | | XA6SLX75T | 0.88/0.94 | N/A | 1.06/0.96 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 1.55/1.33 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 1.06/0.96 | 1.29/1.67 | ns |
| XQ6SLX75T | 0.88/0.94 | N/A | 1.06/0.96 | N/A | ns | | |
| XQ6SLX150 | N/A | N/A | 0.64/1.30 | 1.27/1.56 | ns | | |
| XQ6SLX150T | 0.58/1.30 | N/A | 0.64/1.30 | N/A | ns | | |

Notes:

- Setup and Hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the Global Clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the Global Clock input signal using the fastest process, lowest temperature, and highest voltage. The timing values were measured using the fine-phase adjustment feature of the DCM. These measurements include CMT jitter; DCM CLK0 driving PLL, PLL CLKOUT0 driving BUFG. Package skew is not included in these measurements.
- IFF = Input Flip-Flop

Source-Synchronous Switching Characteristics

The parameters in this section provide the necessary values for calculating timing budgets for Spartan-6 FPGA source-synchronous transmitter and receiver data-valid windows.

Table 78: Duty Cycle Distortion and Clock-Tree Skew

| Symbol | Description | Device ⁽¹⁾ | Speed Grade | | | | Units |
|--------------------------|--|-----------------------|---------------------------------------|------|------|------|-------|
| | | | -3 | -3N | -2 | -1L | |
| T _{DCD_CLK} | Global Clock Tree Duty Cycle Distortion ⁽²⁾ | LX4 | 0.20 | N/A | 0.20 | 0.35 | ns |
| | | LX9 | 0.20 | 0.20 | 0.20 | 0.35 | ns |
| | | LX16 | 0.20 | 0.20 | 0.20 | 0.35 | ns |
| | | LX25 | 0.20 | 0.20 | 0.20 | 0.35 | ns |
| | | LX25T | 0.20 | 0.20 | 0.20 | N/A | ns |
| | | LX45 | 0.20 | 0.20 | 0.20 | 0.35 | ns |
| | | LX45T | 0.20 | 0.20 | 0.20 | N/A | ns |
| | | LX75 | 0.20 | 0.20 | 0.20 | 0.35 | ns |
| | | LX75T | 0.20 | 0.20 | 0.20 | N/A | ns |
| | | LX100 | 0.20 | 0.20 | 0.20 | 0.35 | ns |
| | | LX100T | 0.20 | 0.20 | 0.20 | N/A | ns |
| | | LX150 | 0.35 | 0.35 | 0.35 | 0.35 | ns |
| | | LX150T | 0.35 | 0.35 | 0.35 | N/A | ns |
| | | T _{CKSKEW} | Global Clock Tree Skew ⁽³⁾ | LX4 | 0.25 | N/A | 0.25 |
| LX9 | 0.25 | | | 0.25 | 0.25 | 0.29 | ns |
| LX16 | 0.15 | | | 0.15 | 0.15 | 0.22 | ns |
| LX25 | 0.26 | | | 0.26 | 0.26 | 0.41 | ns |
| LX25T | 0.26 | | | 0.26 | 0.26 | N/A | ns |
| LX45 | 0.20 | | | 0.20 | 0.20 | 0.28 | ns |
| LX45T | 0.20 | | | 0.20 | 0.20 | N/A | ns |
| LX75 | 0.56 | | | 0.56 | 0.56 | 0.50 | ns |
| LX75T | 0.56 | | | 0.56 | 0.56 | N/A | ns |
| XC6SLX100 ⁽⁴⁾ | 0.22 | | | 0.22 | 0.22 | 0.21 | ns |
| XA6SLX100 ⁽⁴⁾ | N/A | | | N/A | 0.43 | N/A | ns |
| LX100T | 0.22 | | | 0.22 | 0.22 | N/A | ns |
| LX150 | 0.48 | | | 0.48 | 0.48 | 0.35 | ns |
| LX150T | 0.48 | | | 0.48 | 0.48 | N/A | ns |
| T _{DCD_BUFIO2} | I/O clock tree duty cycle distortion | LX devices | 0.25 | 0.25 | 0.25 | 0.50 | ns |
| | | LXT devices | 0.25 | 0.25 | 0.25 | N/A | ns |

Table 78: Duty Cycle Distortion and Clock-Tree Skew (Cont'd)

| Symbol | Description | Device ⁽¹⁾ | Speed Grade | | | | Units |
|------------------------|---|-----------------------|-------------|------|------|------|-------|
| | | | -3 | -3N | -2 | -1L | |
| T _{BUFIOSKEW} | I/O clock tree skew across one clock region | LX4 | 0.06 | N/A | 0.06 | 0.07 | ns |
| | | LX9 | 0.06 | 0.06 | 0.06 | 0.07 | ns |
| | | LX16 | 0.06 | 0.06 | 0.06 | 0.07 | ns |
| | | LX25 | 0.06 | 0.06 | 0.06 | 0.07 | ns |
| | | LX25T | 0.06 | 0.06 | 0.06 | N/A | ns |
| | | LX45 | 0.06 | 0.06 | 0.06 | 0.07 | ns |
| | | LX45T | 0.06 | 0.06 | 0.06 | N/A | ns |
| | | LX75 | 0.06 | 0.06 | 0.06 | 0.07 | ns |
| | | LX75T | 0.06 | 0.06 | 0.06 | N/A | ns |
| | | LX100 | 0.06 | 0.06 | 0.06 | 0.07 | ns |
| | | LX100T | 0.06 | 0.06 | 0.06 | N/A | ns |
| | | LX150 | 0.06 | 0.06 | 0.06 | 0.07 | ns |
| | | LX150T | 0.06 | 0.06 | 0.06 | N/A | ns |

Notes:

- LXT devices are not available with a -1L speed grade. The LX4 is not available in -3N speed grade.
- These parameters represent the worst-case duty cycle distortion observable at the pins of the device using LVDS output buffers. For cases where other I/O standards are used, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
- The T_{CKSKEW} value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx FPGA Editor and Timing Analyzer tools to evaluate clock skew specific to your application.
- The T_{CKSKEW} is 0.43 ns for the XA6SLX100 device using a -2 speed grade and 0.22 ns for the XC6SLX100 devices using the -2 speed grade.

Table 79: Package Skew

| Symbol | Description | Device | Package ⁽²⁾ | Value | Units |
|----------------------|-----------------------------|--------|------------------------|-------|-------|
| T _{PKGSKEW} | Package Skew ⁽¹⁾ | LX4 | TQG144 | N/A | ps |
| | | | CPG196 | 23 | ps |
| | | | CSG225 | 58 | ps |
| | | LX9 | TQG144 | N/A | ps |
| | | | CPG196 | 23 | ps |
| | | | CSG225 | 58 | ps |
| | | | FT(G)256 | 88 | ps |
| | | | CSG324 | 64 | ps |
| | | LX16 | CPG196 | 19 | ps |
| | | | CSG225 | 70 | ps |
| | | | FT(G)256 | 71 | ps |
| | | | CSG324 | 54 | ps |
| | | LX25 | FT(G)256 | 90 | ps |
| | | | CSG324 | 61 | ps |
| FG(G)484 | 84 | | ps | | |
| LX25T | CSG324 | 48 | ps | | |
| | FG(G)484 | 112 | ps | | |

Table 79: Package Skew (Cont'd)

| Symbol | Description | Device | Package ⁽²⁾ | Value | Units |
|----------------------|-----------------------------|--------|------------------------|-------|-------|
| T _{PKGSKEW} | Package Skew ⁽¹⁾ | LX45 | CSG324 | 70 | ps |
| | | | CS(G)484 | 99 | ps |
| | | | FG(G)484 | 109 | ps |
| | | | FG(G)676 | 138 | ps |
| | | LX45T | CSG324 | 75 | ps |
| | | | CS(G)484 | 100 | ps |
| | | | FG(G)484 | 95 | ps |
| | | LX75 | CS(G)484 | 101 | ps |
| | | | FG(G)484 | 107 | ps |
| | | | FG(G)676 | 161 | ps |
| | | LX75T | CS(G)484 | 107 | ps |
| | | | FG(G)484 | 110 | ps |
| | | | FG(G)676 | 134 | ps |
| | | LX100 | CS(G)484 | 95 | ps |
| | | | FG(G)484 | 155 | ps |
| | | | FG(G)676 | 144 | ps |
| | | LX100T | CS(G)484 | 88 | ps |
| | | | FG(G)484 | 111 | ps |
| | | | FG(G)676 | 147 | ps |
| | | | FG(G)900 | 134 | ps |
| | | LX150 | CS(G)484 | 84 | ps |
| | | | FG(G)484 | 103 | ps |
| | | | FG(G)676 | 115 | ps |
| | | | FG(G)900 | 121 | ps |
| LX150T | CS(G)484 | 83 | ps | | |
| | FG(G)484 | 88 | ps | | |
| | FG(G)676 | 141 | ps | | |
| | FG(G)900 | 120 | ps | | |

Notes:

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from Pad to Ball.
2. Some of the devices are available in both Pb and Pb-free (additional G) packages as standard ordering options. See [DS160: Spartan-6 Family Overview](#) for more information.

Table 80: Sample Window

| Symbol | Description | Device ⁽¹⁾ | Speed Grade | | | | Units |
|--------------------------|---|-----------------------|-------------|-----|-----|-----|-------|
| | | | -3 | -3N | -2 | -1L | |
| T _{SAMP} | Sampling Error at Receiver Pins ⁽²⁾ | All | 510 | 510 | 530 | 740 | ps |
| T _{SAMP_BUFIO2} | Sampling Error at Receiver Pins using BUFIO2 ⁽³⁾ | All | 430 | 430 | 450 | 590 | ps |

Notes:

1. LXT devices are not available with a -1L speed grade.
2. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the DCM to capture the DDR input registers' edges of operation. These measurements include:
 - CLK0 DCM jitter
 - DCM accuracy (phase offset)
 - DCM phase shift resolution
 These measurements do not include package or clock tree skew.
3. This parameter indicates the total sampling error of Spartan-6 FPGA DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO2 clock network and IODELAY2 to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

Table 81: Source-Synchronous Pin-to-Pin Setup/Hold and Clock-to-Out Using BUFIO2

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|-----------------------------------|------------|-------------|-----------|-----------|------------|-------|
| | | | -3 | -3N | -2 | -1L | |
| Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO2 | | | | | | | |
| T_{PSCS}/T_{PHCS} | IFF setup/hold using BUFIO2 clock | XC6SLX4 | 0.57/0.94 | N/A | 0.95/1.12 | 0.27/1.56 | ns |
| | | XC6SLX9 | 0.40/0.95 | 0.50/0.96 | 0.60/1.12 | 0.27/1.56 | ns |
| | | XC6SLX16 | 0.48/0.74 | 0.55/0.75 | 0.69/0.83 | 1.27/1.31 | ns |
| | | XC6SLX25 | 0.28/1.02 | 0.28/1.12 | 0.28/1.24 | 0.15/1.78 | ns |
| | | XC6SLX25T | 0.28/1.02 | 0.28/1.12 | 0.28/1.24 | N/A | ns |
| | | XC6SLX45 | 0.42/1.19 | 0.44/1.29 | 0.50/1.40 | 0.12/1.83 | ns |
| | | XC6SLX45T | 0.42/1.19 | 0.44/1.29 | 0.50/1.40 | N/A | ns |
| | | XC6SLX75 | 0.38/1.48 | 0.38/1.63 | 0.38/1.84 | 0.05/2.78 | ns |
| | | XC6SLX75T | 0.38/1.48 | 0.38/1.63 | 0.38/1.84 | N/A | ns |
| | | XC6SLX100 | 0.06/1.48 | 0.06/1.63 | 0.06/1.87 | -0.03/2.72 | ns |
| | | XC6SLX100T | 0.06/1.48 | 0.06/1.63 | 0.06/1.87 | N/A | ns |
| | | XC6SLX150 | 0.04/1.73 | 0.04/1.75 | 0.04/1.98 | -0.08/3.07 | ns |
| | | XC6SLX150T | 0.04/1.73 | 0.04/1.75 | 0.04/1.98 | N/A | ns |
| | | XA6SLX4 | 0.64/0.96 | N/A | 0.97/1.12 | N/A | ns |
| | | XA6SLX9 | 0.44/0.99 | N/A | 0.62/1.16 | N/A | ns |
| | | XA6SLX16 | 0.50/0.78 | N/A | 0.69/0.83 | N/A | ns |
| | | XA6SLX25 | 0.28/1.04 | N/A | 0.28/1.25 | N/A | ns |
| | | XA6SLX25T | 0.28/1.04 | N/A | 0.28/1.25 | N/A | ns |
| | | XA6SLX45 | 0.43/1.21 | N/A | 0.50/1.40 | N/A | ns |
| | | XA6SLX45T | 0.43/1.21 | N/A | 0.50/1.40 | N/A | ns |
| | | XA6SLX75 | 0.38/1.49 | N/A | 0.38/1.84 | N/A | ns |
| | | XA6SLX75T | 0.38/1.49 | N/A | 0.38/1.84 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 1.01/1.63 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 0.38/1.84 | 0.05/2.78 | ns |
| | | XQ6SLX75T | 0.38/1.49 | N/A | 0.38/1.84 | N/A | ns |
| | | XQ6SLX150 | N/A | N/A | 0.04/1.98 | -0.08/3.07 | ns |
| | | XQ6SLX150T | 0.04/1.75 | N/A | 0.04/1.98 | N/A | ns |

Table 81: Source-Synchronous Pin-to-Pin Setup/Hold and Clock-to-Out Using BUFIO2 (Cont'd)

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|-------------------------------------|------------|-------------|------|------|------|-------|
| | | | -3 | -3N | -2 | -1L | |
| Pin-to-Pin Clock-to-Out Using BUFIO2 | | | | | | | |
| T _{ICKOFCS} | OFF clock-to-out using BUFIO2 clock | XC6SLX4 | 5.51 | N/A | 6.95 | 8.45 | ns |
| | | XC6SLX9 | 5.51 | 5.89 | 6.95 | 8.45 | ns |
| | | XC6SLX16 | 5.31 | 5.70 | 6.67 | 8.21 | ns |
| | | XC6SLX25 | 5.53 | 6.00 | 7.02 | 8.72 | ns |
| | | XC6SLX25T | 5.53 | 6.00 | 7.02 | N/A | ns |
| | | XC6SLX45 | 5.76 | 6.18 | 7.22 | 8.77 | ns |
| | | XC6SLX45T | 5.76 | 6.18 | 7.22 | N/A | ns |
| | | XC6SLX75 | 5.94 | 6.46 | 7.57 | 9.72 | ns |
| | | XC6SLX75T | 5.94 | 6.46 | 7.57 | N/A | ns |
| | | XC6SLX100 | 6.09 | 6.53 | 7.60 | 9.66 | ns |
| | | XC6SLX100T | 6.09 | 6.53 | 7.60 | N/A | ns |
| | | XC6SLX150 | 6.29 | 6.69 | 7.81 | 9.94 | ns |
| | | XC6SLX150T | 6.29 | 6.69 | 7.81 | N/A | ns |
| | | XA6SLX4 | 5.83 | N/A | 6.95 | N/A | ns |
| | | XA6SLX9 | 5.83 | N/A | 6.95 | N/A | ns |
| | | XA6SLX16 | 5.65 | N/A | 6.68 | N/A | ns |
| | | XA6SLX25 | 5.85 | N/A | 7.03 | N/A | ns |
| | | XA6SLX25T | 5.85 | N/A | 7.03 | N/A | ns |
| | | XA6SLX45 | 6.07 | N/A | 7.25 | N/A | ns |
| | | XA6SLX45T | 6.07 | N/A | 7.25 | N/A | ns |
| | | XA6SLX75 | 6.26 | N/A | 7.57 | N/A | ns |
| | | XA6SLX75T | 6.26 | N/A | 7.57 | N/A | ns |
| | | XA6SLX100 | N/A | N/A | 7.48 | N/A | ns |
| | | XQ6SLX75 | N/A | N/A | 7.57 | 9.72 | ns |
| | | XQ6SLX75T | 6.26 | N/A | 7.57 | N/A | ns |
| | | XQ6SLX150 | N/A | N/A | 7.81 | 9.94 | ns |
| XQ6SLX150T | 6.62 | N/A | 7.81 | N/A | ns | | |

Revision History

The following table shows the revision history for this document.

| Date | Version | Description of Revisions |
|----------|---------|---|
| 06/24/09 | 1.0 | Initial Xilinx release. |
| 08/26/09 | 1.1 | Added V_{FS} to Table 1 and Table 2 . Added R_{FUSE} to Table 2 . Added XC6SLX75 and XC6SLX75T to V_{BATT} and I_{BATT} in Table 1 , Table 2 , and Table 4 . Corrected the quiescent supply current for the XC6SLX4 in Table 5 . Updated Table 11 . Removed DV_{PPIN} from Figure 2 . Removed $F_{PCIECORE}$ from Table 24 and added values to $F_{PCIEUSER}$. Added more networking applications to Table 25 . Updated values for $T_{SUSPENDLOW_AWAKE}$, $T_{SUSPEND_ENABLE}$, and T_{SCP_AWAKE} in Table 46 . Numerous changes to Table 47 , page 54 including the addition of new values to various specifications, revising the $T_{SMCKCSO}$ description, and changing the units of T_{POR} . Also, removed <i>Dynamic Reconfiguration Port (DRP) for DCM and PLL Before and After DCLK</i> section from Table 47 and updated all the notes. In Table 52 , added to F_{INMAX} , revised F_{OUTMAX} , and removed PLL Maximum Output Frequency for BUFIO2. Revised values for DCM_DELAY_STEP in Table 54 . Updated CLKIN_FREQ_FX values in Table 55 . |
| 01/04/10 | 1.2 | Added -4 speed grade to entire document. Updated speed specification of -4, -3, -2 speed grades to version 1.03. Added -1L speed grade numbers per speed specification 1.00. Updated T_{SOL} in Table 1 . Added -1L rows for LVCMOS12, LVCMOS15, and LVCMOS18 in Table 9 . Revised much of the detail in GTP Transceiver Specifications in Table 12 through Table 23 . Added -2 data to Table 25 . Updated F_{MAX} in Table 44 . Updated descriptions for $T_{DNACLKL}$ and $T_{DNACLKH}$ in Table 45 and revised values for all parameters. Removed $T_{INITADDR}$ from Table 47 and added new data. Updated values in Table 48 through Table 62 . Added Table 51 (BUFPLL) and Table 57 (DCM_CLKGEN). Removed $T_{LOCKMAX}$ note from Table 52 . Updated note 3 in Table 53 . In Table 79 : removed XC6SLX75CSG324 and XC6SLX75TCSG324; added XC6SLX75FG(G)484 and XC6SLX75FG(G)484. |
| 02/22/10 | 1.3 | Production release of XC6SLX16 -2 speed grade devices. The changes to Table 26 and Table 27 includes updating this data sheet to the data in ISE v11.5 software with speed specification v1.06. Updated maximum of V_{IN} and V_{TS} and note 2 in Table 1 . In Table 2 , changed V_{IN} , added I_{IN} and note 5, revised notes 1, 6, and 7, and added note 8 to R_{FUSE} . In Table 4 , removed previous note 1 and added data to I_{RPU} , I_{RPD} , and I_{BATT} , changed C_{IN} , added R_{DT} and R_{IN_TERM} , and added note 2 and 3. Updated V_{CCO2} in Table 6 . Added Table 7 and Table 8 . Removed PCI66_3 from Table 9 . Updated PCI33_3 and I2C in Table 9 . Updated the description of Table 11 . Completely updated Table 25 . Updated Table 28 including adding values for PCI33_3. Updated V_{REF} value for HSTL_III_18 in Table 31 . Updates missing V_{REF} values in Table 32 . Added Simultaneously Switching Outputs , page 36 . Removed T_{GSRQ} and T_{RPW} from Table 35 and Table 36 . Also removed T_{DOQ} from Table 36 . Removed T_{ISDO_DO} and note 1 from Table 37 . Removed T_{OSCK_S} and combinatorial section from Table 38 . In Table 39 , removed T_{IODDO_T} and added new tap parameters and note 2. In Table 40 , Table 41 , and Table 42 , made typographical edits and removed notes. Removed clock CLK section in Table 41 . Removed clock CLK section and T_{REG_MUX} and T_{REG_M31} in Table 42 . Added block RAM F_{MAX} values to Table 43 . Updated values and added note 2 to Table 45 . Added values to Table 46 and removed note 1. Numerous changes to Table 47 . Completely updated Table 57 . Revised data in Table 62 . Removed note 3 from Table 71 . Added values to Table 79 . Added data to Table 80 and Table 81 . |
| 03/10/10 | 1.4 | Production release of XC6SLX45 -2 speed grade devices, which includes changes to Table 26 and Table 27 updating this data sheet to the data in ISE v11.5 software with speed specification v1.07. Fixed R_{IN_TERM} description in Table 4 . Added PCI66_3 to Table 7 and replaced note 1. Corrected note 1 and the V, Max for TMDS_33 in Table 8 . In Table 10 , added note 1 to LVPECL_33 and TMDS_33. Also updated specifications for TMDS_33. Updated the GTP Transceiver Specifications section including adding values to Table 16 , Table 17 , and Table 20 through Table 23 . Added PCI66_3 back into Table 9 , Table 28 , Table 31 , Table 32 , and Table 34 . Updated note 3 on Table 32 . In Table 34 , corrected some typographical errors and fixed SSO limits for bank1/3 in FG(G)484 package. Corrected T_{OSCKC_OCE} in Table 38 . In Table 57 , updated CLKFX_FREEZE_VAR and CLKFX_FREEZE_TEMP_SLOPE and added typical values to $T_{CENTER_LOW_SPREAD}$ and $T_{CENTER_HIGH_SPREAD}$. Updated and added values to Table 63 through Table 78 , and Table 81 . In Table 79 , revised the XC6SLX16-CSG324 and the XC6SLX45-CSG484 and FG(G)484 values. |

| Date | Version | Description of Revisions |
|----------|---------|--|
| 06/14/10 | 1.5 | <p>In Table 2, added note 5 and added temperature range to V_{FS} and R_{FUSE}. Removed speed grade delineation, revised I_{RPD} description, and updated note 2 in Table 4. Added note 2 to Table 7. Added DIFF_MOBILE_DDR to Table 8 and Table 10. Added note 4 to Table 15. Changed minimum DV_{PPIN} in Table 16. Updated $F_{GTPDRCLK}$ in Table 19. Increased maximum T_{LLSKEW} in Table 22. Updated descriptions and added data to Table 23. Removed note 1 and added new data to the Networking Applications section in Table 25. Updated Table 26 and Table 27 to the data in ISE v12.1 software with speed specification v1.08. In Table 28, added DIFF_MOBILE_DDR and updated -4 speed grade data. Updated the maximum I/O pairs per bank in Table 33. Updated note 2 on Table 39. Revised the F_{MAX} in Table 44. In Table 47, updated description for $T_{SMCKCSO}$, revised values for T_{POR} and added Min value, added $T_{BPIICCK}$ and $T_{SPIICCK}$. Also in Table 47, added device dependencies to F_{SMCCK} and F_{RBCKK}. Updated and added data to Table 63 through Table 78, and Table 81. In Table 79, added data on the XC6SLX45-FG(G)676 and revised the XC6SLX45T and XC6SLX150T values.</p> <p>The following changes to this specification are addressed in the product change notice XCN10024, <i>MCB Performance and JTAG Revision Code for Spartan-6 LX16 and LX45 FPGAs</i>. In Table 2, revised the V_{CCINT} to add the memory controller block extended performance specifications. In Table 25, changed the standard specifications and added extended performance specifications for the memory controller block and note 2. Added note 4 and updated values in Table 34.</p> |
| 06/24/10 | 1.6 | <p>Production release of XC6SLX45T (-2 and -3 speed grades), XC6SLX16 and XC6SLX45 (-3 speed grade) devices which includes changes to Table 26 and Table 27 (ISE v12.1 software with speed specification v1.08).</p> <p>Added the -3N speed grade, which designates Spartan-6 devices that do not support MCB functionality. This includes changes to Table 2 (note 2), Table 25 (note 4), and Switching Characteristics (Table 26).</p> <p>Updated Simultaneously Switching Outputs discussion. Added -3 speed grade values for T_{TAP} and F_{MINCAL} values in Table 39. In Table 40, updated T_{RPW} (-2 and -3 speed grade) values and F_{TOG} (-3 speed grade) values. In Table 48, updated T_{GIO} (-2 and -3 speed grade) values. Updated -3 values in spread spectrum section of Table 57.</p> |
| 07/16/10 | 1.7 | <p>Production release of specific devices listed in Table 26 and Table 27 using ISE v12.2 software with speed specification v1.11. Added note 4 advising designers of the patch which contains v1.11. Also updated the -1L speed specification to v1.04. Updated numerous -4 and -1L values. Added -4 T_{TAP} values and F_{MINCAL} to Table 39. Revised T_{CINCK}/T_{CKCIN} in Table 40. In Table 41, revised T_{SHCKO}. In Table 42, revised T_{REG}. Added new -1L values to Table 47. Added and updated values in Table 79.</p> |
| 07/26/10 | 1.8 | <p>Production release of XC6SLX25, XC6SLX25T, XC6SLX100 and XC6SLX100T in the specific speed grades listed in Table 26 and Table 27 using ISE v12.2 software with speed specification v1.11. Added note 7 to Table 2 and moved V_{FS} and R_{FUSE} to a new Table 3. Added I_{HS} and note 4 to Table 4. Added note 1 to Table 28. Added and updated SSO limits per V_{CC0}/GND pairs in Table 34. Added note 3 to Table 47. In Table 54, removed -1L specifications for CLKOUT_PER_JITT_DV1/2 and revised CLKIN_CLKFB_PHASE and CLKOUT_PHASE_DLL values. Updated note 3 in both Table 56 and Table 57.</p> |
| 08/23/10 | 1.9 | <p>Updated values for $F_{GTPRANGE1}$, $F_{GTPRANGE2}$, and $F_{GPLLMIN}$ in Table 18. Revised -3 and -4 values in Table 21. Removed the -1L speed grade readback support restriction and note 3 in Table 47.</p> |
| 11/05/10 | 1.10 | <p>Production release of XC6SLX4 and XC6SLX9 in the specific speed grades listed in Table 26 and Table 27 using ISE v12.3 software with speed specification v1.12 for the -2 speed grade available in the 12.3 <i>Speed Files Patch</i>. Added note 3 advising designers of the patch which contains v1.12.</p> <p>In Table 2, added note 4. In Table 4, added note 2. In Table 10, added notes 2 and 3. In Table 44, added note 2. In Table 47, updated symbol for T_{SMWCKK}/T_{SMCKKW}, changed -1L values for $T_{USERCCLKH}$ and $T_{USERCCLKL}$, and added and revised the modes for F_{MCKK} and F_{SMCKK}. In Table 53, redefined and expanded description for CLKIN_FREQ_DLL and rewrote note 3. Updated title of Table 58. Also in Table 78, revised T_{DCD_CLK} for XC6SLX150 and XC6SLX150T. Changed description of T_{PSFD}/T_{PHFD} in Table 71.</p> <p>For the -1L speed grade, updated data sheet to ISE 12.3 software with speed specification v1.05 which revised the values in the following tables: Table 25, Table 28, Table 35, Table 36, Table 37, Table 40 through Table 43, Table 48 through Table 56, Table 62 through Table 78, Table 80, and Table 81. Updated Notice of Disclaimer.</p> |

| Date | Version | Description of Revisions |
|----------|---------|---|
| 01/10/11 | 1.11 | <p>Production release of XC6SLX4 and XC6SLX9 in the specific speed grades listed in Table 26 and Table 27 using ISE v12.4 software with speed specification v1.15 for the -4, -3, -3N, and -2 speed grades. Added note 3 to Table 27. Also updated the -1L speed grade requirements to ISE v12.4 software with speed specification v1.06. Revised -3N definition throughout the document.</p> <p>Added note 4 to Table 2 and updated note 5. Added information on V_{CCINT} to note 1 in Table 5. Updated Networking Applications -3 values in Table 25 to match improvements made in ISE v12.4. In Table 28, added note 1 and revised the T_{IOTP} values for LVDS_33, LVDS_25, MINI_LVDS_33, MINI_LVDS_25, RSDS_33, RSDS_25, TMDS_33, PPDS_33, and PPDS_25. Added note 3 to Table 55.</p> |
| 02/11/11 | 1.12 | <p>As described in XCN11008: Product Discontinuation Notice For Spartan-6 LXT -4 Devices, the -4 speed specifications have been discontinued. As outlined in page 2 of the XCN, designers currently using -4 speed specifications should rerun timing analysis using the new -3 speed specifications before moving to a replacement device.</p> <p>Updated the networking applications section of Table 25. Updated -2 speed specifications throughout document and added note 3 to Table 27 advising designers to use the -2 speed specification update (v1.17) with the ISE 12.4 software patch. Added F_{CLKDIV} to Table 37 and Table 38. Updated note 2 in Table 39. Updated units for $T_{SMCKCSO}$ and T_{BPICCO} in Table 47. Updated -1L in Table 71. Removed Note 2: <i>Package delay information is available for these device/package combinations. This information can be used to deskew the package</i> from Table 79.</p> |
| 03/31/11 | 2.0 | <p>Production release of XC6SLX45 in the -1L speed grades listed in Table 26 and Table 27 using ISE v13.1 software with -1L speed specification v1.06.</p> <p>In Table 39, removed values in the -1L column and added note 3 as IODELAY2 only supports Tap0 for lower-power devices. Updated copyright page 1 and Notice of Disclaimer.</p> |
| 05/20/11 | 2.1 | <p>Production release of XC6SLX100 and XC6SLX150 in the specific speed grades listed in Table 26 and Table 27 using ISE v13.1 software with -1L speed specification v1.06. Updated Table 27 and Note 7 with changes per XCN11012: Speed File Change for -3N Devices. Revised Switching Characteristics section for speed specifications: v1.18 for -3, -3N, and -2; including improvements in Table 73 through Table 77 and Table 81.</p> <p>Removed <i>Memory Controller Block</i> from the performance heading in Table 2 and revised Note 2. In Table 4, added Note 1 to C_{IN} and updated the description of R_{IN_TERM}. Updated Note 1 in Table 5. Updated Note 1 of Table 7. In Table 25, added and removed -1L specifications, increased the standard performance DDR3 specifications, removed the extended performance DDR3 row and updated Note 3 and Note 4. Clarified the introductory information for Table 28 and Table 30.</p> <p>In Table 32: Revised V_{MEAS} value for LVCMOS12; revised V_{REF} for LVDS_25, LVDS_33, BLVDS_25, MINI_LVDS_25, MINI_LVDS_33, RSDS_25, and RSDS_33; revised R_{REF} for BLVDS_25 and TMDS_33; and added Note 4 and Note 5. Updated Note 2 and Note 3 in Table 39.</p> <p>In Table 47, revised the values and description of T_{POR} including adding Note 3. Also in Table 47, augmented the description and added specifications for F_{RBCK} and removed XC6SLX4 from F_{MCCK} (maximum frequency, parallel mode (Master SelectMAP/BPI)). Added BUFGMUX to Table 48 title. Added Table 50.</p> <p>In Table 52, revised specifications for $T_{EXTFVAR}$ and $F_{INJITTER}$. In Table 54 removed the 5 MHz < $CLKIN_FREQ_DLL$ parameter in the LOCK_DLL description. In both Table 56 and Table 57, removed the 5 MHz < F_{CLKIN} parameter in the LOCK_FX description. In Table 58, updated description for PSCLK_FREQ and PSCLK_PULSE.</p> <p>Revised title and symbol of Table 70, added new speed specifications for -1L, and added Note 2. Added Table 71.</p> |
| 07/11/11 | 2.2 | <p>Added the Automotive XA Spartan-6 and Defense-grade Spartan-6Q devices to all appropriate tables while sometimes removing the XC6S nomenclature. Added expanded temperature range (Q) to all appropriate tables. Updated T_{SOL} packages in Table 1. Added R_{OUT_TERM} to Table 4. Updated Note 2 on Table 13.</p> <p>Production release of the XC6SLX4, XC6SLX9, XC6SLX16, XC6SLX25, XC6SLX75, XQ6SLX75, and XQ6SLX150 in Table 26 and Table 27 using ISE v13.2 software with -1L speed specification v1.07.</p> <p>Production release of the XA6SLX16, XA6SLX25T, XA6SLX45, XA6SLX45T, XQ6SLX75, XQ6SLX75T, XQ6SLX150, and XQ6SLX150T in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19.</p> <p>Added Table 29: IOB Switching Characteristics for the Automotive XA Spartan-6 and the Spartan-6Q Devices(1). Updated CS(G)484 from CSG484 throughout data sheet. Clarified Note 3 in Table 39.</p> |
| 08/08/11 | 2.3 | <p>Production release of the XA6SLX25, XA6SLX75, and XA6SLX75T in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19.</p> |

| Date | Version | Description of Revisions |
|----------|---------|---|
| 09/14/11 | 2.4 | <p>Production release of the XA6SLX4 and XA6SLX9 devices in Table 26 and Table 27 using ISE v13.2 software with -2 and -3 speed specification v1.19. Added production released version of the XA6SLX100 to Table 26 and Table 27 using ISE v13.3 software with -2 speed specification v1.20.</p> <p>Updated R_{OUT_TERM} description in Table 4. Fixed the LVPECL V_H error in Table 31. Updated introduction in Simultaneously Switching Outputs. Added the XA6SLX100 to Table 63 through Table 78, and Table 81. Added Note 4 to Table 78 because the $T_{CKSKREW}$ for the XC6SLX100 is not the same as the $T_{CKSKREW}$ for the XA6SLX100.</p> <p>Revised the revision history for version 1.6 dated 06/24/10. Removed the parenthetical statement about the -3N speed grade: (specifications are identical to the -3 speed grade).</p> |
| 10/17/11 | 3.0 | <p>Changed the data sheet from Preliminary Product Specification to Product Specification.</p> <p>Updated the Switching Characteristics, page 19 speed specification version ISE v13.3 software to -2 and -3 speed specification v1.20 and -1L speed specification of v1.08. Also updated Note 1 in Table 27.</p> <p>In Table 43, <i>Block RAM Switching Characteristics</i>, the F_{MAX} value for the -2 speed grade has been changed from 260 MHz to 280 MHz.</p> <p>In Table 54, <i>Switching Characteristics for the DLL</i>, a Note 6 was added and linked to CLKIN_CLKFB_PHASE.</p> |
| 06/27/14 | 3.1 | <p>Added definition of T_{SOL} to Note 6 in Table 1. Added maximum current condition through ground clamp diode to I_{IN} in Table 2. Added (HSWAPEN = 1) to I_{HS} in Table 4. Replaced XPOWER with Xilinx Power throughout. In Table 16, moved value of 1000 mV from Max to Min column and added sentence about DV_{PP_OUTPUT} being the minimum guaranteed value at the maximum setting to Note 1. Updated introductory paragraphs in Simultaneously Switching Outputs. Added Note 1 to Table 35. Added Note 1 to Table 36. Corrected Note 2 in Table 39 to say "Maximum tap delay." Added alternate symbols to Table 45. In Table 48, updated symbols for T_{GSI} and T_{GIO} and added Note 1. Added Note 1 to Table 49. Updated descriptions of F_{INMAX} in Table 52. Replaced BUFG with BUFGMUX in Note 3 of Table 53 and Note 3 of Table 54. In Table 56, updated subheading to "Phase Alignment (Phase Error)." In Table 57, updated Note 6 and added Note 7.</p> |
| 01/30/15 | 3.1.1 | Corrected table note reference in Table 52 . |

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