

XCR3256XL-10FTG256I Datasheet

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XCR3256XL-10FTG256I

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| | |
|------------------------------|-------------------------------------|
| DiGi Electronics Part Number | XCR3256XL-10FTG256I-DG |
| Manufacturer | AMD |
| Manufacturer Product Number | XCR3256XL-10FTG256I |
| Description | IC CPLD 256MC 9.1NS 256FTBGA |
| Detailed Description | Embedded, Integrated Circuits (ICs) |



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

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Purchase and inquiry

Manufacturer Product Number:

XCR3256XL-10FTG256I

Series:

CoolRunner XPLA3

DiGi-Electronics Programmable:

Not Verified

Delay Time tpd(1) Max:

9.1 ns

Number of Logic Elements/Blocks:

16

Number of Gates:

6000

Operating Temperature:

-40°C ~ 85°C (TA)

Package / Case:

256-LBGA

Base Product Number:

XCR3256

Manufacturer:

AMD

Product Status:

Last Time Buy

Programmable Type:

In System Programmable (min 1K program/erase cycles)

Voltage Supply - Internal:

2.7V ~ 3.6V

Number of Macrocells:

256

Number of I/O:

164

Mounting Type:

Surface Mount

Supplier Device Package:

256-FTBGA (17x17)

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

3 (168 Hours)

ECCN:

EAR99



XCR3256XL 256 Macrocell CPLD

DS013 (v2.7) March 31, 2006

Product Specification

Features

- Low power 3.3V 256 macrocell CPLD
- 7.0 ns pin-to-pin logic delays
- System frequencies up to 154 MHz
- 256 macrocells with 6,000 usable gates
- Available in small footprint packages
 - 144-pin TQFP (120 user I/O pins)
 - 208-pin PQFP (164 user I/O)
 - 256-ball FBGA (164 user I/O)
 - 280-ball CS BGA (164 user I/O)
- Optimized for 3.3V systems
 - Ultra low power operation
 - Typical Standby Current of 18 μ A at 25°C
 - 5V tolerant I/O pins with 3.3V core supply
 - Advanced 0.35 micron five layer metal EEPROM process
 - Fast Zero Power™ (FZP) CMOS design technology
 - 3.3V PCI electrical specification compatible outputs (no internal clamp diode on any input or I/O)
- Advanced system features
 - In-system programming
 - Input registers
 - Predictable timing model
 - Up to 23 clocks available per function block
 - Excellent pin retention during design changes
 - Full IEEE Standard 1149.1 boundary-scan (JTAG)
 - Four global clocks
 - Eight product term control terms per function block
- Fast ISP programming times
- Port Enable pin for additional I/O
- 2.7V to 3.6V supply voltage at industrial grade voltage range
- Programmable slew rate control per output
- Security bit prevents unauthorized access
- Refer to the CoolRunner™ XPLA3 family data sheet ([DS012](#)) for architecture description

Description

The CoolRunner™ XPLA3 XCR3256XL device is a 3.3V, 256 macrocell CPLD targeted at power sensitive designs that require leading edge programmable logic solutions. A total of 16 function blocks provide 6,000 usable gates. Pin-to-pin propagation delays are as fast as 7.0 ns with a maximum system frequency of 154 MHz.

TotalCMOS Design Technique for Fast Zero Power

CoolRunner XPLA3 CPLDs offer a TotalCMOS™ solution, both in process technology and design technique. These CPLDs employ a cascade of CMOS gates to implement their sum of products, instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx CPLDs to offer devices that are both high performance and low power, breaking the paradigm that to have low power, you must have low performance. Refer to [Figure 1](#) and [Table 1](#) showing the I_{CC} vs. Frequency of our XCR3256XL TotalCMOS CPLD (data taken with 16 resettable up/down, 16-bit counters at 3.3V, 25°C).

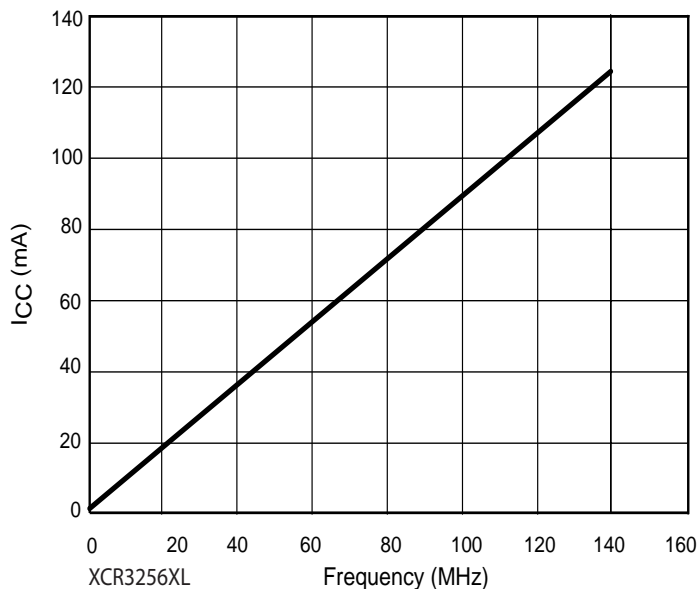


Figure 1: Typical I_{CC} vs. Frequency at $V_{CC} = 3.3V$, 25°C

Table 1: Typical I_{CC} vs. Frequency at $V_{CC} = 3.3V$, 25°C

| Frequency (MHz) | 0 | 1 | 10 | 20 | 40 | 60 | 80 | 100 | 120 | 140 |
|-----------------------|-------|------|------|------|------|------|------|------|-------|-------|
| Typical I_{CC} (mA) | 0.018 | 0.98 | 9.69 | 19.3 | 38.1 | 56.2 | 73.7 | 90.8 | 107.3 | 123.9 |

DC Electrical Characteristics Over Recommended Operating Conditions⁽¹⁾

| Symbol | Parameter | Test Conditions | Typical | Min. | Max. | Unit |
|------------------|--|--|---------|--------------------|------|---------|
| $V_{OH}^{(2)}$ | Output High voltage | $V_{CC} = 3.0V$ to $3.6V$, $I_{OH} = -8$ mA | - | 2.4 | - | |
| | | $V_{CC} = 2.7V$ to $3.0V$, $I_{OH} = -8$ mA | - | 2.0 | - | |
| | | $I_{OH} = -500$ μA | - | 90% $V_{CC}^{(3)}$ | - | |
| V_{OL} | Output Low voltage for 3.3V outputs | $I_{OL} = 8$ mA | - | - | 0.4 | V |
| I_{IL} | Input leakage current | $V_{IN} = GND$ or V_{CC} to 5.5V | - | -10 | 10 | μA |
| I_{IH} | I/O High-Z leakage current | $V_{IN} = GND$ or V_{CC} to 5.5V | - | -10 | 10 | μA |
| $I_{CCSB}^{(7)}$ | Standby current | $V_{CC} = 3.6V$ | 30.5 | - | 100 | μA |
| I_{CC} | Dynamic current ^(4,5) | $f = 1$ MHz | - | - | 2 | mA |
| | | $f = 50$ MHz | - | - | 60 | mA |
| C_{IN} | Input pin capacitance ⁽⁶⁾ | $f = 1$ MHz | - | - | 8 | pF |
| C_{CLK} | Clock input capacitance ⁽⁶⁾ | $f = 1$ MHz | - | 5 | 12 | pF |
| $C_{I/O}$ | I/O pin capacitance ⁽⁶⁾ | $f = 1$ MHz | - | - | 10 | pF |

Notes:

- See the CoolRunner XPLA3 family data sheet (DS012) for recommended operating conditions.
- See [Figure 2](#) for output drive characteristics of the XPLA3 family.
- This parameter guaranteed by design and characterization, not by testing.
- See [Table 1](#), [Figure 1](#) for typical values.
- This parameter measured with a 16-bit, resettable up/down counter loaded into every function block, with all outputs disabled and unloaded. Inputs are tied to V_{CC} or ground. This parameter guaranteed by design and characterization, not testing.
- Typical values, not tested.
- Typical value at 70° C.

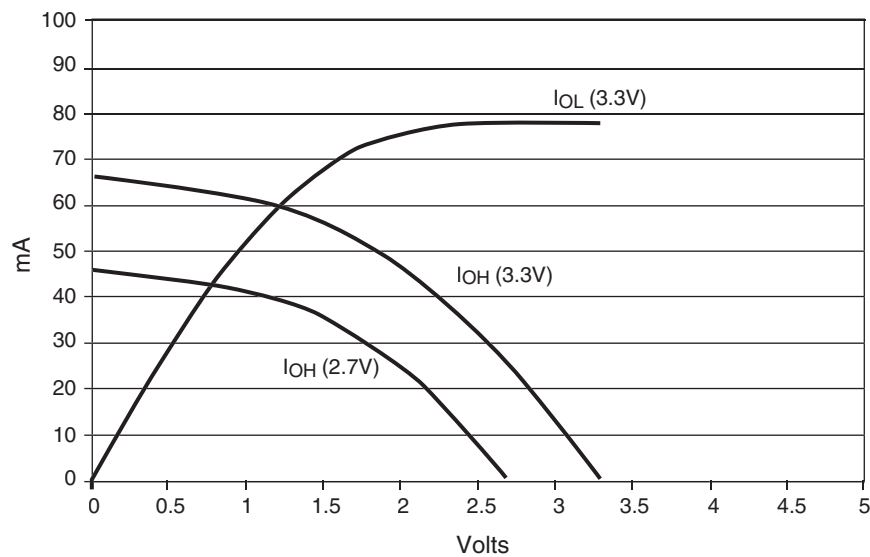


Figure 2: Typical I/V Curve for the CoolRunner XPLA3 Family, 25°C

AC Electrical Characteristics Over Recommended Operating Conditions^(1,2)

| Symbol | Parameter | -7 | | -10 | | -12 | | Unit |
|------------------------------------|---|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| T _{PD1} | Propagation delay time (single p-term) | - | 7.0 | - | 9.0 | - | 10.8 | ns |
| T _{PD2} | Propagation delay time (OR array) ⁽³⁾ | - | 7.5 | - | 10.0 | - | 12.0 | ns |
| T _{CO} | Clock to output (global synchronous pin clock) | - | 4.5 | - | 5.8 | - | 6.9 | ns |
| T _{SUF} | Setup time (fast input register) | 2.5 | - | 3.0 | - | 3.0 | - | ns |
| T _{SU1} ⁽⁴⁾ | Setup time (single p-term) | 4.3 | - | 5.5 | - | 6.7 | - | ns |
| T _{SU2} | Setup time (OR array) | 4.8 | - | 6.5 | - | 7.9 | - | ns |
| T _H ⁽⁴⁾ | Hold time | 0 | - | 0 | - | 0 | - | ns |
| T _{WLH} ⁽⁴⁾ | Global Clock pulse width (High or Low) | 3.0 | - | 4.0 | - | 5.0 | - | ns |
| T _{PLH} ⁽⁴⁾ | P-term clock pulse width | 4.5 | - | 6.0 | - | 7.5 | - | ns |
| T _{APRPW} | Asynchronous preset/reset pulse width (High or Low) | 4.5 | - | 6.0 | - | 7.5 | - | ns |
| T _R ⁽⁴⁾ | Input rise time | - | 20 | - | 20 | - | 20 | ns |
| T _L ⁽⁴⁾ | Input fall time | - | 20 | - | 20 | - | 20 | ns |
| f _{SYSTEM} ⁽⁴⁾ | Maximum system frequency | - | 154 | - | 105 | - | 88 | MHz |
| T _{CONFIG} ⁽⁴⁾ | Configuration time ⁽⁵⁾ | - | 200 | - | 200 | - | 200 | μs |
| T _{INIT} ⁽⁴⁾ | ISP initialization time | - | 200 | - | 200 | - | 200 | μs |
| T _{POE} ⁽⁴⁾ | P-term OE to output enabled | - | 9.0 | - | 11.0 | - | 13.0 | ns |
| T _{POD} ⁽⁴⁾ | P-term OE to output disabled ⁽⁶⁾ | - | 9.0 | - | 11.0 | - | 13.0 | ns |
| T _{PCO} ⁽⁴⁾ | P-term clock to output | - | 8.0 | - | 10.3 | - | 12.4 | ns |
| T _{PAO} ⁽⁴⁾ | P-term set/reset to output valid | - | 9.0 | - | 11.0 | - | 13.0 | ns |

Notes:

1. Specifications measured with one output switching.
2. See XPLA3 family data sheet ([DS012](#)) for recommended operating conditions.
3. See [Figure 4](#) for derating.
4. These parameters guaranteed by design and/or characterization, not testing.
5. Typical current draw during configuration is 10 mA at 3.6V.
6. Output C_L = 5 pF.

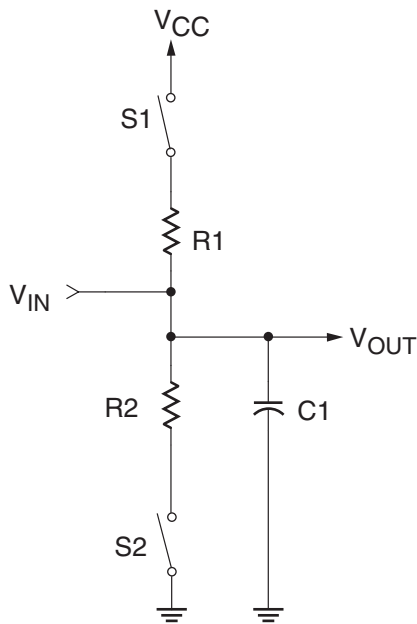
Internal Timing Parameters^(1,2)

| Symbol | Parameter | -7 | | -10 | | -12 | | Unit |
|---|--------------------------------------|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Buffer Delays | | | | | | | | |
| T _{IN} | Input buffer delay | - | 2.5 | - | 3.3 | - | 4.0 | ns |
| T _{FIN} | Fast input buffer delay | - | 2.7 | - | 3.3 | - | 3.3 | ns |
| T _{GCK} | Global clock buffer delay | - | 1.0 | - | 1.3 | - | 1.5 | ns |
| T _{OUT} | Output buffer delay | - | 2.5 | - | 3.2 | - | 3.8 | ns |
| T _{EN} | Output buffer enable/disable delay | - | 4.5 | - | 5.2 | - | 6.0 | ns |
| Internal Register and Combinatorial Delays | | | | | | | | |
| T _{LDI} | Latch transparent delay | - | 1.3 | - | 1.6 | - | 2.0 | ns |
| T _{SUI} | Register setup time | 0.8 | - | 1.0 | - | 1.2 | - | ns |
| T _{HI} | Register hold time | 0.3 | - | 0.5 | - | 0.7 | - | ns |
| T _{ECSU} | Register clock enable setup time | 2.0 | - | 2.5 | - | 3.0 | - | ns |
| T _{ECHO} | Register clock enable hold time | 3.0 | - | 4.5 | - | 5.5 | - | ns |
| T _{COI} | Register clock to output delay | - | 1.0 | - | 1.3 | - | 1.6 | ns |
| T _{AOI} | Register async. S/R to output delay | - | 2.0 | - | 2.0 | - | 2.2 | ns |
| T _{RAI} | Register async. recovery | - | 5.0 | - | 7.0 | - | 8.0 | ns |
| T _{PTCK} | Product term clock delay | - | 2.0 | - | 2.5 | - | 3.0 | ns |
| T _{LOGI1} | Internal logic delay (single p-term) | - | 2.0 | - | 2.5 | - | 3.0 | ns |
| T _{LOGI2} | Internal logic delay (PLA OR term) | - | 2.5 | - | 3.5 | - | 4.2 | ns |
| Feedback Delays | | | | | | | | |
| T _F | ZIA delay | - | 2.2 | - | 3.7 | - | 4.4 | ns |
| Time Adders | | | | | | | | |
| T _{LOGI3} | Fold-back NAND delay | - | 2.0 | - | 2.5 | - | 3.0 | ns |
| T _{UDA} | Universal delay | - | 2.0 | - | 2.5 | - | 3.0 | ns |
| T _{SLEW} | Slew rate limited delay | - | 4.0 | - | 5.0 | - | 6.0 | ns |

Notes:

1. These parameters guaranteed by design and/or characterization, not testing.
2. See the CoolRunner XPLA3 family data sheet ([DS012](#)) for the timing model.

Switching Characteristics



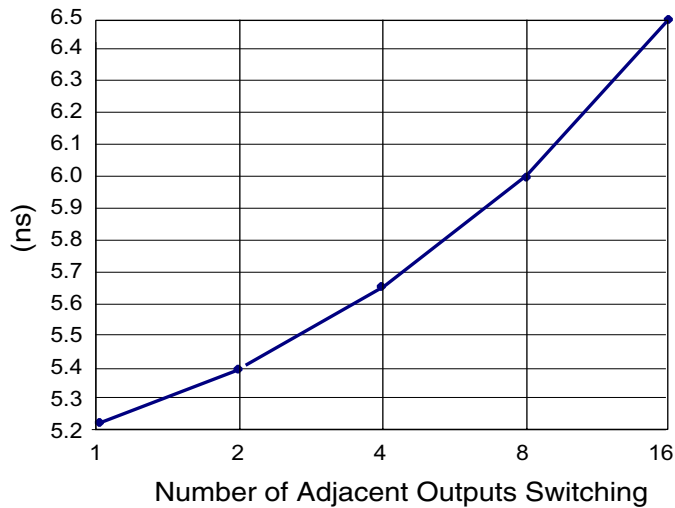
| Component | Values |
|-----------|--------|
| R1 | 390Ω |
| R2 | 390Ω |
| C1 | 35 pF |

| Measurement | S1 | S2 |
|-------------------------|--------|--------|
| T _{POE (High)} | Open | Closed |
| T _{POE (Low)} | Closed | Open |
| T _P | Closed | Closed |

Note: For T_{POD}, C1 = 5 pF. Delay measured at output level of V_{OL} + 300 mV, V_{OH} - 300 mV.

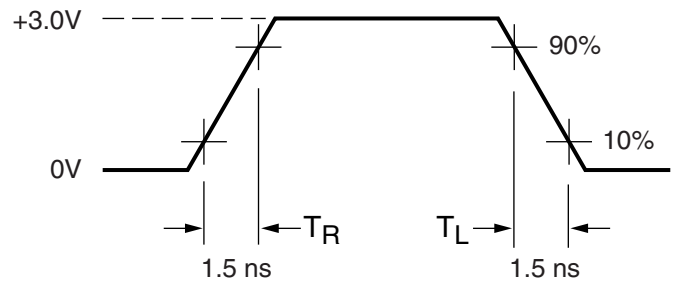
DS013_03_102401

Figure 3: AC Load Circuit



DS013_04_042800

Figure 4: Derating Curve for T_{PD2}



Measurements:

All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

DS017_05_042800

Figure 5: Voltage Waveform

Pin Descriptions

Table 2: XCR3256XL User I/O Pins

| | TQ144 | PQ208 | FT256 | CS280 |
|---------------------|-------|-------|-------|-------|
| Total User I/O Pins | 120 | 164 | 164 | 164 |

Table 3: XCR3256XL I/O Pins

| Function Block | Macro-cell | TQ144 | PQ208 | FT256 | CS280 |
|----------------|------------|--------------------|-------|-------|-------|
| 1 | 1 | 106 | 6 | C16 | E18 |
| 1 | 2 | - | 7 | F12 | E19 |
| 1 | 3 | 104 ⁽¹⁾ | 8 | D16 | F15 |
| 1 | 4 | 103 | 9 | E14 | F17 |
| 1 | 5 | 102 | 10 | E15 | F18 |
| 1 | 6 | - | - | - | - |
| 1 | 7 | - | - | - | - |
| 1 | 8 | - | - | - | - |
| 1 | 9 | - | - | - | - |
| 1 | 10 | - | - | - | - |
| 1 | 11 | - | - | - | - |
| 1 | 12 | 101 | 11 | F13 | F19 |
| 1 | 13 | 100 | 12 | E16 | G16 |
| 1 | 14 | 99 | 13 | F14 | G17 |
| 1 | 15 | - | 15 | F15 | G19 |
| 1 | 16 | - | 16 | G12 | H16 |
| 2 | 1 | 107 | 4 | E13 | B19 |
| 2 | 2 | 108 | 3 | D15 | B18 |
| 2 | 3 | - | 206 | C13 | B17 |
| 2 | 4 | - | 205 | A14 | A18 |
| 2 | 5 | 109 | 204 | E11 | A17 |
| 2 | 6 | - | - | - | - |
| 2 | 7 | - | - | - | - |
| 2 | 8 | - | - | - | - |
| 2 | 9 | - | - | - | - |
| 2 | 10 | - | - | - | - |
| 2 | 11 | - | - | - | - |
| 2 | 12 | 110 | 203 | A13 | C16 |
| 2 | 13 | 111 | 202 | D12 | A16 |
| 2 | 14 | - | 201 | B13 | E15 |
| 2 | 15 | 112 | 199 | C12 | D15 |
| 2 | 16 | 113 | 198 | A12 | A15 |

Table 3: XCR3256XL I/O Pins (Continued)

| Function Block | Macro-cell | TQ144 | PQ208 | FT256 | CS280 |
|----------------|------------|-------------------|--------------------|--------------------|--------------------|
| 3 | 1 | 98 | 17 | G15 | H17 |
| 3 | 2 | 97 | 18 | G13 | H18 |
| 3 | 3 | 96 | 19 | F16 | H19 |
| 3 | 4 | 94 | 20 | G14 | J16 |
| 3 | 5 | 93 | 21 | G16 | J17 |
| 3 | 6 | - | - | - | - |
| 3 | 7 | - | - | - | - |
| 3 | 8 | - | - | - | - |
| 3 | 9 | - | - | - | - |
| 3 | 10 | - | - | - | - |
| 3 | 11 | - | - | - | - |
| 3 | 12 | 92 | 22 | H13 | J18 |
| 3 | 13 | - | 24 | H12 | K16 |
| 3 | 14 | 91 | 25 | H15 | K17 |
| 3 | 15 | 90 | 26 | H14 | K18 |
| 3 | 16 | - | 27 | H16 | L16 |
| 4 | 1 | 114 | 197 | D11 | E14 |
| 4 | 2 | 116 | 196 | A11 | D14 |
| 4 | 3 | 117 | 195 | E10 | A14 |
| 4 | 4 | - | 194 | B12 | C13 |
| 4 | 5 | 118 | 193 | C11 | B13 |
| 4 | 6 | - | - | - | - |
| 4 | 7 | - | - | - | - |
| 4 | 8 | - | - | - | - |
| 4 | 9 | - | - | - | - |
| 4 | 10 | - | - | - | - |
| 4 | 11 | - | - | - | - |
| 4 | 12 | 119 | 192 | B11 | A13 |
| 4 | 13 | 120 | 190 | A10 | A12 |
| 4 | 14 | 121 | 189 ⁽¹⁾ | C10 ⁽¹⁾ | C12 ⁽¹⁾ |
| 4 | 15 | - | 188 | A9 | B12 |
| 4 | 16 | 122 | 187 | D9 | D12 |
| 5 | 1 | 89 ⁽¹⁾ | 28 | J14 | L17 |
| 5 | 2 | - | 29 | J15 | L18 |
| 5 | 3 | 88 | 30 ⁽¹⁾ | J13 ⁽¹⁾ | L19 ⁽¹⁾ |
| 5 | 4 | 87 | 31 | J16 | M16 |
| 5 | 5 | 86 | 33 | L14 | M18 |

Table 3: XCR3256XL I/O Pins (Continued)

| Function Block | Macro-cell | TQ144 | PQ208 | FT256 | CS280 |
|----------------|------------|-------|-------|-------|-------|
| 5 | 6 | - | - | - | - |
| 5 | 7 | - | - | - | - |
| 5 | 8 | - | - | - | - |
| 5 | 9 | - | - | - | - |
| 5 | 10 | - | - | - | - |
| 5 | 11 | - | - | - | - |
| 5 | 12 | 84 | 34 | K15 | M17 |
| 5 | 13 | - | 35 | K14 | N16 |
| 5 | 14 | 83 | 36 | K16 | N19 |
| 5 | 15 | 82 | 37 | K13 | N18 |
| 5 | 16 | - | 38 | L15 | N17 |
| 6 | 1 | - | 78 | R9 | U10 |
| 6 | 2 | 55 | 77 | N9 | T10 |
| 6 | 3 | 56 | 76 | T10 | W11 |
| 6 | 4 | - | 73 | P10 | U11 |
| 6 | 5 | 60 | 71 | R10 | T11 |
| 6 | 6 | - | - | - | - |
| 6 | 7 | - | - | - | - |
| 6 | 8 | - | - | - | - |
| 6 | 9 | - | - | - | - |
| 6 | 10 | - | - | - | - |
| 6 | 11 | - | - | - | - |
| 6 | 12 | 61 | 70 | T11 | W12 |
| 6 | 13 | 62 | 69 | N10 | U12 |
| 6 | 14 | 63 | 68 | P11 | T12 |
| 6 | 15 | - | 67 | M10 | V13 |
| 6 | 16 | 65 | 66 | R11 | U13 |
| 7 | 1 | 81 | 39 | K12 | P16 |
| 7 | 2 | - | 40 | L16 | P18 |
| 7 | 3 | 80 | 42 | M15 | R19 |
| 7 | 4 | 79 | 43 | N15 | R16 |
| 7 | 5 | 78 | 44 | L13 | R18 |
| 7 | 6 | - | - | - | - |
| 7 | 7 | - | - | - | - |
| 7 | 8 | - | - | - | - |
| 7 | 9 | - | - | - | - |
| 7 | 10 | - | - | - | - |

Table 3: XCR3256XL I/O Pins (Continued)

| Function Block | Macro-cell | TQ144 | PQ208 | FT256 | CS280 |
|----------------|------------|-------|-------|-------|-------|
| 7 | 11 | - | - | - | - |
| 7 | 12 | 77 | 45 | M16 | R17 |
| 7 | 13 | - | 46 | M14 | R15 |
| 7 | 14 | 75 | 47 | N16 | T17 |
| 7 | 15 | 74 | 48 | L12 | T16 |
| 7 | 16 | - | 49 | P15 | U19 |
| 8 | 1 | 66 | 65 | T12 | T13 |
| 8 | 2 | 67 | 64 | R12 | W14 |
| 8 | 3 | 68 | 62 | N11 | T14 |
| 8 | 4 | 69 | 61 | T13 | R14 |
| 8 | 5 | - | 60 | P12 | W15 |
| 8 | 6 | - | - | - | - |
| 8 | 7 | - | - | - | - |
| 8 | 8 | - | - | - | - |
| 8 | 9 | - | - | - | - |
| 8 | 10 | - | - | - | - |
| 8 | 11 | - | - | - | - |
| 8 | 12 | 70 | 59 | R13 | U15 |
| 8 | 13 | - | 58 | M11 | V15 |
| 8 | 14 | 71 | 57 | T14 | T15 |
| 8 | 15 | - | 56 | N12 | V16 |
| 8 | 16 | 72 | 55 | R14 | W17 |
| 9 | 1 | 2 | 153 | D3 | B1 |
| 9 | 2 | 1 | 154 | C1 | C3 |
| 9 | 3 | - | 159 | B4 | A4 |
| 9 | 4 | - | 160 | E6 | B5 |
| 9 | 5 | 143 | 161 | A4 | C5 |
| 9 | 6 | - | - | - | - |
| 9 | 7 | - | - | - | - |
| 9 | 8 | - | - | - | - |
| 9 | 9 | - | - | - | - |
| 9 | 10 | - | - | - | - |
| 9 | 11 | - | - | - | - |
| 9 | 12 | - | 162 | C5 | A5 |
| 9 | 13 | 142 | 163 | B5 | E6 |
| 9 | 14 | 141 | 164 | D6 | D6 |
| 9 | 15 | 140 | 166 | A5 | B6 |

Table 3: XCR3256XL I/O Pins (Continued)

| Function Block | Macro-cell | TQ144 | PQ208 | FT256 | CS280 |
|----------------|------------|------------------|--------------------|-------------------|-------------------|
| 9 | 16 | 139 | 167 | C6 | A6 |
| 10 | 1 | 4 ⁽¹⁾ | 151 | D1 | D2 |
| 10 | 2 | - | 150 | E4 | D1 |
| 10 | 3 | 5 | 149 | D2 | E3 |
| 10 | 4 | 6 | 148 | E3 | E2 |
| 10 | 5 | 7 | 147 | E1 | E4 |
| 10 | 6 | - | - | - | - |
| 10 | 7 | - | - | - | - |
| 10 | 8 | - | - | - | - |
| 10 | 9 | - | - | - | - |
| 10 | 10 | - | - | - | - |
| 10 | 11 | - | - | - | - |
| 10 | 12 | 8 | 146 | F4 | E1 |
| 10 | 13 | - | 145 | F1 | F5 |
| 10 | 14 | 9 | 144 | G5 | F3 |
| 10 | 15 | 10 | 142 | E2 | F4 |
| 10 | 16 | 11 | 141 | F3 | G3 |
| 11 | 1 | - | 168 | B6 | D7 |
| 11 | 2 | - | 169 | E7 | C7 |
| 11 | 3 | 138 | 170 | A6 | B7 |
| 11 | 4 | - | 171 | D7 | A7 |
| 11 | 5 | 137 | 172 | B7 | C8 |
| 11 | 6 | - | - | - | - |
| 11 | 7 | - | - | - | - |
| 11 | 8 | - | - | - | - |
| 11 | 9 | - | - | - | - |
| 11 | 10 | - | - | - | - |
| 11 | 11 | - | - | - | - |
| 11 | 12 | 136 | 173 | C7 | B8 |
| 11 | 13 | 134 | 175 | C8 | C9 |
| 11 | 14 | 133 | 176 ⁽¹⁾ | A7 ⁽¹⁾ | B9 ⁽¹⁾ |
| 11 | 15 | 132 | 177 | D8 | D10 |
| 11 | 16 | 131 | 178 | B8 | C10 |
| 12 | 1 | - | 140 | F2 | G2 |
| 12 | 2 | - | 139 | G4 | G1 |
| 12 | 3 | 12 | 138 | G1 | G4 |
| 12 | 4 | 14 | 137 | H1 | H1 |

Table 3: XCR3256XL I/O Pins (Continued)

| Function Block | Macro-cell | TQ144 | PQ208 | FT256 | CS280 |
|----------------|------------|-------------------|--------------------|-------------------|-------------------|
| 12 | 5 | 15 | 136 | H4 | H3 |
| 12 | 6 | - | - | - | - |
| 12 | 7 | - | - | - | - |
| 12 | 8 | - | - | - | - |
| 12 | 9 | - | - | - | - |
| 12 | 10 | - | - | - | - |
| 12 | 11 | - | - | - | - |
| 12 | 12 | 16 | 135 | G2 | H2 |
| 12 | 13 | - | 133 | J1 | J2 |
| 12 | 14 | 18 | 132 | J3 | J3 |
| 12 | 15 | 19 | 131 | H2 | K2 |
| 12 | 16 | - | 130 | J5 | K3 |
| 13 | 1 | - | 79 | P9 | W10 |
| 13 | 2 | 54 | 80 | T9 | T9 |
| 13 | 3 | 53 | 81 | P8 | U9 |
| 13 | 4 | - | 84 | R8 | T8 |
| 13 | 5 | 49 | 86 | N8 | T7 |
| 13 | 6 | - | - | - | - |
| 13 | 7 | - | - | - | - |
| 13 | 8 | - | - | - | - |
| 13 | 9 | - | - | - | - |
| 13 | 10 | - | - | - | - |
| 13 | 11 | - | - | - | - |
| 13 | 12 | 48 | 87 | T8 | W7 |
| 13 | 13 | 47 | 88 | P7 | V7 |
| 13 | 14 | 46 | 89 | R7 | U7 |
| 13 | 15 | - | 90 | P6 | W6 |
| 13 | 16 | 45 | 91 | T7 | T6 |
| 14 | 1 | 20 ⁽¹⁾ | 129 | J2 | K4 |
| 14 | 2 | - | 128 | J4 | L1 |
| 14 | 3 | 21 | 127 ⁽¹⁾ | K1 ⁽¹⁾ | L2 ⁽¹⁾ |
| 14 | 4 | 22 | 126 | K3 | L3 |
| 14 | 5 | 23 | 124 | K2 | M1 |
| 14 | 6 | - | - | - | - |
| 14 | 7 | - | - | - | - |
| 14 | 8 | - | - | - | - |
| 14 | 9 | - | - | - | - |

Table 3: XCR3256XL I/O Pins (Continued)

| Function Block | Macro-cell | TQ144 | PQ208 | FT256 | CS280 |
|----------------|------------|-------|-------|-------|-------|
| 14 | 10 | - | - | - | - |
| 14 | 11 | - | - | - | - |
| 14 | 12 | 25 | 123 | L1 | M3 |
| 14 | 13 | - | 122 | K4 | M4 |
| 14 | 14 | 26 | 121 | L3 | N1 |
| 14 | 15 | 27 | 120 | K5 | N2 |
| 14 | 16 | 28 | 119 | M1 | N3 |
| 15 | 1 | 44 | 92 | N7 | V6 |
| 15 | 2 | 43 | 93 | R6 | U6 |
| 15 | 3 | 42 | 95 | M7 | R6 |
| 15 | 4 | 41 | 96 | T5 | W5 |
| 15 | 5 | 40 | 97 | T6 | T5 |
| 15 | 6 | - | - | - | - |
| 15 | 7 | - | - | - | - |
| 15 | 8 | - | - | - | - |
| 15 | 9 | - | - | - | - |
| 15 | 10 | - | - | - | - |
| 15 | 11 | - | - | - | - |
| 15 | 12 | - | 98 | R5 | V5 |
| 15 | 13 | 39 | 99 | N6 | U5 |
| 15 | 14 | 38 | 100 | T4 | W4 |
| 15 | 15 | - | 101 | P5 | U4 |
| 15 | 16 | 37 | 102 | R4 | W3 |
| 16 | 1 | - | 118 | L2 | P1 |
| 16 | 2 | - | 117 | M2 | P2 |
| 16 | 3 | 29 | 115 | M3 | P4 |
| 16 | 4 | 30 | 114 | N2 | R3 |
| 16 | 5 | 31 | 113 | L5 | R2 |
| 16 | 6 | - | - | - | - |
| 16 | 7 | - | - | - | - |
| 16 | 8 | - | - | - | - |
| 16 | 9 | - | - | - | - |
| 16 | 10 | - | - | - | - |
| 16 | 11 | - | - | - | - |
| 16 | 12 | 32 | 112 | P1 | R4 |
| 16 | 13 | - | 111 | M4 | T3 |
| 16 | 14 | 34 | 110 | R1 | U1 |

Table 3: XCR3256XL I/O Pins (Continued)

| Function Block | Macro-cell | TQ144 | PQ208 | FT256 | CS280 |
|----------------|------------|-------|-------|-------|-------|
| 16 | 15 | 35 | 109 | N3 | V1 |
| 16 | 16 | 36 | 108 | T1 | U2 |

Notes:

- JTAG pins.

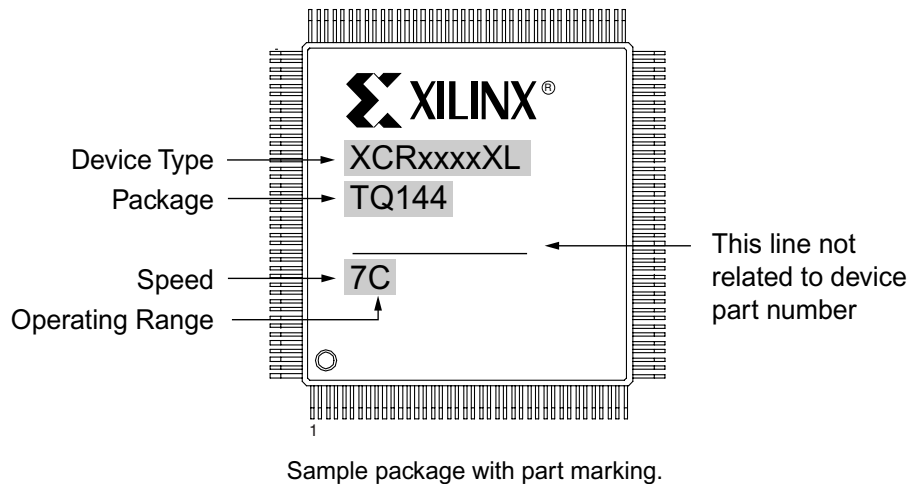
Table 4: XCR3256XL Global, JTAG, Port Enable, Power, and No Connect Pins

| Pin Type | TQ144 | PQ208 | FT256 | CS280 |
|-------------|---|--|--|---|
| IN0 / CLK0 | 128 | 181 | B9 | A10 |
| IN1 / CLK1 | 127 | 182 | A8 | D11 |
| IN2 / CLK2 | 126 | 183 | C9 | C11 |
| IN3 / CLK3 | 125 | 184 | B10 | B11 |
| TCK | 89 | 30 | J13 | L19 |
| TDI | 4 | 176 | A7 | B9 |
| TDO | 104 | 189 | C10 | C12 |
| TMS | 20 | 127 | K1 | L2 |
| PORT_EN | 13 ⁽¹⁾ | 116 ⁽¹⁾ | N1 ⁽¹⁾ | P3 ⁽¹⁾ |
| Vcc | 24, 50, 51, 58, 73, 76, 95, 115, 123, 130, 144 | 5, 23, 41, 63, 74, 83, 85, 107, 125, 143, 165, 179, 186, 191 | E8, E9, F7, F8, F9, F10, G6, G11, H5, H6, H11, J6, J11, J12, K6, K11, L7, L8, L9, L10, M8, M9 | A11, B10, C6, C14, D13, D17, F2, J19, L4, P15, T18, U8, U14, V2, V9, V11 |
| GND | 3, 17, 33, 52, 57, 59, 64, 85, 105, 124, 129, 135 | 14, 32, 50, 72, 75, 82, 94, 134, 152, 174, 180, 185, 200 | E5, F6, F11, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, L6, L11 | E5, E7, E8, E9, E10, E11, E12, E13, G5, G15, H5, H15, J5, J15, K5, K15, L5, L15, M5, M15, N5, N15, R7, R8, R9, R10, R11, R12, R13 |
| No Connects | - | 1, 2, 51, 52, 53, 54, 103, 104, 105, 106, 155, 156, 157, 158, 207, 208 | A1, A2, A3, A15, A16, B1, B2, B3, B14, B15, B16, C2, C3, C4, C14, C15, D4, D5, D10, D13, D14, E12, F5, G3, H3, L4, M5, M6, M12, M13, N4, N5, N13, N14, P2, P3, P4, P13, P14, P16, R2, R3, R15, R16, T2, T3, T15, T16 | A1, A2, A3, A8, A9, A19, B2, B3, B4, B14, B15, B16, C1, C2, C4, C15, C17, C18, C19, D3, D4, D5, D8, D9, D16, D18, D19, E16, E17, F1, F16, G18, H4, J1, J4, K1, K19, M2, M19, N4, P5, P17, P19, R1, R5, T1, T2, T4, T19, U3, U16, U17, U18, V3, V4, V8, V10, V12, V14, V17, V18, V19, W1, W2, W8, W9, W13, W16, W18, W19 |

Notes:

1. Port Enable is brought High to enable JTAG pins when JTAG pins are used as I/O. See family data sheet ([DS012](#)) for full explanation.

Device Part Marking and Ordering Combination Information



| Device Ordering and Part Marking Number | Speed (pin-to-pin delay) | Pkg. Symbol | No. of Pins | Package Type | Operating Range ⁽¹⁾ |
|---|--------------------------|-------------|-------------|--|--------------------------------|
| XCR3256XL-7TQ144C | 7.5 ns | TQ144 | 144-pin | Thin Quad Flat Pack (TQFP) | C |
| XCR3256XL-7TQG144C | 7.5 ns | TQG144 | 144-pin | Thin Quad Flat Pack (TQFP); Pb-Free | C |
| XCR3256XL-7PQ208C | 7.5 ns | PQ208 | 208-pin | Plastic Quad Flat Pack (PQFP) | C |
| XCR3256XL-7PQG208C | 7.5 ns | PQG208 | 208-pin | Plastic Quad Flat Pack (PQFP); Pb-Free | C |
| XCR3256XL-7FT256C | 7.5 ns | FT256 | 256-ball | Fine-Pitch BGA (FT) | C |
| XCR3256XL-7CS280C | 7.5 ns | CS280 | 280-ball | Chip Scale Package (CSP) | C |
| XCR3256XL-7CSG280C | 7.5 ns | CSG280 | 280-ball | Chip Scale Package (CSP); Pb-Free | C |
| XCR3256XL-10TQ144C | 10 ns | TQ144 | 144-pin | Thin Quad Flat Pack (TQFP) | C |
| XCR3256XL-10TQG144C | 10 ns | TQG144 | 144-pin | Thin Quad Flat Pack (TQFP); Pb-Free | C |
| XCR3256XL-10PQ208C | 10 ns | PQ208 | 208-pin | Plastic Quad Flat Pack (PQFP) | C |
| XCR3256XL-10PQG208C | 10 ns | PQG208 | 208-pin | Plastic Quad Flat Pack (PQFP); Pb-Free | C |
| XCR3256XL-10FT256C | 10 ns | FT256 | 256-ball | Fine-Pitch BGA (FT) | C |
| XCR3256XL-10CS280C | 10 ns | CS280 | 280-ball | Chip Scale Package (CSP) | C |
| XCR3256XL-10CSG280C | 10 ns | CSG280 | 280-ball | Chip Scale Package (CSP); Pb-Free | C |
| XCR3256XL-10TQ144I | 10 ns | TQ144 | 144-pin | Thin Quad Flat Pack (TQFP) | I |
| XCR3256XL-10TQG144I | 10 ns | TQG144 | 144-pin | Thin Quad Flat Pack (TQFP); Pb-Free | I |
| XCR3256XL-10PQ208I | 10 ns | PQ208 | 208-pin | Plastic Quad Flat Pack (PQFP) | I |
| XCR3256XL-10PQG208I | 10 ns | PQG208 | 208-pin | Plastic Quad Flat Pack (PQFP); Pb-Free | I |
| XCR3256XL-10FT256I | 10 ns | FT256 | 256-ball | Fine-Pitch BGA (FT) | I |
| XCR3256XL-10CS280I | 10 ns | CS280 | 280-ball | Chip Scale Package (CSP) | I |
| XCR3256XL-10CSG280I | 10 ns | CSG280 | 280-ball | Chip Scale Package (CSP); Pb-Free | I |
| XCR3256XL-12TQ144C | 12 ns | TQ144 | 144-pin | Thin Quad Flat Pack (TQFP) | C |
| XCR3256XL-12TQG144C | 12 ns | TQG144 | 144-pin | Thin Quad Flat Pack (TQFP); Pb-Free | C |
| XCR3256XL-12PQ208C | 12 ns | PQ208 | 208-pin | Plastic Quad Flat Pack (PQFP) | C |
| XCR3256XL-12PQG208C | 12 ns | PQG208 | 208-pin | Plastic Quad Flat Pack (PQFP); Pb-Free | C |

| Device Ordering and Part Marking Number | Speed (pin-to-pin delay) | Pkg. Symbol | No. of Pins | Package Type | Operating Range ⁽¹⁾ |
|---|--------------------------|-------------|-------------|--|--------------------------------|
| XCR3256XL-12FT256C | 12 ns | FT256 | 256-ball | Fine-Pitch BGA (FT) | C |
| XCR3256XL-12CS280C | 12 ns | CS280 | 280-ball | Chip Scale Package (CSP) | C |
| XCR3256XL-12CSG280C | 12 ns | CSG280 | 280-ball | Chip Scale Package (CSP); Pb-Free | C |
| XCR3256XL-12TQ144I | 12 ns | TQ144 | 144-pin | Thin Quad Flat Pack (TQFP) | I |
| XCR3256XL-12TQG144I | 12 ns | TQG144 | 144-pin | Thin Quad Flat Pack (TQFP); Pb-Free | I |
| XCR3256XL-12PQ208I | 12 ns | PQ208 | 208-pin | Plastic Quad Flat Pack (PQFP) | I |
| XCR3256XL-12PQG208I | 12 ns | PQG208 | 208-pin | Plastic Quad Flat Pack (PQFP); Pb-Free | I |
| XCR3256XL-12FT256I | 12 ns | FT256 | 256-ball | Fine-Pitch BGA (FT) | I |
| XCR3256XL-12CS280I | 12 ns | CS280 | 280-ball | Chip Scale Package (CSP) | I |
| XCR3256XL-12CSG280I | 12 ns | CSG280 | 280-ball | Chip Scale Package (CSP); Pb-Free | I |

Notes:

1. C = Commercial: $T_A = 0^\circ$ to $+70^\circ\text{C}$; I = Industrial: $T_A = -40^\circ$ to $+85^\circ\text{C}$

Warranty Disclaimer

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Additional Information

[CoolRunner XPLA3 Data Sheets and Application Notes](#) [Device Packages](#)

[Device Package User Guide](#)

Revision History

The following table shows the revision history for this document

| Date | Version | Revision |
|----------|---------|--|
| 01/21/00 | 1.0 | Initial Xilinx release. |
| 02/10/00 | 1.1 | Updated Pinout table. |
| 05/03/00 | 1.2 | Minor updates and added Boundary Scan to pinout table. |
| 11/20/00 | 1.3 | Updated pinout tables; corrected note in Table 4 to read: "port enable pin is brought High". |
| 12/11/00 | 1.4 | Updated specifications and pinout tables. |
| 01/17/01 | 1.5 | Removed Timing Model. |
| 03/05/01 | 1.6 | Added 256-ball Fine-Pitch Ball Grid Array Package. |
| 04/11/01 | 1.7 | Added Typical I/V curve, Figure 2 ; added Table 2 : Total User I/O; changed V_{OH} spec. |
| 04/19/01 | 1.8 | Updated Typical I/V curve, Figure 2 : added voltage levels. |

| Date | Version | Revision |
|----------|---------|---|
| 01/08/02 | 1.9 | Moved ICC vs Freq. Figure 1 and Table 1 to page 1. Added single p-term setup time (T_{SU1}) to AC Table, renamed T_{SU} to T_{SU2} for setup time through the OR array. Updated T_{SUF} spec to match software timing. Added T_{INIT} spec. Updated T_{CONFIG} spec. Updated T_{HI} spec to correct a typo. Updated AC Load Circuit diagram to more closely resemble true test conditions, added note for T_{POD} delay measurement. |
| 11/20/02 | 2.0 | Updated T_{PCO} (added T_{PTCK}), T_{FIN} , and T_{OUT} to match timing model and software. Updated the following specs based on characterization of product after move to UMC fabrication: f_{SYSTEM} , V_{OH} , T_{CONFIG} , T_{INIT} , T_{LOGI3} , T_F . Updated Typical I_{CC} vs. Freq. and Derating Curve for T_{PD2} (improved to 6.5 ns for 16 outputs switching) per new characterization data. Updated ordering information to new format. |
| 01/27/03 | 2.1 | Moved incorrect note for V_{OH} to line 2 from line 3 in DC table. |
| 07/15/03 | 2.2 | Updated test conditions for I_{IL} and I_{IH} . |
| 08/21/03 | 2.3 | Updated Package Device Marking Pin 1 orientation. |
| 11/5/03 | 2.4 | Updated from Preliminary Product Specification to Product Specification. |
| 02/13/04 | 2.5 | Add T_{sol} specification. Add links to application notes and data sheets. |
| 04/08/05 | 2.6 | Added I_{CCSB} Typical and T_{APRPW} specifications. Removed T_{SOL} specification. |
| 03/31/06 | 2.7 | Added Warranty Disclaimer. Added Pb-Free ordering information. |

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