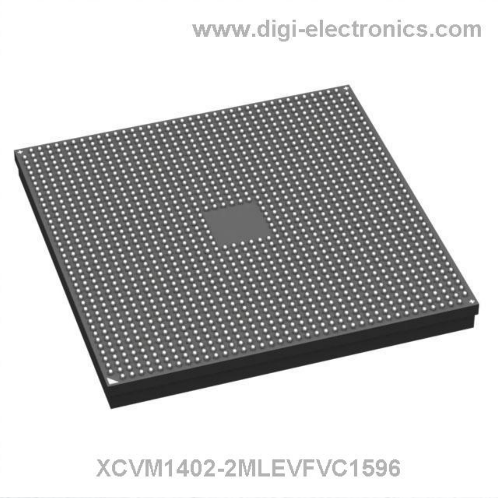
XCVM1402-2MLEVFVC1596 Datasheet



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DiGi Electronics Part Number	XCVM1402-2MLEVFVC1596-DG
Manufacturer	AMD
Manufacturer Product Number	XCVM1402-2MLEVFVC1596
Description	IC VERSALPRIME ACAP FPGA 1596BGA
Detailed Description	Dual ARM® Cortex®-A72 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5F with CoreSight™ System On Chip (SOC) IC Versal™ Prime Versal™ Prime FPGA, 1.2M Logic Cells 600MHz, 1.4GHz 1596-BGA (37.5x37.5)

Tel: +00 852-30501935
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Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
XCVM1402-2MLEVFVC1596	AMD
Series:	Product Status:
Versal™ Prime	Active
Architecture:	Core Processor:
MPU, FPGA	Dual ARM® Cortex®-A72 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5F w
Flash Size:	RAM Size:
-	-
Peripherals:	Connectivity:
DDR, DMA, PCIe	CANbus, EBI/EMI, Ethernet, I2C, MMC/SD/SDIO, SPI, UART/USART, USB OTG
Speed:	Primary Attributes:
600MHz, 1.4GHz	Versal™ Prime FPGA, 1.2M Logic Cells
Operating Temperature:	Package / Case:
0°C ~ 100°C (TJ)	1596-BFBGA
Supplier Device Package:	Number of I/O:
1596-BGA (37.5x37.5)	748

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	4 (72 Hours)

Versal Architecture and Product Data Sheet: Overview

DS950 (v2.7) November 10, 2025 **Product Specification**

General Description

AMD Versal™ adaptive SoCs combine adaptable processing and acceleration engines with programmable logic and configurable connectivity to enable customized, heterogeneous hardware solutions for a wide variety of applications across many markets. The devices include transformational features like an integrated silicon host interconnect shell, AI Engines, programmable logic, and processing system, providing superior performance/watt over conventional FPGAs, CPUs, and GPUs.

AI Edge Series Gen 2: Enhancing the production-proven Versal architecture, this series supports flexible, real-time preprocessing, efficient AI inference, and high-performance postprocessing—reducing area and complexity.

AI Edge Series: Designed with safety in mind, this series delivers an adaptive technology platform that combines high AI inference performance, low latency, and power efficiency for edge applications.

AI Core Series: The high-compute series with medium density programmable logic and connectivity capability coupled with AI and DSP acceleration engines.

Prime Series Gen 2: Delivering performance and efficiency for video, control, and software-defined applications, this series combines a high-performance processing system, enhanced functional safety and security features, and an expanded suite of hard IP.

Prime Series: A mid-range series with medium density programmable logic, signal processing, and connectivity capability.

Premium Series Gen 2: A heterogeneous compute platform engineered to help users reach high levels of acceleration for a wide range of compute-intensive workloads by providing high compute density, custom memory hierarchy, and DSP Engine resources.

Premium Series: The high-end, high bandwidth series, rich in networking interfaces, security engines, and providing high compute density.

HBM Series: For memory-bound, compute-intensive applications, the series features heterogeneous integration of 3D IC memory, secure connectivity, and adaptive compute to eliminate performance bottlenecks.

RF Series: This series integrates high-frequency, high sample-rate RF-sampling data converters with integrated signal processing IP for high-performance RF systems.

Series Comparisons

Table 1: **Device Resources**

Resources and Capabilities	AI Edge Series Gen 2	AI Edge Series	AI Core Series	Prime Series Gen 2	Prime Series	Premium Series Gen 2	Premium Series	HBM Series	RF Series
Programmable Network on Chip (NoC)	✓	✓	✓	✓	✓	✓	✓	✓	✓
System Logic Cells (K)	207–1,188	44–1,139	815–1,968	207–1,188	329–2,233	1,408–3,273	833–18,507	3,837–5,631	1,205–2,474
Hierarchical Memory (Mb)	21–97	40–177	91–191	21–97	54–282	145–327	128–1,116	509–752	156–189
DSP Engines	184–2,064	90–1,312	984–1,968	184–2,064	464–3,984	3,332–7,616	1,140–14,352	7,392–10,848	2,256–3,976
AI Engines	24–144	8–304	152–400	–	–	–	0–472	–	120–126
Serial Transceivers	8–24	0–44	32–44	8–24	8–48	24–72	44–168	88–128	8–20
Max. Serial Bandwidth (full duplex) (Tb/s)	1.4	2.5	2.5	1.4	7.8	14.6	17.6	11.2	2.3
I/O	356–634	192–608	446–770	356–634	316–770	380–788	132–2,494	780	452–548
Memory Controllers	3–5	1–3	3–4	3–5	1–4	4–8	2–16	4	4
HBM (GB)	–	–	–	–	–	–	–	8–32	–
Graphics Processor Unit (GPU)	✓	–	–	✓	–	–	–	–	–
Video Codec Unit (VCU)	✓	–	–	✓	–	–	–	–	–
Image Signal Processor (ISP)	✓	–	–	–	–	–	–	–	–
RF-ADCs / RF-DACs	–	–	–	–	–	–	–	–	✓
LDPC Decoder	–	–	–	–	–	✓	–	–	✓
FFT/iFFT	–	–	–	–	–	–	–	–	✓
1 GSPS Channelizer	–	–	–	–	–	–	–	–	✓
Poly Block	–	–	–	–	–	–	–	–	✓

Summary of Features

Architecture

Versal adaptive SoCs are built around an integrated shell composed of a programmable network on chip (NoC), which enables seamless memory-mapped access to the full height and width of the device. Devices comprise: a multicore scalar processing system; an integrated block for PCIe® with DMA and Cache Coherent Interconnect Designs (CPM); SIMD VLIW AI Engine accelerators for artificial intelligence and complex signal processing; and programmable logic (PL). The platform management controller, adjacent to the processing system, is responsible for booting and configuring the device. Versal devices typically have I/O and memory controllers on the north and south edges of the device and serial transceivers on the east and west edges. The NoC spans the full height and width of the device.

Compute and Acceleration

Some Versal adaptive SoCs have an array of signal processing cores that are highly optimized for functions in machine learning, convolutional neural networks, wireless radio, backhaul, cable, and radar applications. The array consists of a number of AI Engines, each comprising a 32-bit scalar RISC processor, fixed and floating point vector units, data memory, and interconnect. AI Engines can be used as a single tile, as the complete array, or at any granularity in between. The creation of custom acceleration and compute engines in the AI Engine array is done at a high-level through C and C++.

Every Versal device has an Arm®-based processing system, comprising application processors and real-time processors. The processing system includes a number of peripherals for communication standards and can communicate with DDR memory via the programmable NoC as well as on-chip memory and local cache.

The PL is made up of configurable logic blocks, containing 6-input look-up tables (LUTs) and flip-flops; different-sized memory blocks; 36 Kb block RAM and 288 Kb UltraRAM; multiport RAM (MPRAM); digital signal processing (DSP) blocks; and a wealth of interconnect, switches, and muxes to connect blocks together. All resources are arranged in columns. The PL is divided into regions that are a fixed height. Each region has its own clocking capabilities and NoC access points.

Platform Management

The platform management controller resides adjacent to, but is independent from, the processing system. It is responsible for the boot and configuration of the device from the primary boot source. The platform management controller is also responsible for configuring the PL, which can be configured before or after the processing system. It also controls encryption, authentication, system monitoring, and device debug capabilities of the platform.

Connectivity

The south edge of the Versal devices typically contains a number of I/O banks and associated memory controllers to read from and write to DDR4, LPDDR4, DDR5, LPDDR5, and LPDDR5X memory. I/O can be used independently from the dedicated memory controllers for many functions, including any with soft memory controllers created in the PL. The east and west edges of the device typically contain serial transceivers capable of communicating up to 112 Gb/s. The PL can also contain integrated blocks for high-value functions, such as the integrated block for PCIe (PL PCIE), multirate Ethernet MAC, 600G Ethernet MAC, 600G Interlaken, and 400G High-Speed Crypto (HSC) Engine.

Versal RF Series includes high-performance RF-sampling ADCs and DACs that are monolithically integrated as hard IP tiles, providing a low power consumption and latency data interface between the converters and programmable logic. The RF data converters support input and output frequencies up to K_u band and direct sample at high sample rates to provide wide band sampling. In addition to the RF sampling, RF-ADCs and RF-DACs include additional digital processing logic such as programmable filters, digital-up converter (DUC) and digital-down converter (DDC).

Resource and Packaging Information

Versal AI Edge Series Gen 2

Table 2: **Versal AI Edge Series Gen 2: Resources**

	2VE3304	2VE3358	2VE3504	2VE3558	2VE3804	2VE3858
AI Engine-ML v2 Tiles	24	24	96	96	144	144
AIE-ML v2 Data Memory (Mb)	12	12	48	48	72	72
AIE-ML v2 Shared Memory (Mb)	48	48	96	96	288	288
DSP Engines	184	184	700	700	2,064	2,064
Maximum DSP Cascade	92	92	164	164	188	188
System Logic Cells	206,920	206,920	492,188	492,188	1,188,040	1,188,040
CLB Flip Flops	189,184	189,184	450,000	450,000	1,086,208	1,086,208
LUTs	94,592	94,592	225,000	225,000	543,104	543,104
Distributed RAM (Mb)	2.9	2.9	6.9	6.9	16.6	16.6
Block RAM Blocks	141	141	388	388	1,342	1,342
Block RAM (Mb)	5	5	13.6	13.6	47.2	47.2
UltraRAM Blocks	47	47	12	12	118	118
UltraRAM (Mb)	13.2	13.2	3.4	3.4	33.2	33.2
MMCM	5	5	6	6	8	8
APU	Arm® Cortex®-A78AE; 64 KB I w/parity & D w/ECC L1 Cache; 512 KB L2 Cache; 1 MB L3 Cache (per 2-core cluster); CMN600 w/4 MB System-Level Cache (shared)					
RPU	Arm Cortex-R52; 32 KB L1 Cache w/ECC; 128 KB TCM w/ECC					
Memory	2 MB On-Chip Memory w/ECC					
High-Speed Connectivity	PCI Express® Gen5 x4[(1)]; USB 3.2; DisplayPort™ 1.4; 10G Ethernet; 1G Ethernet; UFS 3.1					
General Connectivity	CAN/CAN-FD; SPI; UART; USB 2.0; I2C/I3C; GPIO					
NoC to PL Master / Slave Ports	5/4	5/4	10/7	10/7	30/24	30/24
DDR Bus Width	96	96	128	128	160	160
DDR Memory Controllers (DDRMC5E)	3	3	4	4	5	5
PCIe (PL PCIE5)	1 x Gen5 x4	1 x Gen5 x4	3 x Gen5 x4	3 x Gen5 x4	4 x Gen5 x4	4 x Gen5 x4
100G Multirate Ethernet MAC	1	1	1	1	3	3
GTYP Transceivers (PL only)	4	4	12	12	20	20
PS-Dedicated Transceivers[(2)]	4 x GTYP 4 x GTR	4 x GTYP 4 x GTR	4 x GTYP 4 x GTR	4 x GTYP 4 x GTR	4 x GTYP 4 x GTR	4 x GTYP 4 x GTR
GPU Cores (Arm Mali-G78AE)	4	4	4	4	4	4
Video Codec Unit (VCU)	-	1	-	1	-	1
Image Signal Processor	-	1	-	3	-	3

Notes:

1. PS-dedicated PCIe Gen 5 support is provided by the MDB5 hard IP block.
2. PS-dedicated transceivers connectivity: GTYP: 10G Ethernet, PCI Express, and HSDP; GTR: USB and DisplayPort.

Table 3: **Versal AI Edge Series Gen 2: Device-Package Combinations and Maximum I/O**

	2VE3304	2VE3358	2VE3504	2VE3558	2VE3804	2VE3858
	X5IO DDR Only, X5IO DDR+PL, X5IO PL Only HDIO, MIO GTYP (PL Only), GTYP (PS Only), GTR					
SFVA1089	176, 48, 32 22, 78 4, 4, 4	176, 48, 32 22, 78 4, 4, 4				
SFVA1440		168, 64, 32 44, 78 4, 4, 4		192, 136, 0 88, 78 4, 4, 4		
SSVA1440	168, 64, 32 44, 78 4, 4, 4	168, 64, 32 44, 78 4, 4, 4	192, 136, 0 88, 78 4, 4, 4	192, 136, 0 88, 78 4, 4, 4		
SSVA2112			232, 152, 0 44, 78 12, 4, 4	232, 152, 0 44, 78 12, 4, 4	208, 272, 32 44, 78 20, 4, 4	208, 272, 32 44, 78 20, 4, 4

Versal AI Edge Series

Table 4: **Versal AI Edge Series: Resources**

	VE2002	VE2102	VE2202	VE2302	VE1752	VE2602	VE2802
AI Engines-ML (AIE-ML)	8	12	24	34	0	152	304
AI Engines (AIE)	0	0	0	0	304	0	0
AIE/AIE-ML Data Memory (Mb)	4	6	12	17	76	76	152
AIE-ML Shared Memory (Mb)	48	48	68	68	0	304	304
DSP Engines	90	176	324	464	1,312	984	1,312
Maximum DSP Cascade	44	44	116	116	164	164	164
System Logic Cells	43,750	80,080	229,688	328,720	981,120	820,313	1,139,040
CLB Flip-Flops	40,000	73,216	210,000	300,544	897,024	750,000	1,041,408
LUTs	20,000	36,608	105,000	150,272	448,512	375,000	520,704
Distributed RAM (Mb)	0.6	1.1	3.2	4.6	13.7	11.4	15.9
Block RAM Blocks	24	47	108	155	954	476	600
Block RAM (Mb)	0.8	1.7	3.8	5.4	33.5	16.7	21.1
UltraRAM Blocks	24	47	108	155	462	224	264
UltraRAM (Mb)	6.8	13.2	30.4	43.6	129.9	63.0	74.3
Accelerator RAM (Mb)	32	32	32	32	0	0	0
MMCM	4	4	4	4	9	9	9
APU	Dual-core Arm Cortex-A72; 48 KB/32 KB L1 Cache w/ parity & ECC; 1 MB L2 Cache w/ ECC						
RPU	Dual-core Arm Cortex-R5F; 32 KB/32 KB L1 Cache; 256 KB TCM w/ECC						
Memory	256 KB On-Chip Memory w/ECC						
Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)						
NoC to PL Master / Slave Ports	2/2	2/2	5/5	5/5	21/21	21/21	21/21
DDR Bus Width	64	64	64	64	192	192	192
DDR Memory Controllers (DDRMC)	1	1	1	1	3	3	3
PCIe w/DMA (CPM4)	–	–	–	–	1 x Gen4x16	–	–
PCIe w/DMA (CPM5)	–	–	–	–	–	1 x Gen4x16	1 x Gen4x16
PCIe (PL PCIE4)	–	–	1 x Gen4x8	1 x Gen4x8	4 x Gen4x8	–	–
PCIe (PL PCIE5)	–	–	–	–		4 x Gen4x8	4 x Gen4x8
40G Multirate Ethernet MAC	0	0	1	1	2	2	2
GTY Transceivers(1)	0	0	0	0	44	0	0
GTYP Transceivers(1)	0	0	8	8	0	32(2)	32(2)
Video Decoder Engines (VDEs)	–	–	–	–	–	2	4

Notes:

1. Refer to DC and AC switching characteristics data sheet for performance per speed grade.
2. 16 GTYP transceivers are dedicated to CPM5 for PCI Express use.

Table 5: **Versal AI Edge Series: Device-Package Combinations and Maximum I/O**

	VE2002	**VE2102**	**VE2202**	**VE2302**	**VE1752**	**VE2602**	**VE2802**
	XPIO DDR Only, XPIO DDR+PL, XPIO PL Only HDIO, MIO GTY, GTYP						
SBVA484	108, 0, 54 0, 78 0, 0	108, 0, 54 0, 78 0, 0					
SBVA625	132, 30, 54 0, 78 0, 0	132, 30, 54 0, 78 0, 0					
SFVA784	132, 30, 54 0, 78 0, 0	132, 30, 54 0, 78 0, 0	132, 30, 54 22, 78 0, 8	132, 30, 54 22, 78 0, 8			
NSVG1369					132, 246, 0 44, 78 24, 0		
NSVH1369						132, 192, 0 44, 78 0, 32	132, 192, 0 44, 78 0, 32
VSVA1596					192, 186, 0 44, 78 32, 0		
VSVH1760						186, 300, 0 44, 78 0, 32	186, 300, 0 44, 78 0, 32
VSVA2197					192, 294, 0 44, 78 44, 0		

Versal AI Core Series

Table 6: **Versal AI Core Series: Resources**

	VC1502	VC1702	VC1802	VC1902	VC2602	VC2802
AI Engines (AIE)	198	304	300	400	0	0
AI Engines-ML (AIE-ML)	0	0	0	0	152	304
AIE/AIE-ML Data Memory (Mb)	50	76	75	100	76	152
AIE-ML Shared Memory (Mb)	0	0	0	0	304	304
DSP Engines	1,032	1,312	1,600	1,968	984	1,312
Maximum DSP Cascade	164	164	164	164	164	164
System Logic Cells	814,520	981,120	1,585,938	1,968,400	820,313	1,139,040
CLB Flip-Flops	744,704	897,024	1,450,000	1,799,680	750,000	1,041,408
LUTs	372,352	448,512	725,000	899,840	375,000	520,704
Distributed RAM (Mb)	11.3	13.7	22.1	27.5	11.4	15.9
Block RAM Blocks	848	954	800	967	476	600
Block RAM (Mb)	29.8	33.5	28.1	34.0	16.7	21.1
UltraRAM Blocks	390	462	325	463	224	264
UltraRAM (Mb)	109.7	129.9	91.4	130.2	63.0	74.3
Accelerator RAM (Mb)	0	0	0	0	0	0
MMCM	9	9	12	12	9	9
APU	Dual-core Arm Cortex-A72; 48 KB/32 KB L1 Cache w/ parity & ECC; 1 MB L2 Cache w/ ECC					
RPU	Dual-core Arm Cortex-R5F; 32 KB/32 KB L1 Cache; TCM w/ECC					
Memory	256 KB On-Chip Memory w/ECC					
Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)					
NoC to PL Master / Slave Ports	21/21	21/21	28/28	28/28	21/21	21/21
DDR Bus Width	192	192	256	256	192	192
DDR Memory Controllers (DDRMC)	3	3	4	4	3	3
PCIe w/DMA (CPM4)	1 x Gen4x16	1 x Gen4x16	1 x Gen4x16	1 x Gen4x16	–	–
PCIe w/DMA (CPM5)	–	–	–	–	2 x Gen5x8	2 x Gen5x8
PCIe (PL PCIE4)	4 x Gen4x8	4 x Gen4x8	4 x Gen4x8	4 x Gen4x8	–	–
PCIe (PL PCIE5)	–	–	–	–	4 x Gen5x4	4 x Gen5x4
100G Multirate Ethernet MAC	3	4	4	4	2	2
GTY Transceivers[1]	32	44	44	44	0	0
GTYP Transceivers[1]	0	0	0	0	32[2]	32[2]
Video Decoder Engines (VDEs)	–	–	–	–	2	4

Notes:

1. Refer to DC and AC switching characteristics data sheet for performance per speed grade.
2. 16 GTYP transceivers are dedicated to CPM5 for PCI Express use.

Table 7: **Versal AI Core Series: Device-Package Combinations and Maximum I/O**

	VC1502	VC1702	VC1802	VC1902	VC2602	VC2802
	XPIO DDR Only, XPIO DDR+PL, XPIO PL Only HDIO, MIO GTY, GTYP					
NSVG1369	132, 246, 0 22, 78 24, 0	132, 246, 0 44, 78 24, 0				
NSVH1369					132, 192, 0 44, 78 0, 32	132, 192, 0 44, 78 0, 32
VIVA1596			132, 246, 0 44, 78 32, 0	132, 246, 0 44, 78 32, 0		
VSVA1596	132, 246, 0 22, 78 32, 0	132, 246, 0 44, 78 32, 0				
VSVD1760			186, 462, 0 0, 78 24, 0	186, 462, 0 0, 78 24, 0		
VSVH1760					186, 300, 0 44, 78 0, 32	186, 300, 0 44, 78 0, 32
VSVA2197	192, 294, 0 22, 78 32, 0	192, 294, 0 44, 78 44, 0	186, 462, 0 44, 78 44, 0	186, 462, 0 44, 78 44, 0		

Versal Prime Series Gen 2

Table 8: **Versal Prime Series Gen 2: Resources**

		2VM3358	2VM3558	2VM3654	2VM3858
#Application Cores / #Real-Time Cores		8/10	8/10	4/6	8/10
Application Cores	Core Details	Arm® Cortex®-A78AE; 64 KB I w/parity & D w/ECC L1 Cache; 512 KB L2 Cache			
	Cores Per Cluster / #Clusters	2/4	2/4	4/1	2/4
	L3 Cache Per Cluster (MB)	1	1	2	1
	System-Level Cache (MB)	4	4	–	4
Real-Time Cores	Core Details	Arm Cortex-R52; 32 KB L1 Cache w/ECC; 128 KB TCM w/ECC			
	Cores Per Cluster / #Clusters	2/5	2/5	2/3	2/5
On-Chip Memory w/ECC (MB)		2	2	1	2
High-Speed Connectivity		PCI Express® Gen5 x4;(1)(2) USB 3.2; DisplayPort 1.4; 10G Ethernet; 1G Ethernet; UFS 3.1			
General Connectivity		CAN/CAN-FD; SPI; UART; USB 2.0; I2C/I3C; GPIO			
System Logic Cells		206,920	492,188	695,800	1,188,040
CLB Flip Flops		189,184	450,000	636,160	1,086,208
LUTs		94,592	225,000	318,080	543,104
DSP Engines		184	700	1,428	2,064
Maximum DSP Cascade		92	164	166	188
NoC to PL Master / Slave Ports		5/4	10/7	11/7	30/24
Distributed RAM (Mb)		2.9	6.9	9.7	16.6
Block RAM Blocks		141	388	631	1,342
Block RAM (Mb)		5	13.6	22.2	47.2
UltraRAM Blocks		47	12	83	118
UltraRAM (Mb)		13.2	3.4	23.3	33.2
Total PL Memory (Mb)		21.1	23.9	55.2	97.0
MMCM		5	6	4	8
DDR Memory Controllers (DDRMC5E)		3	4	1	5
DDR Memory Controllers (DDRMC5X)		–	–	3	–
Total DDR Bus Width		96	128	128	160
GPU Cores (Arm Mali™-G78AE)		4	4	1	4
Video Codec Unit (VCU)		1	1	2	1
GTYP Transceivers (PL only)		4	12	24	20
PS-Dedicated Transceivers(3)		4 x GTYP, 4 x GTR	4 x GTYP, 4 x GTR	4 x GTYP, 4 x GTR	4 x GTYP, 4 x GTR
PCIe (PL PCIE5)		1 x Gen5 x4	3 x Gen5 x4	2 x Gen5 x4	4 x Gen5 x4
100G Multirate Ethernet MAC		1	1	2	3
High-Speed Crypto Engines		–	–	1	–

Notes:

1. The 2VM3654 offers 1 x PS-based PCIe Gen5 controllers. All other devices offer 2 x PCIe Gen5 controllers.
2. PS-dedicated PCIe Gen 5 support is provided by the MDB5 hard IP block.
3. PS-dedicated transceivers connectivity: GTYP: 10G Ethernet, PCI Express, and HSDP; GTR: USB and DisplayPort.

Table 9: **Versal Prime Series Gen 2: Device-Package Combinations and Maximum I/O**

	2VM3358	**2VM3558**	**2VM3654**	**2VM3858**
	X5IO DDR Only, X5IO DDR+PL, X5IO PL Only HDIO, MIO GTYP (PL Only), GTYP (PS Only), GTR			
SFVA1089	176, 48, 32 22, 78 4, 4, 4			
SSVA1440	168, 64, 32 44, 78 4, 4, 4	192, 136, 0 88, 78 4, 4, 4		
SFVA1221			56, 168, 0 0, 78 12, 4, 4	
SFVK1760			104, 184, 0 22, 78 24, 4, 4	
SSVA2112		232, 152, 0 44, 78 12, 4, 4	104, 184, 0 22, 78 20, 4, 4	208, 272, 32 44, 78 20, 4, 4

Versal Prime Series

Table 10: **Versal Prime Series: Resources**

	VM1102	VM1302	VM1402	VM1502	VM1802	VM2152	VM2202	VM2302	VM2502	VM2902
System Logic Cells	328,720	703,360	1,237,600	981,120	1,968,400	757,120	1,139,040	1,574,720	1,969,240	2,233,280
CLB Flip-Flops	300,544	643,072	1,131,520	897,024	1,799,680	692,224	1,041,408	1,439,744	1,800,448	2,041,856
LUTs	150,272	321,536	565,760	448,512	899,840	346,112	520,704	719,872	900,224	1,020,928
Distributed RAM (Mb)	4.6	9.8	17.3	13.7	27.5	10.6	15.9	22.0	27.5	31.2
Block RAM Blocks	155	503	1,150	954	967	759	600	1,405	1,341	1,981
Block RAM (Mb)	5.4	17.7	40.4	33.5	34.0	26.7	21.1	49.4	47.1	69.6
UltraRAM Blocks	155	179	286	462	463	191	264	453	677	645
UltraRAM (Mb)	43.6	50.3	80.4	129.9	130.2	53.7	74.3	127.4	190.4	181.4
Accelerator RAM (Mb)	32	–	–	–	–	–	–	–	–	–
DSP Engines	464	848	1,696	1,312	1,968	1,704	1,312	1,904	3,984	2,672
Maximum DSP Cascade	116	212	212	164	164	142	164	238	166	334
MMCM	4	8	12	9	12	6	9	9	13	9
APU	Dual-core Arm Cortex-A72; 48 KB/32 KB L1 Cache w/ parity & ECC; 1 MB L2 Cache w/ ECC									
RPU	Dual-core Arm Cortex-R5F; 32 KB/32 KB L1 Cache; TCM w/ECC									
Memory	256 KB On-Chip Memory w/ECC									
Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)									
NoC to PL Master / Slave Ports	5/5	9/9	18/18	21/21	28/25	16/12	21/21	30/30	28/28	42/42
DDR Bus Width	64	128	256	192	256	128	192	192	256	192
DDR4 Memory Controllers (DDRMC)	1	2	4	3	4	–	3	3	4	2
DDR5 Memory Controllers (DDRMC5C)	–	–	–	–	–	4	–	–	–	–
PCIe w/DMA (CPM4)	–	1 x Gen4x16	1 x Gen4x16	1 x Gen4x16	1 x Gen4x16	–	–	–	–	–
PCIe w/DMA (CPM5)	–	–	–	–	–	–	2 x Gen5x8	–	2 x Gen5x8	–
PCIe (PL PCIE4)	–	2 x Gen4x8	2 x Gen4x8	4 x Gen4x8	4 x Gen4x8	–	–	–	–	–
PCIe (PL PCIE5)	1 x Gen4x8	–	–	–	–	2 x Gen5x4	4 x Gen5x4	2 x Gen5x4	–	2 x Gen5x4
100G Multirate Ethernet MAC	1	2	2	4	4	2	2	6	–	6
600G Ethernet MAC	–	–	–	–	–	1	–	–	–	–
High-Speed Crypto Engines	–	–	–	–	–	1	–	–	–	–
GTY Transceivers(1)	–	24	24	44	44	–	–	–	–	–
GTYP Transceivers(1)	8	–	–	–	–	8	32(2)	8	16(2)	8
GTM Transceivers(1) 58 Gb/s (112 Gb/s)	–	–	–	–	–	8 (4)	–	36 (0)	–	36 (0)

Notes:
1. Refer to DC and AC switching characteristics data sheet for performance per speed grade.
2. 16 GTYP transceivers are dedicated to CPM5 for PCI Express use.

Table 11: **Versal Prime Series: Device-Package Combinations and Maximum I/O**

	VM1102	VM1302	VM1402	VM1502	VM1802	VM2152	VM2202	VM2302	VM2502	VM2902
	XPIO DDR Only, XPIO DDR+PL, XPIO PL Only HDIO, MIO GTY, GTYP, GTM (112G)					X5IO: DDR Only, DDR+PL, PL Only HDIO, MIO GTY, GTYP, GTM (112G)	XPIO DDR Only, XPIO DDR+PL, XPIO PL Only HDIO, MIO GTY, GTYP, GTM (112G)			
SFVA784	132, 30, 54 22, 78 0, 8, 0									
NBVB1024		132, 84, 0 22, 78 16, 0, 0	132, 192, 0 22, 78 16, 0, 0							
NFVD1024						136, 120, 0 22, 78 0, 8, 8 (4)				
NFVB1369				132, 246, 0 22, 78 16, 0, 0						
NSVF1369		168, 156, 0 22, 78 8, 0, 0	168, 480, 0 22, 78 8, 0, 0							
NSVH1369							132, 192, 0 44, 78 0, 32, 0			
NFVM1369						136, 248, 0 44, 78 0, 8, 8 (4)				
VFVC1596		168, 264, 0 22, 78 24, 0, 0	168, 480, 0 22, 78 24, 0, 0							
VFVC1760(2)				132, 246, 0 44, 78 44, 0, 0	132, 246, 0 44, 78 44, 0, 0					
VSVD1760(3)(4)		168, 156, 0 0, 78 16, 0, 0	168, 480, 0 0, 78 16, 0, 0		186, 462, 0 0, 78 24, 0, 0					
VFVF1760(1)								132, 192, 0 0,78 0, 8, 36 (0)		132, 192, 0 22,78 0, 8, 36 (0)
VSVI1760									132, 516, 0 0, 78 0, 16, 0	
VSVA2197				192, 294, 0 44, 78 44, 0, 0	186, 462, 0 44, 78 44, 0, 0					

Notes:

1. Some packages are compatible with Versal Premium Series devices.
2. Devices in VFVC1760 support peak LPDDR4 in 162 I/O only. The remaining 216 I/O support limited data rates. See the associated data sheet.
3. VM1302 in VSVD1760 supports peak LPDDR4 in 162 I/O only. The remaining 162 I/O support limited data rates. See the associated data sheet.
4. VM1402 in VSVD1760 supports peak LPDDR4 in 324 I/O only. The remaining 324 I/O support limited data rates. See the associated data sheet.

Versal Premium Series Gen 2

Table 12: **Versal Premium Series Gen 2: Resources**

	2VP3102	2VP3202	2VP3402	2VP3502	2VP3602
System Logic Cells	1,407,560	1,743,560	2,561,160	3,273,480	3,273,480
CLB Flip-Flops	1,286,912	1,594,112	2,341,632	2,992,896	2,992,896
LUTs	643,456	797,056	1,170,816	1,496,448	1,496,448
Distributed RAM (Mb)	20	24	36	46	46
Block RAM Blocks	1246	1,510	2,230	2,806	2,806
Block RAM (Mb)	44	53	78	99	99
UltraRAM Blocks	288	360	504	648	648
UltraRAM (Mb)	81	101	142	182	182
DSP Engines	3,332	4,004	6,080	2,856	7,616
Maximum DSP Cascade	238	286	238	238	238
MMCM	7	7	13	13	13
APU	Dual-core Arm Cortex-A72; 48 KB/32 KB L1 Cache w/ parity & ECC; 1 MB L2 Cache w/ ECC				
RPU	Dual-core Arm Cortex-R5F; 32 KB/32 KB L1 Cache; TCM w/ECC				
Memory	256 KB On-Chip Memory w/ECC				
Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)				
NoC to PL Master / Slave Ports	24/20	28/24	44/32	52/40	52/40
DDR Bus Width	128	128	256	256	256
DDR Memory Controllers (DDRMC5E)	4	4	8	8	8
GTM2 Transceivers	32	32	56	72	72
PCIe w/DMA & CXL® 3.1 (CPM6)	2x Gen6x8	2x Gen6x8	2x Gen6x8	2x Gen6x8	2x Gen6x8
100G Multirate Ethernet MAC	2	2	1	1	1
600G Ethernet MAC	1	2	3	5	5
High-Speed Crypto Engines	2	2	1	1	1
LDPC Decoder	4	6	0	0	0

Table 13: **Versal Premium Series Gen 2: Device-Package Combinations and Maximum I/O**

	2VP3102	2VP3202	2VP3402	2VP3502	2VP3602
	X5IO DDR Only, X5IO DDR+PL, X5IO PL Only HDIO, MIO GTM2 PL Only 56G (112G),(1)(3) GTM2 CPM6 32G (64G)(1)(2)(3)				
NSVO1369	104, 224, 0 22, 52 16 (8), 8 (4)	104, 224, 0 22, 52 24 (12), 8 (4)			
VSVJ1760	136, 248, 32 22, 78 16 (12), 16 (16)	136, 248, 32 22, 78 16 (12), 16 (16)			
VSVA3014			104, 576, 32 0, 78 40 (20), 16 (16)	104, 576, 32 0, 78 48 (24), 16 (16)	104, 576, 32 0, 78 48 (24), 16 (16)
VSVC3340			104, 600, 32 0, 78 40 (40), 16 (16)	104, 600, 32 0, 78 56 (56), 16 (16)	104, 600, 32 0, 78 56 (56), 16 (16)

Notes:

1. All GTM2 PL Only can operate at 56G; the quantity that can operate up to 112G is shown in parentheses. All GTM2 CPM can operate at 32G; the quantity that can operate up to 64G is shown in parentheses.
2. GTM2 transceivers connected to CPM6 can also bypass CPM6 (using the GT Direct mode) and access PL to support select non-PCIe protocols up to 32G NRZ (in -3 speedgrade) or 25G NRZ (in -2 speedgrade).
3. Refer to DC and AC switching characteristics data sheet for performance per speed grade.

Versal Premium Series

Table 14: **Versal Premium Series: Resources**

	VP1002	VP1052	VP1102	VP1202	VP1402	VP1502	VP2502	VP1552	VP1702	VP1802	VP2802	VP1902
System Logic Cells	833,000	1,185,800	1,574,720	1,969,240	2,233,280	3,763,480	3,737,720	3,836,840	5,557,720	7,351,960	7,326,200	18,506,880
CLB Flip-Flops	761,600	1,084,160	1,439,744	1,800,448	2,041,856	3,440,896	3,417,344	3,507,968	5,081,344	6,721,792	6,698,240	16,920,576
LUTs	380,800	542,080	719,872	900,224	1,020,928	1,720,448	1,708,672	1,753,984	2,540,672	3,360,896	3,349,120	8,460,288
Distributed RAM (Mb)	12	17	22	27	31	53	52	54	78	103	102	258
Block RAM Blocks	535	751	1,405	1,341	1,981	2,541	2,541	2,541	3,741	4,941	4,941	6,808
Block RAM (Mb)	19	26	49	47	70	89	89	89	132	174	174	239
UltraRAM Blocks	345	489	453	677	645	1,301	1,301	1,301	1,925	2,549	2,549	2,200
UltraRAM (Mb)	97	138	127	190	181	366	366	366	541	717	717	619
Multiport RAM (Mb)	80	80	–	–	–	–	–	–	–	–	–	–
DSP Engines	1,140	1,572	1,904	3,984	2,672	7,440	7,392	7,392	10,896	14,352	14,304	6,864
Maximum DSP Cascade	190	262	238	166	334	166	166	166	166	166	166	286
AI Engines (AIE)	–	–	–	–	–	–	472	–	–	–	472	–
AIE Data Memory (Mb)	–	–	–	–	–	–	118	–	–	–	118	–
MMCM	7	7	9	13	9	13	13	13	13	13	13	48
APU	Dual-core Arm Cortex-A72; 48 KB/32 KB L1 Cache w/ parity & ECC; 1 MB L2 Cache w/ ECC											
RPU	Dual-core Arm Cortex-R5F; 32 KB/32 KB L1 Cache; TCM w/ECC											
Memory	256 KB On-Chip Memory w/ECC											
Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)											
NoC to PL Master / Slave Ports	16/16	22/22	30/30	28/28	42/42	52/52	52/52	52/52	76/76	100/100	100/100	192/192
DDR Bus Width	128	128	192	256	192	256	256	256	256	256	256	896
DDR Memory Controllers (DDRMC)	2	2	3	4	3	4	4	4	4	4	4	14
PCIe w/DMA (CPM4)	2 x Gen4x4	2 x Gen4x4	–	–	–	–	–	–	–	–	–	–
PCIe w/DMA (CPM5)	–	–	–	2 x Gen5x8	–	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8	–
PCIe (PL PCIE4)	1 x Gen4x8	1 x Gen4x8	–	–	–	–	–	–	–	–	–	–
PCIe (PL PCIE5)	–	–	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	8 x Gen5x4	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	16 x Gen5x4
100G Multirate Ethernet MAC	3	5	6	2	6	4	4	4	6	8	8	12
600G Ethernet MAC	2	3	7	1	11	3	3	1	5	7	7	4
600G Interlaken	1	2	–	–	–	1	1	–	2	3	3	0
High-Speed Crypto Engines	1	1	3	1	4	2	2	2	3	4	4	0
GTY Transceivers[1]	8	8	–	–	–	–	–	–	–	–	–	–
GTYP Transceivers[1]	–	–	8	28[3]	8	28[3]	28[3]	68[3]	28[3]	28[3]	28[3]	128
GTM Transceivers[1] 58Gb/s (112 Gb/s)	24 (12)	36 (18)	64 (32)	20 (10)	96 (64)[2]	60 (30)	60 (30)	20 (10)	100 (50)	140 (70)	140 (70)	32 (16)

Notes:

1. Refer to DC and AC switching characteristics data sheet for performance per speed grade.
2. The VP1402 device in the VSVD2197 package can run 64 GTM transceivers in any 8 quads at 112 Gb/s.
3. 16 GTYP transceivers are dedicated to CPM5 for PCI Express use.

Table 15: **Versal Premium Series: Device-Package Combinations and Maximum I/O**

	VP1002	VP1052	VP1102	VP1202	VP1402	VP1502	VP2502	VP1552	VP1702	VP1802	VP2802	VP1902
	XPIO: DDR Only, DDR+PL, PL Only HDIO, MIO GTY, GTM (112G)		XPIO DDR Only, XPIO DDR+PL, XPIO PL Only HDIO, MIO GTYP, GTM (112G)									
SBVJ1369		192, 132, 0 0, 78 8, 16 (8)										
NFVI1369	138, 24, 0 0, 78 8, 24 (12)	138, 24, 0 0, 78 8, 36 (18)										
VFVF1760[1]	192, 132, 0 0, 78 8, 24 (12)	192, 132, 0 0, 78 8, 36 (18)	132, 192, 0 0, 78 8, 36 (18)		132, 192, 0 22, 78 8, 36 (18)							
VSVD2197					0, 54, 0 0, 78 8, 96, (64)[3]							
VSVA2785[2]			180, 306, 0 0, 78 8, 64 (32)	132, 516, 54 0, 78 28, 20 (10)	180, 306, 0 44, 78 8, 80 (40)	132, 516, 54 0, 78 28, 56 (28)		132, 516, 54 0, 78 68, 16 (8)				
VSVA3340					180, 306, 0 44, 78 8, 96 (48)	132, 354, 0 0, 78 28, 60 (30)		132, 354, 0 0, 78 68, 20 (10)	132, 354, 0 0, 78 28, 88 (44)			
VSVB3340							132, 516, 54 0, 78 28, 60 (30)					
LSVC4072										132, 516, 54 0, 78 28, 140 (70)		
VSVA5601							132, 516, 54 0, 78 28, 60 (30)		132, 516, 54 0, 78 28, 100 (50)	132, 516, 54 0, 78 28, 140 (70)	132, 516, 54 0, 78 28, 140 (70)	
VSVA6865												264, 2064, 0 88, 52 64, 32 (16)
VSVB6865												0, 1890, 0 88, 52 128, 32 (16)

Notes:
1. Some packages are compatible with Versal Prime Series devices.
2. VP1202, VP1502, and VP1552 in VSVA2785 support peak LPDDR4 data rates in 486 I/O only. The remaining 216 I/O support limited data rates. See the associated data sheet.
3. GTM transceivers can operate at data rates up to 112 Gb/s by combining two transceivers together. The VP1402 device in the VSVD2197 package can run 64 GTM transceivers at 112 Gb/s.

Versal HBM Series

Table 16: **Versal HBM Series: Resources**

	VH1522	VH1542	VH1582	VH1742	VH1782
System Logic Cells	3,836,840	3,836,840	3,836,840	5,631,080	5,631,080
CLB Flip-Flops	3,507,968	3,507,968	3,507,968	5,148,416	5,148,416
LUTs	1,753,984	1,753,984	1,753,984	2,574,208	2,574,208
Distributed RAM (Mb)	54	54	54	79	79
Block RAM Blocks	2,541	2,541	2,541	3,741	3,741
Block RAM (Mb)	89	89	89	132	132
UltraRAM Blocks	1,301	1,301	1,301	1,925	1,925
UltraRAM (Mb)	366	366	366	541	541
HBM (GB)	8	16	32	16	32
DSP Engines	7,392	7,392	7,392	10,848	10,848
Maximum DSP Cascade	166	166	166	166	166
MMCM	13	13	13	13	13
APU	Dual-core Arm Cortex-A72; 48 KB/32 KB L1 Cache w/ parity & ECC; 1 MB L2 Cache w/ ECC				
RPU	Dual-core Arm Cortex-R5F; 32 KB/32 KB L1 Cache; TCM w/ECC				
Memory	256 KB On-Chip Memory w/ECC				
Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)				
NoC to PL Master / Slave Ports	52/52	52/52	52/52	76/76	76/76
DDR Bus Width	256	256	256	256	256
DDR Memory Controllers (DDRMC)	4	4	4	4	4
PCIe w/DMA (CPM5)	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8	2 x Gen5x8
PCIe (PL PCIE5)	8 x Gen5x4	8 x Gen5x4	8 x Gen5x4	8 x Gen5x4	8 x Gen5x4
100G Multirate Ethernet MAC	4	4	4	6	6
600G Ethernet MAC	1	1	1	3	3
600G Interlaken	–	–	–	1	1
High-Speed Crypto Engines	2	2	2	3	3
GTYP Transceivers(1)	68(3)	68(3)	68(3)	68(3)	68(3)
GTM Transceivers(2) 58 Gb/s (112 Gb/s)	20 (10)	20 (10)	20 (10)	60 (30)	60 (30)

Notes:

1. Refer to DC and AC switching characteristics data sheet for performance per speed grade.
2. GTM transceivers can operate at data rates up to 112 Gb/s by combining two transceivers together.
3. 16 GTYP transceivers are dedicated to CPM5 for PCI Express use.

Table 17: **Versal HBM Series: Device-Package Combinations and Maximum I/O**

	VH1522	VH1542	VH1582	VH1742	VH1782
	XPIO DDR Only, XPIO DDR+PL, XPIO PL Only HDIO, MIO GTYP, GTM (112G)				
VSVA3697	132, 516, 54 0, 78 68, 20 (10)	132, 516, 54 0, 78 68, 20 (10)	132, 516, 54 0, 78 68, 20 (10)		
LSVA4737		132, 516, 54 0, 78 68, 20 (10)	132, 516, 54 0, 78 68, 20 (10)	132, 516, 54 0, 78 68, 60 (30)	132, 516, 54 0, 78 68, 60 (30)

Versal RF Series

Table 18: **Versal RF Series: Resources**

		VR1602	VR1652	VR1902	VR1952
14-bit RF-ADC	# of ADCs	16	4	16	8
	Max Rate (GSPS)	8	32	8	32
14-bit RF-DAC	# of DACs	16	8	16	16
	Max Rate (GSPS)	16	16	16	16
LDPC Decoder		4	4	6	6
1 GSPS Channelizer		224	224	320	320
FFT/iFFT		28	28	40	40
Poly Block		–	–	24(1)	24(1)
AI Engines (AIE)		126	126	120	120
AIE Data Memory (Mb)		32	32	30	30
DSP Engines		2,256	2,256	3,976	3,976
Maximum DSP Cascade		188	188	284	284
System Logic Cells		1,205,400	1,205,400	2,473,800	2,473,800
CLB Flip-Flops		1,102,080	1,102,080	2,261,760	2,261,760
LUTs		551,040	551,040	1,130,880	1,130,880
Distributed RAM (Mb)		17	17	35	35
Block RAM Blocks		1,109	1,109	2,266	2,266
Block RAM (Mb)		39	39	80	80
UltraRAM Blocks		357	357	262	262
UltraRAM (Mb)		100	100	74	74
MMCM		9	9	9	9
APU		Dual-core Arm Cortex-A72, 48 KB/32 KB L1 Cache w/ parity & ECC; 1 MB L2 Cache w/ ECC			
RPU		Dual-core Arm Cortex-R5F, 32 KB/32 KB L1 Cache, and 256 KB TCM w/ECC			
Memory		256 KB On-Chip Memory w/ECC			
Connectivity		Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)			
NoC to PL Master / Slave Ports		22/16	22/16	42/36	42/36
DDR Bus Width		160	160	160	160
DDR Memory Controllers (DDRMC5E)		5	5	5	5
PCIe (PL PCIE5)		1 x Gen5x4	1 x Gen5x4	1 x Gen5x4	1 x Gen5x4
100G Multirate Ethernet MAC		2	2	2	2
600G Ethernet MAC		–	–	3	3
X5IO		448	448	448	448
HDIO		22	22	22	22
GTYP Transceivers		12	12	–	–
GTM Transceivers (56G (112G))		8 (4)	8 (4)	–	–
GTM2 Transceivers (56G (112G))		–	–	20 (10)	20 (10)

Notes:

1. Each poly block can be also configured as 16 channelizers. Two poly blocks can be combined to form a resampler.

Table 19: **Versal RF Series: Device-Package Combinations and Maximum I/O**

	VR1602	VR1652	VR1902	VR1952
	X5IO DDR Only, X5IO DDR+PL, X5IO PL Only HDIO, MIO GTYP, GTM (112G) RF-ADC (8G), RF-ADC (32G), RF-DAC (16G)		X5IO DDR Only, X5IO DDR+PL, X5IO PL Only HDIO, MIO GTM2 (112G) RF-ADC (8G), RF-ADC (32G), RF-DAC (16G)	
VSVG1596	144, 208, 0 22, 78 4, 4 (2) 12, 0, 8	144, 208, 0 22, 78 4, 4 (2) 0, 4, 8		
VSVA2488	144, 304, 0 22, 78 12, 8 (4) 16, 0, 16	144, 304, 0 22, 78 12, 8 (4) 0, 4, 8	136, 248, 64 22, 78 20 (10) 16, 0, 16	136, 248, 64 22, 78 20 (10) 0, 8, 16

Device Layout (Architecture and Interconnect)

Versal devices are built from a library of building blocks dedicated to processing, compute, acceleration, and connectivity. Figure 1 shows the layout of a device with the NoC connecting to an external host processor via the CPM and the various heterogeneous processing elements: PL, vector-based accelerators (AI Engines), and scalar processing accelerators.

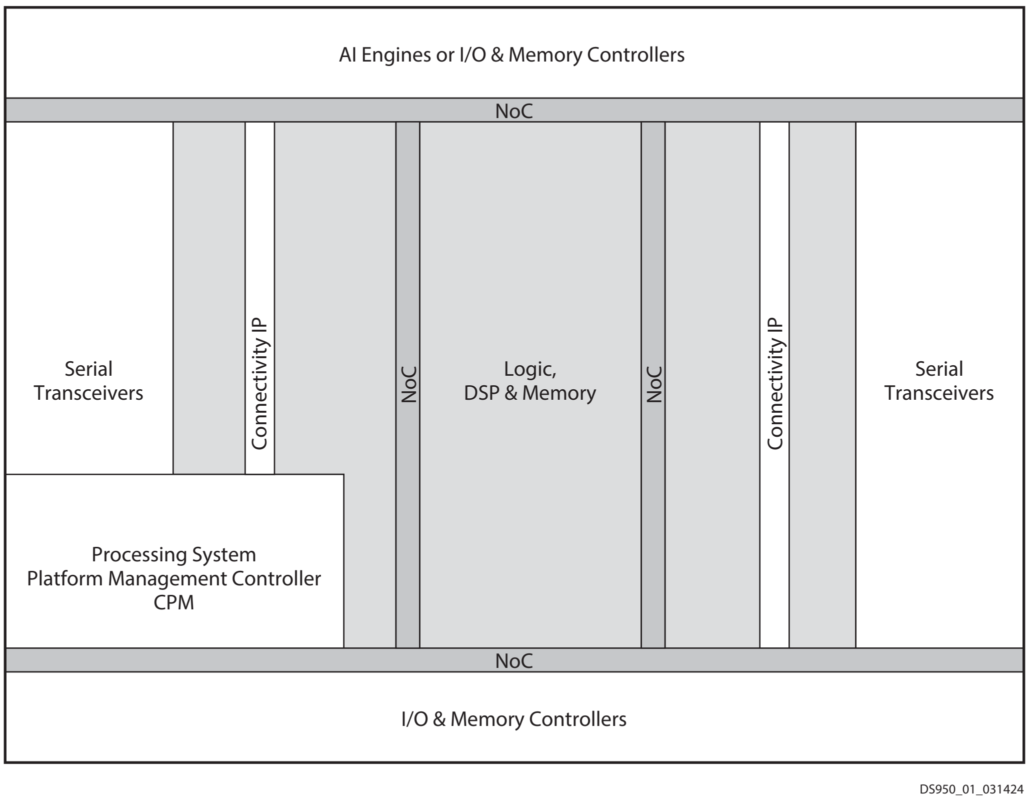


Figure 1: **Versal Device Layout**

Serial transceivers are located on the east and west edges of the device with I/O and memory controllers on the south and north of the device. In Versal devices with AI Engines, there is an acceleration array on the north edge of the device in place of the I/O and memory controllers. Connectivity IP is located in columns close to the serial transceivers. Resources are connected together through a matrix of programmable interconnect routes for local and regional signal connectivity as well as the NoC for high bandwidth and long distance communication around the device.

NoC

The programmable NoC is an AXI-4 based network of interconnect within the Versal architecture that easily enables high-bandwidth connections to be routed around the device. The NoC extends in both horizontal and vertical directions to the edges of the device. It exists to connect together areas of the device that demand and use large quantities of data alleviating any resource burden on the local and regional device interconnect. The NoC is a full blocking crossbar between memory controllers, programmable logic, processing system, AI Engines, and platform management controller. Examples of NoC connections include:

- Sharing device access to DRAM (DDR memory)
- PL to PL connections
- Memory mapped access to the AI Engine array
- Connecting between processing system and PL
- Connecting between the processing system and DDR memory

In devices built using stacked silicon interconnect (SSI) technology, the vertical NoC columns connect between adjacent super logic regions (SLRs), which allows device configuration data to travel between primary and secondary SLRs.

Platform Management Controller

The platform management controller is responsible for managing Versal devices with the following main categories of responsibility: securely booting and configuring the platform; and life-cycle management, which includes device integrity and debug, and system monitoring.

Boot and Configuration

The platform management controller is responsible for booting Versal devices from the primary boot source in a multi-stage boot process that supports both a non-secure and a secure boot. For a secure boot, the AES-GCM, SHA3-384 decryption/authentication, and ECDSA/RSA blocks decrypt and authenticate the image. Upon reset, the mode pins are read to determine the primary boot device, such as quad SPI, octal SPI, SD, or eMMC. The platform management controller then proceeds to execute the code out of on-chip BootROM and copies the platform loader and manager (PLM) from the boot device to the on-chip memory while undergoing authentication and decryption. The configuration of the PL is also undertaken by the PLM. The device image is loaded from its storage medium, and after authentication and decryption, is sent to the PL configuration interface.

It is also possible to reconfigure portions of the PL using Dynamic Function eXchange (DFX). A new device image for a portion of the PL can be loaded from the processing system, through the primary or secondary boot interfaces, e.g., PCIe or Ethernet. Upon reconfiguration, a portion of the PL provides the new functionality determined by the new device image, enabling users to quickly adapt the functionality of their design to changing system requirements.

Primary Public Keys

Versal devices use primary public keys (PPKs) for signature verification. Devices have either three or five PPKs as listed in the table below.

Table 20: **Primary Public Keys per Series**

Series	AI Edge Gen 2	AI Edge	AI Core	Prime Gen 2	Prime	Premium Gen 2	Premium	HBM	RF
3 Keys	2VE3304 2VE3358 2VE3504 2VE3558 2VE3804 2VE3858	VE1752	VC1502 VC1702 VC1802 VC1902	2VM3358 2VM3558 2VM3654 2VM3858	VM1302 VM1402 VM1502 VM1802 VM2302 VM2502 VM2902		VP1102 VP1202 VP1402 VP1502 VP1552 VP1702 VP1802 VP2502 VP2802	VH1522 VH1542 VH1582 VH1742 VH1782	
5 Keys		VE2002 VE2102 VE2202 VE2302 VE2602 VE2802	VC2602 VC2802		VM1102 VM2152 VM2202	2VP3102 2VP3202 2VP3402 2VP3502 2VP3602	VP1002 VP1052 VP1902		VR1602 VR1652 VR1902 VR1952

System Monitoring

The platform management controller contains system monitoring capability for monitoring voltage and temperature in the processing system and PL to enhance the overall safety, security, and reliability of the system. The core of the system monitor is a 10-bit 200kSPS ADC, which can be accessed via JTAG, PMBus, or I2C interfaces, via the processing system directly, and via the PL through the NoC.

Device Integrity and Debug

JTAG is the primary interface for Versal device debug features. The JTAG architecture has two IEEE Std 1149.1 compliant TAP controllers that are connected in series: the Arm DAP controller and the platform management controller TAP controller. The Arm DAP controller is the main controller for debug functions supporting: processing system CoreSight debug architecture, debug of the PL, programming of supported external flash memory, and eFUSE/BBRAM programming. The TAP controller supports: reading the device IDCODE, programming of the PL, and boundary scan.

The platform management controller also contains a high-speed debug port (HSDP) that can be used as a faster debug method than the primary JTAG interface. The HSDP interface is a high-throughput interface consisting of separate ingress and egress simplex Aurora 64B/66B channels that leverage the transceivers to the north of the processing system. The HSDP allows daisy-chaining of channels from different devices. The HSDP can also be accessed by the serial transceivers in the PL via an Aurora bridge also in the PL.

External Flash Memory Interfaces

The SD/eMMC controller supports 1- and 4-bit data interfaces at low, default, high-speed, and ultra-high-speed (UHS) clock rates. This controller also supports 1-, 4-, or 8-bit-wide eMMC interfaces that are compliant to the eMMC 4.51 specification. eMMC is one of the primary boot modes and supports boot from managed NAND devices. The controller has a built-in DMA for enhanced performance.

The quad SPI controller is one of the primary boot devices. It supports 4-byte and 3-byte addressing modes. In both addressing modes, single, dual-stacked, and dual-parallel configurations are supported. Single mode supports a quad serial NOR flash memory, while in double stacked and double parallel modes, it supports two quad serial NOR flash memories.

The octal SPI controller is one of the primary boot and configuration devices. It has an 8-pin interface and provides up to 400 MB/s of bandwidth in double data rate mode and up to 166 MB/s in single data rate mode. It has two chip-selects to support deeper memory and a built-in DMA for enhanced performance.

Slave Boot Modes

In addition to JTAG, SelectMAP is also an available slave boot mode. SelectMAP is a high bandwidth, stream oriented, parallel interface that can be configured as 8-, 16- or 32-bit wide. It runs up to 200 MHz.

Compute and Acceleration Engines

AI Engine Array

Some Versal devices contain a two-dimensional array of AI Engines. There are three types: AIE, AIE-ML, and AIE-ML v2. Each tile contains: an AI Engine, a high-performance VLIW vector (SIMD) processor; integrated data memory; and interconnects for streaming, configuration, and debug. Alongside the tiles is the AI Engine array interface that provides the necessary logic to connect the AI Engine array to the other resources in the PL, processing system, and the NoC. Devices with an AIE-ML array include additional rows of 512 KB memory tiles.

Table 21 and Table 22 show the size of the arrays in columns and rows and the number of interface tiles to PL and NoC.

Table 21: **AI Engine Array Size**

	AI Edge Series Gen 2						**AI Edge Series**						
	2VE3304	2VE3358	2VE3504	2VE3558	2VE3804	2VE3858	VE2002	VE2102	VE2202	VE2302	VE1752	VE2602	VE2802
Columns of AI Engines	12	12	24	24	36	36	12	12	17	17	38	38	38
Rows of AI Engines	2	2	4	4	4	4	1	1	2	2	8	4	8
AI Engine to PL Interface Tiles	7	7	18	18	27	27	7	7	12	12	27	28	28
AI Engine to NoC Interface Tiles	–	–	–	–	–	–	2	2	6	6	12	12	12
Columns of Memory Tiles	12	12	24	24	36	36	12	12	17	17	0	38	38
Rows of Memory Tiles	1	1	1	1	2	2	1	1	1	1	0	2	2

Table 22: **AI Engine Array Size**

	AI Core Series						**Premium Series**		**RF Series**			
	VC1502	VC1702	VC1802	VC1902	VC2602	VC2802	VP2502	VP2802	VR1602	VR1652	VR1902	VR1952
Columns of AI Engines	33	38	50	50	38	38	59	59	42	42	40	40
Rows of AI Engines	6	8	6	8	4	8	8	8	3	3	3	3
AI Engine to PL Interface Tiles	27	27	39	39	28	28	47	47	28	28	34	34
AI Engine to NoC Interface Tiles	12	12	16	16	12	12	20	20	16	16	5	5
Columns of Memory Tiles	0	0	0	0	38	38	0	0	0	0	0	0
Rows of Memory Tiles	0	0	0	0	2	2	0	0	0	0	0	0

AI Engine

The AI Engine contains a scalar unit, a vector unit, load units, and a memory interface. The scalar unit contains: a 32-bit scalar RISC processor with register files for general-purpose, pointer, configuration, and backup registers; and a 32x32-bit scalar multiplier. The AI Engine also supports non-linear functions including sine/cosine (AIE only), squareroot, and inverse-squareroot. Three address generator units (AGUs) are available: two dedicated as load units, and one dedicated as a store unit. The vector unit contains: 512-bit vector fixed-point / integer unit. Devices with AIE contain a single-precision floating point vector unit. Devices with AIE-ML and AIE-ML v2 contain a floating-point vector unit also used for Bfloat16 and MX6/MX9 (AIE-ML v2 only) support. The vector units in AIE, AIE-ML, and AIE-ML v2 support concurrent operation on multiple vector lanes. Within each AI Engine is a dedicated, single-port, 16 KB program memory (128-bit wide and 1k deep). The program memory supports instruction compression and has ECC protection and reporting

AI Engine Data Memory

Separate from the AI Engine, each tile contains 32 KB of data memory for AIE and 64 KB of data memory for AIE-ML and AIE-ML v2, divided into eight single-port banks. This structure allows up to eight parallel memory access transactions every clock cycle, with five cycle access latency. Stall signals identify memory access conflicts during which time any outstanding memory operations are buffered. Each data memory module supports memory error detection (parity) and reporting. The data memory also contains DMA logic that supports incoming stream to local memory, outgoing stream from local memory, and buffered streams in local memory. Support for two-dimensional stride access enables any AI Engine to access data memories in adjacent AI Engine tiles in the north, south, east, and west directions, allowing a single AIE to access up to 128 KB of data memory and a single AIE-ML / AIE-ML v2 to access up to 256 KB of data memory.

AIE-ML/AIE-ML v2 Memory Tiles

Devices with AIE-ML or AIE-ML v2 array also includes, at the bottom of the array, memory tiles that contain high-density (512 KB) and high bandwidth memory, divided into 8 banks, and an integrated DMA to access local memory and neighboring memories.

Processing System

All Versal devices contain a processing system (PS) consisting of APU, RPU, and peripherals. The processing system is part of a group of architectural elements that include the platform management controller (PMC), CPM block (available in some devices), NoC, and integrated memory controllers that are tightly coupled, but are also capable of operating independently from each other. The simplified layout is shown in Figure 2.

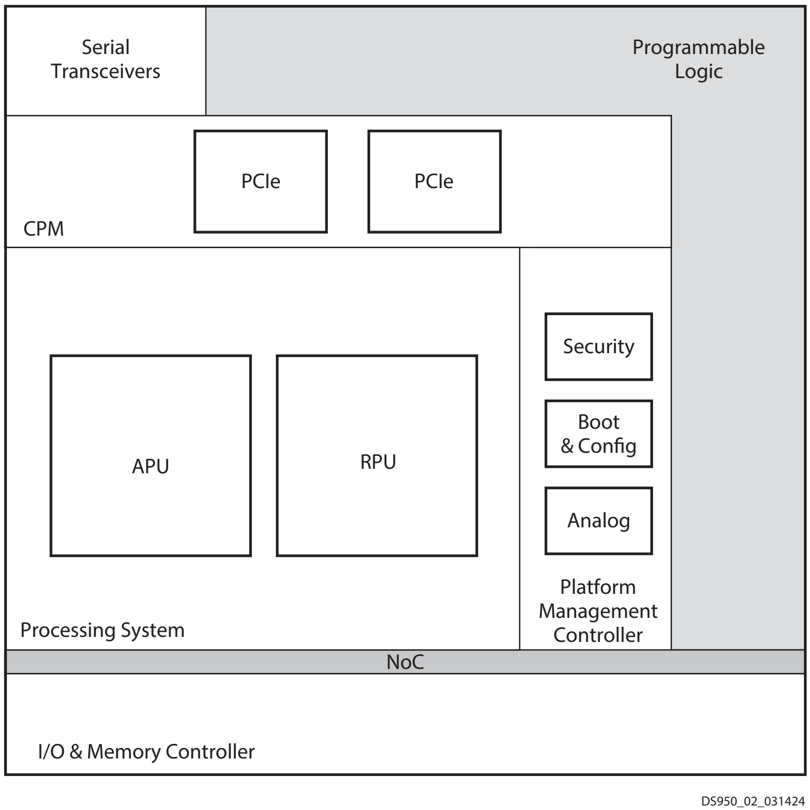


Figure 2: **Processing System and Surrounding Blocks**

The platform management controller is responsible for booting the processing system from one of its primary boot sources. The PS also has direct access to the features inside the CPM, which talks to the serial transceivers directly to the north for implementation of high-performance interconnect based on PCI-SIG technologies. Programmable logic can be configured at any stage of the process and can be performed before or after the processing system is booted.

There are several different types of processing systems in the Versal architecture. Table 23 outlines the key features of each.

Table 23: **Processing System Feature Comparison**

	Series / Devices	AI Edge, AI Core, Prime, Premium Gen 2, Premium, HBM, RF	Prime Gen 2: 2VM3654	AI Edge Gen 2, Prime Gen 2: 2VM3358, 2VM3558, 2VM3858
Application Cores	# of Application Cores	2	4	4–8
	Core Details	Arm Cortex-A72; 48 KB/32 KB L1 Cache w/ parity & ECC; 1 MB L2 Cache w/ ECC	Arm Cortex-A78AE; 64 KB I w/parity & D w/ECC L1 Cache; 512 KB L2 Cache	Arm Cortex-A78AE; 64 KB I w/parity & D w/ECC L1 Cache; 512 KB L2 Cache
	Cores per Cluster	2	4	2
	# of Clusters	1	1	4
	L3 Cache per Cluster (MB)	–	2	1
	System-Level Cache (MB)	–	–	4
Real-Time Cores	# of Real-Time Cores	2	6	4–10
	Core Details	Arm Cortex-R5F; 32 KB/32 KB L1 Cache; TCM w/ECC	Arm Cortex-R52; 32 KB L1 Cache w/ECC; 128 KB TCM w/ECC	Arm Cortex-R52; 32 KB L1 Cache w/ECC; 128 KB TCM w/ECC
	Cores per Cluster	2	2	2
	# of Clusters	1	3	5
On-Chip Memory with ECC		256 KB	1 MB	2 MB
High-Speed Connectivity		Ethernet (x2)	PCI Express Gen5 x4 (x1); USB 3.2 (x1); DisplayPort 1.4 (x1); 10G Ethernet (x1); 1G Ethernet (x1); UFS 3.2 (x1)	PCI Express Gen5 x4 (x1); USB 3.2 (x1); DisplayPort 1.4 (x1); 10G Ethernet (x1); 1G Ethernet (x1); UFS 3.1 (x1)
General Connectivity		UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)	CAN/CAN-FD (x2); SPI (x2); UART (x2); USB 2.0 (x2); I2C/I3C (x2); GPIO	CAN/CAN-FD (x2); SPI (x2); UART (x2); USB 2.0 (x2); I2C/I3C (x2); GPIO

Application Processing Unit (APU)

The APU features Arm Cortex-A72 processors or Arm Cortex-A78AE processors.

Arm Cortex-A72

Arm Cortex-A72 cores are 64-bit-wide application processors based on the Arm-v8A architecture, which supports hardware virtualization. In addition to the cache structure outlined in Table 23, each of the Cortex-A72 cores has a NEON SIMD engine and a single and double precision floating point unit. The APU consists of a snoop control unit that keeps the L1 caches coherent, thus, eliminating the need for coherency to use software bandwidth. The APU also has a built-in interrupt controller supporting virtual interrupts.

The APU communicates to the rest of the processing system through the 128-bit AXI coherent extension (ACE) port via Cache Coherent Interconnect (CCI) block, using the system memory management unit (SMMU). The APU is also connected to the PL through the 128-bit accelerator coherency port (ACP), providing a low latency coherent port for accelerators in the PL. To support real-time debug and trace, each core also has an Embedded Trace Macrocell (ETM) that communicates with the Arm CoreSight™ Debug System.

Arm Cortex-A78AE

The Arm Cortex-A78AE cores can operate split or in lock-step mode. The APU communicates with the rest of the processing system via the coherent hub interface (CHI) based coherency interconnect (CMN-600 w/AE). The coherent interconnect enables the PS to satisfy safety requirements, provides snoopable LLC, enables efficient L3 stashing, and provides sufficient bandwidth and QoS for incoming traffic and traffic to the NoC.

Real-Time Processing Unit (RPU)

The RPU features Arm Cortex-R5F processors or Arm Cortex-R52 processors.

Arm Cortex-R5F

Arm Cortex-R5F cores are 32-bit real-time processor cores based on the Arm-v7R architecture. Each of the Cortex-R5F cores has 32 KB of Level 1 (L1) instruction and data cache with ECC protection. In addition to the L1 caches, each of the Cortex-R5F cores also has a 128 KB tightly coupled memory (TCM) interface for real-time single cycle access. The RPU also has a dedicated interrupt controller and floating point unit. The RPU can operate in either split or lock-step mode. In split mode, both processors run independently of each other. In lock-step mode, they run in parallel with each other, with integrated comparator logic, and the TCMs are used as a 256 KB unified memory. The on-chip memory (OCM) is accessed through two 128-bit AXI interfaces with one AXI interface dedicated to the two Cortex-R5F processors and the other AXI interface available to the APU and other masters.

The RPU communicates with the rest of the processing system via the 128-bit AXI-4 ports connected to the low power domain switch. It also communicates directly with the PL through 128-bit low latency AXI-4 ports. To support real-time debug and trace, each core also has an embedded trace macrocell (ETM) that communicates with the Arm CoreSight Debug System.

Arm Cortex-R52

To provide high-level safety, the Arm Cortex-R52 cores are configurable as split-lock (split or lock-step). The cores are organized into independent, dual-core clusters. The RPU communicates with the rest of the PS via the low-power domain (LPD), non-coherent interconnect. The on-chip memory (OCM) is also connected to the LPD interconnect. The OCM is organized into two banks of 0.5 MB. Each bank can be accessed through a dedicated 128-bit AXI interface via the LPD interconnect.

Connectivity Peripherals

In the processing system, many peripherals are used to connect to external devices over industry-standard protocols, including CAN-FD, SPI, USB, Ethernet, I2C, and UART. Many of the peripherals support clock gating and power gating modes to reduce dynamic and static power consumption. These peripherals either use multiplexed I/O (MIO) to connect to the external components, or if required, they can also be routed into and through the PL using the extended multiplexed I/O (EMIO). Table 23 lists the peripherals available in the different processing system configurations.

Programmable Logic

Configurable Logic Block (CLB)

Every configurable logic block (CLB) contains 32 look-up tables (LUTs) and 64 flip-flops. The LUTs can be configured as either one 6-input LUT with one output, or as two 5-input LUTs with separate outputs but common inputs. Each LUT can optionally be registered in a flip-flop. In addition to the LUTs and flip-flops, the CLB contains arithmetic carry logic and multiplexers to create wider logic functions. Within each CLB, 16 LUTs can be configured as a 64-bit RAM, as a 32-bit shift register (SRL32), or as two 16-bit shift registers (SRL16s). For every group of 64 flip-flops, there are four clocks signals, four set/reset signals, and 16 clock enables. Within every CLB are dedicated interconnect paths for connecting LUTs together without having to exit and re-enter a CLB and cascade muxes. This enables a flexible carry logic structure that allows a carry chain to start at any bit in the chain.

Internal Memory

Each Versal device contains several programmable, internal storage capabilities. In addition to the distributed RAM capability in the CLB, there are dedicated blocks for building various size storage elements.

On-Chip Memory (OCM)

In addition to the 32 KB of L1 data cache, the RPU contains OCM with ECC. The OCM is accessed through AXI interfaces. Memory accesses from the RPU are treated with higher priority than memory accesses through the general 128-bit AXI interface.

Accelerator RAM

Some Versal devices include accelerator RAM, an additional 4 MB of on-chip memory with ECC located adjacent to the processing system. This memory provides direct access from the RPU via a 128-bit AXI interface and can also be accessed from the PL through three 256-bit AXI interfaces. PL access is not available in the VE2002 and VE2102 devices. The memory is divided into four banks supporting concurrent read or write accesses from the PL and RPU to different banks.

Block RAM

True dual-port block RAMs, each having 36 Kb of storage capacity, can be configured as either one 36 Kb RAM, or two completely independent 18 Kb RAMs. Each port can be configured as 4K × 9, 2K × 18, 1K × 36, or 512 x 72 in simple dual-port mode. The two ports can have different aspect ratios. Also, the read port width can be different from the write port width for each port.

Synchronous operation: Each memory access, read, and write is controlled by the clock. All inputs, data, address, clock enable, and write enable are registered. The data output is always latched, retaining data until the next operation. An optional output data pipeline register allows higher clock rates at the cost of an extra cycle of latency. During a write operation, the data output can be made to reflect the previously stored data, the newly written data, or remain unchanged. There is independent reset control of output latches and registers.

Asynchronous operation: The data outputs can also be set/reset asynchronously. The sleep input, which places the array in a low-power state, can be optionally asynchronous.

True dual-port operation: The block RAM has two completely independent ports that share nothing but the stored data.

Simple dual-port operation: One port is dedicated as a write port and the other as a read port. The data width can thus be extended to 72 bits for the 36 Kb full block RAM or 36 bits for the "split" 18 Kb block RAM.

Cascade mode supports all configurations available in 36 Kb RAM or 18 Kb RAM. Cascading refers to combining multiple block RAMs to build larger ones, without using additional logic resources.

Each 64-bit-wide block RAM can generate, store, and use eight additional bits to perform single-bit error correction and double-bit error detection (ECC) during the read process. The ECC logic can also be used without the memory array to support the implementation of ECC on user designed internal datapaths or memory controllers. Block RAM contents can be initialized or cleared by the configuration device image.

UltraRAM

Dual-port UltraRAMs, each having 288K bits of storage capacity, can be configured as one 288 Kb RAM. Each port can be configured as 32K x 9, 16K x 18, 8K x 36, or 4K x 72. The two ports can have different aspect ratios.

Synchronous operation only: Each memory access, read, and write is controlled by the clock. All inputs, data, address, clock enable, and write enable are registered. The data output is always latched, retaining data until the next operation. An optional output data pipeline register allows higher clock rates at the cost of an extra cycle of latency.

Asynchronous control: The data outputs can also be set/reset asynchronously. The sleep input, which places the array in a low power state, can be optionally asynchronous.

Pseudo dual-port operation: There are two ports on the memory. Each is capable of reading or writing in a single cycle. The ports are sequenced in a fixed order, allowing up to two transactions per cycle. (Both ports write, both ports read, or one port reads while the other writes.) This necessitates that the two ports share a common clock. During a write operation, the data output remains unchanged on a given port. There is independent reset control of output latches and registers.

ECC logic in the UltraRAM supports error checking and correction. Both ports have dedicated ECC for either read or write. The ECC logic is organized for 64-bit-wide data, which can generate, store, and use eight additional bits to perform single-bit error correction and double-bit error detection (ECC) during the read process.

It is possible to cascade the address and data of adjacent blocks to build deeper memories. Optional pipelining is also available to maintain the clock rate through tall cascades of UltraRAM.

Multiport RAM

Multiport RAM (MPRAM) is an array of eight 5 Mb RAMs, totaling 40 Mb. Each RAM has one write and one read port of 128-bit data. In addition, up to two write and two read 128-bit ports provide access to all eight RAMs.

Each 5 Mb RAM can be accessed individually (unit access) in simple dual-port mode supporting simultaneous write and read at 128-bit. Total storage is 40960 words of 128-bit data. Two global read and two global write ports allow 128-bit access to all eight RAMs (global access), totaling 8x40960 words of 128-bit data (40 Mb total). Global access can be combined with unit access, for example, global write with unit reads on multiple RAMs.

Internally, RAMs are accessed at twice the interface clock frequency and can operate in write-before-read mode or read-before-write mode. All RAMs support error checking and correction (ECC) with single error correction, double error detection with flags for each RAM. Unused RAMs will be shut down to save power.

Digital Signal Processing (DSP)

DSP applications use many binary multipliers and accumulators, best implemented in dedicated DSP Engines. Versal devices have many dedicated, low-power DSP Engines, combining high speed with small size while retaining system design flexibility.

Each DSP Engine fundamentally consists of a dedicated 27 × 24 bit twos complement multiplier and a 58-bit accumulator. The multiplier can be dynamically bypassed, and two 58-bit inputs can feed a single-instruction-multiple-data (SIMD) arithmetic unit (dual 24-bit add/subtract/accumulate or quad 12-bit add/subtract/accumulate), or a logic unit that can generate any one of ten different logic functions of the two operands.

The DSP Engine includes an additional pre-adder, typically used in symmetrical filters. This pre-adder improves performance in densely packed designs and reduces the DSP Engine count by up to 50%. The 116-bit-wide XOR function, programmable to 12, 22, 24, 34, 58, or 116-bit widths, enables performance improvements when implementing forward error correction and cyclic redundancy checking algorithms.

The DSP Engine also includes a 58-bit-wide pattern detector that can be used for convergent or symmetric rounding. The pattern detector is also capable of implementing 116-bit-wide logic functions when used in conjunction with the logic unit.

The DSP Engine provides extensive pipelining and extension capabilities that enhance the speed and efficiency of many applications beyond digital signal processing, such as wide dynamic bus shifters, memory address generators, wide bus multiplexers, and memory-mapped I/O register files. The accumulator can also be used as a synchronous up/down counter.

DSP Engines can be cascaded with length limitations to make larger functions. Maximum cascade length per device is listed in the device resource tables.

The DSP Engine layout enables new modes of operation in addition to the conventional fixed-point operation.

Three element vector / INT8 dot product: The DSP Engine can be used in vector fixed-point ALU mode in which the 27 x 24 bit multiplier is replaced by a three-dimensional vector dot-product unit. The dot-product unit supports element-wise product negation with negate pins.

Complex 18b x 18b: Using two back to back DSP Engines, the Versal architecture enables creation of an 18 x 18 + 58 twos complement complex multiply accumulator in which each of the two complex inputs can be optionally conjugated.

Single precision floating point: The DSP Engine contains a floating-point multiplier and a floating-point adder with separate outputs in binary32 format. Each floating-point multiplier input can be in either binary32 (single-precision or FP32) or binary16 (half-precision or FP16) format.

Connectivity

Transceivers

GTY/GTYP transceivers support data rates up to 32.75 Gb/s. GTM and GTM2 transceivers support data rates up to 112 Gb/s depending on the Versal device. Data rates lower than the minimum specified data rate can be achieved by using oversampling in the programmable logic.

GTY/GTYP Transceivers

The serial transmitter and receiver are independent circuits that use an advanced phase-locked loop (PLL) architecture to multiply the reference frequency input by certain programmable numbers between 4 and 25 to become the bit-serial data clock. Each transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

Transmitter (GTY/GTYP)

The transmitter is fundamentally a parallel-to-serial converter with a conversion ratio of 16, 20, 32, 40, 64, 80, 128, or 160. This allows the designer to trade off datapath width against timing margin in high-performance designs. These transmitter outputs drive the PC board with a single-channel differential output signal. TXOUTCLK is the appropriately divided serial data clock and can be used directly to register the parallel data coming from the internal logic. The incoming parallel data is fed through an optional FIFO and has additional hardware support for the 8B/10B, 64B/66B, or 64B/67B encoding schemes to provide a sufficient number of transitions. The bit-serial output signal drives two package pins with differential signals. This output signal pair has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to reduce power consumption.

Receiver (GTY/GTYP)

The receiver is fundamentally a serial-to-parallel converter, changing the incoming bit-serial differential signal into a parallel stream of words, each 16, 20, 32, 40, 64, 80, 128, or 160. This allows the designer to trade off internal datapath width against logic timing margin. The receiver takes the incoming differential data stream, feeds it through programmable DC automatic gain control, linear and decision feedback equalizers (to compensate for PC board, cable, optical and other interconnect characteristics), and uses the reference clock input to initiate clock recognition. There is no need for a separate clock line. The data pattern uses non-return-to-zero (NRZ) encoding and optionally ensures sufficient data transitions by using the selected encoding scheme. Parallel data is then transferred into the device logic using the RXUSRCLK clock. For short channels, the transceivers offer a special low-power mode (LPM) to reduce power consumption by approximately 30%.

The receiver DC automatic gain control and linear and decision feedback equalizers can optionally "auto-adapt" to automatically learn and compensate for different interconnect characteristics. This enables even more margin for 10G+ and 25G+ backplanes.

Out-of-Band Signaling

The transceivers provide out-of-band (OOB) signaling, often used to send low-speed signals from the transmitter to the receiver while high-speed serial data transmission is not active. This is typically done when the link is in a powered-down state or has not yet been initialized. This benefits PCIe and SATA/SAS applications.

GTM Transceivers

The serial transmitter and receiver are independent circuits that use an advanced phase-locked loop (PLL) architecture to multiply the reference frequency input by certain programmable numbers between 16 and 160 to become the bit-serial data clock. Each transceiver has a large number of user-definable features and parameters. All of these can be defined during device configuration, and many can also be modified during operation.

Transmitter (GTM)

The transmitter is fundamentally a parallel-to-serial converter. These transmitter outputs drive pulse amplitude modulated signals with either four levels (PAM4) or two levels (NRZ) to the PC board with a single-channel differential output signal. TXOUTCLK is the appropriately divided serial data clock and can be used directly to register the parallel data coming from the internal logic. The incoming parallel data can optionally leverage a Reed-Solomon, RS(544,514) Forward Error Correction encoder and/or 64b66b data encoder. The bit-serial output signal drives two package pins with PAM4 differential signals. This output signal pair has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to reduce power consumption.

Receiver (GTM)

The receiver is fundamentally a serial-to-parallel converter, changing the incoming PAM4 differential signal into a parallel stream of words. The receiver takes the incoming differential data stream, feeds it through automatic gain compensation (AGC) and a continuous time linear equalizer (CTLE), after which it is sampled with a high-speed analog to digital converter. Further equalization is completed digitally via a decision feedback equalizer (DFE) and feed forward equalizer (FFE) implemented in DSP logic before the recovered bits are parallelized and provided to the PCS. This equalization provides the flexibility to receive data over channels ranging from very short chip-to-chip to high loss backplane applications across all supported rates. Clock recovery circuitry generates a clock derived from the high-speed PLL to clock in serial data and provides an appropriately divided and phase-aligned clock, RXOUTCLK, to internal logic.

Parallel data can optionally be transferred into an RS-FEC and/or 64b/66b decoder before being presented to the programmable logic interface.

GTM2 Transceivers

The GTM2 consists of a transmitter and receiver pair that are capable of sending and receiving high-speed serial data using non-return to zero (NRZ) or pulse amplitude modulation with 4-levels (PAM4), signaling at rates from 1.25 Gb/s NRZ to 112 Gb/s PAM4. To achieve these rates, the GTM2 can use a selection of the ring oscillator-based PLLs (RPLLs) and LC-oscillator-based PLLs (LCPLLs) to multiply an input reference clock by values from 16 to 160, including non-integer values. The GTM2 supports a wide variety of features often required by serial protocols, including 8b10b or 64b66b encoding, gray encoding, and transmit and receive FIFOs for frequency and phase compensation. The GTM2 is instantiated in groups of four, referred to as GTM2 quads, though individual quads can be shared or combined as necessary via the Versal adaptive SoC transceiver wizard subsystem IP.

Transmitter (GTM2)

The transmitter is fundamentally a parallel-to-serial converter. These transmitter outputs drive pulse amplitude modulated signals with either four levels (PAM4) or two levels (NRZ) to the PC board with a single-channel differential output signal. TXOUTCLK is the appropriately divided serial data clock and can be used directly to register the parallel data coming from the internal logic. The bit-serial output signal drives two package pins with PAM4 or NRZ differential signals. This output signal pair has programmable signal swing as well as multiple programmable pre- and post-emphasis taps to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing and emphasis can be lowered to reduce power consumption and enhance performance.

Receiver (GTM2)

The receiver is fundamentally a parallel-to-serial converter, changing the incoming PAM4 or NRZ differential signal into a parallel stream of words. The receiver takes the incoming differential data stream, feeds it through automatic gain compensation (AGC) and a continuous time linear equalizer (CTLE), after which it is sampled with a high-speed analog to digital converter. Further equalization is completed digitally via a decision feedback equalizer (DFE) and feed forward equalizer (FFE) implemented in DSP logic before the recovered bits are parallelized and provided to the PCS. This equalization provides the flexibility to receive data over channels ranging from very short chip-to-chip to high loss backplane applications across all supported rates. Clock recovery circuitry generates a clock derived from the high-speed PLL to clock in serial data and provides an appropriately divided and phase-aligned clock, RXOUTCLK, to internal logic.

GTR Transceivers

The GTR transceivers support data rates of up to 10.0 Gb/s to enable the USB3.2 Gen2 and DisplayPort 1.4 integrated IP. The GTR transceivers are connected directly to their adjacent protocol IP for ease of integration. Configured through the PS-Wizard, up to two lanes can be used to support USB3.2 or up to four lanes can be used to support DisplayPort 1.4.

A GTR Quad (4 duplex TX/RX pairs) can support following configurations:

- 1 or 2 lanes of USB3.2
- 1 or 2 lanes of USB3.2 and 1 or 2 lanes of DisplayPort 1.4
- 1, 2 or 4 lanes of DisplayPort 1.4

Integrated Block for PCI Express

The Versal architecture uses different types of integrated blocks to enable PCIe designs. Versal devices can contain one or more instances of a programmable logic integrated block for PCIe designs (PL PCIE), which reside in the PL as illustrated in Figure 1. Versal devices can also contain one CPM, which resides adjacent to the processing system as illustrated in Figure 2. Multiple versions of both these integrated blocks exist in the Versal architecture. Some devices also include an MDB, which resides adjacent to the processing system. Details are shown in Table 24.

PL PCIE

PL PCIE communicates with the adjacent serial transceivers and supports the protocols, data rates, and link widths shown in Table 24. Each PL PCIE can be configured as an Endpoint or Root Port. The Root Port configuration can be used to build the basis for a compatible Root Complex, to allow custom chip-to-chip communication via the PCI Express protocol, and to attach endpoint devices, such as Ethernet controllers or Fibre Channel HBAs, to the device. For high-performance applications, advanced buffering techniques of the PL PCIE offer a flexible maximum payload size. The PL PCIE interfaces to the integrated high-speed transceivers for serial connectivity and to PL memory resources for data buffering. Combined, these elements implement the Physical Layer, Data Link Layer, and Transaction Layer of the PCI Express protocol.

CPM

The CPM has dedicated connects to a set of 16 adjacent serial transceivers and supports the protocols, data rates, and link widths shown in Table 24. The CPM contains sub-blocks for two PCIe functions, one or two optional DMA controllers, plus an optional coherent cache function. Both sub-blocks for PCIe can be configured as an Endpoint, and depending on the CPM version, either one or both of these sub-blocks has access to the available DMA controllers and can also be configured as a Root Port. The DMA controllers provide dedicated connections to the NoC.

The CPM also incorporates cache coherent interconnect functionality to allow construction of accelerator designs with CXL® interfaces. The CPM is configured separately from the PL, enabling the CPM to become operational early in the boot sequence.

MDB

The MDB has dedicated connections to a set of four integrated serial transceivers and supports the protocols, data rates, and link widths shown in Table 24. The MDB contains sub-blocks for up to two subsystems for PCIe, each subsystem including a controller, a bridge, and an optional DMA. Each subsystem can be configured as an Endpoint or a Root Port. The DMA/Bridge functions are tightly coupled to the processing system interconnect. The MDB is configured separately from the PL, enabling the MDB to become operational early in the boot sequence.

Table 24: **Supported Protocols, Data Rates, and Link Widths**

	PL PCIE4	CPM4	PL PCIE5	CPM5	CPM6	MDB5
Governing Specifications	PCI Express Base Specification Rev 4.0	PCI Express Base Specification Rev 4.0	PCI Express Base Specification Rev 5.0	PCI Express Base Specification Rev 5.0	PCI Express Base Specification Rev 6.1 Compute Express Link Specification Rev 3.1	PCI Express Base Specification Rev 5.0
Max. PCIe Link Configurations	Gen4x8 Gen3x16	Gen4x16 2 x Gen4x8	Gen5x4 Gen4x8 Gen3x16	2 x Gen5x8 Gen4x16 2 x Gen4x8	2 x Gen6x8 2 x Gen5x8 2 x Gen4x8 2 x Gen3x8	Gen5x4 2 x Gen5x2 Gen5x2
Key PCIe Features	SR-IOV 4PF / 252VF	SR-IOV 4PF / 252VF	SR-IOV 8PF / 2KVF	SR-IOV 16PF / 4KVF	SR-IOV 8PF / 256VF IDE, PTM	SR-IOV 8PF / 64VF
Optional Integrated DMAs	–	Choice of one: QDMA (2K queues) or XDMA	–	2 x QDMA (4K queues)	2 x CPM6 DMA / bridge (64 Read/Write channels)	Up to 2 x MDB5 DMA / bridge (8 Read/Write channels)
CXL Features	–	–	–	–	CXL 3.1 256B FLIT CXL 2.0 68B FLIT	–

Ethernet

The Versal architecture contains integrated blocks for Ethernet functionality capable of operating at different data rates.

600G Channelized Multirate Ethernet Subsystem (DCMAC)

The 600G channelized multirate Ethernet subsystem provides up to 600G of Ethernet bandwidth that can be configured for various rates including 1x400GE, 3x200GE, and 6x100GE. The DCMAC handles all protocol-related functions of an Ethernet MAC, PCS, and FEC, including handshaking, synchronizing, and error checking. It also provides a segmented AXI4-Stream interface for packet data and an AXI4-Lite interface for statistics and management.

The DCMAC can be configured to include forward error correction (FEC) capability, supporting: Clause 91 RS(528, 514) KR4 FEC; Clause 91 RS(544, 514) KP4 FEC; Clause 119 RS(544, 514) KP4 FEC, and Clause 134 RS(544, 514) FEC.

The DCMAC flexible interface (FLEXIF) supports several operating modes including OTN mode, FlexE mode, and PCS mode.

Multirate Ethernet MAC (MRMAC)

The multirate Ethernet MAC (MRMAC) provides high-performance, low latency Ethernet ports supporting a wide range of customization and statistics gathering. Supported configurations are: 1 x 100GE; 2 x 50GE; 1 x 40GE; 4 x 25GE; and 4 x 10GE.

The MRMAC supports the following FECs defined and required by IEEE standards: Clause 91 RS(528, 514) KR4 FEC, for 25/50/100GE NRZ support; Clause 91 RS(544, 514) KP4 FEC for 50/100GE PAM4 support; and Clause 74 FEC, for 10/25/40/50GE low-latency support. The MRMAC has a rich set of bypass modes to enable access to FEC-only mode (for custom protocols) and FEC+PCS (for protocol testers).

The MRMAC also supports a new high-precision timestamping feature to enable sub-nanosecond accuracy on IEEE Std 1588 timestamps. This provides hardware support for new IEEE Std 1588-based time-sensitive networks (TSN) as well as the next generation Ethernet-based wireless fronthaul protocol (eCPRI).

600G Interlaken with FEC

The integrated 600G Interlaken block with FEC supports channelized interfaces operating up to 600 Gb/s with built-in flow control. Each 600G Interlaken block can be configured as 12x56.42G, 24x28.21G, or 24x12.5G. The flexible AXI-Stream user interface is configurable in width from 2048b to 512b. Pairs of lanes share 100G RS(544, 514) FEC and can support FEC-only mode.

High-Speed Crypto (HSC) Engine

The High-Speed Crypto (HSC) Engine implements an AES-GCM-256/128 engine that provides up to 400 Gb/s of bulk encryption capability on up to 40 channels that can be connected to the DCMAC. Each HSC Engine supports both MACSec and IPSec at up to 400 Gb/s configurable as 1x400G, 2x200G, or 4x100G channels with up to 128 Source Addresses (SA) per 100G.

I/O

Four types of programmable I/Os exist in the programmable logic with additional I/Os available in the processing system. See Table 25.

Table 25: **Programmable I/O**

I/O Type	X5IO	XPIO	HDIO	MIO
Voltage	1.0V–1.2V	1.0V–1.5V	1.8V–3.3V	1.8V–3.3V
Purpose	Highest performance, DDR5, LPDDR5, LPDDR5X	High performance, DDR4, LPDDR4	Lower performance, wider voltage range	Support processing system peripherals

X5IO

X5IO are optimized for high-performance communication including, but not limited to, interfacing to DDR5, LPDDR5, and LPDDR5X memory through the integrated memory controller blocks. X5IO are arranged in banks of 32 I/O and organized as two groups of four 8-bit octads. X5IO support standards with maximum supply voltage of 1.2V. Every X5IO bank includes a physical layer interface (PHY) that can operate in 4:1, 8:1, and 16:1 modes.

XPIO

XPIO are optimized for high-performance communication including, but not limited to, interfacing to DDR4 memory through the integrated memory controller blocks. XPIO are arranged in banks of 54 I/O and organized as nine 6-bit nibbles. XPIO support standards with maximum supply voltage of 1.5V. Every XPIO bank includes a physical layer interface (PHY) that can operate in 4:1 mode for use with the integrated memory controllers or 8:1 mode for use with custom circuitry.

HDIO

High-density I/O (HDIO) banks are designed to be a cost-effective method for supporting lower speed, higher voltage range I/O standards. Arranged in banks of 22, the number of HDIO varies depending on Versal device and package. HDIOs offer single-ended I/O including 3.3V and 2.5V LVTTL and LVCMOS. HDIOs also offer differential receivers for low-speed clock inputs and pseudo-differential transmitters. There is Internal V_{REF} support. The system designer can specify the slew rate and the output strength. The input is always active but is usually ignored while the output is active. Each pin can optionally have a weak pull-up resistor, a weak pull-down resistor, or weak keeper.

MIO

Multiple banks of general-purpose I/O are implemented within the processing system and platform management controller, each with a dedicated power supply. The main category of I/O are the three banks of multiplexed I/O (MIO), which can be accessed by the processing system and the platform management controller. Fixed-function I/O are also available for control and configuration functions.

RF-ADC and RF-DAC

The RF-ADCs and RF-DACs are implemented in a tile structure. Each tile has an RF-sample PLL clock and either four RF-ADCs and eight digital-down conversion (DDC) blocks, or four RF-DACs and eight digital-up conversion (DUC) blocks. The RF-ADC and RF-DAC tiles contain additional digital logic for coarse and fine mixing, optional filtering, and signal processing. RF-ADC tiles are available in two configurations: quad and single. Quad tiles have all four RF-ADCs operating independently while a single tile time-interleaves all four RD-ADCs to provide a single RF-ADC sampling at 4x the individual RF-ADC rate. Quad and single RF-ADC configurations are not configurable but are package compatible. Foreground and background RF-ADC calibration is included to minimize interleaving spurs. Clocks can be forwarded between tiles to simplify system design, and devices support multi-tile synchronization using SYSREF signal.

The RF-ADC tiles have the following features:

- Quad and single (4x sample rate) RF-ADC tile configurations
  - Up to 8 GSPS in quad configuration, 32 GSPS in single configuration
  - 14-bit resolution with calibration
- Up to 18 GHz input frequency
  - Operates to DC
- 2 DDCs per RF-ADC
  - Multiband support
- Hard channelizer
- Foreground and background calibration
- Quadrature modulator correction
  - Gain/phase/offset correction per RF-ADC pair

The RF-DAC tiles have the following features:

- Quad tile configurations
  - Up to 16 GSPS in quad configuration
  - 14-bit resolution with calibration
- Up to 18 GHz output frequency
  - Inverse sinc and mix-mode filters
  - 1st, 2nd, and 3rd Nyquist zone operation
- 2 DUCs per RF-DAC
  - Multiband support
- Hard inverse channelizer
- Quadrature modulator correction
  - Gain/phase/offset correction per RF-DAC pair

Signal Processing Integrated IP

Some Versal devices include integrated signal processing blocks to increase compute at a lower total power consumption. The signal processing blocks are FFT/iFFT, channelizer, LDPC decoder, and poly block. Each IP block is optimized to provide additional compute for typical signal processing applications at lower power than with full programmable logic implementations.

FFT/iFFT

- Streaming architecture supports up to 4 GSPS throughput with 500 MHz clocking and one, two, four, or eight parallel I/O samples per cycle
- Supports power-of-2 FFT with point sizes ranging from 8 to 4096
- Point size and transform direction are switchable on a block-by-block basis
- Supports scaled 16-bit or 18-bit I/Q inputs and 16-bit, 18-bit, or unscaled 31-bit I/Q outputs

Channelizer

- Operates as an 8-channel channelizer/inverse channelizer, or up to an 8-channel FIR filter
- Supports throughputs up to 2 GSPS as a channelizer or inverse channelizer, and up to 1 GSPS as a single FIR filter
- Optional support for an oversampled by 2X channelizer or inverse channelizer
- Supports 16-bit or 18-bit I/Q fixed-point inputs and outputs
- Provisions a flexible FIR unit cascade capable of supporting:
    - 64 taps (real) or 32 taps (complex) per phase for each of 8 channels when operating as a channelizer or inverse channelizer
    - 32 taps (real) or 16 taps (complex) per phase for each of 8 channels when operating as an oversampled channelizer or inverse channelizer
    - 64 taps (real) or 32 taps (complex) when operating as an asymmetric filter
    - 128-taps (real) or 64 taps (complex) when operating as a symmetric filter

LDPC Decoder

- Implements streaming LDPC decoding of quasi-cyclic codes including standard codes from DVB/S2X, 5G wireless, IEEE Ste 802.11 WIFI, and DOCSYS
- Supports peak throughputs on the order of:
    - 4 Gb/s DVB-S2 LDPC decoder @ 8 iterations
    - 3.7 Gb/s DVB/S2X LDPC decoer @ 8 iterations
    - 7.7 Gb/s 5G LDPC decoder @ 8 iterations
- Performs normalized min-sum or offset min-sum soft-decision decoding algorithms

- Supports configurable saturation of LLR values, programmable number of decoding iterations, early termination based on parity check status, or info/parity stasis

Poly Block

- Flexible polyphase engine for building a variety of high-performance DSP functions:
  - Multi-channel FIR filter with up to 8 coefficient sets
  - Single-channel FIR filter supporting up to 128 taps (real) up to 8 GSPS
  - Channelizer supporting 8 channels up to 128 taps (real) up to 1 GSPS
  - Arbitrary rate resampler supporting up to 64 taps (real) up to 8 GSPS
  - Matrix multiply supporting (16 x 16) x (16 x 1) configurations
- Supports 16-bit I/Q I/O and 24-bit (real) coefficients
- Supporting 1 GHz core operation with 500 MHz I/O interface & up to SSR=8

Clocking

Multiple clock generation blocks are used to synthesize clock frequencies. Clock buffers and routing connect the signals to their destinations.

Processing System Clocking

All clocks in the processing system belong to one of three groups: the main PLL clocks; the internal ring oscillator clock and interface clocks.

Main PLL Clocks

The majority of the logic in the processing system is clocked from the three PLLs in the processing system and one PLL in the platform management controller through user configurable clock divider circuits. These divider circuits generate clocks to all CPUs, main interconnects, the platform management controller, and all peripherals. The clocks and their associated PLLs are spread across three power domains: the PMC domain, containing the platform management controller; the low-power domain, containing the RPU and all peripheral clocks; and the full-power domain, containing all other clocks and their PLLs.

Internal Ring Oscillator

The platform management controller operates as the security manager for the device and uses a clock provided by an internal ring oscillator.

Interface Clocks

This category includes clocks that are directly supplied from outside the processing system and includes clocks for the external interfaces, including Ethernet, USB, SWDT, and CAN-FD.

PL Clocking

Clock signals travel around the Versal devices on a network of bidirectional, horizontal, and vertical routing tracks that support many independent clock networks. The vertical tracks reside adjacent to the NoC columns. The programmable logic is divided into clock regions that each have a horizontal clock spine through the middle that can carry 24 clock signals. Clock signals travel along these horizontal clock spines and are then driven into the individual clocked elements within the PL such as flip-flops, DSP Engines, block RAM, and UltraRAM. Clock buffers and clock management components reside adjacent to the XPIO rows on south and (sometimes) north edges of the device.

Clock Management

To generate multiple clock frequencies and phases from an input clock source, Versal devices contain mixed-mode clock managers (MMCMs) and phase-locked loops (PLLs). MMCMs reside adjacent to the horizontal NoC row adjacent to the XPIO and PLLs reside in the XPIO banks. The MMCM and PLL share many characteristics. Both can serve as a frequency synthesizer for a wide range of frequencies and as a jitter filter for incoming clocks. At the center of both components is a voltage-controlled oscillator (VCO), which speeds up and slows down depending on the input voltage it receives from the phase frequency detector (PFD).

There are three sets of programmable frequency dividers: D, M, and O. The predivider D, programmable by configuration and afterwards via the dynamic reconfiguration port (DRP), reduces the input frequency and feeds one input of the traditional PLL phase/frequency comparator. The feedback divider M (programmable by configuration and afterwards via DRP) acts as a multiplier because it divides the VCO output frequency before feeding the other input of the phase comparator. D and M must be chosen appropriately to keep the VCO within its specified frequency range. The VCO has eight equally spaced output phases (0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°). Each can be selected to drive one of the output dividers (six for the PLL, O0 to O5, and seven for the MMCM, O0 to O6), each programmable by configuration to divide by any integer from 1 to 128.

MMCM additional programmable features: The MMCM has a fractional counter in either the feedback path (acting as a multiplier) or in one output path. Fractional counters allow non-integer increments of 1/8 and can thus increase frequency synthesis capabilities by a factor of 8. The MMCM can also provide fixed or dynamic phase shift in small increments that depend on the VCO frequency.

Memory Controllers

Versal architecture contains different types of dedicated memory controllers. Each memory controller has four bidirectional 128-bit system ports and contains a scheduler with transaction reordering capability to improve memory access efficiency. The memory controller operates at half the DRAM clock rate. For example, if the DRAM data rate per bit is 3200 Mb/s, then the DRAM clock rate is 1600 MHz, and the memory controller clock rate is 800 MHz. The memory controllers talk to the dedicated memory PHY (XPHY) in the XPIO banks which, in turn, interface with the I/O pins.

Table 26: **Supported Standards and Features**

	DDRMC	DDRMC5c	DDRMC5e	DDRMC5x
Supported Standards	DDR4 LPDDR4	DDR5 LPDDR5	DDR5 LPDDR5X	DDR5 LPDDR5X
Features	Sideband ECC	Sideband ECC Inline ECC XTS GCM	Sideband ECC Inline ECC XTS GCM w/ countermeasures	Sideband ECC (x16 only) Inline ECC

Stacked Silicon Interconnect (SSI) Technology

The Versal architecture uses the established SSI technology to build 3D ICs that exceed what can be achieved using monolithic die. SSI technology enables multiple super-logic regions (SLRs) to be combined on a passive interposer layer, using proven manufacturing and assembly techniques from industry leaders. Signals travel between adjacent SLRs through many distributed, low-latency connections.

Table 27 shows the number of SLRs in devices that use SSI technology and their dimensions.

Table 27: **SLR Count and Dimensions**

		Versal Premium Series							Versal HBM Series[1]				
	Device	VP1502	VP1552	VP1702	VP1802	VP2502	VP2802	VP1902	VH1522	VH1542	VH1582	VH1742	VH1782
# SLRs		2	2	3	4	2	4	4	2	2	2	3	3
SLR Width (in Regions)		10	10	10	10	10	10	9	10	10	10	10	10
Height (in Regions)	SLR3	–	–	–	6	–	6	12	–	–	–	–	–
	SLR2	–	–	6	6	–	6	12	–	–	–	6	6
	SLR1	6	6	6	6	6	6	12	6	6	6	6	6
	SLR0	7	7	7	7	7	7	12	7	7	7	7	7

Notes:

1. Versal HBM Series information refers to logic SLRs only.

High Bandwidth Memory (HBM)

Versal HBM devices, built on SSI technology, include high bandwidth memory (HBM) DRAM integrated on the same silicon interposer as the SLRs. One or two, 4-high or 8-high stacks of memory are available, delivering a maximum capacity of 32 GB. The HBM interfaces with the SLRs through the silicon interposer with 16 channels of 64 bidirectional data signals per memory stack.

Video Decoder Unit (VDU)

The video decoder unit (VDU) comprises two or four video decoder engines (VDEs) containing a decode or decompress function supporting H.264 and H.265 standards. Each VDE can be used stand-alone, or they can be combined to achieve higher throughput. Maximum throughput is shown in Table 28.

Table 28: **VDE Supported Modes**

One VDE	Two VDEs	Four VDEs
1 x 4Kp60 2 x 4Kp30 8 x 1080p30 16 x 720p30 32 x 720p15	2 x 4Kp60 4 x 4Kp30 16 x 1080p30 32 x 720p30 64 x 720p15	4 x 4Kp60 8 x 4Kp30 32 x 1080p30 64 x 720p30 128 x 720p15

The VDU interfaces to the PL via two 128-bit master AXI ports for decoder access to memory, one 32-bit AXI master port for MCU access to memory, and one 32-bit APB or AXI-Lite slave port for register programming.

GPU

Versal AI Edge Series Gen 2 and Prime Series Gen 2 contain an Arm Mali™-G78AE graphics processor unit (GPU) that uses a unified shader core architecture. The single shader processor core type can execute all types of shader code including vertex shaders, fragment shaders, and compute kernels. All cores have access to a shared L2 cache to reduce wasted memory bandwidth due to repeated data fetches. The GPU can be configured as a single partition with four shader cores or two partitions with two shader cores each.

Supported pixel formats include RGB 8/10/16 bit in a variety of container formats, YUV In 8/10/16 bit, and YUV Out 8/10 bit. Adaptive scalable texture compression (ASTC) is supported in both low dynamic range (LDR) and high dynamic range (HDR), enabling support for both 2D and 3D images. Arm frame buffer compression (AFBC) v1.3 supports 4x4 pixel block size.

Image Signal Processor

The image signal processor (ISP) contains one to three ISP tiles for preprocessing raw image sensor data. Each ISP tile supports a maximum pixel rate of 600 megapixels per second with a maximum horizontal or vertical resolution of 4096 pixels. Input pixel depth in linear and compressed formats are supported.

ISP tiles are compatible with standard Bayer input (RGGB, GRBG, BGGR), monochrome (CCCC), RYYCy, RCCG, RCCC, and RGB-IR sensor types. An AXI4-Stream interface accepts streaming live data from a MIPI CSI-2 interface. ISP tiles also accept memory-input data from DMA read functionality and input test patterns from an in-built test pattern generator (TPG).

Video output formats such as YUV 4:2:0, YUV 4:2:2, Y only, 8 or 10 bits per component, and RGB888 are supported through AXI4-streaming for live out, and AXI4-memory mapped interfaces for memory out. Each ISP has dual output capability enabling primary output and secondary output with separate controls. One input stream can be processed by a single ISP tile for different primary and secondary output streams. RGB-IR image sensor data can be processed to provide RGB data on the primary output and IR data on the secondary output. In the memory out I/O type, both primary and secondary output DMA support raster half-DWORD aligned frame buffer format suitable for 10-bit max color depth.

Video Codec Unit

The video codec unit (VCU) in some Versal AI Edge Series Gen 2 and Prime Series Gen 2 devices provides HEVC/AVC encoding and decoding. Each video encoder instance supports up to 4K60 4:4:4 12-bit single stream. Each video decoder engine supports up to 4K60. The VCU can simultaneously encode and decode up to 32 streams with a maximum aggregated bandwidth of 3840x2160 @ 60 fps.

The VCU supports: H.264, H.265, and JPEG (decode) standards; 4:2:0, 4:2:2, 4:4:4, and monochrome formats; and 8-, 10-, and 12-bit depths. DCI 4K (4096x2160) @ 60 fps is supported. The encoder supports DCI 4K60 with 950 MHz, and the decoder supports DCI4K60 with 918 MHz.

Ordering Information

Table 29 shows the speed and temperature grades available in the different device series.

Table 29: **Speed Grade and Temperature Grade**

Series	XC Devices	Speed, Voltage, Static Power, and Temperature Information		
		Extended		Industrial
		0° to +100°C	0° to +110°C(1)	–40° to +110°C(1)
AI Edge Gen 2	2VE3304 2VE3358 2VE3504 2VE3558 2VE3804 2VE3858	-1MSE	-2MSE	-2MSI
		-1LSE	-2MLE	-2MLI
			-2LSE	-1MSI
			-2LLE	-1MLI
				-2LLI
				-1LSI
				-1LLI
AI Edge	VE2002 VE2102 VE2202 VE2302 VE1752 VE2602 VE2802	-1MSE	-2MSE	-2HSI
		-1LSE	-2MLE	-2MSI
			-2LSE	-2MLI
			-2LLE	-1MSI
				-1MLI
				-2LLI
				-1LSI
				-1LLI
AI Core	VC1502 VC1702 VC1802 VC1902 VC2602 VC2802	-1MSE	-2MSE	-2HSI
		-1LSE	-2MLE	-2MSI
			-2LSE	-2MLI
			-2LLE	-1MSI
				-1MLI
				-2LLI
				-1LSI
				-1LLI
Prime Gen 2	2VM3358 2VM3558 2VM3654 2VM3858	-1MSE	-2MSE	-2MSI
		-1LSE	-2MLE	-2MLI
			-2LSE	-1MSI
			-2LLE	-1MLI
				-2LLI
				-1LSI
				-1LLI

Table 29: **Speed Grade and Temperature Grade *(Cont'd)***

Series	XC Devices	Speed, Voltage, Static Power, and Temperature Information		
		Extended		Industrial
		0° to +100°C	0° to +110°C[1]	–40° to +110°C[1]
Prime	VM1102 VM1302 VM1402 VM1502 VM1802 VM2202	-1MSE	-2MSE	-2HSI
		-1LSE	-2MLE	-2MSI
			-2LSE	-2MLI
			-2LLE	-1MSI
				-1MLI
				-2LLI
				-1LSI
				-1LLI
	VM2152	-1MSE	-2MSE	-2HSI
		-1LSE	-2MLE	-2MSI
			-2LSE	-2MLI
			-2LLE	-1MSI
				-1MLI
				-1LSI
				-1LLI
	VM2302 VM2502 VM2902	-3HSE	-2MSE	-2MSI
		-1MSE	-2MLE	-2MLI
		-1LSE	-2LSE	-1MSI
			-2LLE	-1MLI
				-1LSI
				-1LLI
Premium Gen 2	2VP3102 2VP3202	-1MSE	-2MSE	-2HSI
		-1LSE	-2MLE	-2MSI
			-2LSE	-2MLI
			-2LLE	-1MSI
				-1MLI
				-1LSI
				-1LLI
	2VP3402 2VP3502 2VP3602	-3HSE	-2MSE	-2MSI
		-1MSE	-2MLE	-2MLI
		-1LSE	-2LSE	-1MSI
			-2LLE	-1MLI
				-1LSI
				-1LLI

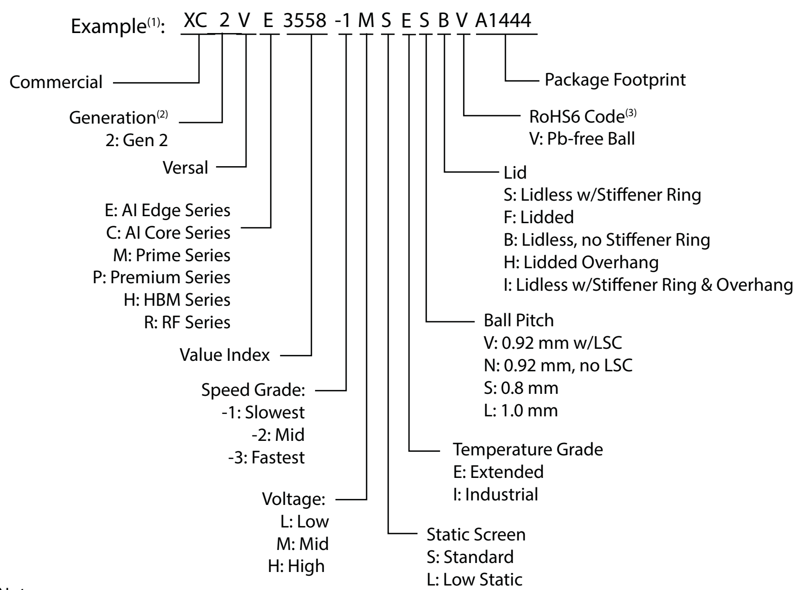
Table 29: **Speed Grade and Temperature Grade *(Cont'd)***

Series	XC Devices	Speed, Voltage, Static Power, and Temperature Information		
		Extended		Industrial
		0° to +100°C	0° to +110°C[(1)]	–40° to +110°C[(1)]
Premium	VP1002 VP1052	-1MSE	-2MSE	-2HSI
		-1LSE	-2MLE	-2MSI
			-2LSE	-2MLI
			-2LLE	-1MSI
				-1MLI
				-2LLI
				-1LSI
				-1LLI
	VP1102 VP1202 VP1402 VP1502 VP2502 VP1552 VP1702 VP1802 VP2802	-3HSE	-2MSE	-2MSI
		-1MSE	-2MLE	-2MLI
		-1LSE	-2LSE	-1MSI
			-2LLE	-1MLI
				-1LSI
				-1LLI
	VP1902	-3HSE	-2MSE	
		-1MSE	-2MLE	
		-1LSE	-2LSE	
			-2LLE	
HBM	All	-3HSE	-2MSE	
		-1MSE	-2MLE	
		-1LSE	-2LSE	
			-2LLE	
RF	VR1602 VR1652 VR1902 VR1952	-1MSE	-2MSE	-2HSI
		-1LSE	-2MLE	-2MSI
			-2LSE	-2MLI
			-2LLE	-1MSI
				-1MLI
				-2LLI
				-1LSI
				-1LLI

Notes:

1. In extended and industrial temperature grades, some ordering combinations can operate for a limited time with a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage. Operation at 110°C Tj is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of device lifetime.

The ordering information shown in Figure 3 applies to Versal devices.



Notes:
1. Mechanical samples are available. Contact Sales for information.
2. This character is only present in Versal AI Edge Series Gen 2, Prime Series Gen 2, or Premium Series Gen 2 devices.
3. All packages have Pb-free bumps.

DS950_03_041725

Figure 3: **Versal Device Ordering Information**

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
11/10/2025	2.7	Updated Table 2 (Versal AI Edge Series Gen 2) and Table 13 (Versal Premium Series Gen 2). Updated Signal Processing Integrated IP and Table 18 (Versal RF Series). Removed CCIX.
06/30/2025	2.6	Updated Table 3 (SBVA1440 package to SSVA1440 package), Table 8 (updates to 2VM3654), and Table 9 (SBVA1440 package to SSVA1440 package).
05/22/2025	2.5	Added DSP Cascade information to Digital Signal Processing (DSP) and in device tables. Added 2VP3502 device in Table 12, Table 13, Table 20, and Table 29. Added MDB and GTR Transceivers section.s Updated Table 2, Table 4, Table 6, Table 8, Table 10, Table 12, Table 13, Table 14, Table 16, Table 18, Arm Cortex-R5F, On-Chip Memory (OCM), Accelerator RAM, Digital Signal Processing (DSP), Table 24 (added MDB5), X5IO, and Figure 3.
12/10/2024	2.4	Added Versal RF Series throughout document. Updated General Description, Table 1, Connectivity, Table 2, Table 20, Table 21, RF-ADC and RF-DAC, Table 29, and Figure 3. Added Table 18, Table 19, Table 22, and Signal Processing Integrated IP.
11/12/2024	2.3	Added Versal Premium Series Gen 2 throughout document. Updated General Description, Table 1, Table 3, Table 8, Table 9, Table 20, Table 24, Table 25, Table 29, and X5IO. Added Table 12, Table 13, Table 23, LDPC Decoder, GTM2 Transceivers, and Table 26. General update of the Processing System.
06/04/2024	2.2	Updated Table 2 and Table 29.
04/24/2024	2.1	Updated Table 5, Table 7, Table 11, Table 15, and Table 17.
04/09/2024	2.0	Added AI Edge Series Gen 2 and Prime Series Gen 2 throughout document. Updated General Description, Table 1, Compute and Acceleration (summary), Compute and Acceleration Engines, Processing System, Ordering Information, and Figure 3. Added AI Edge Series Gen 2 resource (Table 2) and packaging information (Table 3). Added Prime Series Gen 2 resource (Table 8) and packaging information (Table 9). Added PSX Processing System, GPU, Image Signal Processor, and Video Codec Unit. Updated Table 20.
02/26/2024	1.21	Updated General Description, Figure 2, Table 1, Table 10, Table 11, Table 14, and Table 15 (added SBVJ1369 package).
11/14/2023	1.20	Added VM2152 device (Table 10, Table 11, Table 29). Added X5IO; updated Table 25. Updated Connectivity, page 3, and Memory Controllers.
09/25/2023	1.19	Removed VSVC2021 package from Premium series (Table 15). Removed Soft-Decision Forward Error Correction (SD-FEC) section.
06/27/2023	1.18	Updated Table 1, Table 6, Table 7, Table 10, Table 14, Table 15, Table 27, and Table 29. Added Primary Public Keys table (Table 20) and AI Engine Array Size (Table 21). Added VP1902 and VSVA6865 and VSVB6865 packages and Multiport RAM. Removed VC1352.
11/18/2022	1.17	Updated AI Edge series information in Table 4 and Table 5. Updated AI Core series information in Table 6 and Table 7. Added NSVH1369 package to VM2202 and VSVI1760 package to VM2502 and removed VSVC2197 in Table 11. Removed VSVC2197 from Table 15 and updated HDIO counts.
04/20/2022	1.16	Added four Premium devices to Table 14, Table 15, and Table 29: VP1002, VP1052, VP2502, and VP2802.
02/28/2022	1.15	Updated Table 1, Table 11, Table 14, and Table 15.
12/09/2021	1.14	Updated Table 1 and Table 29. Added table note to Table 4, Table 6, Table 10, Table 14, Table 15, and Table 16.
10/19/2021	1.13	Updated Table 1, Table 4, Table 5, Table 6, Table 7, Table 11, Table 15, Table 27, and Table 29.

Date	Version	Description of Revisions
07/14/2021	1.12	Added HBM series throughout document. Added Video Decoder Unit (VDU). Updated Table 1. Updated I/O information in Table 5, Table 7, Table 11, and Table 15. Updated package information in Table 11. Updated Table 29.
06/29/2021	1.11	Added VDU information to product tables. Updated package information in Table 5. Updated VC1502 in Table 6 and Table 7. Added note to Table 10. Made typographical edit to Table 11.
06/09/2021	1.10	Added AI Edge series throughout document. Added two AI Core devices to Table 6: VC2602 and VC2802. Updated Compute and Acceleration Engines.
04/26/2021	1.9	Added VM2202. Updated Table 6, Table 7, Table 10, Table 11, and Table 29.
02/26/2021	1.8	Updated Table 1, Table 7, Table 11, Table 15, and Figure 3. Added Table 29.
08/27/2020	1.7	Updated Table 1, Table 10, Table 11, and added Stacked Silicon Interconnect (SSI) Technology.
05/11/2020	1.6	Updated Table 10, Table 11, and Table 14.
03/10/2020	1.5.1	Typographical edits.
03/10/2020	1.5	Updated Table 1 and added Versal Premium series information throughout document.
01/16/2020	1.4	Updated Figure 3. Corrected revision history date of v1.3.
12/16/2019	1.3	Added Ordering Information. Updated Table 1, Table 6, Table 7, Table 10, Table 11, and Boot and Configuration.
07/03/2019	1.2	Updated External Flash Memory Interfaces and HDIO.
05/16/2019	1.1	Updated Table 1, Table 7, Table 10, Table 11, NoC, and Connectivity Peripherals.
10/02/2018	1.0	Initial release.

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