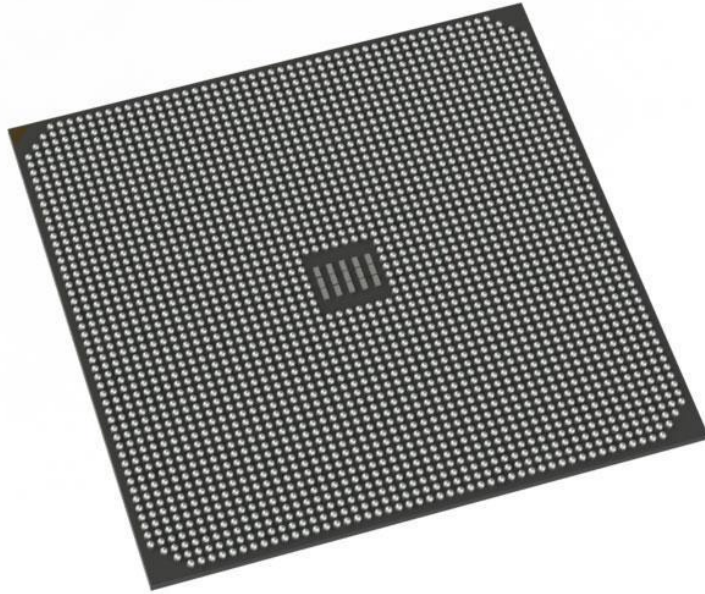


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XCVP1502-2LLEVSVA3340

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2LLEVSVA3340 Datasheet

DiGi Electronics Part Number XCVP1502-2LLEVSVA3340-DG

Manufacturer [AMD](#)

Manufacturer Product Number XCVP1502-2LLEVSVA3340

Description IC VERSAL PREM ACAP FPGA 3340BGA

Detailed Description Dual ARM® Cortex®-A72 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5F with CoreSight™ System On Chip (SOC) IC Versal® Premium Versal™ Premium FPGA, 3.7M Logic Cells 450MHz, 1.08GHz 3340-FCB GA (55x55)

Tel: +00 852 30501935

RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

XCVP1502-2LLEVSVA3340

Series:

Versal® Premium

Architecture:

MPU, FPGA

Flash Size:

-

Peripherals:

DDR, DMA, PCIe

Speed:

450MHz, 1.08GHz

Operating Temperature:

0°C ~ 100°C (TJ)

Supplier Device Package:

3340-FCBGA (55x55)

Manufacturer:

AMD

Product Status:

Active

Core Processor:

Dual ARM® Cortex®-A72 MPCore™ with CoreSight™, Dual ARM®Cortex™-R5F w

RAM Size:

256KB

Connectivity:

CANbus, EBI/EMI, Ethernet, I2C, MMC/SD/SDIO, SPI, UART/USART, USB OTG

Primary Attributes:

Versal™ Premium FPGA, 3.7M Logic Cells

Package / Case:

3340-BFBGA, FCBGA

Number of I/O:

486

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AMD Versal™ AI Core Series Product Selection Guide

AMD Versal™ AI Core Series – Resources

All parameters listed are maximum values. Verify all data in this document with the device data sheets or product guides.

	VC1502	VC1702	VC1802	VC1902	VC2602	VC2802	
AI Engine	AI Engines Tiles	198	304	300	400	0	0
	AI Engine-ML Tiles	0	0	0	0	152	304
	AI Engine Data Memory (Mb)	50	76	75	100	76	152
	AIE-ML Shared Memory (Mb)	0	0	0	0	304	304
Programmable Logic	System Logic Cells (K)	815	981	1,586	1,968	820	1,139
	LUTs	372,352	448,512	725,000	899,840	375,000	520,704
	DSP Engines	1,032	1,312	1,600	1,968	984	1,312
	Distributed RAM (Mb)	11	14	22	27	11	16
Memory	Total Block RAM (Mb)	30	34	28	34	17	21
	UltraRAM (Mb)	110	130	91	130	63	74
	Accelerator RAM (Mb)	0	0	0	0	0	0
	Total PL Memory (Mb)	151	178	141	191	91	111
	DDR Memory Controllers (DDRM/C)	3	3	4	4	3	3
	DDR Bus Width	192	192	256	256	192	192
Processing System	Application Processing Unit	Dual-core Arm® Cortex®-A72, 48 KB/32 KB L1 Cache w/ parity & ECC; 1 MB L2 Cache w/ ECC					
	Real-Time Processing Unit	Dual-core Arm Cortex-R5F, 32 KB/32 KB L1 Cache, and 256 KB TCM w/ECC					
	Memory	256 KB On-Chip Memory w/ECC					
	Connectivity	Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)					
Serial Transceivers	GTY Transceivers	32	44	44	44	0	0
	GTYP Transceivers	0	0	0	0	32 ⁽¹⁾	32 ⁽¹⁾
Integrated Protocol IP	PCIe® w/DMA (CPM4)	1 x Gen4x16	1 x Gen4x16	1 x Gen4x16	1 x Gen4x16	–	–
	PCIe w/DMA (CPM5)	–	–	–	–	2 x Gen5x8	2 x Gen5x8
	PCIe (PL PCIE4)	4 x Gen4x8	4 x Gen4x8	4 x Gen4x8	4 x Gen4x8	–	–
	PCIe (PL PCIE5)	–	–	–	–	4 x Gen5x4	4 x Gen5x4
	100G Multirate Ethernet MAC	3	4	4	4	2	2
Platform	Video Decoder Engines (VDEs)	–	–	–	–	2	4
	Platform Management Controller	Boot, Security, Safety, Monitoring, and High-Speed Debug					
Ordering Information	Extended Temp ⁽²⁾	-1MSE, -1LSE, -2MSE, -2MLE, -2LSE, -2LLE					
	Industrial Temp ⁽²⁾	-1MSI, -1MLI, -1LSI, -1LLI, -2MSI, -2MLI, -2LLI, -2HSI					

Notes:

- 16 GTYP transceivers are dedicated to CPM5 for PCI Express use.
- In extended and industrial temperature grades, some ordering combinations can operate for a limited time with a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage. Operation at 110°C Tj is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of device lifetime.

AMD Versal™ AI Core Series – Packaging

		VC1502	VC1702	VC1802	VC1902	VC2602	VC2802
Package	Package Dimensions (mm)	Ball Pitch (mm)	XPIO DDR Only, XPIO DDR+PL, XPIO PL Only HDIO, MIO GTY, GTYP				
NSVG1369	35x35	0.92	132, 246, 0 22, 78 24, 0	132, 246, 0 44, 78 24, 0			
NSVH1369	35x35	0.92				132, 192, 0 44, 78 0, 32	132, 192, 0 44, 78 0, 32
VSVA1596	37.5x37.5	0.92	132, 246, 0 22, 78 32, 0	132, 246, 0 44, 78 32, 0			
VIVA1596	40x40	0.92			132, 246, 0 44, 78 32, 0	132, 246, 0 44, 78 32, 0	
VSVD1760	40x40	0.92			186, 462, 0 0, 78 24, 0	186, 462, 0 0, 78 24, 0	
VSVH1760	40x40	0.92				186, 300, 0 44, 78 0, 32	186, 300, 0 44, 78 0, 32
VSVA2197	45x45	0.92	192, 294, 0 22, 78 32, 0	192, 294, 0 44, 78 44, 0	186, 462, 0 44, 78 44, 0	186, 462, 0 44, 78 44, 0	

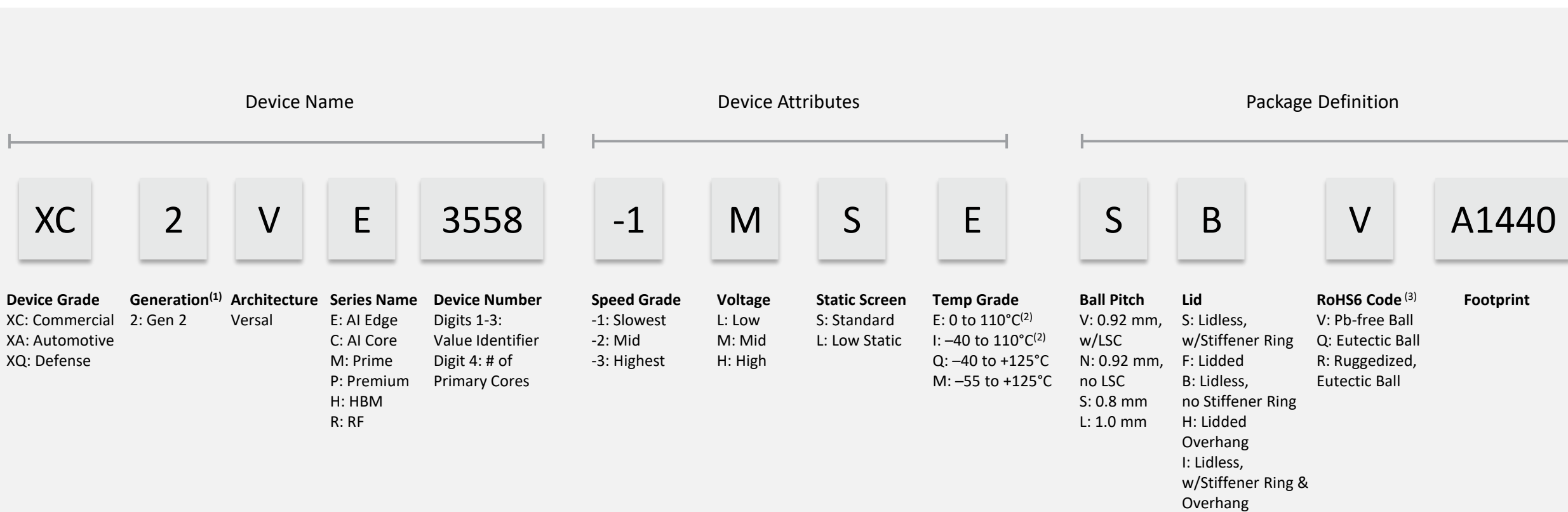
All parameters listed are maximum values. Verify all data in this document with the device data sheets or product guides.

AMD Versal™ AI Core Series – Figures of Merit

		VC1502	VC1702	VC1802	VC1902	VC2602	VC2802
AI Engine	AI Engine Peak Perf – INT8	TOPS	66	101	100	133	202
	AI Engine Peak Perf – INT8x16	TOPS	33	51	50	67	101
	AI Engine Peak Perf – INT16	TOPS	16	25	25	33	51
	AI Engine Peak Perf – CINT16	Complex TOPS	4.1	6.3	6.2	8.3	12.6
	AI Engine Peak Perf – FP32	TFLOPs	4.1	6.3	6.2	8.3	16.6
	AI Engine Peak SRAM Bandwidth	Tb/s	264	405	399	532	405
Programmable Logic	DSP Engine Peak Perf – INT8	TOPS	7.1	9.1	11.0	13.6	9.1
	DSP Engine Peak Perf – INT24	TOPS	2.4	3.0	3.7	4.5	3.0
	DSP Engine Peak Perf – CINT18	Complex TOPS	1.0	1.3	1.6	1.9	1.3
	DSP Engine Peak Perf – FP32	TFLOPs	1.7	2.1	2.6	3.2	2.1
Processing System	Arm® Cortex-A72 Performance	DMIPs	18,942	18,942	18,942	18,942	19,516
	Arm Cortex-R5F Performance	DMIPs	2,672	2,672	2,672	2,672	2,672
Memory	Total Bandwidth - Block RAM	Tb/s	122	137	115	139	86
	Total Bandwidth - Ultra RAM	Tb/s	41	49	35	49	28
	Total Bandwidth - Accelerator RAM	Tb/s	0.0	0.0	0.0	0.0	0.0
	Total SRAM Bandwidth	Tb/s	164	186	150	188	114
I/O	Transceiver Bandwidth	Tb/s	1.81	2.48	2.48	2.48	2.10
	Sensor I/O Bandwidth	Gb/s	941	941	1,478	1,478	960
Platform	DDR4 Memory Bandwidth	GB/s	76.8	76.8	102.4	102.4	76.8
	LPDDR4 Memory Bandwidth	GB/s	102.4	102.4	136.5	136.5	102.4
	NoC Cross-sectional Bandwidth	Tb/s	1.7	1.7	2.2	2.2	1.7

All parameters listed are maximum values. Verify all data in this document with the device data sheets or product guides.

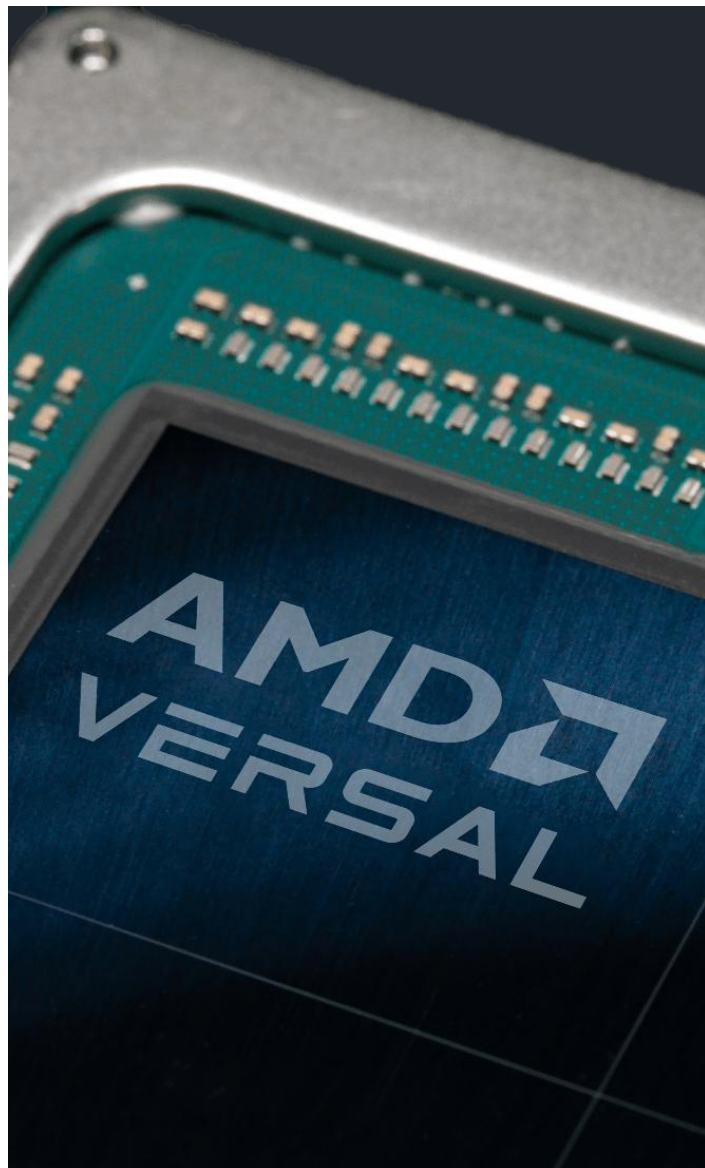
AMD Versal™ Device Ordering Information



Note:

1. This character is only present in Versal AI Edge Series Gen 2, Prime Series Gen 2, and Premium Series Gen 2 devices.
2. Operation at 110°C Tj is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of device lifetime—except -1E and -3E (standard 0–100°C).
3. All packages have Pb-free bumps.

AMD Versal™ Adaptive SoC Portfolio



<p><u>Prime Series</u></p>	<p>Mid-Range Devices with Option for High-End Scalar Compute</p> <ul style="list-style-type: none"> Gen 1: Broad range of capabilities incl. PCIe® Gen 5, DDR5/LPDDR5¹ Gen 2: Adds up to 10X scalar compute², LPDDR5X, VCU 	General-Purpose
<p><u>Premium Series</u></p>	<p>High-End Devices Maximizing Connectivity, Hard IP, & DSP</p> <ul style="list-style-type: none"> Gen 1: 112G SerDes, PCIe Gen 5, DDR4, High-Speed Crypto, AIE Gen 2: Adds 128G SerDes, PCIe Gen 6, CXL® 3.1, DDR5/LPDDR5X 	
<p><u>HBM Series</u></p>	<p>Adds Integrated HBM Memory to Premium Series Capabilities</p> <ul style="list-style-type: none"> 8, 16, or 32 GB of HBM2e per device 6X memory bandwidth at up to 65% lower power³ 	Specialized
<p><u>AI Edge Series</u></p>	<p>End-to-End Acceleration for AI-Driven Embedded Systems</p> <ul style="list-style-type: none"> Gen 1: PL for preprocessing, AIE-ML for high-perf. inference Gen 2: Adds up to 10X scalar compute² for postprocessing, add'l FuSa 	
<p><u>AI Core Series</u></p>	<p>High-Throughput DSP & AI in a Mid-Size Footprint</p> <ul style="list-style-type: none"> AIE for strong DSP performance/watt & perf/area AIE-ML for high-performance inference w/PCIe Gen 5, 100 GbE 	
<p><u>RF Series</u></p>	<p>Integrated RF-ADC/RF-DACs w/New DSP Hard IP</p> <ul style="list-style-type: none"> 16 GSPS RF-DACs, 8 GSPS or 32 GSPS RF-ADCs, AIE FFT/iFFT, Channelizer, LDPC, Frac. Resampler, Polyphase Filters 	

1. DDR5/LPDDR5 support is available in the VM2152 device. All other first-generation Versal Prime Series devices support DDR4/LPDDR4/LPDDR4X.

2. Pre-silicon estimated performance. See Endnotes VER-027.

3. See Endnotes VER-013.



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