

# XCVU125-2FLVC2104I Datasheet



DiGi Electronics Part Number	XCVU125-2FLVC2104I-DG
Manufacturer	<a href="#">AMD</a>
Manufacturer Product Number	XCVU125-2FLVC2104I
Description	IC FPGA 416 I/O 2104FCBGA
Detailed Description	Virtex® UltraScale™ Field Programmable Gate Array (FPGA) IC 416 90726400 1566600 2104-BBGA, FCBGA

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## Purchase and inquiry

Manufacturer Product Number:

XCVU125-2FLVC2104I

Series:

Virtex® UltraScale™

DiGi-Electronics Programmable:

Not Verified

Number of Logic Elements/Cells:

1566600

Number of I/O:

416

Mounting Type:

Surface Mount

Package / Case:

2104-BBGA, FCBGA

Base Product Number:

XCVU125

Manufacturer:

AMD

Product Status:

Active

Number of LABs/CLBs:

89520

Total RAM Bits:

90726400

Voltage - Supply:

0.922V ~ 0.979V

Operating Temperature:

-40°C ~ 100°C (TJ)

Supplier Device Package:

2104-FCBGA (47.5x47.5)

## Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

4 (72 Hours)

ECCN:

3A001A7B



# Virtex UltraScale FPGAs Data Sheet: DC and AC Switching Characteristics

DS893 (v1.12) May 23, 2019

Product Specification

## Summary

The Xilinx® Virtex® UltraScale™ FPGAs are available in -3, -2, -1 speed grades, with -3 having the highest performance.

DC and AC characteristics are specified in commercial, extended, and industrial temperature ranges. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1 speed grade industrial device are the same as for a -1 speed grade commercial device). However, only selected speed grades and/or devices are available in each temperature range.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

This data sheet, part of an overall set of documentation on the UltraScale architecture-based devices, is available on the Xilinx website at [www.xilinx.com/ultrascale](http://www.xilinx.com/ultrascale).

## DC Characteristics

Table 1: Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Description	Min	Max	Units
<b>FPGA Logic</b>				
V <sub>CCINT</sub>	Internal supply voltage.	-0.500	1.100	V
V <sub>CCINT_IO</sub> <sup>(2)</sup>	Internal supply voltage for the I/O banks.	-0.500	1.100	V
V <sub>CCAUX</sub>	Auxiliary supply voltage.	-0.500	2.000	V
V <sub>CCBRAM</sub>	Supply voltage for the block RAM memories.	-0.500	1.100	V
V <sub>CCO</sub>	Output drivers supply voltage for HR I/O banks.	-0.500	3.400	V
	Output drivers supply voltage for HP I/O banks.	-0.500	2.000	V
V <sub>CCAUX_IO</sub> <sup>(3)</sup>	Auxiliary supply voltage for the I/O banks.	-0.500	2.000	V
V <sub>REF</sub>	Input reference voltage.	-0.500	2.000	V
V <sub>IN</sub> <sup>(4)(5)(6)</sup>	I/O input voltage for HR I/O banks.	-0.400	V <sub>CCO</sub> + 0.550	V
	I/O input voltage for HP I/O banks.	-0.550	V <sub>CCO</sub> + 0.550	V
	I/O input voltage (when V <sub>CCO</sub> = 3.3V) for V <sub>REF</sub> and differential I/O standards except TMDS_33 <sup>(7)</sup> .	-0.400	2.625	V
V <sub>BATT</sub>	Key memory battery backup supply.	-0.500	2.000	V
I <sub>DC</sub>	Available output current at the pad.	-20	20	mA
I <sub>RMS</sub>	Available RMS output current at the pad.	-20	20	mA

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**Table 1: Absolute Maximum Ratings<sup>(1)</sup> (Cont'd)**

Symbol	Description	Min	Max	Units
<b>GTH or GTY Transceiver</b>				
V <sub>MGTAVCC</sub>	Analog supply voltage for the GTH or GTY transmitter and receiver circuits.	-0.500	1.100	V
V <sub>MGTAVTT</sub>	Analog supply voltage for the GTH or GTY transmitter and receiver termination circuits.	-0.500	1.320	V
V <sub>MGTVCCAUX</sub>	Auxiliary analog Quad PLL (QPLL) voltage supply for the GTH or GTY transceivers.	-0.500	1.935	V
V <sub>MGTREFCLK</sub>	GTH or GTY transceiver reference clock absolute input voltage.	-0.500	1.320	V
V <sub>MGTAVTTRCAL</sub>	Analog supply voltage for the resistor calibration circuit of the GTH or GTY transceiver column.	-0.500	1.320	V
V <sub>IN</sub>	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage.	-0.500	1.260	V
I <sub>DCIN-FLOAT</sub>	DC input current for receiver input pins DC coupled RX termination = floating.	-	0 <sup>(8)</sup>	mA
I <sub>DCIN-MGTAVTT</sub>	DC input current for receiver input pins DC coupled RX termination = V <sub>MGTAVTT</sub> .	-	10	mA
I <sub>DCIN-GND</sub>	DC input current for receiver input pins DC coupled RX termination = GND.	-	10	mA
I <sub>DCIN-PROG</sub>	DC input current for receiver input pins DC coupled RX termination = Programmable.	-	N/A <sup>(8)</sup>	mA
I <sub>DCOUT-FLOAT</sub>	DC output current for transmitter pins DC coupled RX termination = floating.	-	0 <sup>(8)</sup>	mA
I <sub>DCOUT-MGTAVTT</sub>	DC output current for transmitter pins DC coupled RX termination = V <sub>MGTAVTT</sub> .	-	6	mA
<b>System Monitor</b>				
V <sub>CCADC</sub>	System Monitor supply relative to GNDADC.	-0.500	2.000	V
V <sub>REFP</sub>	System Monitor reference input relative to GNDADC.	-0.500	2.000	V
<b>Temperature</b>				
T <sub>STG</sub>	Storage temperature (ambient).	-65	150	°C
T <sub>SOL</sub>	Maximum soldering temperature <sup>(9)</sup> .	-	260	°C
T <sub>j</sub>	Maximum junction temperature <sup>(9)</sup> .	-	125	°C

**Notes:**

- Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
- V<sub>CCINT\_IO</sub> must be connected to V<sub>CCINT</sub>.
- V<sub>CCAUX\_IO</sub> must be connected to V<sub>CCAUX</sub>.
- The lower absolute voltage specification always applies.
- For I/O operation, see the *UltraScale Architecture SelectIO Resources User Guide* (UG571).
- The maximum limit applied to DC signals. For maximum undershoot and overshoot AC specifications, see Table 4 and Table 5.
- See Table 12 for TMDS\_33 specifications.
- For more information on supported GTH or GTY transceiver terminations see the *UltraScale Architecture GTH Transceiver User Guide* (UG576) or the *UltraScale Architecture GTY Transceiver User Guide* (UG578).
- For soldering guidelines and thermal considerations, see the *UltraScale and UltraScale+ FPGAs Packaging and Pinout Specifications* (UG575).

**Table 2: Recommended Operating Conditions<sup>(1)(2)</sup>**

Symbol	Description	Min	Typ	Max	Units
<b>FPGA Logic</b>					
V <sub>CCINT</sub>	Internal supply voltage for 0.95V devices.	0.922	0.950	0.979	V
	Internal supply voltage for 1.0V devices.	0.970	1.000	1.030	V
V <sub>CCINT_IO</sub> <sup>(3)</sup>	Supply voltage for the 0.95V device I/O banks.	0.922	0.950	0.979	V
	Supply voltage for the 1.0V device I/O banks.	0.970	1.000	1.030	V
V <sub>CCBRAM</sub>	Block RAM supply voltage for 0.95V devices.	0.922	0.950	0.979	V
	Block RAM supply voltage for 1.0V devices.	0.970	1.000	1.030	V
V <sub>CCAUX</sub>	Auxiliary supply voltage.	1.746	1.800	1.854	V
V <sub>CCO</sub> <sup>(4)(5)</sup>	Supply voltage for HR I/O banks.	1.140	–	3.400	V
	Supply voltage for HP I/O banks.	0.950	–	1.890	V
V <sub>CCAUX_IO</sub> <sup>(6)</sup>	Auxiliary I/O supply voltage.	1.746	1.800	1.854	V
V <sub>IN</sub> <sup>(7)</sup>	I/O input voltage.	–0.200	–	V <sub>CCO</sub> + 0.200	V
	I/O input voltage (when V <sub>CCO</sub> = 3.3V) for V <sub>REF</sub> and differential I/O standards except TMDS_33 <sup>(8)</sup> .	–	0.400	2.625	V
I <sub>IN</sub> <sup>(9)</sup>	Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode.	–	–	10.000	mA
V <sub>BATT</sub> <sup>(10)</sup>	Battery voltage.	1.000	–	1.890	V
<b>GTH or GTY Transceiver</b>					
V <sub>MGTAVCC</sub> <sup>(11)</sup>	Analog supply voltage for the GTH transceiver.	0.970	1.000	1.030	V
	Analog supply voltage for the GTY transceiver operating at line rates ≤28.21 Gb/s.	0.970	1.000	1.030	V
	Analog supply voltage for the GTY transceiver operating at line rates >28.21 Gb/s.	1.000	1.030	1.060	V
V <sub>MGTAVTT</sub> <sup>(11)</sup>	Analog supply voltage for the GTH transmitter and receiver termination circuits.	1.170	1.200	1.230	V
	Analog supply voltage for GTY receiver and transmitter termination circuits with the transceiver operating at line rates ≤28.21 Gb/s.	1.170	1.200	1.230	V
	Analog supply voltage for GTY receiver and transmitter termination circuits with the transceiver operating at line rates >28.21 Gb/s.	1.200	1.230	1.260	V
V <sub>MGTVCCAUX</sub> <sup>(11)</sup>	Auxiliary analog QPLL voltage supply for the transceivers	1.750	1.800	1.850	V
V <sub>MGTAVTTRCAL</sub> <sup>(11)</sup>	Analog supply voltage for the resistor calibration circuit of the GTH transceiver column.	1.170	1.200	1.230	V
	Analog supply voltage for the resistor calibration circuit of the GTY transceiver column operating at line rates ≤28.21 Gb/s.	1.170	1.200	1.230	V
	Analog supply voltage for the resistor calibration circuit of the GTY transceiver column operating at line rates >28.21 Gb/s.	1.200	1.230	1.260	V

**Table 2: Recommended Operating Conditions<sup>(1)(2)</sup> (Cont'd)**

Symbol	Description	Min	Typ	Max	Units
<b>SYSMON</b>					
$V_{CCADC}$	SYSMON supply relative to GNDADC.	1.746	1.800	1.854	V
$V_{REFP}$	Externally supplied reference voltage.	1.200	1.250	1.300	V
<b>Temperature</b>					
$T_j$	Junction temperature operating range for commercial (C) temperature devices.	0	–	85	°C
	Junction temperature operating range for extended (E) temperature devices.	0	–	100	°C
	Junction temperature operating range for industrial (I) temperature devices.	–40	–	100	°C

**Notes:**

- All voltages are relative to ground.
- For the design of the power distribution system consult *UltraScale Architecture PCB Design Guide (UG583)*.
- $V_{CCINT\_IO}$  must be connected to  $V_{CCINT}$ .
- For  $V_{CCO\_0}$ , the minimum recommended operating voltage for power on and during configuration is 1.425V. After configuration, data is retained even if  $V_{CCO}$  drops to 0V.
- Includes  $V_{CCO}$  of 1.0V (HP I/O only), 1.2V, 1.35V, 1.5V, 1.8V, 2.5V (HR I/O only) at  $\pm 5\%$ , and 3.3V (HR I/O only) at  $+3/-5\%$ .
- $V_{CCAUX\_IO}$  must be connected to  $V_{CCAUX}$ .
- The lower absolute voltage specification always applies.
- See [Table 12](#) for TMDS\_33 specifications.
- A total of 200 mA per 52-pin bank should not be exceeded.
- $V_{BATT}$  is required only when using bitstream encryption. If battery is not used, connect  $V_{BATT}$  to either ground or  $V_{CCAUX}$ .
- Each voltage listed requires filtering as described in *UltraScale Architecture GTH Transceiver User Guide (UG576)* or *UltraScale Architecture GTY Transceiver User Guide (UG578)*.

**Table 3: DC Characteristics Over Recommended Operating Conditions**

Symbol	Description	Min	Typ <sup>(1)</sup>	Max	Units
V <sub>DRINT</sub>	Data retention V <sub>CCINT</sub> voltage (below which configuration data might be lost).	0.82	–	–	V
V <sub>DRAUX</sub>	Data retention V <sub>CCAUX</sub> voltage (below which configuration data might be lost).	1.50	–	–	V
I <sub>REF</sub>	V <sub>REF</sub> leakage current per pin.	–	–	15	μA
I <sub>L</sub>	Input or output leakage current per pin (sample-tested).	–	–	15 <sup>(2)</sup>	μA
C <sub>IN</sub> <sup>(3)</sup>	Die input capacitance at the pad (HP I/O).	–	–	3.75	pF
	Die input capacitance at the pad (HR I/O).	–	–	7.00	pF
I <sub>RPU</sub>	Pad pull-up (when selected) at V <sub>IN</sub> = 0V, V <sub>CCO</sub> = 3.3V.	75	–	175	μA
	Pad pull-up (when selected) at V <sub>IN</sub> = 0V, V <sub>CCO</sub> = 2.5V.	50	–	169	μA
	Pad pull-up (when selected) at V <sub>IN</sub> = 0V, V <sub>CCO</sub> = 1.8V.	60	–	678	μA
	Pad pull-up (when selected) at V <sub>IN</sub> = 0V, V <sub>CCO</sub> = 1.5V.	30	–	450	μA
	Pad pull-up (when selected) at V <sub>IN</sub> = 0V, V <sub>CCO</sub> = 1.2V.	10	–	262	μA
I <sub>RPD</sub>	Pad pull-down (when selected) at V <sub>IN</sub> = 3.3V.	60	–	190	μA
	Pad pull-down (when selected) at V <sub>IN</sub> = 1.8V.	29	–	685	μA
I <sub>CCADC</sub>	Analog supply current, per SYSMON instance, in the powered up state.	–	–	19.2	mA
I <sub>BATT</sub> <sup>(4)</sup>	Battery supply current.	–	–	150	nA
<i>Calibrated programmable on-die termination (DCI) in HP I/O banks<sup>(6)</sup> (measured per JEDEC specification).</i>					
R <sup>(7)</sup>	Thevenin equivalent resistance of programmable input termination to V <sub>CCO</sub> /2 where ODT = RTT_40.	–10% <sup>(5)</sup>	40	+10% <sup>(5)</sup>	Ω
	Thevenin equivalent resistance of programmable input termination to V <sub>CCO</sub> /2 where ODT = RTT_48.	–10% <sup>(5)</sup>	48	+10% <sup>(5)</sup>	Ω
	Thevenin equivalent resistance of programmable input termination to V <sub>CCO</sub> /2 where ODT = RTT_60.	–10% <sup>(5)</sup>	60	+10% <sup>(5)</sup>	Ω
	Programmable input termination to V <sub>CCO</sub> where ODT = RTT_40.	–10% <sup>(5)</sup>	40	+10% <sup>(5)</sup>	Ω
	Programmable input termination to V <sub>CCO</sub> where ODT = RTT_48.	–10% <sup>(5)</sup>	48	+10% <sup>(5)</sup>	Ω
	Programmable input termination to V <sub>CCO</sub> where ODT = RTT_60.	–10% <sup>(5)</sup>	60	+10% <sup>(5)</sup>	Ω
	Programmable input termination to V <sub>CCO</sub> where ODT = RTT_120.	–10% <sup>(5)</sup>	120	+10% <sup>(5)</sup>	Ω
	Programmable input termination to V <sub>CCO</sub> where ODT = RTT_240.	–10% <sup>(5)</sup>	240	+10% <sup>(5)</sup>	Ω

**Table 3: DC Characteristics Over Recommended Operating Conditions (Cont'd)**

Symbol	Description	Min	Typ <sup>(1)</sup>	Max	Units
<i>Uncalibrated programmable on-die termination in HP I/Os banks (measured per JEDEC specification)</i>					
R <sup>(7)</sup>	Thevenin equivalent resistance of programmable input termination to V <sub>CCO</sub> /2 where ODT = RTT_40.	-50%	40	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to V <sub>CCO</sub> /2 where ODT = RTT_48.	-50%	48	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to V <sub>CCO</sub> /2 where ODT = RTT_60.	-50%	60	+50%	Ω
	Programmable input termination to V <sub>CCO</sub> where ODT = RTT_40.	-50%	40	+50%	Ω
	Programmable input termination to V <sub>CCO</sub> where ODT = RTT_48.	-50%	48	+50%	Ω
	Programmable input termination to V <sub>CCO</sub> where ODT = RTT_60.	-50%	60	+50%	Ω
	Programmable input termination to V <sub>CCO</sub> where ODT = RTT_120.	-50%	120	+50%	Ω
	Programmable input termination to V <sub>CCO</sub> where ODT = RTT_240.	-50%	240	+50%	Ω
<i>Uncalibrated programmable on-die termination in HR I/O banks (measured per JEDEC specification).</i>					
R <sup>(7)</sup>	Thevenin equivalent resistance of programmable input termination to V <sub>CCO</sub> /2 where ODT = RTT_40.	-50%	40	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to V <sub>CCO</sub> /2 where ODT = RTT_48.	-50%	48	+50%	Ω
	Thevenin equivalent resistance of programmable input termination to V <sub>CCO</sub> /2 where ODT = RTT_60.	-50%	60	+50%	Ω
Internal V <sub>REF</sub>	50% V <sub>CCO</sub>	V <sub>CCO</sub> × 0.49	V <sub>CCO</sub> × 0.50	V <sub>CCO</sub> × 0.51	V
	70% V <sub>CCO</sub>	V <sub>CCO</sub> × 0.69	V <sub>CCO</sub> × 0.70	V <sub>CCO</sub> × 0.71	V
Differential termination	Programmable differential termination (TERM_100).	–	100	–	Ω
n	Temperature diode ideality factor.	–	1.002	–	–
r	Temperature diode series resistance.	–	2	–	Ω

**Notes:**

1. Typical values are specified at nominal voltage, 25°C.
2. For HP I/O banks with a V<sub>CCO</sub> of 1.8V and separated V<sub>CCO</sub> and V<sub>CCAUX\_IO</sub> power supplies, the I<sub>L</sub> maximum current is 70 μA.
3. This measurement represents the die capacitance at the pad, not including the package.
4. Maximum value specified for worst case process at 25°C. For XCVU125, XCVU160, XCVU190, and XCVU440 devices multiply the value by the number of super-logic regions (SLRs) in the device.
5. If VRP resides at a different bank (DCI cascade), the range increases to ±15%.
6. VRP resistor tolerance is (240Ω ±1%).
7. On-die input termination resistance, for more information see the *UltraScale Architecture SelectIO Resources User Guide (UG571)*.

**Table 4:  $V_{IN}$  Maximum Allowed AC Voltage Overshoot and Undershoot for HR I/O Banks<sup>(1)(2)</sup>**

AC Voltage Overshoot	% of UI at $-40^{\circ}\text{C}$ to $100^{\circ}\text{C}$	AC Voltage Undershoot	% of UI at $-40^{\circ}\text{C}$ to $100^{\circ}\text{C}$
$V_{CCO} + 0.30$	100%	-0.30	100%
$V_{CCO} + 0.35$	100%	-0.35	70.00%
$V_{CCO} + 0.40$	100%	-0.40	27.00%
$V_{CCO} + 0.45$	100%	-0.45	10.00%
$V_{CCO} + 0.50$	85.00%	-0.50	5.00%
$V_{CCO} + 0.55$	70.00%	-0.55	2.10%
$V_{CCO} + 0.60$	46.60%	-0.60	1.50%
$V_{CCO} + 0.65$	21.20%	-0.65	1.10%
$V_{CCO} + 0.70$	9.75%	-0.70	0.60%
$V_{CCO} + 0.75$	4.55%	-0.75	0.45%
$V_{CCO} + 0.80$	2.15%	-0.80	0.20%
$V_{CCO} + 0.85$	1.00%	-0.85	0.10%
$V_{CCO} + 0.90$	0.50%	-0.90	0.05%

**Notes:**

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20  $\mu\text{s}$ .

**Table 5:  $V_{IN}$  Maximum Allowed AC Voltage Overshoot and Undershoot for HP I/O Banks<sup>(1)(2)</sup>**

AC Voltage Overshoot	% of UI at $-40^{\circ}\text{C}$ to $100^{\circ}\text{C}$	AC Voltage Undershoot	% of UI at $-40^{\circ}\text{C}$ to $100^{\circ}\text{C}$
$V_{CCO} + 0.05$	100%	-0.05	100%
$V_{CCO} + 0.10$	100%	-0.10	100%
$V_{CCO} + 0.15$	100%	-0.15	100%
$V_{CCO} + 0.20$	100%	-0.20	100%
$V_{CCO} + 0.25$	100%	-0.25	100%
$V_{CCO} + 0.30$	100%	-0.30	100%
$V_{CCO} + 0.35$	92.00%	-0.35	92.00%
$V_{CCO} + 0.40$	70.00%	-0.40	40.00%
$V_{CCO} + 0.45$	30.00%	-0.45	15.00%
$V_{CCO} + 0.50$	15.00%	-0.50	10.00%
$V_{CCO} + 0.55$	10.00%	-0.55	4.00%
$V_{CCO} + 0.60$	8.00%	-0.60	0.00%
$V_{CCO} + 0.65$	6.00%	-0.65	0.00%
$V_{CCO} + 0.70$	4.00%	-0.70	0.00%
$V_{CCO} + 0.75$	2.00%	-0.75	0.00%
$V_{CCO} + 0.80$	2.00%	-0.80	0.00%
$V_{CCO} + 0.85$	2.00%	-0.85	0.00%

**Notes:**

1. A total of 200 mA per bank should not be exceeded.
2. For UI smaller than 20  $\mu\text{s}$ .

**Table 6: Typical Quiescent Supply Current<sup>(1)(2)(3)</sup>**

Symbol	Description	Device	Speed Grade and V <sub>CCINT</sub> Operating Voltages				Units
			1.0V		0.95V		
			-3	-1H	-2	-1	
I <sub>CCINTQ</sub>	Quiescent V <sub>CCINT</sub> supply current.	XCVU065	1581	1437	1437	1437	mA
		XCVU080	2309	2100	2100	2100	mA
		XCVU095	2309	2100	2100	2100	mA
		XCVU125	3161	2875	2875	2875	mA
		XCVU160	4742	4312	4312	4312	mA
		XCVU190	4742	4312	4312	4312	mA
		XCVU440	7988	N/A	7264	7264	mA
I <sub>CCINT_IOQ</sub>	Quiescent current for V <sub>CCINT_IO</sub> supply.	XCVU065	100	89	89	89	mA
		XCVU080	161	143	143	143	mA
		XCVU095	161	143	143	143	mA
		XCVU125	200	178	178	178	mA
		XCVU160	299	266	266	266	mA
		XCVU190	299	266	266	266	mA
		XCVU440	299	N/A	266	266	mA
I <sub>CCOQ</sub>	Quiescent V <sub>CCO</sub> supply current.	XCVU065	1	1	1	1	mA
		XCVU080	1	1	1	1	mA
		XCVU095	1	1	1	1	mA
		XCVU125	1	1	1	1	mA
		XCVU160	1	1	1	1	mA
		XCVU190	1	1	1	1	mA
		XCVU440	1	N/A	1	1	mA
I <sub>CCAUXQ</sub>	Quiescent V <sub>CCAUX</sub> supply current.	XCVU065	187	187	187	187	mA
		XCVU080	273	273	273	273	mA
		XCVU095	273	273	273	273	mA
		XCVU125	373	373	373	373	mA
		XCVU160	560	560	560	560	mA
		XCVU190	560	560	560	560	mA
		XCVU440	1009	N/A	1009	1009	mA
I <sub>CCAUX_IOQ</sub>	Quiescent V <sub>CCAUX_IO</sub> supply current.	XCVU065	74	74	74	74	mA
		XCVU080	124	124	124	124	mA
		XCVU095	124	124	124	124	mA
		XCVU125	148	148	148	148	mA
		XCVU160	223	223	223	223	mA
		XCVU190	223	223	223	223	mA
		XCVU440	223	N/A	223	223	mA

**Table 6: Typical Quiescent Supply Current<sup>(1)(2)(3)</sup> (Cont'd)**

Symbol	Description	Device	Speed Grade and V <sub>CCINT</sub> Operating Voltages				Units
			1.0V		0.95V		
			-3	-1H	-2	-1	
I <sub>CCBRAMQ</sub>	Quiescent V <sub>CCBRAM</sub> supply current.	XCVU065	89	81	81	81	mA
		XCVU080	122	111	111	111	mA
		XCVU095	122	111	111	111	mA
		XCVU125	178	162	162	162	mA
		XCVU160	267	243	243	243	mA
		XCVU190	267	243	243	243	mA
		XCVU440	178	N/A	162	162	mA

**Notes:**

1. Typical values are specified at nominal voltage, 85°C junction temperatures (T<sub>j</sub>) with single-ended SelectIO™ resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at [www.xilinx.com/power](http://www.xilinx.com/power)) to estimate static power consumption for conditions other than those specified.

## Power-On/Off Power Supply Sequencing

The recommended power-on sequence is  $V_{CCINT}/V_{CCINT\_IO}$ ,  $V_{CCBRAM}$ ,  $V_{CCAUX}/V_{CCAUX\_IO}$ , and  $V_{CCO}$  to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If  $V_{CCINT}/V_{CCINT\_IO}$  and  $V_{CCBRAM}$  have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously.  $V_{CCINT\_IO}$  must be connected to  $V_{CCINT}$ . If  $V_{CCAUX}/V_{CCAUX\_IO}$  and  $V_{CCO}$  have the same recommended voltage levels, they can be powered by the same supply and ramped simultaneously.  $V_{CCAUX}$  and  $V_{CCAUX\_IO}$  must be connected together. When the current minimums are met, the device powers on after the  $V_{CCINT}/V_{CCINT\_IO}$ ,  $V_{CCBRAM}$ ,  $V_{CCAUX}/V_{CCAUX\_IO}$ , and  $V_{CCO\_0}$  supplies have all passed through their power-on reset threshold voltages. The device must not be configured until after  $V_{CCINT}$  is applied.

$V_{CCADC}$  and  $V_{REF}$  can be powered at any time and have no power-up sequencing recommendations.

The recommended power-on sequence to achieve minimum current draw for the GTH or GTY transceivers is  $V_{CCINT}$ ,  $V_{MGTAVCC}$ ,  $V_{MGTAVTT}$  OR  $V_{MGTAVCC}$ ,  $V_{CCINT}$ ,  $V_{MGTAVTT}$ . There is no recommended sequencing for  $V_{MGTVCCAUX}$ . Both  $V_{MGTAVCC}$  and  $V_{CCINT}$  can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw. If these recommended sequences are not met, current drawn from  $V_{MGTAVTT}$  can be higher than specifications during power-up and power-down.

Table 7 shows the minimum current, in addition to  $I_{CCO}$ , that are required by Virtex UltraScale FPGAs for proper power-on and configuration. If the current minimums shown in Table 6 and Table 7 are met, the device powers on after all four supplies have passed through their power-on reset threshold voltages. The device must not be configured until after  $V_{CCINT}$  is applied. Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies.

**Table 7: Power-on Current by Device**

Device	$I_{CCINTMIN} + I_{CCINT_IOMIN}$	$I_{CCO}$	$I_{CCAUXMIN} + I_{CCAUX_IOMIN}$	$I_{CCBRAMMIN}$	Units
XCVU065	$I_{CCINTQ} + I_{CCINT_IOQ} + 2199$	$I_{CCO_{OQ}} + 40$	$I_{CCAUXQ} + I_{CCAUX_IOQ} + 267$	$I_{CCBRAMQ} + 100$	mA
XCVU080	$I_{CCINTQ} + I_{CCINT_IOQ} + 3300$	$I_{CCO_{OQ}} + 40$	$I_{CCAUXQ} + I_{CCAUX_IOQ} + 400$	$I_{CCBRAMQ} + 150$	mA
XCVU095	$I_{CCINTQ} + I_{CCINT_IOQ} + 3300$	$I_{CCO_{OQ}} + 40$	$I_{CCAUXQ} + I_{CCAUX_IOQ} + 400$	$I_{CCBRAMQ} + 150$	mA
XCVU125	$I_{CCINTQ} + I_{CCINT_IOQ} + 4397$	$I_{CCO_{OQ}} + 54$	$I_{CCAUXQ} + I_{CCAUX_IOQ} + 533$	$I_{CCBRAMQ} + 200$	mA
XCVU160	$I_{CCINTQ} + I_{CCINT_IOQ} + 6595$	$I_{CCO_{OQ}} + 80$	$I_{CCAUXQ} + I_{CCAUX_IOQ} + 800$	$I_{CCBRAMQ} + 300$	mA
XCVU190	$I_{CCINTQ} + I_{CCINT_IOQ} + 6595$	$I_{CCO_{OQ}} + 80$	$I_{CCAUXQ} + I_{CCAUX_IOQ} + 800$	$I_{CCBRAMQ} + 300$	mA
XCVU440	$I_{CCINTQ} + I_{CCINT_IOQ} + 15549$	$I_{CCO_{OQ}} + 189$	$I_{CCAUXQ} + I_{CCAUX_IOQ} + 1885$	$I_{CCBRAMQ} + 707$	mA

Table 8 shows the power supply ramp time.

**Table 8: Power Supply Ramp Time**

Symbol	Description	Min	Max	Units
$T_{VCCINT}$	Ramp time from GND to 95% of $V_{CCINT}$ .	0.2	40	ms
$T_{VCCINT_IO}$	Ramp time from GND to 95% of $V_{CCINT_IO}$ .	0.2	40	ms
$T_{VCCO}$	Ramp time from GND to 95% of $V_{CCO}$ .	0.2	40	ms
$T_{VCCAUX}$	Ramp time from GND to 95% of $V_{CCAUX}$ .	0.2	40	ms
$T_{VCCBRAM}$	Ramp time from GND to 95% of $V_{CCBRAM}$ .	0.2	40	ms
$T_{MGTAVCC}$	Ramp time from GND to 95% of $V_{MGTAVCC}$ .	0.2	40	ms
$T_{MGTAVTT}$	Ramp time from GND to 95% of $V_{MGTAVTT}$ .	0.2	40	ms
$T_{MGTVCCAUX}$	Ramp time from GND to 95% of $V_{MGTVCCAUX}$ .	0.2	40	ms

## DC Input and Output Levels

Values for  $V_{IL}$  and  $V_{IH}$  are recommended input voltages. Values for  $I_{OL}$  and  $I_{OH}$  are guaranteed over the recommended operating conditions at the  $V_{OL}$  and  $V_{OH}$  test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum  $V_{CCO}$  with the respective  $V_{OL}$  and  $V_{OH}$  voltage levels shown. Other standards are sample tested.

**Table 9: SelectIO DC Input and Output Levels For HR I/O Banks<sup>(1)(2)</sup>**

I/O Standard	$V_{IL}$		$V_{IH}$		$V_{OL}$	$V_{OH}$	$I_{OL}$	$I_{OH}$
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8.0	-8.0
HSTL_I_18	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	8.0	-8.0
HSTL_II	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	16.0	-16.0
HSTL_II_18	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	16.0	-16.0
HSUL_12	-0.300	$V_{REF} - 0.130$	$V_{REF} + 0.130$	$V_{CCO} + 0.300$	20% $V_{CCO}$	80% $V_{CCO}$	0.1	-0.1
LVC MOS12	-0.300	35% $V_{CCO}$	65% $V_{CCO}$	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 3	Note 3
LVC MOS15	-0.300	35% $V_{CCO}$	65% $V_{CCO}$	$V_{CCO} + 0.300$	0.450	$V_{CCO} - 0.450$	Note 4	Note 4
LVC MOS18	-0.300	35% $V_{CCO}$	65% $V_{CCO}$	$V_{CCO} + 0.300$	0.450	$V_{CCO} - 0.450$	Note 4	Note 4
LVC MOS25	-0.300	0.700	1.700	$V_{CCO} + 0.300$	0.400	$V_{CCO} - 0.400$	Note 4	Note 4
LVC MOS33	-0.300	0.800	2.000	3.400	0.400	$V_{CCO} - 0.400$	Note 4	Note 4
LV TTL	-0.300	0.800	2.000	3.400	0.400	2.400	Note 4	Note 4
SSTL12	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	14.25	-14.25
SSTL135	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	13.0	-13.0
SSTL135_R	-0.300	$V_{REF} - 0.090$	$V_{REF} + 0.090$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.150$	$V_{CCO}/2 + 0.150$	8.9	-8.9
SSTL15	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	13.0	-13.0
SSTL15_R	-0.300	$V_{REF} - 0.100$	$V_{REF} + 0.100$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.175$	$V_{CCO}/2 + 0.175$	8.9	-8.9
SSTL18_I	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.470$	$V_{CCO}/2 + 0.470$	8.0	-8.0
SSTL18_II	-0.300	$V_{REF} - 0.125$	$V_{REF} + 0.125$	$V_{CCO} + 0.300$	$V_{CCO}/2 - 0.600$	$V_{CCO}/2 + 0.600$	13.4	-13.4

### Notes:

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide (UG571)*.
3. Supported drive strengths of 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 4, 8, 12, or 16 mA in HR I/O banks.

**Table 10: SelectIO DC Input and Output Levels for HP I/O Banks<sup>(1)(2)(3)</sup>**

I/O Standard	V <sub>IL</sub>		V <sub>IH</sub>		V <sub>OL</sub>	V <sub>OH</sub>	I <sub>OL</sub>	I <sub>OH</sub>
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL_I	-0.300	V <sub>REF</sub> - 0.100	V <sub>REF</sub> + 0.100	V <sub>CCO</sub> + 0.300	0.400	V <sub>CCO</sub> - 0.400	5.8	-5.8
HSTL_I_12	-0.300	V <sub>REF</sub> - 0.080	V <sub>REF</sub> + 0.080	V <sub>CCO</sub> + 0.300	25% V <sub>CCO</sub>	75% V <sub>CCO</sub>	4.1	-4.1
HSTL_I_18	-0.300	V <sub>REF</sub> - 0.100	V <sub>REF</sub> + 0.100	V <sub>CCO</sub> + 0.300	0.400	V <sub>CCO</sub> - 0.400	6.2	-6.2
HSUL_12	-0.300	V <sub>REF</sub> - 0.130	V <sub>REF</sub> + 0.130	V <sub>CCO</sub> + 0.300	20% V <sub>CCO</sub>	80% V <sub>CCO</sub>	0.1	-0.1
LVC MOS12	-0.300	35% V <sub>CCO</sub>	65% V <sub>CCO</sub>	V <sub>CCO</sub> + 0.300	0.400	V <sub>CCO</sub> - 0.400	Note 4	Note 4
LVC MOS15	-0.300	35% V <sub>CCO</sub>	65% V <sub>CCO</sub>	V <sub>CCO</sub> + 0.300	0.450	V <sub>CCO</sub> - 0.450	Note 5	Note 5
LVC MOS18	-0.300	35% V <sub>CCO</sub>	65% V <sub>CCO</sub>	V <sub>CCO</sub> + 0.300	0.450	V <sub>CCO</sub> - 0.450	Note 5	Note 5
LVDCI_15	-0.300	35% V <sub>CCO</sub>	65% V <sub>CCO</sub>	V <sub>CCO</sub> + 0.300	0.450	V <sub>CCO</sub> - 0.450	7.0	-7.0
LVDCI_18	-0.300	35% V <sub>CCO</sub>	65% V <sub>CCO</sub>	V <sub>CCO</sub> + 0.300	0.450	V <sub>CCO</sub> - 0.450	7.0	-7.0
SSTL12	-0.300	V <sub>REF</sub> - 0.100	V <sub>REF</sub> + 0.100	V <sub>CCO</sub> + 0.300	V <sub>CCO</sub> /2 - 0.150	V <sub>CCO</sub> /2 + 0.150	8.0	-8.0
SSTL135	-0.300	V <sub>REF</sub> - 0.090	V <sub>REF</sub> + 0.090	V <sub>CCO</sub> + 0.300	V <sub>CCO</sub> /2 - 0.150	V <sub>CCO</sub> /2 + 0.150	9.0	-9.0
SSTL15	-0.300	V <sub>REF</sub> - 0.100	V <sub>REF</sub> + 0.100	V <sub>CCO</sub> + 0.300	V <sub>CCO</sub> /2 - 0.175	V <sub>CCO</sub> /2 + 0.175	10.0	-10.0
SSTL18_I	-0.300	V <sub>REF</sub> - 0.125	V <sub>REF</sub> + 0.125	V <sub>CCO</sub> + 0.300	V <sub>CCO</sub> /2 - 0.470	V <sub>CCO</sub> /2 + 0.470	7.0	-7.0

**Notes:**

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide (UG571)*.
3. POD10 and POD12 DC input and output levels are shown in [Table 11](#), [Table 16](#), and [Table 17](#).
4. Supported drive strengths of 2, 4, 6, or 8 mA in HP I/O banks.
5. Supported drive strengths of 2, 4, 6, 8, or 12 mA in HP I/O banks.

**Table 11: DC Input Levels for Single-ended POD10 and POD12 I/O Standards<sup>(1)(2)</sup>**

I/O Standard	V <sub>IL</sub>		V <sub>IH</sub>	
	V, Min	V, Max	V, Min	V, Max
POD10	-0.300	V <sub>REF</sub> - 0.068	V <sub>REF</sub> + 0.068	V <sub>CCO</sub> + 0.300
POD12	-0.300	V <sub>REF</sub> - 0.068	V <sub>REF</sub> + 0.068	V <sub>CCO</sub> + 0.300

**Notes:**

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide (UG571)*.

**Table 12: Differential SelectIO DC Input and Output Levels**

I/O Standard	$V_{ICM}(V)$ (1)			$V_{ID}(V)$ (2)			$V_{OCM}(V)$ (3)			$V_{OD}(V)$ (4)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
BLVDS_25	0.300	1.200	1.425	0.100	–	–	–	1.250	–	Note 5		
MINI_LVDS_25	0.300	1.200	$V_{CCAUX}$	0.200	0.400	0.600	1.000	1.200	1.485	0.300	0.450	0.600
SUB_LVDS	0.500	0.900	1.300	0.070	–	–	0.700	0.900	1.100	0.100	0.150	0.200
LVPECL	0.300	1.200	1.425	0.100	0.350	0.600	–	–	–	–	–	–
PPDS_25	0.200	0.900	$V_{CCAUX}$	0.100	0.250	0.400	0.500	0.950	1.400	0.100	0.250	0.400
RSDS_25	0.300	0.900	1.500	0.100	0.350	0.600	1.000	1.200	1.485	0.100	0.350	0.600
SLVS_400_18	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–
SLVS_400_25	0.070	0.200	0.330	0.140	–	0.450	–	–	–	–	–	–
TMDS_33	2.700	2.965	3.230	0.150	0.675	1.200	$V_{CCO} - 0.405$	$V_{CCO} - 0.300$	$V_{CCO} - 0.190$	0.400	0.600	0.800

**Notes:**

- $V_{ICM}$  is the input common mode voltage.
- $V_{ID}$  is the input differential voltage ( $Q - \bar{Q}$ ).
- $V_{OCM}$  is the output common mode voltage.
- $V_{OD}$  is the output differential voltage ( $Q - \bar{Q}$ ).
- $V_{OD}$  for BLVDS will vary significantly depending on topology and loading.
- LVDS\_25 is specified in Table 18.
- LVDS is specified in Table 19.

**Table 13: Complementary Differential SelectIO DC Input and Output Levels for HR I/O Banks**

I/O Standard	$V_{ICM}(V)$ (1)			$V_{ID}(V)$ (2)		$V_{OL}(V)$ (3)	$V_{OH}(V)$ (4)	$I_{OL}$	$I_{OH}$
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.300	0.750	1.125	0.100	–	0.400	$V_{CCO} - 0.400$	8.0	–8.0
DIFF_HSTL_I_18	0.300	0.900	1.425	0.100	–	0.400	$V_{CCO} - 0.400$	8.0	–8.0
DIFF_HSTL_II	0.300	0.750	1.125	0.100	–	0.400	$V_{CCO} - 0.400$	16.0	–16.0
DIFF_HSTL_II_18	0.300	0.900	1.425	0.100	–	0.400	$V_{CCO} - 0.400$	16.0	–16.0
DIFF_HSUL_12	0.300	0.600	0.850	0.100	–	20% $V_{CCO}$	80% $V_{CCO}$	0.1	–0.1
DIFF_SSTL12	0.300	0.600	0.850	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	14.25	–14.25
DIFF_SSTL135	0.300	0.675	1.000	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	13.0	–13.0
DIFF_SSTL135_R	0.300	0.675	1.000	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	8.9	–8.9
DIFF_SSTL15	0.300	0.750	1.125	0.100	–	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	13.0	–13.0
DIFF_SSTL15_R	0.300	0.750	1.125	0.100	–	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	8.9	–8.9
DIFF_SSTL18_I	0.300	0.900	1.425	0.100	–	$(V_{CCO}/2) - 0.470$	$(V_{CCO}/2) + 0.470$	8.0	–8.0
DIFF_SSTL18_II	0.300	0.900	1.425	0.100	–	$(V_{CCO}/2) - 0.600$	$(V_{CCO}/2) + 0.600$	13.4	–13.4

**Notes:**

- $V_{ICM}$  is the input common mode voltage.
- $V_{ID}$  is the input differential voltage.
- $V_{OL}$  is the single-ended low-output voltage.
- $V_{OH}$  is the single-ended high-output voltage.

**Table 14: Complementary Differential SelectIO DC Input and Output Levels for HP I/O Banks<sup>(1)</sup>**

I/O Standard	$V_{ICM}$ (V) <sup>(2)</sup>			$V_{ID}$ (V) <sup>(3)</sup>		$V_{OL}$ (V) <sup>(4)</sup>	$V_{OH}$ (V) <sup>(5)</sup>	$I_{OL}$	$I_{OH}$
	Min	Typ	Max	Min	Max	Max	Min	mA	mA
DIFF_HSTL_I	0.680	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	0.400	$V_{CCO} - 0.400$	5.8	–5.8
DIFF_HSTL_I_12	$0.400 \times V_{CCO}$	$V_{CCO}/2$	$0.600 \times V_{CCO}$	0.100	–	$0.250 \times V_{CCO}$	$0.750 \times V_{CCO}$	4.1	–4.1
DIFF_HSTL_I_18	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	0.400	$V_{CCO} - 0.400$	6.2	–6.2
DIFF_HSUL_12	$(V_{CCO}/2) - 0.120$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.120$	0.100	–	$20\% V_{CCO}$	$80\% V_{CCO}$	0.1	–0.1
DIFF_SSTL12	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	8.0	–8.0
DIFF_SSTL135	$(V_{CCO}/2) - 0.150$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.150$	0.100	–	$(V_{CCO}/2) - 0.150$	$(V_{CCO}/2) + 0.150$	9.0	–9.0
DIFF_SSTL15	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	$(V_{CCO}/2) - 0.175$	$(V_{CCO}/2) + 0.175$	10.0	–10.0
DIFF_SSTL18_I	$(V_{CCO}/2) - 0.175$	$V_{CCO}/2$	$(V_{CCO}/2) + 0.175$	0.100	–	$(V_{CCO}/2) - 0.470$	$(V_{CCO}/2) + 0.470$	7.0	–7.0

**Notes:**

1. DIFF\_POD10 and DIFF\_POD12 HP I/O bank specifications are shown in [Table 15](#), [Table 16](#), and [Table 17](#).
2.  $V_{ICM}$  is the input common mode voltage.
3.  $V_{ID}$  is the input differential voltage.
4.  $V_{OL}$  is the single-ended low-output voltage.
5.  $V_{OH}$  is the single-ended high-output voltage.

**Table 15: DC Input Levels for Differential POD10 and POD12 I/O Standards<sup>(1)(2)</sup>**

I/O Standard	$V_{ICM}$ (V)			$V_{ID}$ (V)	
	Min	Typ	Max	Min	Max
DIFF_POD10	0.63	0.70	0.77	0.14	–
DIFF_POD12	0.76	0.84	0.92	0.16	–

**Notes:**

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).

**Table 16: DC Output Levels for Single-ended and Differential POD10 and POD12 Standards<sup>(1)(2)</sup>**

Symbol	Description	$V_{OUT}$	Min	Typ	Max	Units
$R_{OL}$	Pull-down resistance	$V_{OM\_DC}$ (as described in <a href="#">Table 17</a> )	36	40	44	$\Omega$
$R_{OH}$	Pull-up resistance	$V_{OM\_DC}$ (as described in <a href="#">Table 17</a> )	36	40	44	$\Omega$

**Notes:**

1. Tested according to relevant specifications.
2. Standards specified using the default I/O standard configuration. For details, see the *UltraScale Architecture SelectIO Resources User Guide* ([UG571](#)).

**Table 17: [Table 16](#) Definitions for DC Output Levels for POD Standards**

Symbol	Description	All Devices	Units
$V_{OM\_DC}$	DC output Mid measurement level (for IV curve linearity).	$0.8 \times V_{CCO}$	V

## LVDS DC Specifications (LVDS\_25)

The LVDS\_25 standard is available in the HR I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* (UG571) for more information.

Table 18: LVDS\_25 DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V <sub>CCO</sub>	Supply voltage		2.375	2.500	2.625	V
V <sub>ODIFF</sub> <sup>(1)</sup>	Differential output voltage: ( $\underline{Q} - \overline{Q}$ ), $\underline{Q} = \text{High}$ ( $\overline{Q} - Q$ ), $\overline{Q} = \text{High}$	R <sub>T</sub> = 100Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V <sub>OCM</sub> <sup>(1)</sup>	Output common-mode voltage.	R <sub>T</sub> = 100Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.485	V
V <sub>IDIFF</sub>	Differential input voltage: ( $\underline{Q} - \overline{Q}$ ), $\underline{Q} = \text{High}$ ( $\overline{Q} - Q$ ), $\overline{Q} = \text{High}$		100	350	600 <sup>(2)</sup>	mV
V <sub>ICM_DC</sub> <sup>(3)</sup>	Input common-mode voltage (DC coupling).		0.300	1.200	1.500	V
V <sub>ICM_AC</sub> <sup>(4)</sup>	Input common-mode voltage (AC coupling).		0.600	–	1.100	V

### Notes:

- V<sub>OCM</sub> and V<sub>ODIFF</sub> values are for LVDS\_PRE\_EMPHASIS = FALSE.
- Maximum V<sub>IDIFF</sub> value is specified for the maximum V<sub>ICM</sub> specification. With a lower V<sub>ICM</sub>, a higher V<sub>IDIFF</sub> is tolerated only when the recommended operating conditions and overshoot/undershoot V<sub>IN</sub> specifications are maintained.
- Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ\_NONE (Default).
- External input common mode voltage specification for AC coupled configurations. EQUALIZATION = EQ\_LEVEL0, EQ\_LEVEL1, EQ\_LEVEL2, EQ\_LEVEL3, EQ\_LEVEL4.

## LVDS DC Specifications (LVDS)

The LVDS standard is available in the HP I/O banks. See the *UltraScale Architecture SelectIO Resources User Guide* (UG571) for more information.

Table 19: LVDS DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
V <sub>CCO</sub>	Supply voltage		1.710	1.800	1.890	V
V <sub>ODIFF</sub> <sup>(1)</sup>	Differential output voltage ( $\underline{Q} - \overline{Q}$ ), $\underline{Q} = \text{High}$ ( $\overline{Q} - Q$ ), $\overline{Q} = \text{High}$	R <sub>T</sub> = 100Ω across Q and $\overline{Q}$ signals	247	350	600	mV
V <sub>OCM</sub> <sup>(1)</sup>	Output common-mode voltage.	R <sub>T</sub> = 100Ω across Q and $\overline{Q}$ signals	1.000	1.250	1.425	V
V <sub>IDIFF</sub>	Differential input voltage ( $\underline{Q} - \overline{Q}$ ), $\underline{Q} = \text{High}$ ( $\overline{Q} - Q$ ), $\overline{Q} = \text{High}$		100	350	600 <sup>(2)</sup>	mV
V <sub>ICM_DC</sub> <sup>(3)</sup>	Input common-mode voltage (DC coupling).		0.300	1.200	1.425	V
V <sub>ICM_AC</sub> <sup>(4)</sup>	Input common-mode voltage (AC coupling).		0.600	–	1.100	V

### Notes:

- V<sub>OCM</sub> and V<sub>ODIFF</sub> values are for LVDS\_PRE\_EMPHASIS = FALSE.
- Maximum V<sub>IDIFF</sub> value is specified for the maximum V<sub>ICM</sub> specification. With a lower V<sub>ICM</sub>, a higher V<sub>IDIFF</sub> is tolerated only when the recommended operating conditions and overshoot/undershoot V<sub>IN</sub> specifications are maintained.
- Input common mode voltage for DC coupled configurations. EQUALIZATION = EQ\_NONE (Default).
- External input common mode voltage specification for AC coupled configurations. EQUALIZATION = EQ\_LEVEL0, EQ\_LEVEL1, EQ\_LEVEL2, EQ\_LEVEL3, EQ\_LEVEL4.

## AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications in the Vivado® Design Suite as outlined in [Table 20](#).

*Table 20: Speed Specification Version By Device*

2016.4	Device
1.25	XCVU065, XCVU125, XCVU160, and XCVU190
1.24	XCVU080, XCVU095, and XCVU440

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

### Advance Product Specification

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

### Preliminary Product Specification

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

### Product Specification

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to production before faster speed grades.

## Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Virtex UltraScale FPGAs.

## Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. [Table 21](#) correlates the current status of the Virtex UltraScale FPGAs on a per speed grade basis.

*Table 21: Virtex UltraScale FPGAs Speed Grade Designations*

Device	Speed Grades, Temperature Ranges, and $V_{CCINT}$ Operating Voltages		
	Advance	Preliminary	Production
XCVU065			-3E (1.0V), -1HE (1.0V) <sup>(1)</sup> , -2E/-2I (0.95V), -1I (0.95V), and -1HE (0.95V)
XCVU080			-3E (1.0V), -1HE (1.0V) <sup>(1)</sup> , -2E/-2I (0.95V), -1I (0.95V), and -1HE (0.95V)
XCVU095			-3E (1.0V), -1HE (1.0V) <sup>(1)</sup> , -2E/-2I (0.95V), -1I (0.95V), and -1HE (0.95V)
XCVU125			-3E (1.0V), -1HE (1.0V) <sup>(1)</sup> , -2E/-2I (0.95V), -1I (0.95V), and -1HE (0.95V)
XCVU160			-3E (1.0V), -1HE (1.0V) <sup>(1)</sup> , -2E/-2I (0.95V), -1I (0.95V), and -1HE (0.95V)
XCVU190			-3E (1.0V), -1HE (1.0V) <sup>(1)</sup> , -2E/-2I (0.95V), -1I (0.95V), and -1HE (0.95V)
XCVU440			-3E (1.0V), -2E/-2I (0.95V), and -1C/-1I (0.95V)

**Notes:**

1. The higher performance -1HE devices, where  $V_{CCINT} = 1.0V$ , are listed in the Vivado Design Suite as -1HV.

## Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 22 lists the production released Virtex UltraScale FPGAs, speed grade, and the minimum corresponding supported speed specification version and Vivado software revisions. The Vivado software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

**Table 22: Virtex UltraScale FPGAs Device Production Software and Speed Specification Release<sup>(1)</sup>**

Device	Speed Grades, Temperature Ranges, and V <sub>CCINT</sub> Operating Voltages					
	1.0V		0.95V			
	-3E	-1HE	-2E, -2I	-1I	-1C	-1HE
XCVU065	Vivado Tools 2016.1 v1.25	Vivado Tools 2015.4.2 v1.25	Vivado Tools 2015.4.1 v1.25		N/A	Vivado Tools 2015.4.2 v1.25
XCVU080	Vivado Tools 2015.3 v1.24	Vivado Tools 2015.4.2 v1.24	Vivado Tools 2015.3 v1.24		N/A	Vivado Tools 2015.4.2 v1.24
XCVU095	Vivado Tools 2015.3 v1.24	Vivado Tools 2015.4.2 v1.24	Vivado Tools 2015.3 v1.24		N/A	Vivado Tools 2015.4.2 v1.24
XCVU125	Vivado Tools 2016.1 v1.25	Vivado Tools 2015.4.2 v1.25	Vivado Tools 2015.4.1 v1.25		N/A	Vivado Tools 2015.4.2 v1.25
XCVU160	Vivado Tools 2015.4 v1.25	Vivado Tools 2015.4.2 v1.25	Vivado Tools 2015.4 v1.25		N/A	Vivado Tools 2015.4.2 v1.25
XCVU190	Vivado Tools 2015.4 v1.25	Vivado Tools 2015.4.2 v1.25	Vivado Tools 2015.4 v1.25		N/A	Vivado Tools 2015.4.2 v1.25
XCVU440	Vivado Tools 2016.1 v1.24	N/A	Vivado Tools 2015.4 v1.24			N/A

### Notes:

- For designs developed using Vivado tools prior to 2016.4, see the design advisory answer record [AR68169](#): *Design Advisory for Kintex UltraScale FPGAs and Virtex UltraScale FPGAs—New minimum production speed specification version (Speed File) required for all designs.*

## Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Virtex UltraScale FPGAs. These values are subject to the same guidelines as the [AC Switching Characteristics, page 17](#). In each table, the I/O bank type is either high performance (HP) or high range (HR).

In LVDS component mode:

- For the input/output registers, the Vivado tools limit clock frequencies to 364.9 MHz for -3 and -2 speed grades or 316.4 MHz for -1 speed grade.
- For IDDR, Vivado tools limit clock frequencies to 729.9 MHz for -3 and -2 speed grades or 632.9 MHz for -1 speed grade.
- For ODDR, Vivado tools limit clock frequencies to 730.4 MHz for all speed grades.

**Table 23: LVDS Component Mode Performance**

Description	I/O Bank Type	Speed Grades and V <sub>CCINT</sub> Operating Voltages								Units
		1.0V				0.95V				
		-3		-1H		-2		-1		
		Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (OSERDES 4:1, 8:1)	HP	0	1250	0	1250	0	1250	0	1250	Mb/s
	HR	0	1250	0	1250	0	1250	0	1000	Mb/s
LVDS TX SDR (OSERDES 2:1, 4:1)	HP	0	625	0	625	0	625	0	625	Mb/s
	HR	0	625	0	625	0	625	0	500	Mb/s
LVDS RX DDR (ISERDES 1:4, 1:8) <sup>(1)</sup>	HP	0	1250	0	1250	0	1250	0	1250	Mb/s
	HR	0	1250	0	1250	0	1250	0	1000	Mb/s
LVDS RX SDR (ISERDES 1:2, 1:4) <sup>(1)</sup>	HP	0	625	0	625	0	625	0	625	Mb/s
	HR	0	625	0	625	0	625	0	500	Mb/s

**Notes:**

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) or phase-tracking algorithms are used to achieve maximum performance.

**Table 24: LVDS Native Mode Performance<sup>(1)</sup>**

Description	I/O Bank Type	Speed Grades and V <sub>CCINT</sub> Operating Voltages								Units
		1.0V				0.95V				
		-3		-1H		-2		-1		
		Min	Max	Min	Max	Min	Max	Min	Max	
LVDS TX DDR (TX_BITSLICE 4:1, 8:1)	HP	300	1600	300	1600	300	1600	300	1400	Mb/s
	HR	300	1250	300	1250	300	1250	300	1250	Mb/s
LVDS TX SDR (TX_BITSLICE 2:1, 4:1)	HP	150	800	150	800	150	800	150	700	Mb/s
	HR	150	625	150	625	150	625	150	625	Mb/s

**Table 24: LVDS Native Mode Performance<sup>(1)</sup> (Cont'd)**

Description	I/O Bank Type	Speed Grades and V <sub>CCINT</sub> Operating Voltages								Units
		1.0V				0.95V				
		-3		-1H		-2		-1		
		Min	Max	Min	Max	Min	Max	Min	Max	
LVDS RX DDR (RX_BITSLICE 1:4, 1:8) <sup>(2)</sup>	HP	300	1600 <sup>(3)</sup>	300	1600 <sup>(3)</sup>	300	1600 <sup>(3)</sup>	300	1400 <sup>(3)</sup>	Mb/s
	HR	300	1250	300	1250	300	1250	300	1250	Mb/s
LVDS RX SDR (RX_BITSLICE 1:2, 1:4) <sup>(2)</sup>	HP	150	800	150	800	150	800	150	700	Mb/s
	HR	150	625	150	625	150	625	150	625	Mb/s

**Notes:**

- Native mode is supported through the [High-Speed SelectIO Interface Wizard](#) available with the Vivado Design Suite.
- LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) or phase-tracking algorithms are used to achieve maximum performance.
- Asynchronous receiver performance is limited to 1300 Mb/s for -3, -2, and -1H speed grades, and 1250 Mb/s for the -1 speed grade.

**Table 25: LVDS Native-Mode 1000BASE-X Support<sup>(1)</sup>**

Description	I/O Bank Type	Speed Grades and V <sub>CCINT</sub> Operating Voltages			
		1.0V		0.95V	
		-3	-1H	-2	-1
1000BASE-X	HP	Yes	Yes	Yes	Yes

**Notes:**

- 1000BASE-X support is based on the *IEEE Standard for CSMA/CD Access Method and Physical Layer Specifications* (IEEE Std 802.3-2008).

**Table 26** provides the maximum data rates for applicable memory standards using the Virtex UltraScale FPGAs memory PHY. Refer to [Memory Interfaces](#) for the complete list of memory interface standards supported and detailed specifications. The final performance of the memory interface is determined through a complete design implemented in the Vivado Design Suite, following guidelines in the *UltraScale Architecture PCB Design Guide (UG583)*, electrical analysis, and characterization of the system.

**Table 26: Maximum Physical Interface (PHY) Rate for Memory Interfaces (HP I/O Banks Only)**

Memory Standard	DRAM Type	Speed Grades and V <sub>CCINT</sub> Operating Voltages				Units
		1.0V		0.95V		
		-3	-1H	-2	-1	
DDR4	Single rank component	2400 <sup>(1)</sup>	2400	2400 <sup>(1)</sup>	2133	Mb/s
	1 rank DIMM <sup>(2)(3)</sup>	2133	2133	2133	1866	Mb/s
	2 rank DIMM <sup>(2)(4)</sup>	1866	1866	1866	1600	Mb/s
	4 rank DIMM <sup>(2)(5)</sup>	1333	1333	1333	N/A	Mb/s
DDR3	Single rank component	2133	2133	2133	1866	Mb/s
	1 rank DIMM <sup>(2)(3)</sup>	1866	1866	1866	1600	Mb/s
	2 rank DIMM <sup>(2)(4)</sup>	1600	1600	1600	1333	Mb/s
	4 rank DIMM <sup>(2)(5)</sup>	1066	1066	1066	800	Mb/s

**Table 26: Maximum Physical Interface (PHY) Rate for Memory Interfaces (HP I/O Banks Only)**

Memory Standard	DRAM Type	Speed Grades and V <sub>CCINT</sub> Operating Voltages				Units
		1.0V		0.95V		
		-3	-1H	-2	-1	
DDR3L	Single rank component	1866	1866	1866	1600	Mb/s
	1 rank DIMM <sup>(2)(3)</sup>	1600	1600	1600	1333	Mb/s
	2 rank DIMM <sup>(2)(4)</sup>	1333	1333	1333	1066	Mb/s
	4 rank DIMM <sup>(2)(5)</sup>	800	800	800	606	Mb/s
QDRII+ <sup>(6)</sup>	Single rank component	633	600	600	550	MHz
QDRIV-XP	Single rank component	800	800	800	667	MHz
RLDRAM III	Single rank component	1066	1066	1066	933	MHz
LPDDR3	Single rank component	1600	1600	1600	1600	Mb/s

**Notes:**

1. The XCVU440 supports a maximum of 15 banks of DDR4 memory at 2400 Mb/s, all other memory rates or configurations can utilize all the banks.
2. Dual in-line memory module (DIMM) includes RDIMM, SODIMM, UDIMM, and LRDIMM.
3. Includes: 1 rank 1 slot, DDP 2 rank, LRDIMM 2 or 4 rank 1 slot.
4. Includes: 2 rank 1 slot, 1 rank 2 slot, LRDIMM 2 rank 2 slot.
5. Includes: 2 rank 2 slot, 4 rank 1 slot.
6. The QDRII+ performance specifications are for burst-length 4 (BL = 4) implementations.

## IOB Pad Input, Output, and 3-State

Table 27 (high-range IOB (HR)) and Table 28 (high-performance IOB (HP)) summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{\text{INBUF\_DELAY\_PAD\_I}}$  is the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{\text{OUTBUF\_DELAY\_O\_PAD}}$  is the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{\text{OUTBUF\_DELAY\_TD\_PAD}}$  is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HP I/O banks, the internal DCI termination turn-on time is always faster than  $T_{\text{OUTBUF\_DELAY\_TD\_PAD}}$  when the DCITERMDISABLE pin is used. In HR I/O banks, the on-die termination turn-on time is always faster than  $T_{\text{OUTBUF\_DELAY\_TD\_PAD}}$  when the INTERMDISABLE pin is used.

**Table 27: IOB High Range (HR) Switching Characteristics**

I/O Standards	$T_{\text{INBUF\_DELAY\_PAD\_I}}$				$T_{\text{OUTBUF\_DELAY\_O\_PAD}}$				$T_{\text{OUTBUF\_DELAY\_TD\_PAD}}$				Units
	1.0V		0.95V		1.0V		0.95V		1.0V		0.95V		
	-3	-1H	-2	-1	-3	-1H	-2	-1	-3	-1H	-2	-1	
BLVDS_25	0.46	0.58	0.58	0.64	1.37	1.37	1.37	1.62	1.39	1.40	1.40	1.66	ns
DIFF_HSTL_I_18_F	0.42	0.53	0.53	0.57	0.71	0.71	0.71	0.90	0.82	0.82	0.82	1.06	ns
DIFF_HSTL_I_18_S	0.42	0.53	0.53	0.57	0.83	0.83	0.83	1.02	0.93	0.94	0.94	1.16	ns
DIFF_HSTL_I_F	0.42	0.53	0.53	0.57	0.73	0.73	0.73	0.92	0.90	0.90	0.90	1.14	ns
DIFF_HSTL_I_S	0.42	0.53	0.53	0.57	0.77	0.77	0.77	0.96	0.95	0.98	0.98	1.23	ns

**Table 27: IOB High Range (HR) Switching Characteristics (Cont'd)**

I/O Standards	T <sub>INBUF_DELAY_PAD_I</sub>				T <sub>OUTBUF_DELAY_O_PAD</sub>				T <sub>OUTBUF_DELAY_TD_PAD</sub>				Units
	1.0V		0.95V		1.0V		0.95V		1.0V		0.95V		
	-3	-1H	-2	-1	-3	-1H	-2	-1	-3	-1H	-2	-1	
DIFF_HSTL_II_18_F	0.42	0.53	0.53	0.57	0.80	0.80	0.80	0.99	0.95	0.98	0.98	1.23	ns
DIFF_HSTL_II_18_S	0.42	0.53	0.53	0.57	0.83	0.83	0.83	1.03	1.01	1.03	1.03	1.28	ns
DIFF_HSTL_II_F	0.42	0.53	0.53	0.57	0.71	0.71	0.71	0.91	0.87	0.87	0.87	1.11	ns
DIFF_HSTL_II_S	0.42	0.53	0.53	0.57	0.80	0.80	0.80	0.99	0.95	0.96	0.96	1.20	ns
DIFF_HSUL_12_F	0.42	0.53	0.53	0.57	0.73	0.73	0.73	0.92	0.73	0.73	0.73	0.92	ns
DIFF_HSUL_12_S	0.42	0.53	0.53	0.57	0.82	0.82	0.82	1.01	0.82	0.82	0.82	1.01	ns
DIFF_SSTL12_F	0.42	0.53	0.53	0.57	0.70	0.70	0.70	0.89	0.81	0.81	0.81	1.02	ns
DIFF_SSTL12_S	0.42	0.53	0.53	0.57	1.04	1.04	1.04	1.26	1.04	1.04	1.04	1.26	ns
DIFF_SSTL135_F	0.42	0.53	0.53	0.57	0.70	0.70	0.70	0.88	0.86	0.87	0.87	1.09	ns
DIFF_SSTL135_S	0.42	0.53	0.53	0.57	0.77	0.77	0.77	0.96	0.93	0.94	0.94	1.18	ns
DIFF_SSTL135_R_F	0.42	0.53	0.53	0.57	0.72	0.72	0.72	0.91	0.83	0.84	0.84	1.06	ns
DIFF_SSTL135_R_S	0.42	0.53	0.53	0.57	0.80	0.80	0.80	1.00	0.93	0.93	0.93	1.17	ns
DIFF_SSTL15_F	0.42	0.53	0.53	0.57	0.66	0.66	0.66	0.85	0.81	0.82	0.82	1.05	ns
DIFF_SSTL15_S	0.42	0.53	0.53	0.57	0.78	0.78	0.78	0.98	0.96	0.96	0.96	1.20	ns
DIFF_SSTL15_R_F	0.42	0.53	0.53	0.57	0.73	0.73	0.73	0.92	0.86	0.86	0.86	1.09	ns
DIFF_SSTL15_R_S	0.42	0.53	0.53	0.57	0.81	0.81	0.81	1.01	0.93	0.94	0.94	1.18	ns
DIFF_SSTL18_I_F	0.42	0.53	0.53	0.57	0.74	0.74	0.74	0.94	0.92	0.93	0.93	1.18	ns
DIFF_SSTL18_I_S	0.42	0.53	0.53	0.57	0.86	0.86	0.86	1.05	0.86	0.86	0.86	1.05	ns
DIFF_SSTL18_II_F	0.42	0.53	0.53	0.57	0.71	0.71	0.71	0.90	0.87	0.88	0.88	1.11	ns
DIFF_SSTL18_II_S	0.42	0.53	0.53	0.57	0.83	0.83	0.83	1.03	0.99	1.04	1.04	1.29	ns
HSTL_I_18_F	0.52	0.55	0.55	0.59	0.73	0.73	0.73	0.93	0.84	0.84	0.84	1.08	ns
HSTL_I_18_S	0.52	0.55	0.55	0.59	0.85	0.85	0.85	1.05	0.95	0.96	0.96	1.18	ns
HSTL_I_F	0.52	0.55	0.55	0.59	0.75	0.75	0.75	0.94	0.92	0.92	0.92	1.16	ns
HSTL_I_S	0.52	0.55	0.55	0.59	0.79	0.79	0.79	0.98	0.97	1.00	1.00	1.25	ns
HSTL_II_18_F	0.52	0.55	0.55	0.59	0.82	0.82	0.82	1.01	0.97	1.00	1.00	1.25	ns
HSTL_II_18_S	0.52	0.55	0.55	0.59	0.85	0.85	0.85	1.05	1.03	1.05	1.05	1.30	ns
HSTL_II_F	0.52	0.55	0.55	0.59	0.73	0.73	0.73	0.93	0.89	0.90	0.90	1.13	ns
HSTL_II_S	0.52	0.55	0.55	0.59	0.82	0.82	0.82	1.01	0.98	0.98	0.98	1.22	ns
HSUL_12_F	0.52	0.55	0.55	0.59	0.75	0.75	0.75	0.94	0.75	0.75	0.75	0.94	ns
HSUL_12_S	0.52	0.55	0.55	0.59	0.84	0.84	0.84	1.04	0.96	0.97	0.97	1.15	ns
LVC MOS12_F_12	0.76	0.95	0.95	0.95	0.95	0.95	0.95	1.16	0.95	0.95	0.95	1.16	ns
LVC MOS12_F_4	0.76	0.95	0.95	0.95	1.13	1.16	1.16	1.39	1.13	1.16	1.16	1.39	ns
LVC MOS12_F_8	0.76	0.95	0.95	0.95	0.97	0.97	0.97	1.19	0.97	0.97	0.97	1.19	ns
LVC MOS12_S_12	0.76	0.95	0.95	0.95	1.06	1.06	1.06	1.28	1.06	1.06	1.06	1.28	ns
LVC MOS12_S_4	0.76	0.95	0.95	0.95	1.27	1.36	1.36	1.60	1.27	1.36	1.36	1.60	ns
LVC MOS12_S_8	0.76	0.95	0.95	0.95	1.10	1.10	1.10	1.32	1.10	1.10	1.10	1.32	ns
LVC MOS15_F_12	0.68	0.82	0.82	0.87	0.96	0.96	0.96	1.18	0.96	0.96	0.96	1.18	ns
LVC MOS15_F_16	0.68	0.82	0.82	0.87	0.94	0.94	0.94	1.15	0.94	0.94	0.94	1.17	ns
LVC MOS15_F_4	0.68	0.82	0.82	0.87	1.15	1.15	1.15	1.38	1.15	1.15	1.15	1.38	ns

Table 27: IOB High Range (HR) Switching Characteristics (Cont'd)

I/O Standards	T <sub>INBUF_DELAY_PAD_I</sub>				T <sub>OUTBUF_DELAY_O_PAD</sub>				T <sub>OUTBUF_DELAY_TD_PAD</sub>				Units
	1.0V		0.95V		1.0V		0.95V		1.0V		0.95V		
	-3	-1H	-2	-1	-3	-1H	-2	-1	-3	-1H	-2	-1	
LVC MOS15_F_8	0.68	0.82	0.82	0.87	1.02	1.02	1.02	1.24	1.02	1.02	1.02	1.24	ns
LVC MOS15_S_12	0.68	0.82	0.82	0.87	1.07	1.07	1.07	1.29	1.07	1.07	1.07	1.29	ns
LVC MOS15_S_16	0.68	0.82	0.82	0.87	1.04	1.04	1.04	1.26	1.04	1.04	1.04	1.26	ns
LVC MOS15_S_4	0.68	0.82	0.82	0.87	1.28	1.29	1.29	1.53	1.28	1.29	1.29	1.53	ns
LVC MOS15_S_8	0.68	0.82	0.82	0.87	1.11	1.11	1.11	1.34	1.11	1.11	1.11	1.34	ns
LVC MOS18_F_12	0.64	0.76	0.76	0.79	1.04	1.04	1.04	1.25	1.04	1.04	1.04	1.25	ns
LVC MOS18_F_16	0.64	0.76	0.76	0.79	1.00	1.00	1.00	1.21	1.00	1.00	1.00	1.21	ns
LVC MOS18_F_4	0.64	0.76	0.76	0.79	1.17	1.17	1.17	1.41	1.17	1.17	1.17	1.41	ns
LVC MOS18_F_8	0.64	0.76	0.76	0.79	1.10	1.10	1.10	1.33	1.10	1.10	1.10	1.33	ns
LVC MOS18_S_12	0.64	0.76	0.76	0.79	1.11	1.11	1.11	1.34	1.11	1.11	1.11	1.34	ns
LVC MOS18_S_16	0.64	0.76	0.76	0.79	1.11	1.11	1.11	1.34	1.11	1.11	1.11	1.34	ns
LVC MOS18_S_4	0.64	0.76	0.76	0.79	1.32	1.32	1.32	1.58	1.32	1.32	1.32	1.58	ns
LVC MOS18_S_8	0.64	0.76	0.76	0.79	1.18	1.18	1.18	1.38	1.18	1.18	1.18	1.38	ns
LVC MOS25_F_12	0.83	0.85	0.85	0.90	1.54	1.54	1.54	1.81	1.54	1.54	1.54	1.81	ns
LVC MOS25_F_16	0.83	0.85	0.85	0.90	1.56	1.59	1.59	1.88	1.56	1.59	1.59	1.88	ns
LVC MOS25_F_4	0.83	0.85	0.85	0.90	2.24	2.24	2.24	2.56	2.24	2.24	2.24	2.56	ns
LVC MOS25_F_8	0.83	0.85	0.85	0.90	1.67	1.67	1.67	1.95	1.67	1.67	1.67	1.95	ns
LVC MOS25_S_12	0.83	0.85	0.85	0.90	2.05	2.14	2.14	2.47	2.05	2.14	2.14	2.47	ns
LVC MOS25_S_16	0.83	0.85	0.85	0.90	1.84	1.89	1.89	2.19	1.84	1.89	1.89	2.19	ns
LVC MOS25_S_4	0.83	0.85	0.85	0.90	3.23	3.27	3.27	3.68	3.23	3.27	3.27	3.68	ns
LVC MOS25_S_8	0.83	0.85	0.85	0.90	2.11	2.15	2.15	2.47	2.11	2.15	2.15	2.47	ns
LVC MOS33_F_12	0.96	0.97	0.97	1.03	1.98	1.98	1.98	2.24	1.98	1.98	1.98	2.24	ns
LVC MOS33_F_16	0.96	0.97	0.97	1.03	1.79	1.79	1.79	2.09	1.79	1.79	1.79	2.09	ns
LVC MOS33_F_4	0.96	0.97	0.97	1.03	2.34	2.34	2.34	2.63	2.34	2.34	2.34	2.63	ns
LVC MOS33_F_8	0.96	0.97	0.97	1.03	2.05	2.05	2.05	2.32	2.05	2.05	2.05	2.32	ns
LVC MOS33_S_12	0.96	0.97	0.97	1.03	2.13	2.13	2.13	2.48	2.13	2.13	2.13	2.48	ns
LVC MOS33_S_16	0.96	0.97	0.97	1.03	2.11	2.11	2.11	2.43	2.11	2.11	2.11	2.43	ns
LVC MOS33_S_4	0.96	0.97	0.97	1.03	3.23	3.23	3.23	3.67	3.23	3.23	3.23	3.67	ns
LVC MOS33_S_8	0.96	0.97	0.97	1.03	2.28	2.28	2.28	2.55	2.66	2.67	2.67	2.78	ns
LVDS_25	0.45	0.58	0.58	0.62	0.80	0.83	0.83	0.95	105.74	105.74	105.74	105.85	ns
LVPECL	0.43	0.57	0.57	0.62	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
LVTTTL_F_12	1.04	1.04	1.04	1.05	1.83	1.83	1.83	2.10	1.83	1.83	1.83	2.10	ns
LVTTTL_F_16	1.04	1.04	1.04	1.05	1.79	1.79	1.79	2.06	1.79	1.79	1.79	2.06	ns
LVTTTL_F_4	1.04	1.04	1.04	1.05	2.34	2.34	2.34	2.63	2.34	2.34	2.34	2.63	ns
LVTTTL_F_8	1.04	1.04	1.04	1.05	1.97	1.97	1.97	2.22	1.97	1.97	1.97	2.22	ns
LVTTTL_S_12	1.04	1.04	1.04	1.05	1.90	1.90	1.90	2.19	1.96	1.97	1.97	2.19	ns
LVTTTL_S_16	1.04	1.04	1.04	1.05	2.07	2.07	2.07	2.40	2.07	2.07	2.07	2.40	ns
LVTTTL_S_4	1.04	1.04	1.04	1.05	3.23	3.23	3.23	3.67	3.23	3.23	3.23	3.67	ns
LVTTTL_S_8	1.04	1.04	1.04	1.05	2.22	2.22	2.22	2.47	2.22	2.37	2.37	2.50	ns

**Table 27: IOB High Range (HR) Switching Characteristics (Cont'd)**

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	1.0V		0.95V		1.0V		0.95V		1.0V		0.95V		
	-3	-1H	-2	-1	-3	-1H	-2	-1	-3	-1H	-2	-1	
MINI_LVDS_25	0.45	0.58	0.58	0.62	0.80	0.83	0.83	0.95	105.74	105.74	105.74	105.85	ns
PPDS_25	0.45	0.58	0.58	0.62	0.80	0.83	0.83	0.95	105.74	105.74	105.74	105.85	ns
RSDS_25	0.45	0.58	0.58	0.62	0.80	0.83	0.83	0.95	105.74	105.74	105.74	105.85	ns
SLVS_400_25	0.45	0.58	0.58	0.62	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns
SSTL12_F	0.52	0.55	0.55	0.59	0.72	0.72	0.72	0.91	0.83	0.83	0.83	1.04	ns
SSTL12_S	0.52	0.55	0.55	0.59	0.78	0.78	0.78	0.97	0.88	0.88	0.88	1.11	ns
SSTL135_F	0.52	0.55	0.55	0.59	0.72	0.72	0.72	0.90	0.88	0.89	0.89	1.11	ns
SSTL135_S	0.52	0.55	0.55	0.59	0.77	0.77	0.77	0.97	0.94	0.94	0.94	1.18	ns
SSTL135_R_F	0.52	0.55	0.55	0.59	0.74	0.74	0.74	0.93	0.85	0.86	0.86	1.08	ns
SSTL135_R_S	0.52	0.55	0.55	0.59	0.82	0.82	0.82	1.02	0.95	0.96	0.96	1.19	ns
SSTL15_F	0.52	0.55	0.55	0.59	0.68	0.68	0.68	0.87	0.83	0.84	0.84	1.07	ns
SSTL15_S	0.52	0.55	0.55	0.59	0.80	0.80	0.80	1.00	0.98	0.99	0.99	1.23	ns
SSTL15_R_F	0.52	0.55	0.55	0.59	0.75	0.75	0.75	0.94	0.88	0.89	0.89	1.11	ns
SSTL15_R_S	0.52	0.55	0.55	0.59	0.83	0.83	0.83	1.04	0.95	0.96	0.96	1.20	ns
SSTL18_I_F	0.52	0.55	0.55	0.59	0.76	0.76	0.76	0.96	0.94	0.95	0.95	1.21	ns
SSTL18_I_S	0.52	0.55	0.55	0.59	0.88	0.88	0.88	1.08	0.88	0.88	0.88	1.08	ns
SSTL18_II_F	0.52	0.55	0.55	0.59	0.73	0.73	0.73	0.92	0.89	0.90	0.90	1.14	ns
SSTL18_II_S	0.52	0.55	0.55	0.59	0.85	0.85	0.85	1.05	1.01	1.06	1.06	1.32	ns
SUB_LVDS_25	0.45	0.58	0.58	0.62	0.80	0.83	0.83	0.95	105.74	105.74	105.74	105.85	ns
TMDS_33	0.57	0.65	0.65	0.73	0.80	0.83	0.83	0.95	105.74	105.74	105.74	105.85	ns

Table 28: IOB High Performance (HP) Switching Characteristics

I/O Standards	T <sub>INBUF_DELAY_PAD_I</sub>				T <sub>OUTBUF_DELAY_O_PAD</sub>				T <sub>OUTBUF_DELAY_TD_PAD</sub>				Units
	1.0V		0.95V		1.0V		0.95V		1.0V		0.95V		
	-3	-1H	-2	-1	-3	-1H	-2	-1	-3	-1H	-2	-1	
DIFF_HSTL_I_12_F	0.43	0.48	0.48	0.55	0.46	0.50	0.50	0.54	0.54	0.62	0.62	0.68	ns
DIFF_HSTL_I_12_M	0.43	0.48	0.48	0.55	0.50	0.55	0.55	0.60	0.60	0.68	0.68	0.76	ns
DIFF_HSTL_I_12_S	0.43	0.48	0.48	0.55	0.56	0.61	0.61	0.67	0.67	0.76	0.76	0.85	ns
DIFF_HSTL_I_18_F	0.43	0.48	0.48	0.55	0.45	0.49	0.49	0.53	0.53	0.61	0.61	0.68	ns
DIFF_HSTL_I_18_M	0.43	0.48	0.48	0.55	0.50	0.55	0.55	0.59	0.59	0.68	0.68	0.76	ns
DIFF_HSTL_I_18_S	0.43	0.48	0.48	0.55	0.56	0.62	0.62	0.67	0.67	0.77	0.77	0.86	ns
DIFF_HSTL_I_DCI_12_F	0.43	0.48	0.48	0.55	0.46	0.50	0.50	0.54	0.54	0.62	0.62	0.68	ns
DIFF_HSTL_I_DCI_12_M	0.43	0.48	0.48	0.55	0.50	0.55	0.55	0.60	0.60	0.68	0.68	0.76	ns
DIFF_HSTL_I_DCI_12_S	0.43	0.48	0.48	0.55	0.56	0.61	0.61	0.67	0.67	0.76	0.76	0.85	ns
DIFF_HSTL_I_DCI_18_F	0.43	0.48	0.48	0.55	0.45	0.49	0.49	0.53	0.53	0.61	0.61	0.68	ns
DIFF_HSTL_I_DCI_18_M	0.43	0.48	0.48	0.55	0.50	0.55	0.55	0.59	0.59	0.68	0.68	0.76	ns
DIFF_HSTL_I_DCI_18_S	0.43	0.48	0.48	0.55	0.56	0.62	0.62	0.67	0.67	0.77	0.77	0.86	ns
DIFF_HSTL_I_DCI_F	0.43	0.48	0.48	0.55	0.46	0.50	0.50	0.54	0.54	0.62	0.62	0.68	ns
DIFF_HSTL_I_DCI_M	0.43	0.48	0.48	0.55	0.50	0.55	0.55	0.60	0.60	0.68	0.68	0.76	ns
DIFF_HSTL_I_DCI_S	0.43	0.48	0.48	0.55	0.56	0.61	0.61	0.67	0.67	0.76	0.76	0.85	ns
DIFF_HSTL_I_F	0.43	0.48	0.48	0.55	0.46	0.50	0.50	0.54	0.54	0.62	0.62	0.68	ns
DIFF_HSTL_I_M	0.43	0.48	0.48	0.55	0.50	0.55	0.55	0.60	0.60	0.68	0.68	0.76	ns
DIFF_HSTL_I_S	0.43	0.48	0.48	0.55	0.56	0.61	0.61	0.67	0.67	0.76	0.76	0.85	ns
DIFF_HSUL_12_DCI_F	0.43	0.48	0.48	0.55	0.46	0.50	0.50	0.54	0.54	0.62	0.62	0.68	ns
DIFF_HSUL_12_DCI_M	0.43	0.48	0.48	0.55	0.50	0.55	0.55	0.60	0.60	0.68	0.68	0.76	ns
DIFF_HSUL_12_DCI_S	0.43	0.48	0.48	0.55	0.56	0.61	0.61	0.67	0.67	0.76	0.76	0.85	ns
DIFF_HSUL_12_F	0.43	0.48	0.48	0.55	0.46	0.50	0.50	0.54	0.54	0.62	0.62	0.68	ns
DIFF_HSUL_12_M	0.43	0.48	0.48	0.55	0.50	0.55	0.55	0.60	0.60	0.68	0.68	0.76	ns
DIFF_HSUL_12_S	0.43	0.48	0.48	0.55	0.56	0.61	0.61	0.67	0.67	0.76	0.76	0.85	ns
DIFF_POD10_DCI_F	0.43	0.48	0.48	0.55	0.46	0.50	0.50	0.55	0.58	0.65	0.65	0.73	ns
DIFF_POD10_DCI_M	0.43	0.48	0.48	0.55	0.52	0.58	0.58	0.63	0.62	0.71	0.71	0.79	ns
DIFF_POD10_DCI_S	0.43	0.48	0.48	0.55	0.61	0.68	0.68	0.74	0.69	0.79	0.79	0.88	ns
DIFF_POD10_F	0.43	0.48	0.48	0.55	0.46	0.50	0.50	0.55	0.58	0.65	0.65	0.73	ns
DIFF_POD10_M	0.43	0.48	0.48	0.55	0.52	0.58	0.58	0.63	0.62	0.71	0.71	0.79	ns
DIFF_POD10_S	0.43	0.48	0.48	0.55	0.61	0.68	0.68	0.74	0.69	0.79	0.79	0.88	ns
DIFF_POD12_DCI_F	0.43	0.48	0.48	0.55	0.46	0.50	0.50	0.55	0.58	0.65	0.65	0.73	ns
DIFF_POD12_DCI_M	0.43	0.48	0.48	0.55	0.52	0.58	0.58	0.63	0.62	0.71	0.71	0.79	ns
DIFF_POD12_DCI_S	0.43	0.48	0.48	0.55	0.61	0.68	0.68	0.74	0.69	0.79	0.79	0.88	ns
DIFF_POD12_F	0.43	0.48	0.48	0.55	0.46	0.50	0.50	0.55	0.58	0.65	0.65	0.73	ns
DIFF_POD12_M	0.43	0.48	0.48	0.55	0.52	0.58	0.58	0.63	0.62	0.71	0.71	0.79	ns
DIFF_POD12_S	0.43	0.48	0.48	0.55	0.61	0.68	0.68	0.74	0.69	0.79	0.79	0.88	ns
DIFF_SSTL12_DCI_F	0.43	0.48	0.48	0.55	0.46	0.50	0.50	0.54	0.54	0.62	0.62	0.68	ns
DIFF_SSTL12_DCI_M	0.43	0.48	0.48	0.55	0.50	0.55	0.55	0.60	0.60	0.68	0.68	0.76	ns

**Table 28: IOB High Performance (HP) Switching Characteristics (Cont'd)**

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	1.0V		0.95V		1.0V		0.95V		1.0V		0.95V		
	-3	-1H	-2	-1	-3	-1H	-2	-1	-3	-1H	-2	-1	
DIFF_SSTL12_DCI_S	0.43	0.48	0.48	0.55	0.56	0.61	0.61	0.67	0.67	0.76	0.76	0.85	ns
DIFF_SSTL12_F	0.43	0.48	0.48	0.55	0.46	0.50	0.50	0.54	0.54	0.62	0.62	0.68	ns
DIFF_SSTL12_M	0.43	0.48	0.48	0.55	0.50	0.55	0.55	0.60	0.60	0.68	0.68	0.76	ns
DIFF_SSTL12_S	0.43	0.48	0.48	0.55	0.56	0.61	0.61	0.67	0.67	0.76	0.76	0.85	ns
DIFF_SSTL135_DCI_F	0.43	0.48	0.48	0.55	0.46	0.50	0.50	0.54	0.54	0.62	0.62	0.69	ns
DIFF_SSTL135_DCI_M	0.43	0.48	0.48	0.55	0.50	0.55	0.55	0.60	0.60	0.68	0.68	0.76	ns
DIFF_SSTL135_DCI_S	0.43	0.48	0.48	0.55	0.56	0.61	0.61	0.67	0.67	0.76	0.76	0.85	ns
DIFF_SSTL135_F	0.43	0.48	0.48	0.55	0.46	0.50	0.50	0.54	0.54	0.62	0.62	0.69	ns
DIFF_SSTL135_M	0.43	0.48	0.48	0.55	0.50	0.55	0.55	0.60	0.60	0.68	0.68	0.76	ns
DIFF_SSTL135_S	0.43	0.48	0.48	0.55	0.56	0.61	0.61	0.67	0.67	0.76	0.76	0.85	ns
DIFF_SSTL15_DCI_F	0.43	0.48	0.48	0.55	0.46	0.50	0.50	0.54	0.54	0.62	0.62	0.68	ns
DIFF_SSTL15_DCI_M	0.43	0.48	0.48	0.55	0.50	0.55	0.55	0.60	0.60	0.68	0.68	0.76	ns
DIFF_SSTL15_DCI_S	0.43	0.48	0.48	0.55	0.56	0.61	0.61	0.67	0.67	0.76	0.76	0.85	ns
DIFF_SSTL15_F	0.43	0.48	0.48	0.55	0.46	0.50	0.50	0.54	0.54	0.62	0.62	0.68	ns
DIFF_SSTL15_M	0.43	0.48	0.48	0.55	0.50	0.55	0.55	0.60	0.60	0.68	0.68	0.76	ns
DIFF_SSTL15_S	0.43	0.48	0.48	0.55	0.56	0.61	0.61	0.67	0.67	0.76	0.76	0.85	ns
DIFF_SSTL18_I_DCI_F	0.43	0.48	0.48	0.55	0.45	0.49	0.49	0.53	0.53	0.61	0.61	0.68	ns
DIFF_SSTL18_I_DCI_M	0.43	0.48	0.48	0.55	0.50	0.55	0.55	0.59	0.59	0.68	0.68	0.76	ns
DIFF_SSTL18_I_DCI_S	0.43	0.48	0.48	0.55	0.56	0.62	0.62	0.67	0.67	0.77	0.77	0.86	ns
DIFF_SSTL18_I_F	0.43	0.48	0.48	0.55	0.45	0.49	0.49	0.53	0.53	0.61	0.61	0.68	ns
DIFF_SSTL18_I_M	0.43	0.48	0.48	0.55	0.50	0.55	0.55	0.59	0.59	0.68	0.68	0.76	ns
DIFF_SSTL18_I_S	0.43	0.48	0.48	0.55	0.56	0.62	0.62	0.67	0.67	0.77	0.77	0.86	ns
HSLVDCI_15_F	0.43	0.46	0.46	0.52	0.48	0.53	0.53	0.56	0.57	0.64	0.64	0.71	ns
HSLVDCI_15_M	0.43	0.46	0.46	0.52	0.53	0.57	0.57	0.62	0.62	0.71	0.71	0.79	ns
HSLVDCI_15_S	0.43	0.46	0.46	0.52	0.58	0.64	0.64	0.69	0.70	0.79	0.79	0.88	ns
HSLVDCI_18_F	0.43	0.46	0.46	0.52	0.48	0.53	0.53	0.57	0.57	0.65	0.65	0.71	ns
HSLVDCI_18_M	0.43	0.46	0.46	0.52	0.52	0.57	0.57	0.62	0.62	0.71	0.71	0.79	ns
HSLVDCI_18_S	0.43	0.46	0.46	0.52	0.58	0.64	0.64	0.69	0.70	0.80	0.80	0.90	ns
HSTL_I_12_F	0.43	0.46	0.46	0.52	0.48	0.52	0.52	0.56	0.56	0.63	0.63	0.70	ns
HSTL_I_12_M	0.43	0.46	0.46	0.52	0.52	0.57	0.57	0.61	0.61	0.70	0.70	0.78	ns
HSTL_I_12_S	0.43	0.46	0.46	0.52	0.57	0.63	0.63	0.68	0.69	0.78	0.78	0.87	ns
HSTL_I_18_F	0.43	0.46	0.46	0.52	0.47	0.51	0.51	0.55	0.55	0.63	0.63	0.70	ns
HSTL_I_18_M	0.43	0.46	0.46	0.52	0.52	0.57	0.57	0.61	0.61	0.70	0.70	0.78	ns
HSTL_I_18_S	0.43	0.46	0.46	0.52	0.58	0.63	0.63	0.69	0.69	0.78	0.78	0.88	ns
HSTL_I_DCI_12_F	0.43	0.46	0.46	0.52	0.48	0.52	0.52	0.56	0.56	0.63	0.63	0.70	ns
HSTL_I_DCI_12_M	0.43	0.46	0.46	0.52	0.52	0.57	0.57	0.61	0.61	0.70	0.70	0.78	ns
HSTL_I_DCI_12_S	0.43	0.46	0.46	0.52	0.57	0.63	0.63	0.68	0.69	0.78	0.78	0.87	ns
HSTL_I_DCI_18_F	0.43	0.46	0.46	0.52	0.47	0.51	0.51	0.55	0.55	0.63	0.63	0.70	ns

**Table 28: IOB High Performance (HP) Switching Characteristics (Cont'd)**

I/O Standards	T <sub>INBUF_DELAY_PAD_I</sub>				T <sub>OUTBUF_DELAY_O_PAD</sub>				T <sub>OUTBUF_DELAY_TD_PAD</sub>				Units
	1.0V		0.95V		1.0V		0.95V		1.0V		0.95V		
	-3	-1H	-2	-1	-3	-1H	-2	-1	-3	-1H	-2	-1	
HSTL_I_DCI_18_M	0.43	0.46	0.46	0.52	0.52	0.57	0.57	0.61	0.61	0.70	0.70	0.78	ns
HSTL_I_DCI_18_S	0.43	0.46	0.46	0.52	0.58	0.63	0.63	0.69	0.69	0.78	0.78	0.88	ns
HSTL_I_DCI_F	0.43	0.46	0.46	0.52	0.47	0.52	0.52	0.56	0.56	0.63	0.63	0.70	ns
HSTL_I_DCI_M	0.43	0.46	0.46	0.52	0.52	0.57	0.57	0.61	0.61	0.70	0.70	0.78	ns
HSTL_I_DCI_S	0.43	0.46	0.46	0.52	0.57	0.63	0.63	0.68	0.69	0.78	0.78	0.87	ns
HSTL_I_F	0.43	0.46	0.46	0.52	0.47	0.52	0.52	0.56	0.56	0.63	0.63	0.70	ns
HSTL_I_M	0.43	0.46	0.46	0.52	0.52	0.57	0.57	0.61	0.61	0.70	0.70	0.78	ns
HSTL_I_S	0.43	0.46	0.46	0.52	0.57	0.63	0.63	0.68	0.69	0.78	0.78	0.87	ns
HSUL_12_DCI_F	0.43	0.46	0.46	0.52	0.48	0.52	0.52	0.56	0.56	0.63	0.63	0.70	ns
HSUL_12_DCI_M	0.43	0.46	0.46	0.52	0.52	0.57	0.57	0.61	0.61	0.70	0.70	0.78	ns
HSUL_12_DCI_S	0.43	0.46	0.46	0.52	0.57	0.63	0.63	0.68	0.69	0.78	0.78	0.87	ns
HSUL_12_F	0.43	0.46	0.46	0.52	0.48	0.52	0.52	0.56	0.56	0.63	0.63	0.70	ns
HSUL_12_M	0.43	0.46	0.46	0.52	0.52	0.57	0.57	0.61	0.61	0.70	0.70	0.78	ns
HSUL_12_S	0.43	0.46	0.46	0.52	0.57	0.63	0.63	0.68	0.69	0.78	0.78	0.87	ns
LVC MOS12_F_2	0.56	0.66	0.66	0.74	0.67	0.73	0.73	0.79	0.67	0.73	0.73	0.79	ns
LVC MOS12_F_4	0.56	0.66	0.66	0.74	0.63	0.68	0.68	0.73	0.63	0.68	0.68	0.73	ns
LVC MOS12_F_6	0.56	0.66	0.66	0.74	0.59	0.64	0.64	0.69	0.59	0.65	0.65	0.72	ns
LVC MOS12_F_8	0.56	0.66	0.66	0.74	0.57	0.63	0.63	0.67	0.59	0.66	0.66	0.72	ns
LVC MOS12_M_2	0.56	0.66	0.66	0.74	0.72	0.79	0.79	0.85	0.72	0.79	0.79	0.85	ns
LVC MOS12_M_4	0.56	0.66	0.66	0.74	0.66	0.71	0.71	0.77	0.66	0.71	0.71	0.77	ns
LVC MOS12_M_6	0.56	0.66	0.66	0.74	0.62	0.67	0.67	0.72	0.62	0.69	0.69	0.75	ns
LVC MOS12_M_8	0.56	0.66	0.66	0.74	0.62	0.67	0.67	0.72	0.64	0.71	0.71	0.78	ns
LVC MOS12_S_2	0.56	0.66	0.66	0.74	0.77	0.89	0.89	0.96	0.77	0.89	0.89	0.96	ns
LVC MOS12_S_4	0.56	0.66	0.66	0.74	0.68	0.74	0.74	0.79	0.68	0.74	0.74	0.79	ns
LVC MOS12_S_6	0.56	0.66	0.66	0.74	0.66	0.72	0.72	0.78	0.66	0.72	0.72	0.79	ns
LVC MOS12_S_8	0.56	0.66	0.66	0.74	0.66	0.72	0.72	0.77	0.67	0.74	0.74	0.82	ns
LVC MOS15_F_12	0.45	0.52	0.52	0.58	0.61	0.66	0.66	0.71	0.66	0.73	0.73	0.81	ns
LVC MOS15_F_2	0.45	0.52	0.52	0.58	0.73	0.77	0.77	0.83	0.73	0.77	0.77	0.83	ns
LVC MOS15_F_4	0.45	0.52	0.52	0.58	0.69	0.73	0.73	0.78	0.69	0.73	0.73	0.78	ns
LVC MOS15_F_6	0.45	0.52	0.52	0.58	0.63	0.68	0.68	0.73	0.63	0.70	0.70	0.77	ns
LVC MOS15_F_8	0.45	0.52	0.52	0.58	0.61	0.66	0.66	0.72	0.63	0.71	0.71	0.78	ns
LVC MOS15_M_12	0.45	0.52	0.52	0.58	0.63	0.69	0.69	0.75	0.67	0.77	0.77	0.85	ns
LVC MOS15_M_2	0.45	0.52	0.52	0.58	0.77	0.80	0.80	0.86	0.77	0.80	0.80	0.86	ns
LVC MOS15_M_4	0.45	0.52	0.52	0.58	0.72	0.76	0.76	0.82	0.72	0.76	0.76	0.82	ns
LVC MOS15_M_6	0.45	0.52	0.52	0.58	0.67	0.72	0.72	0.78	0.67	0.74	0.74	0.82	ns
LVC MOS15_M_8	0.45	0.52	0.52	0.58	0.65	0.71	0.71	0.76	0.65	0.76	0.76	0.83	ns
LVC MOS15_S_12	0.45	0.52	0.52	0.58	0.65	0.70	0.70	0.75	0.67	0.75	0.75	0.83	ns
LVC MOS15_S_2	0.45	0.52	0.52	0.58	0.78	0.85	0.85	0.91	0.78	0.85	0.85	0.91	ns

Table 28: IOB High Performance (HP) Switching Characteristics (Cont'd)

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	1.0V		0.95V		1.0V		0.95V		1.0V		0.95V		
	-3	-1H	-2	-1	-3	-1H	-2	-1	-3	-1H	-2	-1	
LVC MOS15_S_4	0.45	0.52	0.52	0.58	0.74	0.78	0.78	0.84	0.74	0.78	0.78	0.84	ns
LVC MOS15_S_6	0.45	0.52	0.52	0.58	0.72	0.76	0.76	0.82	0.72	0.76	0.76	0.84	ns
LVC MOS15_S_8	0.45	0.52	0.52	0.58	0.68	0.73	0.73	0.79	0.68	0.75	0.75	0.83	ns
LVC MOS18_F_12	0.43	0.49	0.49	0.54	0.67	0.72	0.72	0.78	0.67	0.81	0.81	0.90	ns
LVC MOS18_F_2	0.43	0.49	0.49	0.54	0.94	1.07	1.07	1.15	0.94	1.07	1.07	1.15	ns
LVC MOS18_F_4	0.43	0.49	0.49	0.54	0.78	0.82	0.82	0.89	0.78	0.82	0.82	0.89	ns
LVC MOS18_F_6	0.43	0.49	0.49	0.54	0.72	0.77	0.77	0.83	0.72	0.79	0.79	0.88	ns
LVC MOS18_F_8	0.43	0.49	0.49	0.54	0.70	0.75	0.75	0.81	0.72	0.81	0.81	0.89	ns
LVC MOS18_M_12	0.43	0.49	0.49	0.54	0.70	0.76	0.76	0.81	0.74	0.83	0.83	0.92	ns
LVC MOS18_M_2	0.43	0.49	0.49	0.54	0.99	1.10	1.10	1.19	0.99	1.10	1.10	1.19	ns
LVC MOS18_M_4	0.43	0.49	0.49	0.54	0.82	0.86	0.86	0.92	0.82	0.86	0.86	0.92	ns
LVC MOS18_M_6	0.43	0.49	0.49	0.54	0.75	0.80	0.80	0.87	0.75	0.81	0.81	0.90	ns
LVC MOS18_M_8	0.43	0.49	0.49	0.54	0.73	0.78	0.78	0.85	0.73	0.83	0.83	0.92	ns
LVC MOS18_S_12	0.43	0.49	0.49	0.54	0.74	0.78	0.78	0.84	0.76	0.83	0.83	0.92	ns
LVC MOS18_S_2	0.43	0.49	0.49	0.54	1.05	1.16	1.16	1.25	1.05	1.16	1.16	1.25	ns
LVC MOS18_S_4	0.43	0.49	0.49	0.54	0.83	0.86	0.86	0.93	0.83	0.86	0.86	0.93	ns
LVC MOS18_S_6	0.43	0.49	0.49	0.54	0.79	0.82	0.82	0.89	0.79	0.82	0.82	0.90	ns
LVC MOS18_S_8	0.43	0.49	0.49	0.54	0.75	0.80	0.80	0.86	0.75	0.82	0.82	0.90	ns
LVDCI_15_F	0.45	0.52	0.52	0.58	0.48	0.53	0.53	0.56	0.57	0.64	0.64	0.71	ns
LVDCI_15_M	0.45	0.52	0.52	0.58	0.53	0.57	0.57	0.62	0.62	0.71	0.71	0.79	ns
LVDCI_15_S	0.45	0.52	0.52	0.58	0.58	0.64	0.64	0.69	0.70	0.79	0.79	0.88	ns
LVDCI_18_F	0.43	0.49	0.49	0.54	0.48	0.53	0.53	0.57	0.57	0.65	0.65	0.71	ns
LVDCI_18_M	0.43	0.49	0.49	0.54	0.52	0.57	0.57	0.62	0.62	0.71	0.71	0.79	ns
LVDCI_18_S	0.43	0.49	0.49	0.54	0.58	0.64	0.64	0.69	0.70	0.80	0.80	0.90	ns
LVDS	0.42	0.46	0.46	0.51	0.57	0.67	0.67	0.72	890.24	890.26	890.26	890.28	ns
POD10_DCI_F	0.43	0.46	0.46	0.52	0.48	0.52	0.52	0.56	0.59	0.67	0.67	0.74	ns
POD10_DCI_M	0.43	0.46	0.46	0.52	0.54	0.60	0.60	0.65	0.64	0.73	0.73	0.81	ns
POD10_DCI_S	0.43	0.46	0.46	0.52	0.63	0.69	0.69	0.76	0.71	0.81	0.81	0.89	ns
POD10_F	0.43	0.46	0.46	0.52	0.48	0.52	0.52	0.56	0.59	0.67	0.67	0.74	ns
POD10_M	0.43	0.46	0.46	0.52	0.54	0.60	0.60	0.65	0.64	0.73	0.73	0.81	ns
POD10_S	0.43	0.46	0.46	0.52	0.63	0.69	0.69	0.76	0.71	0.81	0.81	0.89	ns
POD12_DCI_F	0.43	0.46	0.46	0.52	0.48	0.52	0.52	0.56	0.59	0.67	0.67	0.74	ns
POD12_DCI_M	0.43	0.46	0.46	0.52	0.54	0.60	0.60	0.65	0.64	0.73	0.73	0.81	ns
POD12_DCI_S	0.43	0.46	0.46	0.52	0.63	0.69	0.69	0.76	0.71	0.81	0.81	0.89	ns
POD12_F	0.43	0.46	0.46	0.52	0.48	0.52	0.52	0.56	0.59	0.67	0.67	0.74	ns
POD12_M	0.43	0.46	0.46	0.52	0.54	0.60	0.60	0.65	0.64	0.73	0.73	0.81	ns
POD12_S	0.43	0.46	0.46	0.52	0.63	0.69	0.69	0.76	0.71	0.81	0.81	0.89	ns
SLVS_400_18	0.42	0.46	0.46	0.51	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ns

**Table 28: IOB High Performance (HP) Switching Characteristics (Cont'd)**

I/O Standards	$T_{INBUF\_DELAY\_PAD\_I}$				$T_{OUTBUF\_DELAY\_O\_PAD}$				$T_{OUTBUF\_DELAY\_TD\_PAD}$				Units
	1.0V		0.95V		1.0V		0.95V		1.0V		0.95V		
	-3	-1H	-2	-1	-3	-1H	-2	-1	-3	-1H	-2	-1	
SSTL12_DCI_F	0.43	0.46	0.46	0.52	0.48	0.52	0.52	0.56	0.56	0.63	0.63	0.70	ns
SSTL12_DCI_M	0.43	0.46	0.46	0.52	0.52	0.57	0.57	0.61	0.61	0.70	0.70	0.78	ns
SSTL12_DCI_S	0.43	0.46	0.46	0.52	0.57	0.63	0.63	0.68	0.69	0.78	0.78	0.87	ns
SSTL12_F	0.43	0.46	0.46	0.52	0.48	0.52	0.52	0.56	0.56	0.63	0.63	0.70	ns
SSTL12_M	0.43	0.46	0.46	0.52	0.52	0.57	0.57	0.61	0.61	0.70	0.70	0.78	ns
SSTL12_S	0.43	0.46	0.46	0.52	0.57	0.63	0.63	0.68	0.69	0.78	0.78	0.87	ns
SSTL135_DCI_F	0.43	0.46	0.46	0.52	0.48	0.52	0.52	0.56	0.56	0.64	0.64	0.70	ns
SSTL135_DCI_M	0.43	0.46	0.46	0.52	0.52	0.57	0.57	0.61	0.61	0.70	0.70	0.78	ns
SSTL135_DCI_S	0.43	0.46	0.46	0.52	0.57	0.63	0.63	0.68	0.69	0.78	0.78	0.87	ns
SSTL135_F	0.43	0.46	0.46	0.52	0.48	0.52	0.52	0.56	0.56	0.64	0.64	0.70	ns
SSTL135_M	0.43	0.46	0.46	0.52	0.52	0.57	0.57	0.61	0.61	0.70	0.70	0.78	ns
SSTL135_S	0.43	0.46	0.46	0.52	0.57	0.63	0.63	0.68	0.69	0.78	0.78	0.87	ns
SSTL15_DCI_F	0.43	0.46	0.46	0.52	0.47	0.52	0.52	0.56	0.56	0.63	0.63	0.70	ns
SSTL15_DCI_M	0.43	0.46	0.46	0.52	0.52	0.57	0.57	0.61	0.61	0.70	0.70	0.78	ns
SSTL15_DCI_S	0.43	0.46	0.46	0.52	0.57	0.63	0.63	0.68	0.69	0.78	0.78	0.87	ns
SSTL15_F	0.43	0.46	0.46	0.52	0.47	0.52	0.52	0.56	0.56	0.63	0.63	0.70	ns
SSTL15_M	0.43	0.46	0.46	0.52	0.52	0.57	0.57	0.61	0.61	0.70	0.70	0.78	ns
SSTL15_S	0.43	0.46	0.46	0.52	0.57	0.63	0.63	0.68	0.69	0.78	0.78	0.87	ns
SSTL18_I_DCI_F	0.43	0.46	0.46	0.52	0.47	0.51	0.51	0.55	0.55	0.63	0.63	0.70	ns
SSTL18_I_DCI_M	0.43	0.46	0.46	0.52	0.52	0.57	0.57	0.61	0.61	0.70	0.70	0.78	ns
SSTL18_I_DCI_S	0.43	0.46	0.46	0.52	0.58	0.63	0.63	0.69	0.69	0.78	0.78	0.88	ns
SSTL18_I_F	0.43	0.46	0.46	0.52	0.47	0.51	0.51	0.55	0.55	0.63	0.63	0.70	ns
SSTL18_I_M	0.43	0.46	0.46	0.52	0.52	0.57	0.57	0.61	0.61	0.70	0.70	0.78	ns
SSTL18_I_S	0.43	0.46	0.46	0.52	0.58	0.63	0.63	0.69	0.69	0.78	0.78	0.88	ns
SUB_LVDS	0.42	0.46	0.46	0.51	0.57	0.67	0.67	0.72	890.24	890.26	890.26	890.28	ns

Table 29 specifies the values of  $T_{\text{OUTBUF\_DELAY\_TE\_PAD}}$  and  $T_{\text{INBUF\_DELAY\_IBUFDIS\_O}}$ .  $T_{\text{OUTBUF\_DELAY\_TE\_PAD}}$  is the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state).  $T_{\text{INBUF\_DELAY\_IBUFDIS\_O}}$  is the IOB delay from IBUFDISABLE to O output. In HP I/O banks, the internal DCI termination turn-off time is always faster than  $T_{\text{OUTBUF\_DELAY\_TE\_PAD}}$  when the DCITERMDISABLE pin is used. In HR I/O banks, the internal IN\_TERM termination turn-off time is always faster than  $T_{\text{OUTBUF\_DELAY\_TE\_PAD}}$  when the INTERMDISABLE pin is used.

Table 29: IOB 3-state Output Switching Characteristics

Symbol	Description	Speed Grades and $V_{\text{CCINT}}$ Operating Voltages				Units
		1.0V		0.95V		
		-3	-1H	-2	-1	
$T_{\text{OUTBUF\_DELAY\_TE\_PAD}}^{(1)}$	T input to pad high-impedance for HR I/O banks	1.37	1.52	1.52	1.69	ns
	T input to pad high-impedance for HP I/O banks	0.62	0.71	0.71	0.78	ns
$T_{\text{INBUF\_DELAY\_IBUFDIS\_O}}$	IBUF turn-on time from IBUFDISABLE to O output for HR I/O banks	0.47	0.65	0.65	0.68	ns
	IBUF turn-on time from IBUFDISABLE to O output for HP I/O banks	1.06	1.21	1.21	1.49	ns

**Notes:**

1. The  $T_{\text{OUTBUF\_DELAY\_TE\_PAD}}$  values are applicable to single-ended I/O standards. For true differential standards, the values are larger. Use the Vivado timing report for the most accurate timing values for your configuration.

## I/O Standard Adjustment Measurement Methodology

### Input Delay Measurements

Table 30 shows the test setup parameters used for measuring input delay.

Table 30: Input Delay Measurement Methodology

Description	I/O Standard Attribute	$V_L^{(1)(2)}$	$V_H^{(1)(2)}$	$V_{\text{MEAS}}^{(1)(4)(6)}$	$V_{\text{REF}}^{(1)(3)(5)}$
LVC MOS, 1.2V	LVC MOS12	0.1	1.1	0.6	–
LVC MOS, LVDCI, HSLVDCI, 1.5V	LVC MOS15, LVDCI_15, HSLVDCI_15	0.1	1.4	0.75	–
LVC MOS, LVDCI, HSLVDCI, 1.8V	LVC MOS18, LVDCI_18, HSLVDCI_18	0.1	1.7	0.9	–
LVC MOS, 2.5V	LVC MOS25	0.1	2.4	1.25	–
LVC MOS, 3.3V	LVC MOS33	0.1	3.2	1.65	–
LVTTL, 3.3V	LVTTL	0.1	3.2	1.65	–
HSTL (high-speed transceiver logic), Class I, 1.2V	HSTL_I_12	$V_{\text{REF}} - 0.5$	$V_{\text{REF}} + 0.5$	$V_{\text{REF}}$	0.60
HSTL, Class I and II, 1.5V	HSTL_I, HSTL_II	$V_{\text{REF}} - 0.65$	$V_{\text{REF}} + 0.65$	$V_{\text{REF}}$	0.75
HSTL, Class I and II, 1.8V	HSTL_I_18, HSTL_II_18	$V_{\text{REF}} - 0.8$	$V_{\text{REF}} + 0.8$	$V_{\text{REF}}$	0.90
HSUL (high-speed unterminated logic), 1.2V	HSUL_12	$V_{\text{REF}} - 0.5$	$V_{\text{REF}} + 0.5$	$V_{\text{REF}}$	0.60
SSTL (stub series terminated logic), 1.2V	SSTL12	$V_{\text{REF}} - 0.5$	$V_{\text{REF}} + 0.5$	$V_{\text{REF}}$	0.60

**Table 30: Input Delay Measurement Methodology (Cont'd)**

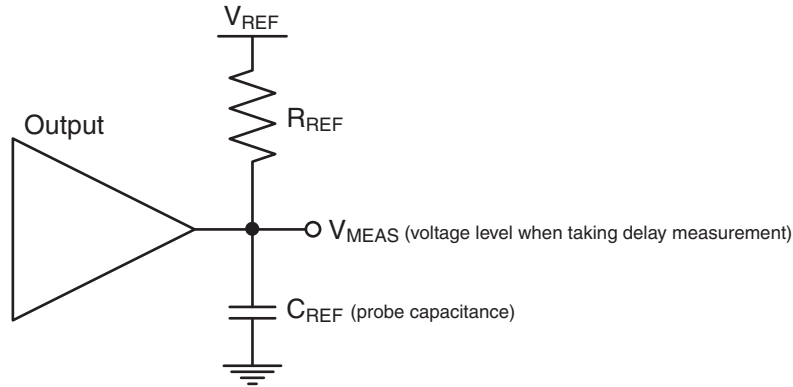
Description	I/O Standard Attribute	$V_L^{(1)(2)}$	$V_H^{(1)(2)}$	$V_{MEAS}^{(1)(4)(6)}$	$V_{REF}^{(1)(3)(5)}$
SSTL, 1.35V	SSTL135, SSTL135_R	$V_{REF} - 0.575$	$V_{REF} + 0.575$	$V_{REF}$	0.675
SSTL, 1.5V	SSTL15, SSTL15_R	$V_{REF} - 0.65$	$V_{REF} + 0.65$	$V_{REF}$	0.75
SSTL, Class I and II, 1.8V	SSTL18_I, SSTL18_II	$V_{REF} - 0.8$	$V_{REF} + 0.8$	$V_{REF}$	0.90
POD10, 1.0V	POD10	$V_{REF} - 0.6$	$V_{REF} + 0.6$	$V_{REF}$	0.70
POD12, 1.2V	POD12	$V_{REF} - 0.74$	$V_{REF} + 0.74$	$V_{REF}$	0.84
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	$0.6 - 0.125$	$0.6 + 0.125$	0 <sup>(6)</sup>	–
DIFF_HSTL, Class I and II, 1.5V	DIFF_HSTL_I, DIFF_HSTL_II	$0.75 - 0.125$	$0.75 + 0.125$	0 <sup>(6)</sup>	–
DIFF_HSTL, Class I and II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	$0.9 - 0.125$	$0.9 + 0.125$	0 <sup>(6)</sup>	–
DIFF_HSUL, 1.2V	DIFF_HSUL_12	$0.6 - 0.125$	$0.6 + 0.125$	0 <sup>(6)</sup>	–
DIFF_SSTL, 1.2V	DIFF_SSTL12	$0.6 - 0.125$	$0.6 + 0.125$	0 <sup>(6)</sup>	–
DIFF_SSTL135/DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	$0.675 - 0.125$	$0.675 + 0.125$	0 <sup>(6)</sup>	–
DIFF_SSTL15/DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	$0.75 - 0.125$	$0.75 + 0.125$	0 <sup>(6)</sup>	–
DIFF_SSTL18_I/DIFF_SSTL18_II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	$0.9 - 0.125$	$0.9 + 0.125$	0 <sup>(6)</sup>	–
DIFF_POD10, 1.0V	DIFF_POD10	$0.70 - 0.125$	$0.70 + 0.125$	0 <sup>(6)</sup>	–
DIFF_POD12, 1.2V	DIFF_POD12	$0.84 - 0.125$	$0.84 + 0.125$	0 <sup>(6)</sup>	–
LVDS (low-voltage differential signaling), 1.8V	LVDS	$0.9 - 0.125$	$0.9 + 0.125$	0 <sup>(6)</sup>	–
LVDS_25, 2.5V	LVDS_25	$1.25 - 0.125$	$1.25 + 0.125$	0 <sup>(6)</sup>	–
SUB_LVDS, 1.8V	SUB_LVDS	$0.9 - 0.125$	$0.9 + 0.125$	0 <sup>(6)</sup>	–
SLVS, 1.8V	SLVS_400_18	$0.9 - 0.125$	$0.9 + 0.125$	0 <sup>(6)</sup>	–
SLVS, 2.5V	SLVS_400_25	$1.25 - 0.125$	$1.25 + 0.125$	0 <sup>(6)</sup>	–
LVPECL, 2.5	LVPECL	$1.25 - 0.125$	$1.25 + 0.125$	0 <sup>(6)</sup>	–
BLVDS_25, 2.5V	BLVDS_25	$1.25 - 0.125$	$1.25 + 0.125$	0 <sup>(6)</sup>	–
MINI_LVDS_25, 2.5V	MINI_LVDS_25	$1.25 - 0.125$	$1.25 + 0.125$	0 <sup>(6)</sup>	–
PPDS_25	PPDS_25	$1.25 - 0.125$	$1.25 + 0.125$	0 <sup>(6)</sup>	–
RSDS_25	RSDS_25	$1.25 - 0.125$	$1.25 + 0.125$	0 <sup>(6)</sup>	–
TMDS_33	TMDS_33	$3 - 0.125$	$3 + 0.125$	0 <sup>(6)</sup>	–

**Notes:**

1. The input delay measurement methodology parameters for LVDCI are the same for LVCMOS standards of the same voltage. Input delay measurement methodology parameters for HSLVDCI are the same as for HSTL\_II standards of the same voltage. Parameters for all other DCI standards are the same for the corresponding non-DCI standards.
2. Input waveform switches between  $V_L$  and  $V_H$ .
3. Measurements are made at typical, minimum, and maximum  $V_{REF}$  values. Reported delays reflect worst case of these measurements.  $V_{REF}$  values listed are typical.
4. Input voltage level from which measurement starts.
5. This is an input voltage reference that bears no relation to the  $V_{REF}/V_{MEAS}$  parameters found in IBIS models and/or noted in Figure 1.
6. The value given is the differential input voltage.

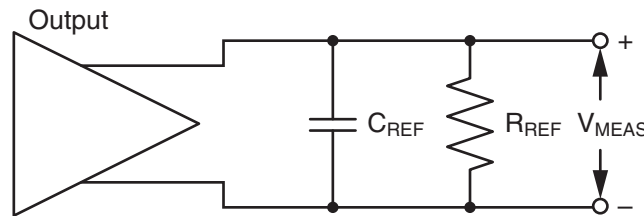
## Output Delay Measurements

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in [Figure 1](#) and [Figure 2](#).



DS893\_01\_051415

Figure 1: Single-Ended Test Setup



DS893\_02\_051415

Figure 2: Differential Test Setup

Parameters  $V_{REF}$ ,  $R_{REF}$ ,  $C_{REF}$ , and  $V_{MEAS}$  fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from [Table 31](#).
2. Record the time to  $V_{MEAS}$ .
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to  $V_{MEAS}$ .
5. Compare the results of [step 2](#) and [step 4](#). The increase or decrease in delay yields the actual propagation delay of the PCB trace.

Table 31: Output Delay Measurement Methodology

Description	I/O Standard Attribute	R <sub>REF</sub> (Ω)	C <sub>REF</sub> <sup>(1)</sup> (pF)	V <sub>MEAS</sub> (V)	V <sub>REF</sub> (V)
LVC MOS, 1.2V	LVC MOS12	1M	0	0.6	0
LVC MOS 1.5V	LVC MOS15	1M	0	0.75	0
LVC MOS 1.8V	LVC MOS18	1M	0	0.9	0
LVC MOS, 2.5V	LVC MOS25	1M	0	1.25	0
LVC MOS, 3.3V	LVC MOS33	1M	0	1.65	0
LVTTL, 3.3V	LVTTL	1M	0	1.65	0
LVDCI/HSLVDCI, 1.5V	LVDCI_15, HSLVDCI_15	50	0	V <sub>REF</sub>	0.75
LVDCI/HSLVDCI, 1.8V	LVDCI_18, HSLVDCI_18	50	0	V <sub>REF</sub>	0.9
HSTL (high-speed transceiver logic), Class I, 1.2V	HSTL_I_12	50	0	V <sub>REF</sub>	0.6
HSTL, Class I, 1.5V	HSTL_I	50	0	V <sub>REF</sub>	0.75
HSTL, Class II, 1.5V	HSTL_II	25	0	V <sub>REF</sub>	0.75
HSTL, Class I, 1.8V	HSTL_I_18	50	0	V <sub>REF</sub>	0.9
HSTL, Class II, 1.8V	HSTL_II_18	25	0	V <sub>REF</sub>	0.9
HSUL (high-speed unterminated logic), Class I, 1.2V	HSUL_12	50	0	V <sub>REF</sub>	0.6
SSTL12, 1.2V	SSTL12	50	0	V <sub>REF</sub>	0.6
SSTL135/SSTL135_R, 1.35V	SSTL135, SSTL135_R	50	0	V <sub>REF</sub>	0.675
SSTL15/SSTL15_R, 1.5V	SSTL15, SSTL15_R	50	0	V <sub>REF</sub>	0.75
SSTL (stub series terminated logic), Class I and Class II, 1.8V	SSTL18_I, SSTL18_II	50	0	V <sub>REF</sub>	0.9
POD10, 1.0V	POD10	50	0	V <sub>REF</sub>	1.0
POD12, 1.2V	POD12	50	0	V <sub>REF</sub>	1.2
DIFF_HSTL, Class I, 1.2V	DIFF_HSTL_I_12	50	0	V <sub>REF</sub>	0.6
DIFF_HSTL, Class I and II, 1.5V	DIFF_HSTL_I, DIFF_HSTL_II	50	0	V <sub>REF</sub>	0.75
DIFF_HSTL, Class I and II, 1.8V	DIFF_HSTL_I_18, DIFF_HSTL_II_18	50	0	V <sub>REF</sub>	0.9
DIFF_HSUL_12, 1.2V	DIFF_HSUL_12	50	0	V <sub>REF</sub>	0.6
DIFF_SSTL12, 1.2V	DIFF_SSTL12	50	0	V <sub>REF</sub>	0.6
DIFF_SSTL135/DIFF_SSTL135_R, 1.35V	DIFF_SSTL135, DIFF_SSTL135_R	50	0	V <sub>REF</sub>	0.675
DIFF_SSTL15/DIFF_SSTL15_R, 1.5V	DIFF_SSTL15, DIFF_SSTL15_R	50	0	V <sub>REF</sub>	0.75
DIFF_SSTL18, Class I and II, 1.8V	DIFF_SSTL18_I, DIFF_SSTL18_II	50	0	V <sub>REF</sub>	0.9
DIFF_POD10, 1.0V	DIFF_POD10	50	0	V <sub>REF</sub>	1.0
DIFF_POD12, 1.2V	DIFF_POD12	50	0	V <sub>REF</sub>	1.2
LVDS (low-voltage differential signaling), 1.8V	LVDS	100	0	0 <sup>(2)</sup>	0
LVDS, 2.5V	LVDS_25	100	0	0 <sup>(2)</sup>	0
BLVDS (Bus LVDS), 2.5V	BLVDS_25	100	0	0 <sup>(2)</sup>	0
Mini LVDS, 2.5V	MINI_LVDS_25	100	0	0 <sup>(2)</sup>	0
PPDS_25	PPDS_25	100	0	0 <sup>(2)</sup>	0
RS DS_25	RS DS_25	100	0	0 <sup>(2)</sup>	0

Table 31: Output Delay Measurement Methodology (Cont'd)

Description	I/O Standard Attribute	R <sub>REF</sub> ( $\Omega$ )	C <sub>REF</sub> <sup>(1)</sup> (pF)	V <sub>MEAS</sub> (V)	V <sub>REF</sub> (V)
SUB_LVDS	SUB_LVDS	100	0	0 <sup>(2)</sup>	0
TMDS_33	TMDS_33	50	0	0 <sup>(2)</sup>	3.3

**Notes:**

- C<sub>REF</sub> is the capacitance of the probe, nominally 0 pF.
- The value given is the differential output voltage.

## Block RAM and FIFO Switching Characteristics

Table 32: Block RAM and FIFO Switching Characteristics

Symbol	Description	Speed Grades and V <sub>CCINT</sub> Operating Voltages				Units
		1.0V		0.95V		
		-3	-1H	-2	-1	
<b>Maximum Frequency</b>						
F <sub>MAX_WF_NC</sub>	Block RAM (WRITE_FIRST and NO_CHANGE modes)	660	585	585	525	MHz
F <sub>MAX_RF</sub>	Block RAM (READ_FIRST mode)	575	510	510	460	MHz
F <sub>MAX_FIFO</sub>	FIFO in all modes without ECC	660	585	585	525	MHz
F <sub>MAX_ECC</sub>	Block RAM and FIFO in ECC configuration without PIPELINE	530	450	450	390	MHz
	Block RAM and FIFO in ECC configuration with PIPELINE and Block RAM in WRITE_FIRST or NO_CHANGE mode	660	585	585	525	MHz
	Block RAM in ECC configuration in READ_FIRST mode with PIPELINE	575	510	510	460	MHz
F <sub>MAX_ADDREN_RDADDRCHANGE</sub>	Block RAM with address enable and read address change compare turned on	575	510	510	460	MHz
T <sub>PW_WF_NC</sub> <sup>(1)</sup>	Block RAM in WRITE_FIRST and NO_CHANGE modes and FIFO. Clock High/Low pulse width	758	855	855	952	ps, Min
T <sub>PW_RF</sub> <sup>(1)</sup>	Block RAM in READ_FIRST modes Clock High/Low pulse width	870	980	980	1087	ps, Min
<b>Block RAM and FIFO Clock-to-Out Delays</b>						
T <sub>RCKO_DO</sub>	Clock CLK to DOUT output (without output register)	1.13	1.44	1.44	1.64	ns, Max
T <sub>RCKO_DO_REG</sub>	Clock CLK to DOUT output (with output register)	0.37	0.44	0.44	0.49	ns, Max

**Notes:**

- The MMCM and PLL DUTY\_CYCLE attribute should be set to 50% to meet the pulse width requirements at the higher frequencies.

## Input/Output Delay Switching Characteristics

Table 33: Input/Output Delay Switching Characteristics

Symbol	Description	Speed Grades and V <sub>CCINT</sub> Operating Voltages				Units
		1.0V		0.95V		
		-3	-1H	-2	-1	
F <sub>REFCLK</sub>	Reference clock frequency for IDELAYCTRL (in component mode)	200 to 800				MHz
	Reference clock frequency when using BITSlice_CONTROL with REFCLK (in native mode (for RX_BITSlice only))	200 to 800				MHz
	Reference clock frequency for BITSlice_CONTROL with PLL_CLK (in native mode) <sup>(1)</sup>	200 to 2400	200 to 2400	200 to 2400	200 to 2133	MHz
T <sub>MINPER_CLK</sub>	Minimum period for IODELAY CLK	2.740	2.740	2.740	3.160	ns
T <sub>MINPER_RST</sub>	Minimum reset pulse width	52.00				ns
T <sub>IDELAY_RESOLUTION</sub> / T <sub>ODELAY_RESOLUTION</sub>	IDELAY/ODELAY chain resolution	2.5 to 15				ps

**Notes:**

1. PLL settings could restrict the minimum allowable data rate. For example, when using a PLL with CLKOUTPHY\_MODE = VCO\_HALF, the minimum frequency is PLL\_F<sub>VCOMIN</sub>/2.

## DSP48 Slice Switching Characteristics

Table 34: DSP48 Slice Switching Characteristics

Symbol	Description	Speed Grades and V <sub>CCINT</sub> Operating Voltages				Units
		1.0V		0.95V		
		-3	-1H	-2	-1	
<b>Maximum Frequency</b>						
F <sub>MAX</sub>	With all registers used	741	661	661	594	MHz
F <sub>MAX_PATDET</sub>	With pattern detector	687	581	581	512	MHz
F <sub>MAX_MULT_NOMREG</sub>	Two register multiply without MREG	462	429	429	361	MHz
F <sub>MAX_MULT_NOMREG_PATDET</sub>	Two register multiply without MREG with pattern detect	428	387	387	326	MHz
F <sub>MAX_PREADD_NOADREG</sub>	Without ADREG	468	429	429	358	MHz
F <sub>MAX_NOPIPELINEREG</sub>	Without pipeline registers (MREG, ADREG)	335	312	312	260	MHz
F <sub>MAX_NOPIPELINEREG_PATDET</sub>	Without pipeline registers (MREG, ADREG) with pattern detect	316	286	286	238	MHz

## Clock Buffers and Networks

Table 35: Clock Buffers Switching Characteristics

Symbol	Description	Speed Grades and V <sub>CCINT</sub> Operating Voltages				Units
		1.0V		0.95V		
		-3	-1H	-2	-1	
<b>Global Clock Switching Characteristics (Including BUFGCTRL)</b>						
F <sub>MAX</sub>	Maximum frequency of a global clock tree (BUFG)	850	725	725	630	MHz
<b>Global Clock Buffer with Input Divide Capability (BUFGCE_DIV)</b>						
F <sub>MAX</sub>	Maximum frequency of a global clock buffer with input divide capability (BUFGCE_DIV)	850	725	725	630	MHz
<b>Global Clock Buffer with Clock Enable (BUFGCE)</b>						
F <sub>MAX</sub>	Maximum frequency of a global clock buffer with clock enable (BUFGCE)	850	725	725	630	MHz
<b>Leaf Clock Buffer with Clock Enable (BUFCE_LEAF)</b>						
F <sub>MAX</sub>	Maximum frequency of a leaf clock buffer with clock enable (BUFCE_LEAF)	850	725	725	630	MHz
<b>GTH/GTY Clock Buffer with Clock Enable and Clock Input Divide Capability (BUFG_GT)</b>						
F <sub>MAX</sub>	Maximum frequency of a serial transceiver clock buffer with clock enable and clock input divide capability	512	512	512	512	MHz

## MMCM Switching Characteristics

Table 36: MMCM Specification

Symbol	Description	Speed Grades and V <sub>CCINT</sub> Operating Voltages				Units
		1.0V		0.95V		
		-3	-1H	-2	-1	
MMCM_F <sub>INMAX</sub>	Maximum input clock frequency	1066	933	933	800	MHz
MMCM_F <sub>INMIN</sub>	Minimum input clock frequency	10	10	10	10	MHz
MMCM_F <sub>INJITTER</sub>	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
MMCM_F <sub>INDUTY</sub>	Input duty cycle range: 10–49 MHz	25–75				%
	Input duty cycle range: 50–199 MHz	30–70				%
	Input duty cycle range: 200–399 MHz	35–65				%
	Input duty cycle range: 400–499 MHz	40–60				%
	Input duty cycle range: >500 MHz	45–55				%
MMCM_F <sub>MIN_PSCLK</sub>	Minimum dynamic phase shift clock frequency	0.01	0.01	0.01	0.01	MHz
MMCM_F <sub>MAX_PSCLK</sub>	Maximum dynamic phase shift clock frequency	550	500	500	450	MHz
MMCM_F <sub>VCOMIN</sub>	Minimum MMCM VCO frequency	600	600	600	600	MHz
MMCM_F <sub>VCOMAX</sub>	Maximum MMCM VCO frequency	1600	1440	1440	1200	MHz
MMCM_F <sub>BANDWIDTH</sub>	Low MMCM bandwidth at typical <sup>(1)</sup>	1.00	1.00	1.00	1.00	MHz
	High MMCM bandwidth at typical <sup>(1)</sup>	4.00	4.00	4.00	4.00	MHz
MMCM_T <sub>STATPHAOFFSET</sub>	Static phase offset of the MMCM outputs <sup>(2)</sup>	0.12	0.12	0.12	0.12	ns
MMCM_T <sub>OUTJITTER</sub>	MMCM output jitter	Note 3				
MMCM_T <sub>OUTDUTY</sub>	MMCM output clock duty cycle precision <sup>(4)</sup>	0.165	0.20	0.20	0.20	ns
MMCM_T <sub>LOCKMAX</sub>	MMCM maximum lock time for MMCM_F <sub>PFDMIN</sub> frequencies above 20 MHz	100	100	100	100	μs
	MMCM maximum lock time for MMCM_F <sub>PFDMIN</sub> frequencies from 10 MHz to 20 MHz	200	200	200	200	μs
MMCM_F <sub>OUTMAX</sub>	MMCM maximum output frequency	850	725	725	630	MHz
MMCM_F <sub>OUTMIN</sub>	MMCM minimum output frequency <sup>(4)(5)</sup>	4.69	4.69	4.69	4.69	MHz
MMCM_T <sub>EXTFDVAR</sub>	External clock feedback variation	< 20% of clock input period or 1 ns Max				
MMCM_RST <sub>MINPULSE</sub>	Minimum reset pulse width	5.00	5.00	5.00	5.00	ns
MMCM_F <sub>PFDMAX</sub>	Maximum frequency at the phase frequency detector	550	500	500	450	MHz
MMCM_F <sub>PFDMIN</sub>	Minimum frequency at the phase frequency detector	10	10	10	10	MHz
MMCM_T <sub>FBDELAY</sub>	Maximum delay in the feedback path	5 ns Max or one clock cycle				
MMCM_F <sub>DRPCLK_MAX</sub>	Maximum DRP clock frequency	200	200	200	200	MHz

### Notes:

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as  $F_{VCO}/128$  assuming output duty cycle is 50%.

## PLL Switching Characteristics

 Table 37: PLL Specification<sup>(1)</sup>

Symbol	Description	Speed Grades and V <sub>CCINT</sub> Operating Voltages				Units
		1.0V		0.95V		
		-3	-1H	-2	-1	
PLL_F <sub>INMAX</sub>	Maximum input clock frequency	1066	933	933	800	MHz
PLL_F <sub>INMIN</sub>	Minimum input clock frequency	70	70	70	70	MHz
PLL_F <sub>INJITTER</sub>	Maximum input clock period jitter	< 20% of clock input period or 1 ns Max				
PLL_F <sub>INDUTY</sub>	Input duty cycle range: 70–399 MHz	35–65				%
	Input duty cycle range: 400–499 MHz	40–60				%
	Input duty cycle range: >500 MHz	45–55				%
PLL_F <sub>VCOMIN</sub>	Minimum PLL VCO frequency	600	600	600	600	MHz
PLL_F <sub>VCOMAX</sub>	Maximum PLL VCO frequency	1335	1335	1335	1200	MHz
PLL_T <sub>STATPHAOFFSET</sub>	Static phase offset of the PLL outputs <sup>(2)</sup>	0.12	0.12	0.12	0.12	ns
PLL_T <sub>OUTJITTER</sub>	PLL output jitter	Note 3				
PLL_T <sub>OUTDUTY</sub>	PLL CLKOUT0/CLKOUT0B/CLKOUT1/CLKOUT1B duty-cycle precision <sup>(4)</sup>	0.165	0.20	0.20	0.20	ns
PLL_T <sub>LOCKMAX</sub>	PLL maximum lock time	100				µs
PLL_F <sub>OUTMAX</sub>	PLL maximum output frequency at CLKOUT0/CLKOUT0B/CLKOUT1/CLKOUT1B	850	725	725	630	MHz
	PLL maximum output frequency at CLKOUTPHY	2670	2670	2670	2400	MHz
PLL_F <sub>OUTMIN</sub>	PLL minimum output frequency at CLKOUT0/CLKOUT0B/CLKOUT1/CLKOUT1B <sup>(5)</sup>	4.69	4.69	4.69	4.69	MHz
	PLL minimum output frequency at CLKOUTPHY	2 x VCO mode: 1200 1 x VCO mode: 600 0.5 x VCO mode: 300				MHz
PLL_RST <sub>MINPULSE</sub>	Minimum reset pulse width	5.00	5.00	5.00	5.00	ns
PLL_F <sub>PFDMAX</sub>	Maximum frequency at the phase frequency detector	667.5	667.5	667.5	600	MHz
PLL_F <sub>PFDMIN</sub>	Minimum frequency at the phase frequency detector	70	70	70	70	MHz
PLL_F <sub>BANDWIDTH</sub>	PLL bandwidth at typical	15	15	15	15	MHz
PLL_F <sub>DRPCLK_MAX</sub>	Maximum DRP clock frequency	200	200	200	200	MHz

### Notes:

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the loop filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard.
4. Includes global clock buffer.
5. Calculated as  $F_{VCO}/128$  assuming output duty cycle is 50%.

## Device Pin-to-Pin Output Parameter Guidelines

The pin-to-pin numbers in [Table 38](#) through [Table 41](#) are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

**Table 38: Global Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)**

Symbol	Description	Device	Speed Grades and V <sub>CCINT</sub> Operating Voltages				Units
			1.0V		0.95V		
			-3	-1H	-2	-1	
<b>SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, without MMCM/PLL.</b>							
T <sub>ICKOF</sub>	Global clock input and output flip-flop without MMCM/PLL (near clock region)	XCVU065	5.04	5.82	5.82	6.83	ns
		XCVU080	5.27	6.09	6.09	7.13	ns
		XCVU095	5.27	6.09	6.09	7.13	ns
		XCVU125	5.04	5.82	5.82	6.86	ns
		XCVU160	5.04	5.82	5.82	6.86	ns
		XCVU190	5.04	5.82	5.82	6.86	ns
		XCVU440	6.14	N/A	7.11	8.38	ns

**Notes:**

- This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.

**Table 39: Global Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)**

Symbol	Description	Device	Speed Grades and V <sub>CCINT</sub> Operating Voltages				Units
			1.0V		0.95V		
			-3	-1H	-2	-1	
<b>SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, without MMCM/PLL.</b>							
T <sub>ICKOF_FAR</sub>	Global clock input and output flip-flop without MMCM/PLL (far clock region)	XCVU065	5.48	6.35	6.35	7.44	ns
		XCVU080	5.77	6.67	6.67	7.69	ns
		XCVU095	5.77	6.67	6.67	7.69	ns
		XCVU125	5.48	6.35	6.35	7.51	ns
		XCVU160	5.48	6.35	6.35	7.51	ns
		XCVU190	5.48	6.35	6.35	7.51	ns
		XCVU440	6.48	N/A	7.49	8.85	ns

**Notes:**

- This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.

**Table 40: Global Clock Input to Output Delay With MMCM**

Symbol	Description	Device	Speed Grades and V <sub>CCINT</sub> Operating Voltages				Units
			1.0V		0.95V		
			-3	-1H	-2	-1	
<b>SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with MMCM.</b>							
T <sub>ICKOFMMCMCC</sub>	Global clock input and output flip-flop <i>with</i> MMCM	XCVU065	1.36	1.61	1.61	1.93	ns
		XCVU080	1.36	1.59	1.59	1.85	ns
		XCVU095	1.36	1.59	1.59	1.85	ns
		XCVU125	1.36	1.61	1.61	1.94	ns
		XCVU160	1.36	1.61	1.61	1.94	ns
		XCVU190	1.36	1.61	1.61	1.94	ns
		XCVU440	1.37	N/A	1.62	1.88	ns

**Notes:**

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.
2. MMCM output jitter is already included in the timing calculation.

**Table 41: Global Clock Input to Output Delay With PLL**

Symbol	Description	Device	Speed Grades and V <sub>CCINT</sub> Operating Voltages				Units
			1.0V		0.95V		
			-3	-1H	-2	-1	
<b>SSTL15 Global Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with PLL.</b>							
T <sub>ICKOF_PLL_CC</sub>	Global clock input and output flip-flop <i>with</i> PLL	XCVU065	4.70	5.38	5.38	6.23	ns
		XCVU080	4.99	5.70	5.70	6.49	ns
		XCVU095	4.99	5.70	5.70	6.49	ns
		XCVU125	4.70	5.38	5.38	6.31	ns
		XCVU160	4.70	5.38	5.38	6.31	ns
		XCVU190	4.70	5.38	5.38	6.31	ns
		XCVU440	5.70	N/A	6.53	7.65	ns

**Notes:**

1. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.
2. PLL output jitter is already included in the timing calculation.

**Table 42: Source Synchronous Output Characteristics (Component Mode)**

Symbol	Description	Speed Grade and V <sub>CCINT</sub> Operating Voltages				Units
		1.0V		0.95V		
		-3	-1H	-2	-1	
T <sub>OUTPUT_LOGIC_DELAY_VARIATION</sub>	Delay mismatch across a transmit bus when using component mode output logic (ODDRE1, OSERDESE3) within a bank	100				ps

## Device Pin-to-Pin Input Parameter Guidelines

The pin-to-pin numbers in [Table 43](#) and [Table 44](#) are based on the clock root placement in the center of the device. The actual pin-to-pin values will vary if the root placement selected is different. Consult the Vivado Design Suite timing report for the actual pin-to-pin values.

Table 43: Global Clock Input Setup and Hold With MMCM

Symbol	Description	Device	Speed Grades and V <sub>CCINT</sub> Operating Voltages				Units	
			1.0V		0.95V			
			-3	-1H	-2	-1		
<b>Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard. <sup>(1)(2)(3)</sup></b>								
T <sub>PSMMCMCC_VU065</sub>	Global clock input and input flip-flop (or latch) with MMCM	Setup	XCVU065	2.36	2.48	2.38	2.67	ns
T <sub>PHMMCMCC_VU065</sub>		Hold	XCVU065	-0.25	-0.25	-0.25	-0.25	ns
T <sub>PSMMCMCC_VU080</sub>		Setup	XCVU080	2.22	2.45	2.25	2.55	ns
T <sub>PHMMCMCC_VU080</sub>		Hold	XCVU080	-0.47	-0.47	-0.47	-0.47	ns
T <sub>PSMMCMCC_VU095</sub>		Setup	XCVU095	2.22	2.45	2.25	2.55	ns
T <sub>PHMMCMCC_VU095</sub>		Hold	XCVU095	-0.47	-0.47	-0.47	-0.47	ns
T <sub>PSMMCMCC_VU125</sub>		Setup	XCVU125	2.21	2.48	2.23	2.66	ns
T <sub>PHMMCMCC_VU125</sub>		Hold	XCVU125	-0.13	-0.13	-0.13	-0.13	ns
T <sub>PSMMCMCC_VU160</sub>		Setup	XCVU160	2.21	2.48	2.23	2.66	ns
T <sub>PHMMCMCC_VU160</sub>		Hold	XCVU160	-0.12	-0.12	-0.12	-0.12	ns
T <sub>PSMMCMCC_VU190</sub>		Setup	XCVU190	2.21	2.48	2.23	2.66	ns
T <sub>PHMMCMCC_VU190</sub>		Hold	XCVU190	-0.13	-0.13	-0.13	-0.13	ns
T <sub>PSMMCMCC_VU440</sub>		Setup	XCVU440	2.31	N/A	2.32	2.86	ns
T <sub>PHMMCMCC_VU440</sub>		Hold	XCVU440	-0.07	N/A	-0.07	-0.07	ns

### Notes:

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 44: Global Clock Input Setup and Hold With PLL

Symbol	Description	Device	Speed Grades and V <sub>CCINT</sub> Operating Voltages				Units	
			1.0V		0.95V			
			-3	-1H	-2	-1		
<b>Input Setup and Hold Time Relative to Global Clock Input Signal using SSTL15 Standard. (1)(2)(3)</b>								
T <sub>PSPLLCC_VU065</sub>	Global clock input and input flip-flop (or latch) with PLL	Setup	XCVU065	-0.70	-0.70	-0.70	-0.70	ns
T <sub>PHPLLCC_VU065</sub>		Hold	XCVU065	2.03	2.27	2.27	2.63	ns
T <sub>PSPLLCC_VU080</sub>		Setup	XCVU080	-0.94	-0.94	-0.94	-0.94	ns
T <sub>PHPLLCC_VU080</sub>		Hold	XCVU080	2.14	2.36	2.36	2.71	ns
T <sub>PSPLLCC_VU095</sub>		Setup	XCVU095	-0.94	-0.94	-0.94	-0.94	ns
T <sub>PHPLLCC_VU095</sub>		Hold	XCVU095	2.14	2.36	2.36	2.71	ns
T <sub>PSPLLCC_VU125</sub>		Setup	XCVU125	-0.67	-0.67	-0.67	-0.67	ns
T <sub>PHPLLCC_VU125</sub>		Hold	XCVU125	2.03	2.27	2.27	2.64	ns
T <sub>PSPLLCC_VU160</sub>		Setup	XCVU160	-0.67	-0.67	-0.67	-0.67	ns
T <sub>PHPLLCC_VU160</sub>		Hold	XCVU160	2.03	2.27	2.27	2.64	ns
T <sub>PSPLLCC_VU190</sub>		Setup	XCVU190	-0.67	-0.67	-0.67	-0.67	ns
T <sub>PHPLLCC_VU190</sub>		Hold	XCVU190	2.03	2.27	2.27	2.64	ns
T <sub>PSPLLCC_VU440</sub>		Setup	XCVU440	-1.16	N/A	-1.16	-1.16	ns
T <sub>PHPLLCC_VU440</sub>		Hold	XCVU440	3.03	N/A	3.44	3.99	ns

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, slowest temperature, and slowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, fastest temperature, and fastest voltage.
2. This table lists representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible I/O and CLB flip-flops are clocked by the global clock net in a single SLR.
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

Table 45: Sampling Window

Symbol	Description	Speed Grades and V <sub>CCINT</sub> Operating Voltages				Units
		1.0V		0.95V		
		-3	-1H	-2	-1	
T <sub>SAMP_BUF<sup>(1)</sup></sub>	Total sampling error of the Virtex UltraScale FPGAs DDR input registers, measured across voltage, temperature, and process	510	610	610	610	ps
T <sub>SAMP_NATIVE_DPA</sub>	Receive sampling error for RX_BITSLICE when using dynamic phase alignment	100	100	100	125	ps
T <sub>SAMP_NATIVE_BISC</sub>	Receive sampling error for RX_BITSLICE when using built-in self-calibration (BISC)	60	60	60	85	ps

**Notes:**

1. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include: CLK0 MMCM jitter, MMCM accuracy (phase offset), and MMCM phase shift resolution. These measurements do not include package or clock tree skew. For detailed component mode sampling window calculations using the parameters in this table, see the Designing Using SelectIO Interface Component Primitives (XAPP1324) application note.

**Table 46: Input Logic Characteristics for Dynamic Phase Aligned Applications (Component Mode)**

Symbol	Description	Speed Grade and V <sub>CCINT</sub> Operating Voltages				Units
		1.0V		0.95V		
		-3	-1H	-2	-1	
T <sub>INPUT_LOGIC_UNCERTAINTY</sub>	Accounts for the setup/hold and any pattern dependent jitter for the input logic (input register, IDDRE1, or ISERDESE3)	40				ps
T <sub>CAL_ERROR</sub>	Calibration error associated with quantization effects based on the IDELAY resolution. Calibration must be performed for each input pin to ensure optimal performance	24				ps

## Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for clock transmitter and receiver data-valid windows.

*Table 47: Package Skew*

Symbol	Description	Device	Package	Value	Units
PKGSKEW	Package skew	XCVU065	FFVC1517	193	ps
		XCVU080	FFVC1517	181	ps
			FFVD1517	113	ps
			FFVB1760	128	ps
			FFVA2104	201	ps
			FFVB2104	191	ps
		XCVU095	FFVC1517	181	ps
			FFVD1517	113	ps
			FFVB1760	128	ps
			FFVA2104	201	ps
			FFVB2104	191	ps
			FFVC2104	245	ps
		XCVU125	FLVD1517	130	ps
			FLVB1760	168	ps
			FLVA2104	173	ps
			FLVB2104	194	ps
			FLVC2104	242	ps
		XCVU160	FLGB2104	226	ps
			FLGC2104	268	ps
		XCVU190	FLGB2104	226	ps
			FLGC2104	268	ps
			FLGA2577	161	ps
		XCVU440	FLGB2377	291	ps
			FLGA2892	310	ps

**Notes:**

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

# GTH Transceiver Specifications

## GTH Transceiver DC Input and Output Levels

Table 48 summarizes the DC specifications of the GTH transceivers in Virtex UltraScale FPGAs. Consult the *UltraScale Architecture GTH Transceiver User Guide (UG576)* for further details.

Table 48: GTH Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
D <sub>VPPIN</sub>	Differential peak-to-peak input voltage (external AC coupled)	> 10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V <sub>IN</sub>	Single-ended input voltage. Voltage measured at the pin referenced to GND	DC coupled V <sub>MGTAVTT</sub> = 1.2V	–400	–	V <sub>MGTAVTT</sub>	mV
V <sub>CMIN</sub>	Common mode input voltage	DC coupled V <sub>MGTAVTT</sub> = 1.2V	–	2/3 V <sub>MGTAVTT</sub>	–	mV
D <sub>VPPOUT</sub>	Differential peak-to-peak output voltage <sup>(1)</sup>	Transmitter output swing is set to 1100	800	–	–	mV
V <sub>CMOUTDC</sub>	Common mode output voltage: DC coupled (equation based)	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V <sub>RX_TERM</sub> <sup>(2)</sup>	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX\_TERM}}{2}\right)$			mV
V <sub>CMOUTAC</sub>	Common mode output voltage: AC coupled (equation based)		$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R <sub>IN</sub>	Differential input resistance		–	100	–	Ω
R <sub>OUT</sub>	Differential output resistance		–	100	–	Ω
T <sub>OSKEW</sub>	Transmitter output pair (TXP and TXN) intra-pair skew (All packages)		–	–	5	ps
C <sub>EXT</sub>	Recommended external AC coupling capacitor <sup>(3)</sup>		–	100	–	nF

### Notes:

- The output swing and pre-emphasis levels are programmable using the attributes discussed in the *UltraScale Architecture GTH Transceiver User Guide (UG576)*, and can result in values lower than reported in this table.
- V<sub>RX\_TERM</sub> is the remote RX termination voltage.
- Other values can be used as appropriate to conform to specific protocols and standards.

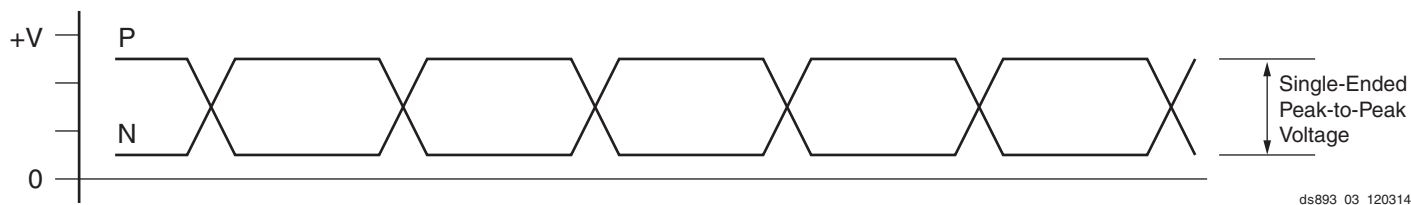


Figure 3: Single-Ended Peak-to-Peak Voltage

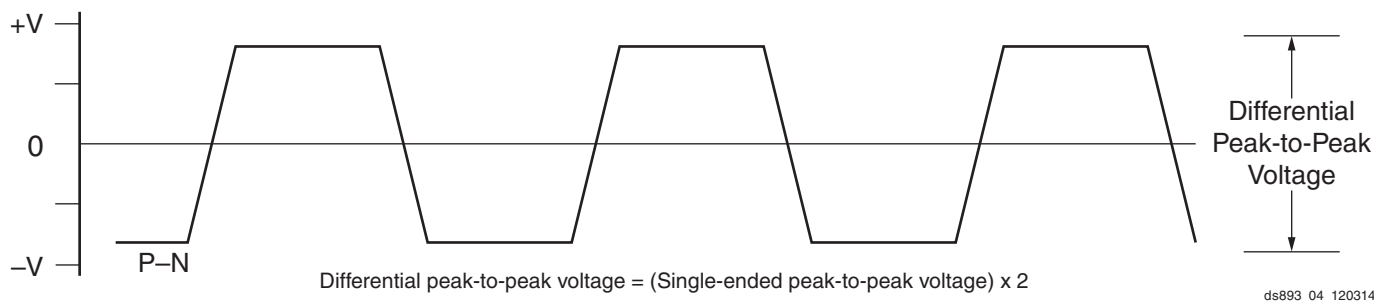


Figure 4: Differential Peak-to-Peak Voltage

Table 49 summarizes the DC specifications of the clock input of the GTH transceivers in Virtex UltraScale FPGAs. Consult the *UltraScale Architecture GTH Transceiver User Guide* (UG576) for further details.

Table 49: GTH Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V <sub>IDIFF</sub>	Differential peak-to-peak input voltage	250	–	2000	mV
R <sub>IN</sub>	Differential input resistance	–	100	–	Ω
C <sub>EXT</sub>	Required external AC coupling capacitor	–	10	–	nF

Table 50: GTH Transceiver Clock Output Level Specification

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>OL</sub>	Output Low voltage for P and N	R <sub>T</sub> = 100Ω across P and N signals	–	400	–	mV
V <sub>OH</sub>	Output High voltage for P and N	R <sub>T</sub> = 100Ω across P and N signals	–	760	–	mV
V <sub>DDOUT</sub>	Differential output voltage: (P–N), P = High (N–P), N = High	R <sub>T</sub> = 100Ω across P and N signals	–	±360	–	mV
V <sub>CMOUT</sub>	Common mode voltage	R <sub>T</sub> = 100Ω across P and N signals	–	580	–	mV

## GTH Transceiver Switching Characteristics

Consult the *UltraScale Architecture GTH Transceiver User Guide* ([UG576](#)) for further information.

Table 51: GTH Transceiver Performance

Symbol	Description	Output Divider	Speed Grades and V <sub>CCINT</sub> Operating Voltages								Units
			1.0V				0.95V				
			-3		-1H		-2		-1		
F <sub>GTHMAX</sub>	GTH maximum line rate		16.375		16.375		16.375		12.5		Gb/s
F <sub>GTHMIN</sub>	GTH minimum line rate		0.5		0.5		0.5		0.5		Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
F <sub>GTHCRANGE</sub>	CPLL line rate range <sup>(1)</sup>	1	4.0	12.5	4.0	12.5	4.0	12.5	4.0	8.5	Gb/s
		2	2.0	6.25	2.0	6.25	2.0	6.25	2.0	4.25	Gb/s
		4	1.0	3.125	1.0	3.125	1.0	3.125	1.0	2.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.5625	0.5	1.0625	Gb/s
		16	N/A								Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
F <sub>GTHQRANGE1</sub>	QPLL0 line rate range <sup>(2)</sup>	1	9.8	16.375	9.8	16.375	9.8	16.375	9.8	12.5	Gb/s
		2	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	Gb/s
		4	2.45	4.0938	2.45	4.0938	2.45	4.0938	2.45	4.0938	Gb/s
		8	1.225	2.0469	1.225	2.0469	1.225	2.0469	1.225	2.0469	Gb/s
		16	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	0.6125	1.0234	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
F <sub>GTHQRANGE2</sub>	QPLL1 line rate range <sup>(3)</sup>	1	8.0	13.0	8.0	13.0	8.0	13.0	8.0	12.5	Gb/s
		2	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
F <sub>CPLLRANGE</sub>	CPLL frequency range		2.0	6.25	2.0	6.25	2.0	6.25	2.0	4.25	GHz
F <sub>QPLLORANGE</sub>	QPLL0 frequency range		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
F <sub>QPLL1RANGE</sub>	QPLL1 frequency range		8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	GHz

### Notes:

1. The values listed are the rounded results of the calculated equation  $(2 \times \text{CPLL\_Frequency}) / \text{Output\_Divider}$ .
2. The values listed are the rounded results of the calculated equation  $(\text{QPLL0\_Frequency}) / \text{Output\_Divider}$ .
3. The values listed are the rounded results of the calculated equation  $(\text{QPLL1\_Frequency}) / \text{Output\_Divider}$ .

Table 52: GTH Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	All Devices	Units
F <sub>GTHDRPCLK</sub>	GTHDRPCLK maximum frequency	250	MHz

Table 53: GTH Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	Min	Typ	Max	Units
$F_{GCLK}$	Reference clock frequency range		60	–	820	MHz
$T_{RCLK}$	Reference clock rise time	20% – 80%	–	200	–	ps
$T_{FCLK}$	Reference clock fall time	80% – 20%	–	200	–	ps
$T_{DCREF}$	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

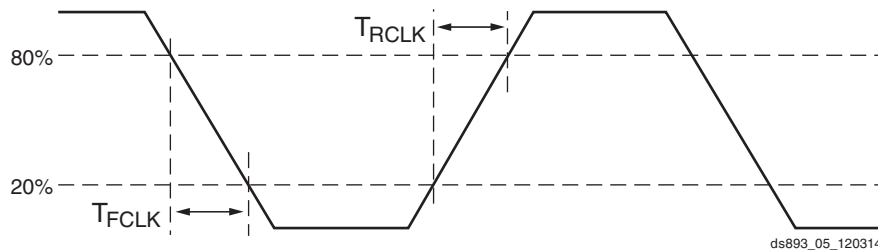


Figure 5: Reference Clock Timing Parameters

Table 54: GTH Transceiver Reference Clock Selection Phase Noise Mask

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
$QPLL_{REFCLKMASK}^{(1)(2)}$	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz	10 kHz	–	–	–105	dBc/Hz
		100 kHz	–	–	–124	
		1 MHz	–	–	–130	
$CPLL_{REFCLKMASK}^{(1)(2)}$	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz	10 kHz	–	–	–105	dBc/Hz
		100 kHz	–	–	–124	
		1 MHz	–	–	–130	
		50 MHz	–	–	–140	

Notes:

- For reference clock frequencies other than 312.5 MHz, adjust the phase-noise mask values by  $20 \times \log(N/312.5)$  where N is the new reference clock frequency in MHz.
- This reference clock phase-noise mask is superseded by any reference clock phase-noise mask that is specified in a supported protocol, e.g., PCIe.

Table 55: GTH Transceiver PLL/Lock Time Adaptation

Symbol	Description	Conditions	Min	Typ	Max	Units
$T_{LOCK}$	Initial PLL lock.		–	–	1	ms
$T_{DLOCK}$	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE)	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input	–	50,000	$37 \times 10^6$	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled		–	50,000	$2.3 \times 10^6$	UI

**Table 56: GTH Transceiver User Clock Switching Characteristics<sup>(1)</sup>**

Symbol	Description	Data Width Conditions (Bit)		Speed Grades and V <sub>CCINT</sub> Operating Voltages				Units
				1.0V		0.95V		
		Internal Logic	Interconnect Logic	-3	-1H	-2	-1	
F <sub>TXOUTPMA</sub>	TXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	511.719	390.625	MHz
F <sub>RXOUTPMA</sub>	RXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	511.719	390.625	MHz
F <sub>TXOUTPROGDIV</sub>	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	511.719	MHz
F <sub>RXOUTPROGDIV</sub>	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	511.719	MHz
F <sub>TXIN</sub>	TXUSRCLK maximum frequency	16	16, 32	511.719	511.719	511.719	390.625	MHz
		32	32, 64	511.719	511.719	511.719	390.625	MHz
		20	20, 40	409.375	409.375	409.375	312.500	MHz
		40	40, 80	409.375	409.375	409.375	312.500	MHz
F <sub>RXIN</sub>	RXUSRCLK maximum frequency	16	16, 32	511.719	511.719	511.719	390.625	MHz
		32	32, 64	511.719	511.719	511.719	390.625	MHz
		20	20, 40	409.375	409.375	409.375	312.500	MHz
		40	40, 80	409.375	409.375	409.375	312.500	MHz
F <sub>TXIN2</sub>	TXUSRCLK2 maximum frequency	16	16	511.719	511.719	511.719	390.625	MHz
		16, 32	32	511.719	511.719	511.719	390.625	MHz
		32	64	255.860	255.860	255.860	195.313	MHz
		20	20	409.375	409.375	409.375	312.500	MHz
		20, 40	40	409.375	409.375	409.375	312.500	MHz
		40	80	204.688	204.688	204.688	156.250	MHz
F <sub>RXIN2</sub>	RXUSRCLK2 maximum frequency	16	16	511.719	511.719	511.719	390.625	MHz
		16, 32	32	511.719	511.719	511.719	390.625	MHz
		32	64	255.860	255.860	255.860	195.313	MHz
		20	20	409.375	409.375	409.375	312.500	MHz
		20, 40	40	409.375	409.375	409.375	312.500	MHz
		40	80	204.688	204.688	204.688	156.250	MHz

**Notes:**

1. Clocking must be implemented as described in *UltraScale Architecture GTH Transceiver User Guide (UG576)*.

**Table 57: GTH Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F <sub>GTHTX</sub>	Serial data rate range		0.500	–	F <sub>GTHMAX</sub>	Gb/s
T <sub>RTX</sub>	TX rise time	20%–80%	–	21	–	ps
T <sub>FTX</sub>	TX fall time	80%–20%	–	21	–	ps
T <sub>LLSKEW</sub>	TX lane-to-lane skew <sup>(1)</sup>		–	–	500	ps
V <sub>TXOOBVDPP</sub>	Electrical idle amplitude		–	–	15	mV
T <sub>TXOOBTRANSITION</sub>	Electrical idle transition time		–	–	140	ns
T <sub>J16.3_QPLL</sub>	Total jitter <sup>(2)(4)</sup>	16.3 Gb/s	–	–	0.28	UI
D <sub>J16.3_QPLL</sub>	Deterministic jitter <sup>(2)(4)</sup>		–	–	0.17	UI
T <sub>J15_QPLL</sub>	Total jitter <sup>(2)(4)</sup>	15.0 Gb/s	–	–	0.28	UI
D <sub>J15_QPLL</sub>	Deterministic jitter <sup>(2)(4)</sup>		–	–	0.17	UI
T <sub>J14.1_QPLL</sub>	Total jitter <sup>(2)(4)</sup>	14.1 Gb/s	–	–	0.28	UI
D <sub>J14.1_QPLL</sub>	Deterministic jitter <sup>(2)(4)</sup>		–	–	0.17	UI
T <sub>J14.025_QPLL</sub>	Total jitter <sup>(2)(4)</sup>	14.025 Gb/s	–	–	0.28	UI
D <sub>J14.025_QPLL</sub>	Deterministic jitter <sup>(2)(4)</sup>		–	–	0.17	UI
T <sub>J13.1_QPLL</sub>	Total jitter <sup>(2)(4)</sup>	13.1 Gb/s	–	–	0.28	UI
D <sub>J13.1_QPLL</sub>	Deterministic jitter <sup>(2)(4)</sup>		–	–	0.17	UI
T <sub>J12.5_QPLL</sub>	Total jitter <sup>(2)(4)</sup>	12.5 Gb/s	–	–	0.28	UI
D <sub>J12.5_QPLL</sub>	Deterministic jitter <sup>(2)(4)</sup>		–	–	0.17	UI
T <sub>J12.5_CPLL</sub>	Total jitter <sup>(3)(4)</sup>	12.5 Gb/s	–	–	0.33	UI
D <sub>J12.5_CPLL</sub>	Deterministic jitter <sup>(3)(4)</sup>		–	–	0.17	UI
T <sub>J11.3_QPLL</sub>	Total jitter <sup>(2)(4)</sup>	11.3 Gb/s	–	–	0.28	UI
D <sub>J11.3_QPLL</sub>	Deterministic jitter <sup>(2)(4)</sup>		–	–	0.17	UI
T <sub>J10.3_QPLL</sub>	Total jitter <sup>(2)(4)</sup>	10.3 Gb/s	–	–	0.28	UI
D <sub>J10.3_QPLL</sub>	Deterministic jitter <sup>(2)(4)</sup>		–	–	0.17	UI
T <sub>J10.3_CPLL</sub>	Total jitter <sup>(3)(4)</sup>	10.3 Gb/s	–	–	0.33	UI
D <sub>J10.3_CPLL</sub>	Deterministic jitter <sup>(3)(4)</sup>		–	–	0.17	UI
T <sub>J9.8_QPLL</sub>	Total jitter <sup>(2)(4)</sup>	9.8 Gb/s	–	–	0.28	UI
D <sub>J9.8_QPLL</sub>	Deterministic jitter <sup>(2)(4)</sup>		–	–	0.17	UI
T <sub>J9.8_CPLL</sub>	Total jitter <sup>(3)(4)</sup>	9.8 Gb/s	–	–	0.33	UI
D <sub>J9.8_CPLL</sub>	Deterministic jitter <sup>(3)(4)</sup>		–	–	0.17	UI
T <sub>J8.0_CPLL</sub>	Total jitter <sup>(3)(4)</sup>	8.0 Gb/s	–	–	0.32	UI
D <sub>J8.0_CPLL</sub>	Deterministic jitter <sup>(3)(4)</sup>		–	–	0.17	UI
T <sub>J6.6_CPLL</sub>	Total jitter <sup>(3)(4)</sup>	6.6 Gb/s	–	–	0.30	UI
D <sub>J6.6_CPLL</sub>	Deterministic jitter <sup>(3)(4)</sup>		–	–	0.15	UI
T <sub>J5.0</sub>	Total jitter <sup>(3)(4)</sup>	5.0 Gb/s	–	–	0.30	UI
D <sub>J5.0</sub>	Deterministic jitter <sup>(3)(4)</sup>		–	–	0.15	UI
T <sub>J4.25</sub>	Total jitter <sup>(3)(4)</sup>	4.25 Gb/s	–	–	0.30	UI
D <sub>J4.25</sub>	Deterministic jitter <sup>(3)(4)</sup>		–	–	0.15	UI
T <sub>J4.0L</sub>	Total jitter <sup>(3)(4)</sup>	4.0 Gb/s <sup>(5)</sup>	–	–	0.32	UI
D <sub>J4.0L</sub>	Deterministic jitter <sup>(3)(4)</sup>		–	–	0.16	UI

**Table 57: GTH Transceiver Transmitter Switching Characteristics (Cont'd)**

Symbol	Description	Condition	Min	Typ	Max	Units
T <sub>J3.2</sub>	Total jitter <sup>(3)(4)</sup>	3.2 Gb/s <sup>(6)</sup>	–	–	0.20	UI
D <sub>J3.2</sub>	Deterministic jitter <sup>(3)(4)</sup>		–	–	0.10	UI
T <sub>J2.5</sub>	Total jitter <sup>(3)(4)</sup>	2.5 Gb/s <sup>(7)</sup>	–	–	0.20	UI
D <sub>J2.5</sub>	Deterministic jitter <sup>(3)(4)</sup>		–	–	0.10	UI
T <sub>J1.25</sub>	Total jitter <sup>(3)(4)</sup>	1.25 Gb/s <sup>(8)</sup>	–	–	0.15	UI
D <sub>J1.25</sub>	Deterministic jitter <sup>(3)(4)</sup>		–	–	0.06	UI
T <sub>J500</sub>	Total jitter <sup>(3)(4)</sup>	500 Mb/s <sup>(9)</sup>	–	–	0.10	UI
D <sub>J500</sub>	Deterministic jitter <sup>(3)(4)</sup>		–	–	0.03	UI

**Notes:**

- Using same REFCLK input with TX phase alignment enabled for up to four fully populated GTH Quads at maximum line rate.
- Using QPLL\_FBDIV = 40, 40-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL\_FBDIV = 2, 40-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 10<sup>-12</sup>.
- CPLL frequency at 2.0 GHz and TXOUT\_DIV = 1.
- CPLL frequency at 3.2 GHz and TXOUT\_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT\_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT\_DIV = 4.
- CPLL frequency at 2.0 GHz and TXOUT\_DIV = 4.

**Table 58: GTH Transceiver Receiver Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F <sub>GTHRX</sub>	Serial data rate		0.500	–	F <sub>GTHMAX</sub>	Gb/s
T <sub>RXELECIDLE</sub>	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
R <sub>XOOBVDPP</sub>	OOB detect threshold peak-to-peak		60	–	150	mV
R <sub>XSST</sub>	Receiver spread-spectrum tracking <sup>(1)</sup>	Modulated at 33 kHz	–5000	–	0	ppm
R <sub>XRL</sub>	Run length (CID)		–	–	256	UI
R <sub>XPPMTOL</sub>	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
<b>SJ Jitter Tolerance<sup>(2)</sup></b>						
J <sub>T_SJ16.3</sub>	Sinusoidal jitter (QPLL) <sup>(3)</sup>	16.3 Gb/s	0.30	–	–	UI
J <sub>T_SJ15</sub>	Sinusoidal jitter (QPLL) <sup>(3)</sup>	15.0 Gb/s	0.30	–	–	UI
J <sub>T_SJ14.1</sub>	Sinusoidal jitter (QPLL) <sup>(3)</sup>	14.1 Gb/s	0.30	–	–	UI
J <sub>T_SJ13.1</sub>	Sinusoidal jitter (QPLL) <sup>(3)</sup>	13.1 Gb/s	0.30	–	–	UI
J <sub>T_SJ12.5</sub>	Sinusoidal jitter (QPLL) <sup>(3)</sup>	12.5 Gb/s	0.30	–	–	UI
J <sub>T_SJ11.3</sub>	Sinusoidal jitter (QPLL) <sup>(3)</sup>	11.3 Gb/s	0.30	–	–	UI
J <sub>T_SJ10.3_QPLL</sub>	Sinusoidal jitter (QPLL) <sup>(3)</sup>	10.3 Gb/s	0.30	–	–	UI
J <sub>T_SJ10.3_CPLL</sub>	Sinusoidal jitter (CPLL) <sup>(3)</sup>	10.3 Gb/s	0.30	–	–	UI
J <sub>T_SJ9.8</sub>	Sinusoidal jitter (QPLL) <sup>(3)</sup>	9.8 Gb/s	0.30	–	–	UI
J <sub>T_SJ8.0_QPLL</sub>	Sinusoidal jitter (QPLL) <sup>(3)</sup>	8.0 Gb/s	0.44	–	–	UI

**Table 58: GTH Transceiver Receiver Switching Characteristics (Cont'd)**

Symbol	Description	Condition	Min	Typ	Max	Units
J <sub>T_SJ8.0_CPLL</sub>	Sinusoidal jitter (CPLL) <sup>(3)</sup>	8.0 Gb/s	0.42	–	–	UI
J <sub>T_SJ6.6_CPLL</sub>	Sinusoidal jitter (CPLL) <sup>(3)</sup>	6.6 Gb/s	0.44	–	–	UI
J <sub>T_SJ5.0</sub>	Sinusoidal jitter (CPLL) <sup>(3)</sup>	5.0 Gb/s	0.44	–	–	UI
J <sub>T_SJ4.25</sub>	Sinusoidal jitter (CPLL) <sup>(3)</sup>	4.25 Gb/s	0.44	–	–	UI
J <sub>T_SJ4.0L</sub>	Sinusoidal jitter (CPLL) <sup>(3)</sup>	4.0 Gb/s <sup>(4)</sup>	0.45	–	–	UI
J <sub>T_SJ3.75</sub>	Sinusoidal jitter (CPLL) <sup>(3)</sup>	3.75 Gb/s	0.44	–	–	UI
J <sub>T_SJ3.2</sub>	Sinusoidal jitter (CPLL) <sup>(3)</sup>	3.2 Gb/s <sup>(5)</sup>	0.45	–	–	UI
J <sub>T_SJ2.5</sub>	Sinusoidal jitter (CPLL) <sup>(3)</sup>	2.5 Gb/s <sup>(6)</sup>	0.50	–	–	UI
J <sub>T_SJ1.25</sub>	Sinusoidal jitter (CPLL) <sup>(3)</sup>	1.25 Gb/s <sup>(7)</sup>	0.50	–	–	UI
J <sub>T_SJ500</sub>	Sinusoidal jitter (CPLL) <sup>(3)</sup>	500 Mb/s	0.40	–	–	UI
<b>SJ Jitter Tolerance with Stressed Eye<sup>(2)</sup></b>						
J <sub>T_TJSE3.2</sub>	Total jitter with stressed eye <sup>(8)</sup>	3.2 Gb/s	0.70	–	–	UI
J <sub>T_TJSE6.6</sub>		6.6 Gb/s	0.70	–	–	UI
J <sub>T_SJSE3.2</sub>	Sinusoidal jitter with stressed eye <sup>(8)</sup>	3.2 Gb/s	0.10	–	–	UI
J <sub>T_SJSE6.6</sub>		6.6 Gb/s	0.10	–	–	UI

**Notes:**

- Using RXOUT\_DIV = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 10<sup>-12</sup>.
- The frequency of the injected sinusoidal jitter is 10 MHz.
- CPLL frequency at 2.0 GHz and RXOUT\_DIV = 1.
- CPLL frequency at 3.2 GHz and RXOUT\_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT\_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT\_DIV = 4.
- Composite jitter with RX equalizer enabled. DFE disabled.

## GTH Transceiver Electrical Compliance

The *UltraScale Architecture GTH Transceiver User Guide (UG576)* contains recommended use modes that ensure compliance for the protocols listed in [Table 59](#). The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

*Table 59: GTH Transceiver Protocol List*

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
5.0G Ethernet	IEEE 802.3bx (PAR)	5.0	Compliant
QSGMII	QSGMII v1.2 (Cisco Systems, ENG-46158)	5.0	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
2.5G Ethernet	IEEE 802.3bx (PAR)	2.5	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11G-SR	4.25–12.5	Compliant
PCIe Gen1, 2, 3	PCI Express Base 3.0	2.5, 5.0, and 8.0	Compliant
UHD-SDI <sup>(1)</sup>	SMPTE ST-2081 6G, SMPTE St-2082 12G	6 and 12	Compliant
SDI <sup>(1)</sup>	SMPTE 424M-2006	0.27–2.97	Compliant
Hybrid Memory Cube (HMC)	HMC-15G-SR	12.5 and 15.0	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
HDMI <sup>(2)</sup>	HDMI 2.0	All	Compliant
Passive Optical Network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant
Serial RapidIO	RapidIO Specification 3.1	1.25–10.3125	Compliant
DisplayPort (source only)	DP 1.2B CTS	1.62–5.4	Compliant
Fibre Channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA Revision 3.0 Specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625–12.5	Compliant

### Notes:

- SDI protocols require external circuitry to achieve compliance.
- HDMI protocols require external circuitry to achieve compliance.

## GTH Transceiver Protocol Jitter Characteristics

For [Table 60](#) through [Table 65](#), the *UltraScale Architecture GTH Transceiver User Guide (UG576)* contains recommended settings for optimal usage of protocol specific characteristics.

*Table 60: Gigabit Ethernet Protocol Characteristics (GTH Transceivers)*

Description	Line Rate (Mb/s)	Min	Max	Units
<b>Gigabit Ethernet Transmitter Jitter Generation</b>				
Total transmitter jitter (T <sub>TJ</sub> )	1250	–	0.24	UI
<b>Gigabit Ethernet Receiver High Frequency Jitter Tolerance</b>				
Total receiver jitter tolerance	1250	0.749	–	UI

*Table 61: XAUI Protocol Characteristics (GTH Transceivers)*

Description	Line Rate (Mb/s)	Min	Max	Units
<b>XAUI Transmitter Jitter Generation</b>				
Total transmitter jitter (T <sub>TJ</sub> )	3125	–	0.35	UI
<b>XAUI Receiver High Frequency Jitter Tolerance</b>				
Total receiver jitter tolerance	3125	0.65	–	UI

*Table 62: PCI Express Protocol Characteristics (GTH Transceivers)<sup>(1)</sup>*

Standard	Description	Condition	Line Rate (Mb/s)	Min	Max	Units
<b>PCI Express Transmitter Jitter Generation</b>						
PCI Express Gen 1	Total transmitter jitter		2500	–	0.25	UI
PCI Express Gen 2	Total transmitter jitter		5000	–	0.25	UI
PCI Express Gen 3 <sup>(2)</sup>	Total transmitter jitter uncorrelated		8000	–	31.25	ps
	Deterministic transmitter jitter uncorrelated			–	12	ps
<b>PCI Express Receiver High Frequency Jitter Tolerance</b>						
PCI Express Gen 1	Total receiver jitter tolerance		2500	0.65	–	UI
PCI Express Gen 2 <sup>(2)</sup>	Receiver inherent timing error		5000	0.40	–	UI
	Receiver inherent deterministic timing error			0.30	–	UI
PCI Express Gen 3 <sup>(2)</sup>	Receiver sinusoidal jitter tolerance	0.03 MHz–1.0 MHz	8000	1.00	–	UI
		1.0 MHz–10 MHz		<a href="#">Note 3</a>	–	UI
		10 MHz–100 MHz		0.10	–	UI

### Notes:

1. Tested per card electromechanical (CEM) methodology.
2. Using common REFCLK.
3. Between 1 MHz and 10 MHz the minimum sinusoidal jitter roll-off with a slope of 20 dB/decade.

**Table 63: CEI-6G and CEI-11G Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
<b>CEI-6G Transmitter Jitter Generation</b>					
Total transmitter jitter <sup>(1)</sup>	4976–6375	CEI-6G-SR	–	0.3	UI
		CEI-6G-LR	–	0.3	UI
<b>CEI-6G Receiver High Frequency Jitter Tolerance</b>					
Total receiver jitter tolerance <sup>(1)</sup>	4976–6375	CEI-6G-SR	0.6	–	UI
		CEI-6G-LR	0.95	–	UI
<b>CEI-11G Transmitter Jitter Generation</b>					
Total transmitter jitter <sup>(2)</sup>	9950–11100	CEI-11G-SR	–	0.3	UI
		CEI-11G-LR/MR	–	0.3	UI
<b>CEI-11G Receiver High Frequency Jitter Tolerance</b>					
Total receiver jitter tolerance <sup>(2)</sup>	9950–11100	CEI-11G-SR	0.65	–	UI
		CEI-11G-MR	0.65	–	UI
		CEI-11G-LR	0.825	–	UI

**Notes:**

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

**Table 64: SFP+ Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
<b>SFP+ Transmitter Jitter Generation</b>				
Total transmitter jitter	9830.40 <sup>(1)</sup>	–	0.28	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			
<b>SFP+ Receiver Frequency Jitter Tolerance</b>				
Total receiver jitter tolerance	9830.40 <sup>(1)</sup>	0.7	–	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			

**Notes:**

1. Line rated used for CPRI over SFP+ applications.

**Table 65: CPRI Protocol Characteristics (GTH Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
<b>CPRI Transmitter Jitter Generation</b>				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
	9830.4	–	Note 1	UI
<b>CPRI Receiver Frequency Jitter Tolerance</b>				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2	0.95	–	UI
	6144.0	0.95	–	UI
	9830.4	Note 1	–	UI

**Notes:**

1. Tested per SFP+ specification, see [Table 64](#).

# GTY Transceiver Specifications

## GTY Transceiver DC Input and Output Levels

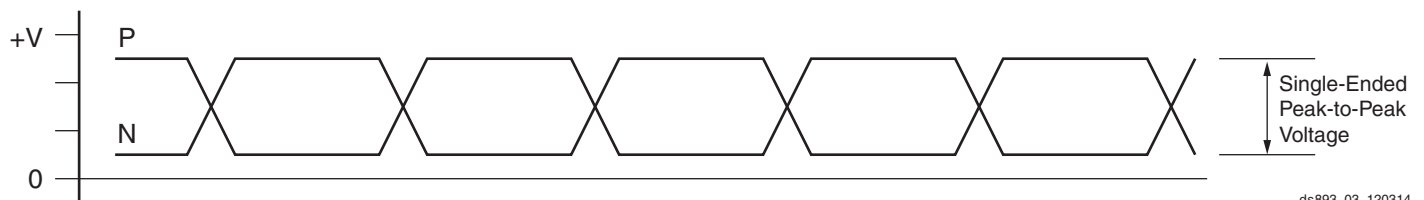
Table 66 summarizes the DC specifications of the GTY transceivers in Virtex UltraScale FPGAs. Consult [High Speed Serial](#) for further details.

Table 66: GTY Transceiver DC Specifications

Symbol	DC Parameter	Conditions	Min	Typ	Max	Units
D <sub>VPPIN</sub>	Differential peak-to-peak input voltage (external AC coupled)	> 10.3125 Gb/s	150	–	1250	mV
		6.6 Gb/s to 10.3125 Gb/s	150	–	1250	mV
		≤ 6.6 Gb/s	150	–	2000	mV
V <sub>IN</sub>	Single-ended input voltage. Voltage measured at the pin referenced to GND.	DC coupled V <sub>MGTAVTT</sub> = 1.2V	–400	–	V <sub>MGTAVTT</sub>	mV
V <sub>CMIN</sub>	Common mode input voltage	DC coupled V <sub>MGTAVTT</sub> = 1.2V	–	2/3 V <sub>MGTAVTT</sub>	–	mV
D <sub>VPPOUT</sub>	Differential peak-to-peak output voltage <sup>(1)</sup>	Transmitter output swing is set to 0x1F	800	–	–	mV
V <sub>CMOUTDC</sub>	Common mode output voltage: DC coupled (equation based)	When remote RX is terminated to GND	$V_{MGTAVTT}/2 - D_{VPPOUT}/4$			mV
		When remote RX termination is floating	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
		When remote RX is terminated to V <sub>RX_TERM</sub> <sup>(2)</sup>	$V_{MGTAVTT} - \frac{D_{VPPOUT}}{4} - \left(\frac{V_{MGTAVTT} - V_{RX\_TERM}}{2}\right)$			mV
V <sub>CMOUTAC</sub>	Common mode output voltage: AC coupled	Equation based	$V_{MGTAVTT} - D_{VPPOUT}/2$			mV
R <sub>IN</sub>	Differential input resistance		–	100	–	Ω
R <sub>OUT</sub>	Differential output resistance		–	100	–	Ω
T <sub>OSKEW</sub>	Transmitter output pair (TXP and TXN) intra-pair skew		–	–	5	ps
C <sub>EXT</sub>	Recommended external AC coupling capacitor <sup>(3)</sup>		–	100	–	nF

**Notes:**

1. The output swing and pre-emphasis levels are programmable using the GTY transceiver attributes and can result in values lower than reported in this table.
2. V<sub>RX\_TERM</sub> is the remote RX termination voltage.
3. Other values can be used as appropriate to conform to specific protocols and standards.



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Figure 6: Single-Ended Peak-to-Peak Voltage

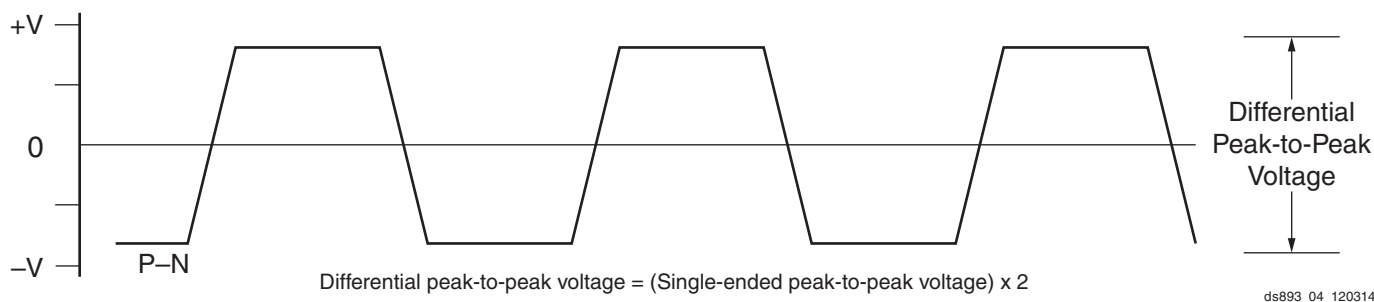


Figure 7: Differential Peak-to-Peak Voltage

Table 67 summarizes the DC specifications of the clock input of the GTY transceivers in Virtex UltraScale FPGAs. Consult High Speed Serial for further details.

Table 67: GTY Transceiver Clock DC Input Level Specification

Symbol	DC Parameter	Min	Typ	Max	Units
V <sub>IDIFF</sub>	Differential peak-to-peak input voltage	250	–	2000	mV
R <sub>IN</sub>	Differential input resistance	–	100	–	Ω
C <sub>EXT</sub>	Required external AC coupling capacitor	–	10	–	nF

Table 68: GTY Transceiver Clock Output Level Specification

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>OL</sub>	Output Low voltage for P and N	R <sub>T</sub> = 100Ω across P and N signals	–	400	–	mV
V <sub>OH</sub>	Output High voltage for P and N	R <sub>T</sub> = 100Ω across P and N signals	–	760	–	mV
V <sub>DDOUT</sub>	Differential output voltage (P–N), P = High (N–P), N = High	R <sub>T</sub> = 100Ω across P and N signals	–	±360	–	mV
V <sub>CMOUT</sub>	Common mode voltage	R <sub>T</sub> = 100Ω across P and N signals	–	580	–	mV

## GTY Transceiver Switching Characteristics

Consult [High Speed Serial](#) for further information.

Table 69: GTY Transceiver Performance

Symbol	Description	Output Divider	Speed Grades and V <sub>CCINT</sub> Operating Voltages								Units
			1.0V				0.95V				
			-3		-1H		-2		-1		
F <sub>GTYMAX</sub>	GTY maximum line rate		30.5		25.8		28.21		12.5		Gb/s
F <sub>GTYMIN</sub>	GTY minimum line rate		0.5		0.5		0.5		0.5		Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
F <sub>GTYCRANGE</sub>	CPLL line rate range <sup>(1)</sup>	1	4.0	12.5	4.0	12.5	4.0	12.5	4.0	8.5	Gb/s
		2	2.0	6.25	2.0	6.25	2.0	6.25	2.0	4.25	Gb/s
		4	1.0	3.125	1.0	3.125	1.0	3.125	1.0	2.125	Gb/s
		8	0.5	1.5625	0.5	1.5625	0.5	1.5625	0.5	1.0625	Gb/s
		16	N/A								Gb/s
		32	N/A								Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
F <sub>GTYQRANGE1</sub>	QPLL0 line rate range	1 <sup>(2)</sup>	19.6	30.5 <sup>(3)</sup>	19.6	25.8	19.6	28.21	N/A	N/A	Gb/s
		1 <sup>(4)</sup>	9.8	16.375	9.8	16.375	9.8	16.375	9.8	12.5	Gb/s
		2 <sup>(4)</sup>	4.9	8.1875	4.9	8.1875	4.9	8.1875	4.9	8.1875	Gb/s
		4 <sup>(4)</sup>	2.45	4.09375	2.45	4.09375	2.45	4.09375	2.45	4.09375	Gb/s
		8 <sup>(4)</sup>	1.225	2.04688	1.225	2.04688	1.225	2.04688	1.225	2.04688	Gb/s
		16 <sup>(4)</sup>	0.6125	1.02344	0.6125	1.02344	0.6125	1.02344	0.6125	1.02344	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
F <sub>GTYQRANGE2</sub>	QPLL1 line rate range	1 <sup>(5)</sup>	16.0	26.0	16.0	26.0	16.0	26.0	N/A	N/A	Gb/s
		1 <sup>(6)</sup>	8.0	13.0	8.0	13.0	8.0	13.0	8.0	12.5	Gb/s
		2 <sup>(6)</sup>	4.0	6.5	4.0	6.5	4.0	6.5	4.0	6.5	Gb/s
		4 <sup>(6)</sup>	2.0	3.25	2.0	3.25	2.0	3.25	2.0	3.25	Gb/s
		8 <sup>(6)</sup>	1.0	1.625	1.0	1.625	1.0	1.625	1.0	1.625	Gb/s
		16 <sup>(6)</sup>	0.5	0.8125	0.5	0.8125	0.5	0.8125	0.5	0.8125	Gb/s
			Min	Max	Min	Max	Min	Max	Min	Max	
F <sub>CPLL</sub> RANGE	CPLL frequency range		2.0	6.25	2.0	6.25	2.0	6.25	2.0	4.25	GHz
F <sub>QPLL0</sub> RANGE	QPLL0 frequency range		9.8	16.375	9.8	16.375	9.8	16.375	9.8	16.375	GHz
F <sub>QPLL1</sub> RANGE	QPLL1 frequency range		8.0	13.0	8.0	13.0	8.0	13.0	8.0	13.0	GHz

### Notes:

- The values listed are the rounded results of the calculated equation  $(2 \times \text{CPLL\_Frequency}) / \text{Output\_Divider}$ .
- The values listed are the rounded results of the calculated equation  $(2 \times \text{QPLL0\_Frequency}) / \text{Output\_Divider}$ . These values are for line rates greater than 16.375 Gb/s.
- This value is limited by F<sub>GTYMAX</sub>.
- The values listed are rounded results from calculated equation  $(\text{QPLL0\_Frequency}) / \text{Output\_Divider}$ .
- The values listed are the rounded results of the calculated equation  $(2 \times \text{QPLL1\_Frequency}) / \text{Output\_Divider}$ . These values are for line rates greater than 16.375 Gb/s.
- The values listed are rounded results from calculated equation  $(\text{QPLL1\_Frequency}) / \text{Output\_Divider}$ .

Table 70: GTY Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics

Symbol	Description	All Devices	Units
$F_{GTYDRPCLK}$	GTYDRPCLK maximum frequency	250	MHz

Table 71: GTY Transceiver Reference Clock Switching Characteristics

Symbol	Description	Conditions	Min	Typ	Max	Units
$F_{GCLK}$	Reference clock frequency range		60	–	820	MHz
$T_{RCLK}$	Reference clock rise time	20% – 80%	–	200	–	ps
$T_{FCLK}$	Reference clock fall time	80% – 20%	–	200	–	ps
$T_{DCREF}$	Reference clock duty cycle	Transceiver PLL only	40	50	60	%

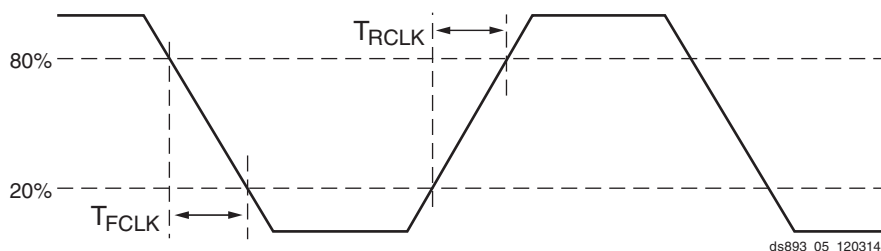


Figure 8: Reference Clock Timing Parameters

Table 72: GTY Transceiver Reference Clock Oscillator Selection Phase Noise Mask (1)

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
$QPLL_{REFCLKMASK}$	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
	QPLL0/QPLL1 reference clock select phase noise mask at REFCLK frequency = 625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	

Table 72: GTY Transceiver Reference Clock Oscillator Selection Phase Noise Mask<sup>(1)</sup> (Cont'd)

Symbol	Description	Offset Frequency	Min	Typ	Max	Units
CPLL <sub>REFCLKMASK</sub>	CPLL reference clock select phase noise mask at REFCLK frequency = 156.25 MHz.	10 kHz	–	–	–112	dBc/Hz
		100 kHz	–	–	–128	
		1 MHz	–	–	–145	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 312.5 MHz.	10 kHz	–	–	–103	dBc/Hz
		100 kHz	–	–	–123	
		1 MHz	–	–	–143	
		50 MHz	–	–	–145	
	CPLL reference clock select phase noise mask at REFCLK frequency = 625 MHz.	10 kHz	–	–	–98	dBc/Hz
		100 kHz	–	–	–117	
		1 MHz	–	–	–140	
		50 MHz	–	–	–144	

Notes:

- For reference clock frequencies not in this table, use the phase-noise mask for the nearest reference clock frequency.

Table 73: GTY Transceiver PLL/Lock Time Adaptation

Symbol	Description	Conditions	Min	Typ	Max	Units
T <sub>LOCK</sub>	Initial PLL lock		–	–	1	ms
T <sub>DLOCK</sub>	Clock recovery phase acquisition and adaptation time for decision feedback equalizer (DFE).	After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input.	–	50,000	37 x 10 <sup>6</sup>	UI
	Clock recovery phase acquisition and adaptation time for low-power mode (LPM) when the DFE is disabled.		–	50,000	2.3 x 10 <sup>6</sup>	UI

Table 74: GTY Transceiver User Clock Switching Characteristics<sup>(1)</sup>

Symbol	Description	Data Width Conditions (Bit)		Speed Grades and V <sub>CCINT</sub> Operating Voltages				Units
				1.0V		0.95V		
		Internal Logic	Interconnect Logic	-3	-1H	-2	-1	
F <sub>TXOUTPMA</sub>	TXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	511.719	390.625	MHz
F <sub>RXOUTPMA</sub>	RXOUTCLK maximum frequency sourced from OUTCLKPMA			511.719	511.719	511.719	390.625	MHz
F <sub>TXOUTPROGDIV</sub>	TXOUTCLK maximum frequency sourced from TXPROGDIVCLK			511.719	511.719	511.719	511.719	MHz
F <sub>RXOUTPROGDIV</sub>	RXOUTCLK maximum frequency sourced from RXPROGDIVCLK			511.719	511.719	511.719	511.719	MHz

Table 74: GTY Transceiver User Clock Switching Characteristics<sup>(1)</sup>

Symbol	Description	Data Width Conditions (Bit)		Speed Grades and V <sub>CCINT</sub> Operating Voltages				Units
				1.0V		0.95V		
		Internal Logic	Interconnect Logic	-3	-1H	-2	-1	
F <sub>TXIN</sub>	TXUSRCLK maximum frequency	16	16, 32	511.719	402.832	511.719	390.625	MHz
		32	32, 64	511.719	402.832	511.719	390.625	MHz
		64	64, 128	476.563	402.832	440.781	195.313	MHz
		20	20, 40	409.375	322.266	409.375	312.500	MHz
		40	40, 80	409.375	322.266	409.375	312.500	MHz
		80	80, 160	381.250	322.266	352.625	156.250	MHz
F <sub>RXIN</sub>	RXUSRCLK maximum frequency	16	16, 32	511.719	402.832	511.719	390.625	MHz
		32	32, 64	511.719	402.832	511.719	390.625	MHz
		64	64, 128	476.563	402.832	440.781	195.313	MHz
		20	20, 40	409.375	322.266	409.375	312.500	MHz
		40	40, 80	409.375	322.266	409.375	312.500	MHz
		80	80, 160	381.250	322.266	352.625	156.250	MHz
F <sub>TXIN2</sub>	TXUSRCLK2 maximum frequency	16	16	511.719	402.832	511.719	390.625	MHz
		16	32	511.719	201.416	511.719	390.625	MHz
		32	32	511.719	402.832	511.719	390.625	MHz
		32	64	476.563	201.416	440.781	195.313	MHz
		64	64	476.563	402.832	440.781	195.313	MHz
		64	128	238.281	201.416	220.391	97.656	MHz
		20	20	409.375	322.266	409.375	312.500	MHz
		20	40	409.375	161.133	409.375	312.500	MHz
		40	40	409.375	322.266	409.375	312.500	MHz
		40	80	381.250	161.133	352.625	156.250	MHz
		80	80	381.250	322.266	352.625	156.250	MHz
		80	160	190.625	161.133	176.313	78.125	MHz

**Table 74: GTY Transceiver User Clock Switching Characteristics<sup>(1)</sup>**

Symbol	Description	Data Width Conditions (Bit)		Speed Grades and V <sub>CCINT</sub> Operating Voltages				Units
				1.0V		0.95V		
		Internal Logic	Interconnect Logic	-3	-1H	-2	-1	
F <sub>RXIN2</sub>	RXUSRCLK2 maximum frequency	16	16	511.719	402.832	511.719	390.625	MHz
		16	32	511.719	201.416	511.719	390.625	MHz
		32	32	511.719	402.832	511.719	390.625	MHz
		32	64	476.563	201.416	440.781	195.313	MHz
		64	64	476.563	402.832	440.781	195.313	MHz
		64	128	238.281	201.416	220.391	97.656	MHz
		20	20	409.375	322.266	409.375	312.500	MHz
		20	40	409.375	161.133	409.375	312.500	MHz
		40	40	409.375	322.266	409.375	312.500	MHz
		40	80	381.250	161.133	352.625	156.250	MHz
		80	80	381.250	322.266	352.625	156.250	MHz
80	160	190.625	161.133	176.313	78.125	MHz		

**Notes:**

1. Clocking must be implemented as described in the *UltraScale Architecture GTY Transceiver User Guide (UG578)*.

**Table 75: GTY Transceiver Transmitter Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F <sub>GTYTX</sub>	Serial data rate range		0.500	–	F <sub>GTYMAX</sub>	Gb/s
T <sub>RTX</sub>	TX rise time	20%–80%	–	21	–	ps
T <sub>FTX</sub>	TX fall time	80%–20%	–	21	–	ps
T <sub>LLSKEW</sub>	TX lane-to-lane skew <sup>(1)</sup>		–	–	500	ps
V <sub>TXOOBVDPP</sub>	Electrical idle amplitude		–	–	15	mV
T <sub>TXOOBTRANSITION</sub>	Electrical idle transition time		–	–	140	ns
T <sub>J30.5_QPLL</sub>	Total jitter <sup>(2)(4)</sup>	30.5 Gb/s	–	–	0.32	UI
D <sub>J30.5_QPLL</sub>	Deterministic jitter <sup>(2)(4)</sup>		–	–	0.17	UI
T <sub>J28.2_QPLL</sub>	Total jitter <sup>(2)(4)</sup>	28.2 Gb/s	–	–	0.30	UI
D <sub>J28.2_QPLL</sub>	Deterministic jitter <sup>(2)(4)</sup>		–	–	0.17	UI
T <sub>J25.78_QPLL</sub>	Total jitter <sup>(2)(4)</sup>	25.78 Gb/s	–	–	0.30	UI
D <sub>J25.78_QPLL</sub>	Deterministic jitter <sup>(2)(4)</sup>		–	–	0.17	UI
T <sub>J16.3_QPLL</sub>	Total jitter <sup>(2)(4)</sup>	16.3 Gb/s	–	–	0.28	UI
D <sub>J16.3_QPLL</sub>	Deterministic jitter <sup>(2)(4)</sup>		–	–	0.17	UI
T <sub>J15_QPLL</sub>	Total jitter <sup>(2)(4)</sup>	15.0 Gb/s	–	–	0.28	UI
D <sub>J15_QPLL</sub>	Deterministic jitter <sup>(2)(4)</sup>		–	–	0.17	UI
T <sub>J14.1_QPLL</sub>	Total jitter <sup>(2)(4)</sup>	14.1 Gb/s	–	–	0.28	UI
D <sub>J14.1_QPLL</sub>	Deterministic jitter <sup>(2)(4)</sup>		–	–	0.17	UI
T <sub>J14.025_QPLL</sub>	Total jitter <sup>(2)(4)</sup>	14.025 Gb/s	–	–	0.28	UI
D <sub>J14.025_QPLL</sub>	Deterministic jitter <sup>(2)(4)</sup>		–	–	0.17	UI
T <sub>J13.1_QPLL</sub>	Total jitter <sup>(2)(4)</sup>	13.1 Gb/s	–	–	0.28	UI
D <sub>J13.1_QPLL</sub>	Deterministic jitter <sup>(2)(4)</sup>		–	–	0.17	UI
T <sub>J12.5_QPLL</sub>	Total jitter <sup>(2)(4)</sup>	12.5 Gb/s	–	–	0.28	UI
D <sub>J12.5_QPLL</sub>	Deterministic jitter <sup>(2)(4)</sup>		–	–	0.17	UI
T <sub>J12.5_CPLL</sub>	Total jitter <sup>(3)(4)</sup>	12.5 Gb/s	–	–	0.33	UI
D <sub>J12.5_CPLL</sub>	Deterministic jitter <sup>(3)(4)</sup>		–	–	0.17	UI
T <sub>J11.3_QPLL</sub>	Total jitter <sup>(2)(4)</sup>	11.3 Gb/s	–	–	0.28	UI
D <sub>J11.3_QPLL</sub>	Deterministic jitter <sup>(2)(4)</sup>		–	–	0.17	UI
T <sub>J10.3_QPLL</sub>	Total jitter <sup>(2)(4)</sup>	10.3125 Gb/s	–	–	0.28	UI
D <sub>J10.3_QPLL</sub>	Deterministic jitter <sup>(2)(4)</sup>		–	–	0.17	UI
T <sub>J10.3_CPLL</sub>	Total jitter <sup>(3)(4)</sup>	10.3125 Gb/s	–	–	0.33	UI
D <sub>J10.3_CPLL</sub>	Deterministic jitter <sup>(3)(4)</sup>		–	–	0.17	UI
T <sub>J9.953_QPLL</sub>	Total jitter <sup>(2)(4)</sup>	9.953 Gb/s	–	–	0.28	UI
D <sub>J9.953_QPLL</sub>	Deterministic jitter <sup>(2)(4)</sup>		–	–	0.17	UI
T <sub>J9.8_QPLL</sub>	Total jitter <sup>(2)(4)</sup>	9.8 Gb/s	–	–	0.28	UI
D <sub>J9.8_QPLL</sub>	Deterministic jitter <sup>(2)(4)</sup>		–	–	0.17	UI
T <sub>J8.0_QPLL</sub>	Total jitter <sup>(2)(4)</sup>	8.0 Gb/s	–	–	0.28	UI
D <sub>J8.0_QPLL</sub>	Deterministic jitter <sup>(2)(4)</sup>		–	–	0.17	UI
T <sub>J8.0_CPLL</sub>	Total jitter <sup>(3)(4)</sup>	8.0 Gb/s	–	–	0.32	UI
D <sub>J8.0_CPLL</sub>	Deterministic jitter <sup>(3)(4)</sup>		–	–	0.17	UI

**Table 75: GTY Transceiver Transmitter Switching Characteristics (Cont'd)**

Symbol	Description	Condition	Min	Typ	Max	Units
T <sub>J6.6_CPLL</sub>	Total jitter <sup>(3)(4)</sup>	6.6 Gb/s	–	–	0.30	UI
D <sub>J6.6_CPLL</sub>	Deterministic jitter <sup>(3)(4)</sup>		–	–	0.15	UI
T <sub>J5.0</sub>	Total jitter <sup>(3)(4)</sup>	5.0 Gb/s	–	–	0.30	UI
D <sub>J5.0</sub>	Deterministic jitter <sup>(3)(4)</sup>		–	–	0.15	UI
T <sub>J4.25</sub>	Total jitter <sup>(3)(4)</sup>	4.25 Gb/s	–	–	0.30	UI
D <sub>J4.25</sub>	Deterministic jitter <sup>(3)(4)</sup>		–	–	0.15	UI
T <sub>J4.00L</sub>	Total jitter <sup>(3)(4)</sup>	4.00 Gb/s	–	–	0.32	UI
D <sub>J4.00L</sub>	Deterministic jitter <sup>(3)(4)</sup>		–	–	0.16	UI
T <sub>J3.75</sub>	Total jitter <sup>(3)(4)</sup>	3.75 Gb/s	–	–	0.20	UI
D <sub>J3.75</sub>	Deterministic jitter <sup>(3)(4)</sup>		–	–	0.10	UI
T <sub>J3.20</sub>	Total jitter <sup>(3)(4)</sup>	3.20 Gb/s <sup>(5)</sup>	–	–	0.20	UI
D <sub>J3.20</sub>	Deterministic jitter <sup>(3)(4)</sup>		–	–	0.10	UI
T <sub>J2.5</sub>	Total jitter <sup>(3)(4)</sup>	2.5 Gb/s <sup>(6)</sup>	–	–	0.20	UI
D <sub>J2.5</sub>	Deterministic jitter <sup>(3)(4)</sup>		–	–	0.10	UI
T <sub>J1.25</sub>	Total jitter <sup>(3)(4)</sup>	1.25 Gb/s <sup>(7)</sup>	–	–	0.15	UI
D <sub>J1.25</sub>	Deterministic jitter <sup>(3)(4)</sup>		–	–	0.05	UI
T <sub>J500</sub>	Total jitter <sup>(3)(4)</sup>	500 Mb/s	–	–	0.10	UI
D <sub>J500</sub>	Deterministic jitter <sup>(3)(4)</sup>		–	–	0.05	UI

**Notes:**

- Using same REFCLK input with TX phase alignment enabled for up to four fully-populated GTY Quads at maximum line rate.
- Using QPLL\_FBDIV = 40, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- Using CPLL\_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
- All jitter values are based on a bit-error ratio of 10<sup>-12</sup>.
- CPLL frequency at 3.2 GHz and TXOUT\_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT\_DIV = 2.
- CPLL frequency at 2.5 GHz and TXOUT\_DIV = 4.

**Table 76: GTY Transceiver Receiver Switching Characteristics**

Symbol	Description	Condition	Min	Typ	Max	Units
F <sub>GTYRX</sub>	Serial data rate		0.500	–	F <sub>GTYMAX</sub>	Gb/s
T <sub>RXELECIDLE</sub>	Time for RXELECIDLE to respond to loss or restoration of data		–	10	–	ns
R <sub>XOOBVDPP</sub>	OOB detect threshold peak-to-peak		60	–	150	mV
R <sub>XSSST</sub>	Receiver spread-spectrum tracking <sup>(1)</sup>	Modulated at 33 kHz	–5000	–	0	ppm
R <sub>XRL</sub>	Run length (CID)		–	–	256	UI
R <sub>XPPMTOL</sub>	Data/REFCLK PPM offset tolerance	Bit rates ≤ 6.6 Gb/s	–1250	–	1250	ppm
		Bit rates > 6.6 Gb/s and ≤ 8.0 Gb/s	–700	–	700	ppm
		Bit rates > 8.0 Gb/s	–200	–	200	ppm
<b>SJ Jitter Tolerance<sup>(2)</sup></b>						
J <sub>T_SJ30.5</sub>	Sinusoidal jitter (QPLL) <sup>(3)</sup>	30.5 Gb/s	0.20	–	–	UI
J <sub>T_SJ28.2</sub>	Sinusoidal jitter (QPLL) <sup>(3)</sup>	28.2 Gb/s	0.25	–	–	UI

**Table 76: GTY Transceiver Receiver Switching Characteristics (Cont'd)**

Symbol	Description	Condition	Min	Typ	Max	Units
J <sub>T_SJ25.78</sub>	Sinusoidal jitter (QPLL) <sup>(3)</sup>	25.78 Gb/s	0.25	–	–	UI
J <sub>T_SJ16.375</sub>	Sinusoidal jitter (QPLL) <sup>(3)</sup>	16.375 Gb/s	0.30	–	–	UI
J <sub>T_SJ15</sub>	Sinusoidal jitter (QPLL) <sup>(3)</sup>	15.0 Gb/s	0.30	–	–	UI
J <sub>T_SJ14.1</sub>	Sinusoidal jitter (QPLL) <sup>(3)</sup>	14.1 Gb/s	0.30	–	–	UI
J <sub>T_SJ13.1</sub>	Sinusoidal jitter (QPLL) <sup>(3)</sup>	13.1 Gb/s	0.30	–	–	UI
J <sub>T_SJ12.5_QPLL</sub>	Sinusoidal jitter (QPLL) <sup>(3)</sup>	12.5 Gb/s	0.30	–	–	UI
J <sub>T_SJ12.5_CPLL</sub>	Sinusoidal jitter (QPLL) <sup>(3)</sup>	12.5 Gb/s	0.30	–	–	UI
J <sub>T_SJ11.3_QPLL</sub>	Sinusoidal jitter (QPLL) <sup>(3)</sup>	11.3 Gb/s	0.30	–	–	UI
J <sub>T_SJ10.32_QPLL</sub>	Sinusoidal jitter (QPLL) <sup>(3)</sup>	10.32 Gb/s	0.30	–	–	UI
J <sub>T_SJ10.32_CPLL</sub>	Sinusoidal jitter (CPLL) <sup>(3)</sup>	10.32 Gb/s	0.30	–	–	UI
J <sub>T_SJ9.8</sub>	Sinusoidal jitter (QPLL) <sup>(3)</sup>	9.8 Gb/s	0.30	–	–	UI
J <sub>T_SJ8.0_QPLL</sub>	Sinusoidal jitter (QPLL) <sup>(3)</sup>	8.0 Gb/s	0.44	–	–	UI
J <sub>T_SJ8.0_CPLL</sub>	Sinusoidal jitter (CPLL) <sup>(3)</sup>	8.0 Gb/s	0.42	–	–	UI
J <sub>T_SJ6.6_CPLL</sub>	Sinusoidal jitter (CPLL) <sup>(3)</sup>	6.6 Gb/s	0.44	–	–	UI
J <sub>T_SJ5.0</sub>	Sinusoidal jitter (CPLL) <sup>(3)</sup>	5.0 Gb/s	0.44	–	–	UI
J <sub>T_SJ4.25</sub>	Sinusoidal jitter (CPLL) <sup>(3)</sup>	4.25 Gb/s	0.44	–	–	UI
J <sub>T_SJ4.00L</sub>	Sinusoidal jitter (CPLL) <sup>(3)</sup>	4.0 Gb/s	0.45	–	–	UI
J <sub>T_SJ3.75</sub>	Sinusoidal jitter (CPLL) <sup>(3)</sup>	3.75 Gb/s	0.45	–	–	UI
J <sub>T_SJ3.20</sub>	Sinusoidal jitter (CPLL) <sup>(3)</sup>	3.2 Gb/s <sup>(4)</sup>	0.45	–	–	UI
J <sub>T_SJ2.5</sub>	Sinusoidal jitter (CPLL) <sup>(3)</sup>	2.5 Gb/s <sup>(5)</sup>	0.50	–	–	UI
J <sub>T_SJ1.25</sub>	Sinusoidal jitter (CPLL) <sup>(3)</sup>	1.25 Gb/s <sup>(6)</sup>	0.50	–	–	UI
J <sub>T_SJ500</sub>	Sinusoidal jitter (CPLL) <sup>(3)</sup>	500 Mb/s	0.50	–	–	UI
<b>SJ Jitter Tolerance with Stressed Eye<sup>(2)</sup></b>						
J <sub>T_TJSE3.2</sub>	Total jitter with stressed eye <sup>(7)</sup>	3.2 Gb/s	0.7	–	–	UI
J <sub>T_TJSE6.6</sub>		6.6 Gb/s	0.7	–	–	UI
J <sub>T_SJSE3.2</sub>	Sinusoidal jitter with stressed eye <sup>(7)</sup>	3.2 Gb/s	0.7	–	–	UI
J <sub>T_SJSE6.6</sub>		6.6 Gb/s	0.7	–	–	UI

**Notes:**

- Using RXOUT\_DIV = 1, 2, and 4.
- All jitter values are based on a bit error ratio of 10<sup>-12</sup>.
- The frequency of the injected sinusoidal jitter is 80 MHz.
- CPLL frequency at 3.2 GHz and RXOUT\_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT\_DIV = 2.
- CPLL frequency at 2.5 GHz and RXOUT\_DIV = 4.
- Composite jitter with RX equalizer enabled. DFE disabled.

## GTY Transceiver Electrical Compliance

The *UltraScale Architecture GTY Transceiver User Guide (UG578)* contains recommended use modes that ensure compliance for the protocols listed in [Table 77](#). The transceiver wizard provides the recommended settings for those use cases and for protocol specific characteristics.

*Table 77: GTY Transceiver Protocol List*

Protocol	Specification	Serial Rate (Gb/s)	Electrical Compliance
CAUI-4	IEEE 802.3-2012	25.78125	Compliant
28 Gb/s Backplane	CEI-25G-LR	25–28.05	Compliant
Interlaken	OIF-CEI-6G, OIF-CEI-11GSR, OIF-CEI-28G-MR	4.25–25.78125	Compliant
100GBASE-KR4	IEEE 802.3bj-2014, CEI-25G-LR	25.78125	Compliant <sup>(1)</sup>
OTU4 (OTL4.4)	OIF-CEI-28G-VSR	27.952493	Compliant
CAUI-10	IEEE 802.3-2012	10.3125	Compliant
nPPI	IEEE 802.3-2012	10.3125	Compliant
10GBASE-KR	IEEE 802.3-2012	10.3125	Compliant
SFP+	SFF-8431 (SR and LR)	9.95328–11.10	Compliant
XFP	INF-8077i, Revision 4.5	10.3125	Compliant
RXAUI	CEI-6G-SR	6.25	Compliant
XAUI	IEEE 802.3-2012	3.125	Compliant
1000BASE-X	IEEE 802.3-2012	1.25	Compliant
OTU2	ITU G.8251	10.709225	Compliant
OTU4 (OTL4.10)	OIF-CEI-11G-SR	11.180997	Compliant
OC-3/12/48/192	GR-253-CORE	0.1555–9.956	Compliant
PCIe Gen1, 2, 3	PCI Express Base 3.0	2.5, 5.0, and 8.0	Compliant
SDI	SMPTE 424M-2006	0.27–2.97	Compliant
Hybrid Memory Cube (HMC)	HMC-15G-SR	12.5 and 15.0	Compliant
CPRI	CPRI_v_6_1_2014-07-01	0.6144–12.165	Compliant
Passive Optical Network (PON)	10G-EPON, 1G-EPON, NG-PON2, XG-PON, and 2.5G-PON	0.155–10.3125	Compliant
JESD204a/b	OIF-CEI-6G, OIF-CEI-11G	3.125–12.5	Compliant
Serial RapidIO	RapidIO Specification 3.1	1.25–10.3125	Compliant
DisplayPort (Source Only)	DP 1.2B CTS	1.62–5.4	Compliant
Fibre Channel	FC-PI-4	1.0625–14.025	Compliant
SATA Gen1, 2, 3	Serial ATA Revision 3.0 Specification	1.5, 3.0, and 6.0	Compliant
SAS Gen1, 2, 3	T10/BSR INCITS 519	3.0, 6.0, and 12.0	Compliant
SFI-5	OIF-SFI5-01.0	0.625 - 12.5	Compliant

### Notes:

1. 25 dB loss at Nyquist without FEC.

## GTY Transceiver Protocol Jitter Characteristics

For Table 78 through Table 82, the *UltraScale Architecture GTY Transceiver User Guide (UG578)* contains recommended settings for optimal usage of protocol specific characteristics.

Table 78: Gigabit Ethernet Protocol Characteristics (GTY Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
<b>Gigabit Ethernet Transmitter Jitter Generation</b>				
Total transmitter jitter (T_TJ)	1250	–	0.24	UI
<b>Gigabit Ethernet Receiver High Frequency Jitter Tolerance</b>				
Total receiver jitter tolerance	1250	0.749	–	UI

Table 79: XAUI Protocol Characteristics (GTY Transceivers)

Description	Line Rate (Mb/s)	Min	Max	Units
<b>XAUI Transmitter Jitter Generation</b>				
Total transmitter jitter (T_TJ)	3125	–	0.35	UI
<b>XAUI Receiver High Frequency Jitter Tolerance</b>				
Total receiver jitter tolerance	3125	0.65	–	UI

Table 80: CEI-6G and CEI-11G Protocol Characteristics (GTY Transceivers)

Description	Line Rate (Mb/s)	Interface	Min	Max	Units
<b>CEI-6G Transmitter Jitter Generation</b>					
Total transmitter jitter <sup>(1)</sup>	4976–6375	CEI-6G-SR	–	0.3	UI
		CEI-6G-LR	–	0.3	UI
<b>CEI-6G Receiver High Frequency Jitter Tolerance</b>					
Total receiver jitter tolerance <sup>(1)</sup>	4976–6375	CEI-6G-SR	0.6	–	UI
		CEI-6G-LR	0.95	–	UI
<b>CEI-11G Transmitter Jitter Generation</b>					
Total transmitter jitter <sup>(2)</sup>	9950–11100	CEI-11G-SR	–	0.3	UI
		CEI-11G-LR/MR	–	0.3	UI
<b>CEI-11G Receiver High Frequency Jitter Tolerance</b>					
Total receiver jitter tolerance <sup>(2)</sup>	9950–11100	CEI-11G-SR	0.65	–	UI
		CEI-11G-MR	0.65	–	UI
		CEI-11G-LR	0.825	–	UI

**Notes:**

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.
2. Tested at line rate of 9950 Mb/s using 155.46875 MHz reference clock and 11100 Mb/s using 173.4375 MHz reference clock.

**Table 81: SFP+ Protocol Characteristics (GTY Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
<b>SFP+ Transmitter Jitter Generation</b>				
Total transmitter jitter	9830.40 <sup>(1)</sup>	–	0.28	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			
<b>SFP+ Receiver Frequency Jitter Tolerance</b>				
Total receiver jitter tolerance	9830.40 <sup>(1)</sup>	0.7	–	UI
	9953.00			
	10312.50			
	10518.75			
	11100.00			

**Notes:**

- Line rated used for CPRI over SFP+ applications.

**Table 82: CPRI Protocol Characteristics (GTY Transceivers)**

Description	Line Rate (Mb/s)	Min	Max	Units
<b>CPRI Transmitter Jitter Generation</b>				
Total transmitter jitter	614.4	–	0.35	UI
	1228.8	–	0.35	UI
	2457.6	–	0.35	UI
	3072.0	–	0.35	UI
	4915.2	–	0.3	UI
	6144.0	–	0.3	UI
	9830.4	–	Note 1	UI
<b>CPRI Receiver Frequency Jitter Tolerance</b>				
Total receiver jitter tolerance	614.4	0.65	–	UI
	1228.8	0.65	–	UI
	2457.6	0.65	–	UI
	3072.0	0.65	–	UI
	4915.2	0.95	–	UI
	6144.0	0.95	–	UI
	9830.4	Note 1	–	UI

**Notes:**

- Tested per SFP+ specification, see [Table 81](#).

## Integrated Interface Block for Interlaken

More information and documentation on solutions using the integrated interface block for Interlaken can be found at [UltraScale Interlaken](#). The *UltraScale Architecture and Product Overview (DS890)* lists the Virtex UltraScale FPGAs that include this block.

Table 83: Maximum Performance for Interlaken Designs

Symbol	Description	Speed Grades and V <sub>CCINT</sub> Operating Voltages								Units
		1.0V				0.95V				
		-3		-1H		-2		-1		
F <sub>RX_SERDES_CLK</sub>	Receive serializer/deserializer clock	402.84		402.84		402.84		195.32		MHz
F <sub>TX_SERDES_CLK</sub>	Transmit serializer/deserializer clock	402.84		402.84		402.84		195.32		MHz
F <sub>DRP_CLK</sub>	Dynamic reconfiguration port clock	250.00		250.00		250.00		250.00		MHz
		Min	Max	Min	Max	Min	Max	Min	Max	
F <sub>CORE_CLK</sub>	Interlaken core clock	300.00 <sup>(1)</sup>	429.69	300.00 <sup>(1)</sup>	429.69	300.00 <sup>(1)</sup>	429.69	300.00	322.27	MHz
		412.50 <sup>(2)</sup>		412.50 <sup>(2)</sup>		412.50 <sup>(2)</sup>				
F <sub>LBUS_CLK</sub>	Interlaken local bus clock	300.00	349.52	300.00	349.52	300.00	349.52	300.00	322.27	MHz

**Notes:**

1. The minimum value for CORE\_CLK is 300 MHz for the 12 x 12.5G Interlaken configuration.
2. The minimum value for CORE\_CLK is 412.5 MHz for the 6 x 25.78125G Interlaken configuration. This 6 x 25.78125G configuration is not supported in the lane logic-only mode.

## Integrated Interface Block for 100G Ethernet MAC and PCS

More information and documentation on solutions using the integrated 100 Gb/s Ethernet block can be found at [UltraScale Integrated 100G Ethernet MAC/PCS](#).

Table 84: Maximum Performance for 100G Ethernet Designs

Symbol	Description	Speed Grades and V <sub>CCINT</sub> Operating Voltages				Units
		1.0V		0.95V		
		-3	-1H	-2	-1	
F <sub>TX_CLK</sub>	Transmit clock	322.27	322.27	322.27	322.27	MHz
F <sub>RX_CLK</sub>	Receive clock	322.27	322.27	322.27	322.27	MHz
F <sub>RX_SERDES_CLK</sub>	Receive serializer/deserializer clock	322.27	322.27	322.27	322.27	MHz
F <sub>DRP_CLK</sub>	Dynamic reconfiguration port clock	250.00	250.00	250.00	250.00	MHz

# Integrated Interface Block for PCI Express Designs

More information and documentation on solutions for PCI Express designs can be found at [PCI Express](#).

Table 85: Maximum Performance for PCI Express Designs

Symbol	Description	Speed Grades and V <sub>CCINT</sub> Operating Voltages				Units
		1.0V		0.95V		
		-3	-1H	-2	-1	
F <sub>PIPECLK</sub>	Pipe clock maximum frequency	250.00	250.00	250.00	250.00	MHz
F <sub>CORECLK</sub>	Core clock maximum frequency	500.00	500.00 <sup>(1)</sup>	500.00	500.00 <sup>(1)</sup>	MHz
F <sub>USERCLK</sub>	User clock maximum frequency	250.00	250.00	250.00	250.00	MHz
F <sub>DRPCLK</sub>	DRP clock maximum frequency	250.00	250.00	250.00	250.00	MHz

**Notes:**

1. PCI Express x8 Gen3 operation is supported in -2 and -3 speed grades. Refer to the *UltraScale Architecture Gen3 Integrated Block for PCI Express v4.1 User Guide (PG156)* for information regarding x8 Gen 3 operation in the -1 speed grade.

# System Monitor Specifications

Table 86: SYSMON Specifications

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
V <sub>CCADC</sub> = 1.8V ±3%, V <sub>REFP</sub> = 1.25V, V <sub>REFN</sub> = 0V, ADCCLK = 5.2 MHz, T <sub>j</sub> = -40°C to 100°C, typical values at T <sub>j</sub> = 40°C						
<b>ADC Accuracy<sup>(1)</sup></b>						
Resolution			10	–	–	Bits
Integral nonlinearity <sup>(2)</sup>	INL		–	–	±2	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic	–	–	±1	LSBs
Offset error		Offset calibration enabled	–	–	±2	LSBs
Gain error			–	–	±0.4	%
Sample rate			–	–	0.2	MS/s
RMS code noise		External 1.25V reference	–	–	1	LSBs
		On-chip reference	–	1	–	LSBs
<b>ADC Accuracy at Extended Temperatures</b>						
Resolution		(T <sub>j</sub> = -55°C to 125°C)	10	–	–	Bits
Integral nonlinearity	INL	(T <sub>j</sub> = -55°C to 125°C)	–	–	±2	LSBs
Differential nonlinearity	DNL	No missing codes, guaranteed monotonic. (T <sub>j</sub> = -55°C to 125°C)	–	–	±1	

**Table 86: SYSMON Specifications (Cont'd)**

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
<b>Analog Inputs<sup>(2)</sup></b>						
ADC input ranges		Unipolar operation	0	–	1	V
		Bipolar operation	–0.5	–	+0.5	V
		Unipolar common mode range (FS input)	0	–	+0.5	V
		Bipolar common mode range (FS input)	+0.5	–	+0.6	V
Maximum external channel input ranges		Adjacent channels set within these ranges should not corrupt measurements on adjacent channels	–0.1	–	V <sub>CCADC</sub>	V
<b>On-Chip Sensor Accuracy</b>						
Temperature sensor error <sup>(1)</sup>		T <sub>j</sub> = –40°C to 100°C (with external REF)	–	–	±4	°C
		T <sub>j</sub> = –55°C to 125°C (with external REF)	–	–	±4.5	°C
		T <sub>j</sub> = –40°C to 100°C (with internal REF)	–	–	±5	°C
		T <sub>j</sub> = –55°C to 125°C (with internal REF)	–	–	±6.5	°C
Supply sensor error <sup>(3)</sup>		T <sub>j</sub> = –40°C to 100°C (with external REF)	–	–	±1	%
		T <sub>j</sub> = –55°C to 125°C (with external REF)	–	–	±2	%
		T <sub>j</sub> = –40°C to 100°C (with internal REF)	–	–	±1.5	%
		T <sub>j</sub> = –55°C to 125°C (with internal REF)	–	–	±2.5	%
<b>Conversion Rate<sup>(4)</sup></b>						
Conversion time—continuous	t <sub>CONV</sub>	Number of ADCCLK cycles	26	–	32	Cycles
Conversion time—event	t <sub>CONV</sub>	Number of ADCCLK cycles	–	–	21	Cycles
DRP clock frequency	DCLK	DRP clock frequency	8	–	250	MHz
ADC clock frequency	ADCCLK	Derived from DCLK	1	–	5.2	MHz
DCLK duty cycle			40	–	60	%
<b>SYSMON Reference<sup>(5)</sup></b>						
External reference	V <sub>REFP</sub>	Externally supplied reference voltage	1.20	1.25	1.30	V
On-chip reference		Ground V <sub>REFP</sub> pin to AGND, -2 and -3 speed grades T <sub>j</sub> = –40°C to 100°C	1.2375	1.25	1.2625	V
		Ground V <sub>REFP</sub> pin to AGND, -1 speed grades T <sub>j</sub> = –40°C to 100°C	1.23125	1.25	1.26875	V
		Ground V <sub>REFP</sub> pin to AGND, T <sub>j</sub> = –55°C to 125°C	1.225	1.25	1.275	V

**Notes:**

1. ADC offset errors are removed by enabling the ADC automatic offset calibration feature. The values are specified for when this feature is enabled.
2. See the *Analog Input* section in the *UltraScale Architecture System Monitor User Guide (UG580)*.
3. Supply sensor offset and gain errors are removed by enabling the automatic offset and gain calibration feature. The values are specified for when this feature is enabled.
4. See the *Adjusting the Acquisition Settling Time* section in the *UltraScale Architecture System Monitor User Guide (UG580)*.
5. Any variation in the reference voltage from the nominal V<sub>REFP</sub> = 1.25V and V<sub>REFN</sub> = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted.

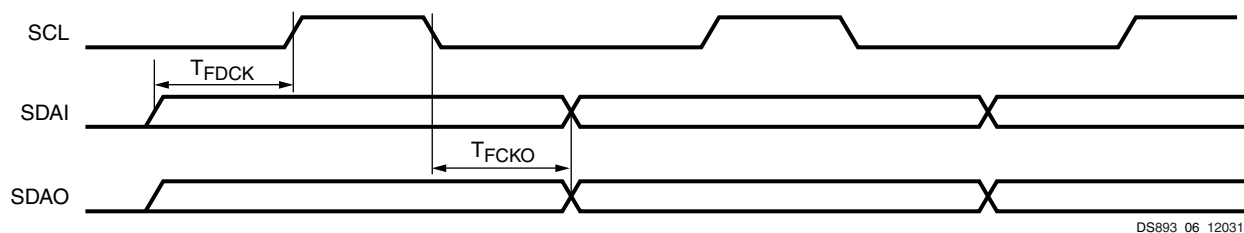
## I2C Interfaces

Table 87: I2C Fast Mode Interface Switching Characteristics<sup>(1)</sup>

Symbol	Description	Min	Typ	Max	Units
$T_{DCFLK}$	SCL duty cycle	–	50	–	%
$T_{FCKO}$	SDAO clock-to-out delay	–	–	900	ns
$T_{FDCK}$	SDAI setup time	100	–	–	ns
$F_{FCLK}$	SCL clock frequency	–	–	400	kHz

**Notes:**

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.



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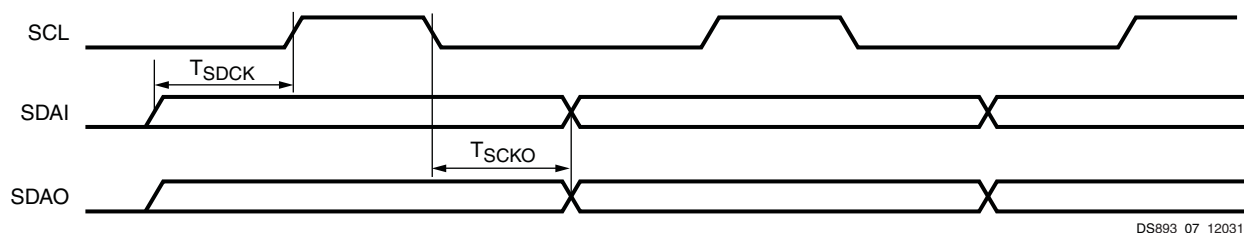
Figure 9: I2C Fast Mode Interface Timing Diagram

Table 88: I2C Standard Mode Interface Switching Characteristics<sup>(1)</sup>

Symbol	Description	Min	Typ	Max	Units
$T_{DCSCLK}$	SCL duty cycle	–	50	–	%
$T_{SCKO}$	SDAO clock-to-out delay	–	–	3450	ns
$T_{SDCK}$	SDAI setup time	250	–	–	ns
$F_{SCLK}$	SCL clock frequency	–	–	100	kHz

**Notes:**

1. Test conditions: LVCMOS33, slow slew rate, 8 mA drive strength, 15 pF loads.



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Figure 10: I2C Standard Mode Interface Timing Diagram

# Configuration Switching Characteristics

Table 89: Configuration Switching Characteristics

Symbol	Description	Speed Grades and V <sub>CCINT</sub> Operating Voltages				Units	
		1.0V		0.95V			
		-3	-1H	-2	-1		
<b>Power-up Timing Characteristics</b>							
T <sub>PL</sub>	Program latency	7.5	7.5	7.5	7.5	ms, Max	
T <sub>POR</sub>	Power-on reset (40 ms maximum ramp rate time)	57	57	57	57	ms, Max	
		0	0	0	0	ms, Min	
	Power-on reset with POR override (2 ms maximum ramp rate time)	15	15	15	15	ms, Max	
		5	5	5	5	ms, Min	
T <sub>PROGRAM</sub>	Program pulse width	250	250	250	250	ns, Min	
<b>CCLK Output (Master Mode)</b>							
T <sub>ICCK</sub>	Master CCLK output delay from INIT_B	150	150	150	150	ns, Min	
T <sub>MCCKL</sub>	Master CCLK clock Low time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max	
T <sub>MCCKH</sub>	Master CCLK clock High time duty cycle	40/60	40/60	40/60	40/60	%, Min/Max	
F <sub>MCCK</sub>	Master CCLK frequency	SPI x2/x4/x8 BPI x8, x16	150	150	150	150	MHz, Max
		SPI x1 and serial SLR-based devices	100	100	100	100	MHz, Max
		SPI x1 and serial all other devices	150	150	150	150	MHz, Max
		SelectMAP	125	125	125	125	MHz, Max
F <sub>MCCK_START</sub>	Master CCLK frequency at start of configuration	3	3	3	3	MHz, Typ	
F <sub>MCCKTOL</sub>	Frequency tolerance, master mode with respect to nominal CCLK	±35	±35	±35	±35	%, Max	
<b>CCLK Input (Slave Modes)</b>							
T <sub>SCCKL</sub>	Slave CCLK clock minimum Low time	2.5	2.5	2.5	2.5	ns, Min	
T <sub>SCCKH</sub>	Slave CCLK clock minimum High time	2.5	2.5	2.5	2.5	ns, Min	
F <sub>SCCK</sub>	Slave CCLK frequency	Serial SLR-based devices	100	100	100	100	MHz, Max
		Serial all other devices	150	150	150	150	MHz, Max
		SelectMAP	125	125	125	125	MHz, Max

**Table 89: Configuration Switching Characteristics (Cont'd)**

Symbol	Description	Speed Grades and V <sub>CCINT</sub> Operating Voltages				Units	
		1.0V		0.95V			
		-3	-1H	-2	-1		
<b>EMCCLK Input (Master Mode)</b>							
T <sub>EMCCKL</sub> <sup>(1)</sup>	External master CCLK Low time		2.50	2.50	2.50	2.50	ns, Min
T <sub>EMCCKH</sub> <sup>(1)</sup>	External master CCLK High time		2.50	2.50	2.50	2.50	ns, Min
F <sub>EMCCK</sub>	External master CCLK frequency	SPI x2/x4/x8 BPI x8, x16	150	150	150	150	MHz, Max
		SPI x1 and serial SLR-based devices	100	100	100	100	MHz, Max
		SPI x1 and serial all other devices	150	150	150	150	MHz, Max
		SelectMAP	125	125	125	125	MHz, Max
<b>Internal Configuration Access Port</b>							
F <sub>ICAPCK</sub>	Internal configuration access port (ICAPE3)	Master SLR ICAP accessing the entire device	125	125	125	125	MHz, Max
		SLR ICAP accessing the local SLR	200	200	200	200	MHz, Max
		All other devices	200	200	200	200	MHz, Max
<b>Master/Slave Serial Mode Programming Switching</b>							
T <sub>DCCK</sub> /T <sub>CCKD</sub>	D <sub>IN</sub> setup/hold		3.0/0	3.0/0	3.0/0	3.0/0	ns, Min
T <sub>CCO</sub>	D <sub>OUT</sub> clock to out		8.0	8.0	8.0	8.0	ns, Max
<b>SelectMAP Mode Programming Switching</b>							
T <sub>SMDCK</sub> /T <sub>SMCKD</sub>	D[31:00] setup/hold		3.5/0	3.5/0	3.5/0	3.5/0	ns, Min
T <sub>SMCSCCK</sub> /T <sub>SMCKCS</sub>	CSI_B setup/hold		4.0/0	4.0/0	4.0/0	4.0/0	ns, Min
T <sub>SMWCK</sub> /T <sub>SMCKW</sub>	RDWR_B setup/hold		10.0/0	10.0/0	10.0/0	10.0/0	ns, Min
T <sub>SMCKCSO</sub>	CSO_B clock to out (330Ω pull-up resistor required)		7.0	7.0	7.0	7.0	ns, Max
T <sub>SMCO</sub>	D[31:00] clock to out in readback		8.0	8.0	8.0	8.0	ns, Max
F <sub>RBCK</sub>	Readback frequency	SLR-based devices	125	125	125	125	MHz, Max
		All other devices	125	125	125	125	MHz, Max
<b>Boundary-Scan Port Timing Specifications</b>							
T <sub>TAPTCK</sub> /T <sub>TCKTAP</sub>	TMS and TDI setup/hold	SLR-based devices	15.0/2.0	15.0/2.0	15.0/2.0	15.0/2.0	ns, Min
		All other devices	3.0/2.0	3.0/2.0	3.0/2.0	3.0/2.0	ns, Min
T <sub>TCKTDO</sub>	TCK falling edge to TDO output	SLR-based devices	23.0	23.0	23.0	23.0	ns, Max
		All other devices	7.0	7.0	7.0	7.0	ns, Max
F <sub>TCK</sub>	TCK frequency	SLR-based devices	20	20	20	20	MHz, Max
		All other devices	50	50	50	50	MHz, Max

**Table 89: Configuration Switching Characteristics (Cont'd)**

Symbol	Description	Speed Grades and V <sub>CCINT</sub> Operating Voltages				Units
		1.0V		0.95V		
		-3	-1H	-2	-1	
<b>BPI Master Flash Mode Programming Switching</b>						
T <sub>BPICCO</sub>	A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out	10.0	10.0	10.0	10.0	ns, Max
T <sub>BPIDCC</sub> /T <sub>BPICCD</sub>	D[15:00] setup/hold	3.5/0	3.5/0	3.5/0	3.5/0	ns, Min
<b>SPI Master Flash Mode Programming Switching</b>						
T <sub>SPIDCC</sub> /T <sub>SPICCD</sub>	D[03:00] setup/hold	3.0/0	3.0/0	3.0/0	3.0/0	ns, Min
T <sub>SPIDCC</sub> /T <sub>SPICCD</sub>	D[07:04] setup/hold	3.5/0	3.5/0	3.5/0	3.5/0	ns, Min
T <sub>SPICCM</sub>	MOSI clock to out	8.0	8.0	8.0	8.0	ns, Max
T <sub>SPICCM2</sub>	D[04] clock to out	10.0	10.0	10.0	10.0	ns, Max
T <sub>SPICFC</sub>	FCS_B clock to out	8.0	8.0	8.0	8.0	ns, Max
T <sub>SPICFC2</sub>	FCS2_B clock to out	10.0	10.0	10.0	10.0	ns, Max
<b>DNA Port Switching</b>						
F <sub>DNACK</sub>	DNA port frequency	200	200	200	200	MHz, Max
<b>STARTUPE3 Ports</b>						
T <sub>USRCLKO</sub>	STARTUPE3 USRCLKO input port to CCLK pin output delay	1.00/ 6.00	1.00/ 6.70	1.00/ 6.70	1.00/ 7.50	ns, Min/Max
T <sub>DO</sub>	DO[3:0] ports to D03-D00 pins output delay	1.00/ 6.70	1.00/ 7.70	1.00/ 7.70	1.00/ 8.40	ns, Min/Max
T <sub>DTS</sub>	DTS[3:0] ports to D03-D00 pins 3-state delays	1.00/ 7.30	1.00/ 8.30	1.00/ 8.30	1.00/ 9.00	ns, Min/Max
T <sub>FCSBO</sub>	FCSBO port to FCS_B pin output delay	1.00/ 6.90	1.00/ 8.00	1.00/ 8.00	1.00/ 8.60	ns, Min/Max
T <sub>FCSBTS</sub>	FCSBTS port to FCS_B pin 3-state delay	1.00/ 6.90	1.00/ 8.00	1.00/ 8.00	1.00/ 8.60	ns, Min/Max
T <sub>USRDONEO</sub>	USRDONEO port to DONE pin output delay	1.00/ 8.50	1.00/ 9.60	1.00/ 9.60	1.00/ 10.40	ns, Min/Max
T <sub>USRDONETS</sub>	USRDONETS port to DONE pin 3-state delay	1.00/ 8.50	1.00/ 9.60	1.00/ 9.60	1.00/ 10.40	ns, Min/Max
T <sub>DI</sub>	D03-D00 pins to DI[3:0] ports input delay	0.5/ 2.6	0.5/ 3.1	0.5/ 3.1	0.5/ 3.5	ns, Min/Max
F <sub>CFGMCLK</sub>	STARTUPE3 CFGMCLK output frequency	50	50	50	50	MHz, Typ
F <sub>CFGMCLKTOL</sub>	STARTUPE3 CFGMCLK output frequency tolerance	±15	±15	±15	±15	%, Max
<b>Startup Timing</b>						
T <sub>DCI_MATCH</sub>	Specifies a stall in the startup cycle until the digitally controlled impedance (DCI) match signals are asserted.	4	4	4	4	ms, Max

**Notes:**

1. When the CCLK is sourced from the EMCCLK pin with a divide-by-one setting, the external EMCCLK must meet these low time and high time requirements.

# eFUSE Programming Conditions

Table 90: eFUSE Programming Conditions<sup>(1)</sup>

Symbol	Description	Min	Typ	Max	Units
$I_{FS}$	$V_{CCAUX}$ supply current	–	–	115	mA
$T_j$	Temperature range	–40	–	125	°C

**Notes:**

- Do not program eFUSE during device configuration (e.g., during configuration, during configuration readback, or when readback CRC is active).

## Revision History

The following table shows the revision history for this document.

Date	Version	Description of Revisions
05/23/2019	1.12	In <a href="#">Table 3</a> , updated the $I_{BATT}$ <a href="#">Note 4</a> for additional calculations when designing with XCVU125, XCVU160, XCVU190, and XCVU440 devices. Added LVDS component mode notes to the <a href="#">Performance Characteristics</a> section.
10/30/2018	1.11	Added <a href="#">Note 3</a> to <a href="#">Table 24</a> . Added <a href="#">Table 42</a> . Updated <a href="#">Table 45</a> . Added <a href="#">Table 46</a> .
01/08/2018	1.10	In <a href="#">Table 1</a> , because the voltages are covered in <a href="#">Table 4</a> , removed the note on $V_{IN}$ for I/O input voltage for HR I/O banks. Added <a href="#">Note 2</a> to <a href="#">Table 4</a> . Revised the $F_{REFCLK}$ descriptions in <a href="#">Table 33</a> . Reduced the typical $T_{RTX}/T_{FTX}$ values in <a href="#">Table 57</a> . Reduced the typical $T_{RTX}/T_{FTX}$ values in <a href="#">Table 75</a> . Added $T_{SPICCM2}$ and $T_{SPICCF2}$ to <a href="#">Table 89</a> .
03/06/2017	1.9	Updated <a href="#">Table 24</a> with clarifications to the SDR minimums. Updated $MMCM\_F_{DRPCLK\_MAX}$ in <a href="#">Table 36</a> and $PLL\_F_{DRPCLK\_MAX}$ in <a href="#">Table 37</a> .
12/22/2016	1.8	The Vivado Design Suite version is update to the latest version listed in <a href="#">Table 20</a> (either v1.23 or v1.24). Per the <i>Kintex UltraScale and Virtex UltraScale FPGA Speed Specification Changes (XCN16031)</i> , <a href="#">Table 22</a> changes the minimum speed specification versions for designing with devices listed in this data sheet per the design advisory answer record <a href="#">AR68169: Design Advisory for Kintex UltraScale FPGAs and Virtex UltraScale FPGAs—New minimum production speed specification version (Speed File) required for all designs</a> . Added $T_{MINPER\_CLK}$ and <a href="#">Note 1</a> to <a href="#">Table 33</a> . Added HP and HR minimum values to <a href="#">Table 23</a> and <a href="#">Table 24</a> . Added $MMCM\_F_{DRPCLK\_MAX}$ to <a href="#">Table 36</a> and $PLL\_F_{DRPCLK\_MAX}$ to <a href="#">Table 37</a> . Added <a href="#">Table 68</a> . Updated the <a href="#">Automotive Applications Disclaimer</a> .
04/04/2016	1.7.1	Updated date and revision.
04/01/2016	1.7	Updated <a href="#">Table 20</a> , <a href="#">Table 21</a> , and <a href="#">Table 22</a> to production release in Vivado Design Suite 2016.1 of the following devices/speed/temperature grades. With these changes, the XC Virtex UltraScale FPGAs are production released. XCVU065: -3E (1.0V) devices XCVU125: -3E (1.0V) devices XCVU440: -3E (1.0V) devices In <a href="#">Table 26</a> , added LPDDR3, added LRDIMMs to the notes, and removed <a href="#">Note 6</a> . In <a href="#">Table 32</a> , added the <a href="#">Block RAM and FIFO Clock-to-Out Delays</a> section.

Date	Version	Description of Revisions
03/02/2016	1.6	Updated <a href="#">Table 20</a> , <a href="#">Table 21</a> , and <a href="#">Table 22</a> with speed specifications for Vivado Design Suite 2015.4.2. Production release ( <a href="#">Table 22</a> ) of the XCVU065, XCVU080, XCVU095, XCVU125, XCVU160, and XCVU190 devices in the -1HE (1.0V) and -1HE (0.95V) speed/temperature grades. This new specification revised the -1HE (1.0V) specifications in <a href="#">Table 43</a> . Added <a href="#">Note 1</a> to <a href="#">Table 26</a> . Updated $V_{MEAS}$ for LVCMOS and LVTTTL in <a href="#">Table 30</a> . Added <a href="#">Table 72</a> .
12/16/2015	1.5	Updated the <a href="#">Power-On/Off Power Supply Sequencing</a> section. Updated <a href="#">Table 20</a> , <a href="#">Table 21</a> , and <a href="#">Table 22</a> with speed specifications for Vivado Design Suite 2015.4.1 v1.20 where applicable. Production release ( <a href="#">Table 22</a> ) of the XCVU065 and XCVU125 devices in the -2E/-2I (0.95V) and -1I (0.95V) speed/temperature grades. Revised the XCVU065 values in <a href="#">Table 43</a> .
11/24/2015	1.4	Added the -1HE (1.0V and 0.95V) speed grade throughout. Revised the <a href="#">GTH or GTY Transceiver</a> section in <a href="#">Table 2</a> . Updated <a href="#">Table 20</a> , <a href="#">Table 21</a> , <a href="#">Table 22</a> , <a href="#">Table 27</a> , and <a href="#">Table 28</a> with speed specifications for Vivado Design Suite 2015.4 v1.19. Production release ( <a href="#">Table 22</a> ) of the XCVU160 and XCVU190 devices in the -3 (1.0V), -2 (0.95V), and -1 (0.95V) speed/temperature grades and XCVU440 in the -2 and -1 speed/temperature grades. Updated <a href="#">Table 69</a> and expanded <a href="#">Table 74</a> with -1HE values.
10/12/2015	1.3	Updated description of $I_{CCADC}$ in <a href="#">Table 3</a> . Updated the description in <a href="#">Power-On/Off Power Supply Sequencing</a> . Updated <a href="#">Table 20</a> , <a href="#">Table 21</a> , <a href="#">Table 22</a> , <a href="#">Table 27</a> , and <a href="#">Table 28</a> with speed specifications for Vivado Design Suite 2015.3 v1.18. Production release ( <a href="#">Table 22</a> ) of the XCVU095 and XCVU080 devices in the -3 (1.0V), -2 (0.95V), and -1 (0.95V) speed/temperature grades. Added protocols to <a href="#">Table 59</a> . Updated $V_{CMOUTDC}$ in <a href="#">Table 66</a> . Added data to <a href="#">Table 75</a> and <a href="#">Table 76</a> . In <a href="#">Table 89</a> , revised values for $F_{SCCK}$ , $F_{EMCCK}$ , $F_{RBCK}$ , and $F_{TCK}$ and added the <a href="#">Startup Timing</a> section.
07/27/2015	1.2	In <a href="#">Table 18</a> and <a href="#">Table 19</a> updated <a href="#">Note 2</a> , <a href="#">Note 3</a> , and <a href="#">Note 4</a> . Updated <a href="#">Table 20</a> and <a href="#">Table 38</a> through <a href="#">Table 44</a> with speed specifications for Vivado Design Suite 2015.2 v1.16. Updated the <a href="#">STARTUPE3 Ports</a> descriptions in <a href="#">Table 89</a> . Updated <a href="#">Note 1</a> in <a href="#">Table 90</a> .

Date	Version	Description of Revisions
05/29/2015	1.1	<p>Entire data sheet is updated. Some of the highlights are noted in this revision history although it is not comprehensive.</p> <p>Updated <a href="#">Note 2</a> and <a href="#">Note 3</a> in <a href="#">Table 1</a> and <a href="#">Note 3</a>, <a href="#">Note 4</a>, and <a href="#">Note 6</a> in <a href="#">Table 2</a>. Added data and <a href="#">Note 2</a> to <a href="#">Table 3</a>. Updated <a href="#">Note 3</a> in <a href="#">Table 6</a>. Revised the <a href="#">Power-On/Off Power Supply Sequencing</a> section. Updated the descriptions in <a href="#">Table 8</a>. Revised the <math>V_{OCM}</math> maximum for <a href="#">MINI_LVDS_25</a> and <a href="#">RSDS_25</a> in <a href="#">Table 12</a>. Revised the <math>V_{ICM}</math> specifications in <a href="#">Table 14</a>. Removed rows from <a href="#">Table 16</a> and <a href="#">Table 17</a>. Removed <math>V_{OH}</math> and <math>V_{OL}</math> rows, revised the <math>V_{OCM}</math> maximum, and revised <math>V_{ICM}</math> in <a href="#">Table 18</a>. Removed <math>V_{OH}</math> and <math>V_{OL}</math> rows and revised <math>V_{ICM}</math> in <a href="#">Table 19</a>. Updated <a href="#">Table 20</a>, <a href="#">Table 27</a>, and <a href="#">Table 28</a> with speed specifications for Vivado Design Suite 2015.1 v1.15. Added <a href="#">Note 1</a> to <a href="#">Table 29</a>.</p> <p>Added the section: <a href="#">I/O Standard Adjustment Measurement Methodology</a>. Updated <a href="#">F<sub>REFCLK</sub></a> in <a href="#">Table 33</a>. Revised <a href="#">MMCM_F<sub>INMAX</sub></a> and <a href="#">MMCM_T<sub>LOCKMAX</sub></a> in <a href="#">Table 36</a>. Updated the descriptions and <a href="#">PLL_F<sub>INMAX</sub></a> in <a href="#">Table 37</a>. Added a discussion on the data in the device pin-to-pin parameter tables on <a href="#">page 40</a> and <a href="#">page 42</a>. Updated <a href="#">Table 45</a>. Updated the package information in <a href="#">Table 47</a>. Updated <a href="#">V<sub>CMOUTDC</sub></a> and added <a href="#">Note 2</a> in <a href="#">Table 48</a>. Added <a href="#">Table 50</a> and <a href="#">Table 54</a>. Updated both <a href="#">Table 57</a> and <a href="#">Table 58</a>. Updated and combined the protocol characteristic sections into the <a href="#">GTH Transceiver Electrical Compliance</a> section. Updated some of the maximum values for <a href="#">F<sub>GTMAX</sub></a>, <a href="#">F<sub>GTQRANGE1</sub></a>, and <a href="#">F<sub>GTQRANGE2</sub></a> in <a href="#">Table 69</a>. Updated <a href="#">F<sub>RXIN2</sub></a> (data width conditions for internal logic) in <a href="#">Table 74</a>. Updated and combined the protocol characteristic sections into the <a href="#">GTY Transceiver Electrical Compliance</a> section. Revised the values for <a href="#">F<sub>LBUS_CLK</sub></a> in <a href="#">Table 83</a>. Revised <a href="#">F<sub>CORECLK</sub></a> and <a href="#">Note 1</a> in <a href="#">Table 85</a>. Updated the <a href="#">On-Chip Sensor Accuracy</a>, <a href="#">On-chip reference</a>, and <a href="#">Note 5</a> in <a href="#">Table 86</a>. In <a href="#">Table 89</a>, added more speed specifications, updated <a href="#">T<sub>POR</sub></a>, <a href="#">T<sub>PL</sub></a>, <a href="#">F<sub>MCCKTOL</sub></a>, and <a href="#">F<sub>RBCK</sub></a>, added the <a href="#">STARTUPE3 Ports</a> section, and added <a href="#">Note 1</a>.</p>
07/10/2014	1.0	Initial Xilinx release.

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