

74LVCE1G00FZ4 Datasheet



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DiGi Electronics Part Number	74LVCE1G00FZ4-DG
Manufacturer	Diodes Incorporated
Manufacturer Product Number	74LVCE1G00FZ4
Description	IC GATE NAND 1CH 2-INP DFN1410-6
Detailed Description	NAND Gate IC 1 Channel X2-DFN1410-6



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Purchase and inquiry

Manufacturer Product Number:

74LVCE1G00FZ4

Series:

74LVCE

Logic Type:

NAND Gate

Number of Inputs:

2

Voltage - Supply:

1.4V ~ 5.5V

Current - Output High, Low:

32mA, 32mA

Input Logic Level - High:

1.7V ~ 2V

Operating Temperature:

-40°C ~ 85°C

Supplier Device Package:

X2-DFN1410-6

Base Product Number:

74LVCE1G00

Manufacturer:

Diodes Incorporated

Product Status:

Discontinued at Digi-Key

Number of Circuits:

1

Features:

-

Current - Quiescent (Max):

10 μ A

Input Logic Level - Low:

0.7V ~ 0.8V

Max Propagation Delay @ V, Max CL:

3.6ns @ 5V, 50pF

Mounting Type:

Surface Mount

Package / Case:

6-XFDNFN

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99



74LVCE1G00

SINGLE 2 INPUT POSITIVE NAND GATE

Description

The 74LVCE1G00 is a single 2-input positive NAND gate with a standard totem pole output. The device is designed for operation with a power supply range of 1.4V to 5.5V. The inputs are tolerant to 5.5V allowing this device to be used in a mixed voltage environment. The device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output preventing damaging current backflow when the device is powered down.

The gate performs the positive Boolean function:

$$Y = \overline{A \bullet B} \text{ or } Y = \overline{A} + \overline{B}$$

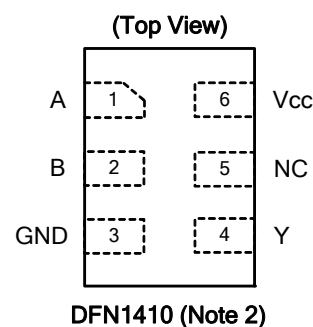
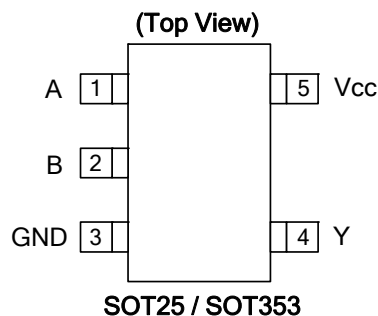
Features

- Extended Supply Voltage Range from 1.4 to 5.5V
- Switching speed characterized for operation at 1.5V
- Offers 30% speed improvement over LVC at 1.8V.
- $\pm 24\text{mA}$ Output Drive at 3.3V
- CMOS low power consumption
- IOFF Supports Partial-Power-Down Mode Operation
- Inputs accept up to 5.5V
- ESD Protection Tested per JESD 22
 - Exceeds 200-V Machine Model (A115-A)
 - Exceeds 2000-V Human Body Model (A114-A)
- Latch-Up Exceeds 100mA per JESD 78, Class II
- Range of Package Options
- Direct Interface with TTL Levels
- SOT25, SOT353, and DFN1410: Assembled with "Green" Molding Compound (no Br, Sb)
- Lead Free Finish/ RoHS Compliant (Note 1)

Notes: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at http://www.diodes.com/products/lead_free.html.

2. Pin 2 and pin 5 of the DFN1410 package are internally connected.

Pin Assignments



Applications

- Voltage Level Shifting
- General Purpose Logic
- Wide array of products such as.
 - PCs, networking, notebooks, netbooks, PDAs
 - Computer peripherals, hard drives, CD/DVD ROM
 - TV, DVD, DVR, set top box
 - Cell Phones, Personal Navigation / GPS
 - MP3 players ,Cameras, Video Recorders



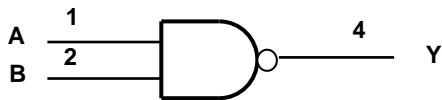
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SINGLE 2 INPUT POSITIVE NAND GATE

Pin Descriptions

Pin Name	Description
A	Data Input
B	Data Input
GND	Ground
Y	Data Output
Vcc	Supply Voltage

Logic Diagram



Function Table

Inputs		Output
A	B	Y
H	H	L
L	X	H
X	L	H

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SINGLE 2 INPUT POSITIVE NAND GATE

Absolute Maximum Ratings (Note 3)

Symbol	Description	Rating	Unit
ESD HBM	Human Body Model ESD Protection	2	KV
ESD MM	Machine Model ESD Protection	200	V
V_{CC}	Supply Voltage Range	-0.5 to 6.5	V
V_I	Input Voltage Range	-0.5 to 6.5	V
V_o	Voltage applied to output in high impedance or I_{OFF} state	-0.5 to 6.5	V
V_o	Voltage applied to output in high or low state	-0.3 to $V_{CC} + 0.5$	V
I_{IK}	Input Clamp Current $V_I < 0$	-50	mA
I_{OK}	Output Clamp Current	-50	mA
I_o	Continuous output current	± 50	mA
	Continuous current through Vdd or GND	± 100	mA
T_J	Operating Junction Temperature	-40 to 150	$^{\circ}C$
T_{STG}	Storage Temperature	-65 to 150	$^{\circ}C$

Note: 3. Stresses beyond the absolute maximum may result in immediate failure or reduced reliability. These are stress values and device operation should be within recommend values.



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SINGLE 2 INPUT POSITIVE NAND GATE

Recommended Operating Conditions (Note 4)

Symbol	Parameter		Min	Max	Unit
V _{CC}	Operating Voltage	Operating	1.4	5.5	V
		Data retention only	1.2		V
V _{IH}	High-level Input Voltage	V _{CC} = 1.4 V to 1.95 V	0.65 X V _{CC}		V
		V _{CC} = 2.3 V to 2.7 V	1.7		
		V _{CC} = 3 V to 3.6 V	2		
		V _{CC} = 4.5 V to 5.5 V	0.7 X V _{CC}		
V _{IL}	Low-level input voltage	V _{CC} = 1.4 V to 1.95 V		0.35 X V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V		0.7	
		V _{CC} = 3 V to 3.6 V		0.8	
		V _{CC} = 4.5 V to 5.5 V		0.3 X V _{CC}	
V _I	Input Voltage		0	5.5	V
V _O	Output Voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} =1.4 V		-3	mA
		V _{CC} = 1.65 V		-4	
		V _{CC} = 2.3 V		-8	
		V _{CC} = 3 V		-16	
		V _{CC} = 4.5 V		-24	
I _{OL}	Low-level output current	V _{CC} =1.4 V		3	mA
		V _{CC} = 1.65 V		4	
		V _{CC} = 2.3 V		8	
		V _{CC} = 3 V		16	
		V _{CC} = 4.5 V		24	
Δt/ΔV	Input transition rise or fall rate	V _{CC} = 1.4 to 3V		20	ns/V
		V _{CC} = 3.3 V ± 0.3 V		10	
		V _{CC} = 5 V ± 0.5 V		5	
T _A	Operating free-air temperature		-40	85	°C

Note: 4. Unused inputs should be held at V_{CC} or Ground.



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SINGLE 2 INPUT POSITIVE NAND GATE

Electrical Characteristics (All typical values are at $V_{CC} = 3.3V$, $T_A = 25^\circ C$)

Over recommended free-air temperature range (unless otherwise noted)

Symbol	Parameter	Test Conditions	Vcc	Min	Typ.	Max	Unit
V_{OH}	High Level Output Voltage	$I_{OH} = -100\mu A$	1.4 V to 5.5V	$V_{CC} - 0.1$			V
		$I_{OH} = -3mA$	1.4 V	1.05			
		$I_{OH} = -4mA$	1.65 V	1.2			
		$I_{OH} = -8mA$	2.3V	1.9			
		$I_{OH} = -16mA$	3 V	2.4			
		$I_{OH} = -24mA$		2.3			
		$I_{OH} = -32mA$	4.5 V	3.8			
V_{OL}	High-level Input Voltage	$I_{OL} = 100\mu A$	1.4 V to 5.5V			0.1	V
		$I_{OL} = 3mA$	1.4 V			.4	
		$I_{OL} = 4mA$	1.65 V			0.45	
		$I_{OL} = 8mA$	2.3V			0.3	
		$I_{OL} = 16mA$	3 V			0.4	
		$I_{OL} = 24mA$				0.55	
		$I_{OL} = 32mA$	4.5			0.55	
I_I	Input Current	$V_I = 5.5 V$ or GND	0 to 5.5 V			± 5	μA
I_{OFF}	Power Down Leakage Current	V_I or $V_O = 5.5V$	0			± 10	μA
I_{CC}	Supply Current	$V_I = 5.5V$ of GND $I_O = 0$	1.4 V to 5.5V			10	μA
ΔI_{CC}	Additional Supply Current	One input at $V_{CC} - 0.6 V$ Other inputs at V_{CC} or GND	3 V to 5.5V			500	μA
C_i	Input Capacitance	$V_i = V_{CC} -$ or GND	3.3		3.5		pF
θ_{JA}	Thermal Resistance Junction-to-Ambient	SOT25	(Note 5)		204		$^\circ C/W$
		SOT353	(Note 5)		371		
		DFN1410	(Note 5)		430		
θ_{JC}	Thermal Resistance Junction-to-Case	SOT25	(Note 5)		52		$^\circ C/W$
		SOT353	(Note 5)		143		
		DFN1410	(Note 5)		190		

Note: 5. Test condition for SOT25, SOT353, and DFN1410: Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.



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SINGLE 2 INPUT POSITIVE NAND GATE

Switching Characteristics

Over recommended free-air temperature range, $C_L = 15\text{pF}$ (see Figure 1)

Parameter	From (Input)	TO (OUTPUT)	$V_{CC} = 1.5\text{ V} \pm 0.1\text{ V}$		$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{pd}	A or B	Y	2.2	7.2	1.5	5	0.6	3.5	0.6	3.1	0.7	3	ns

Over recommended free-air temperature range, $C_L = 30$ or 50pF as noted (see Figure 2)

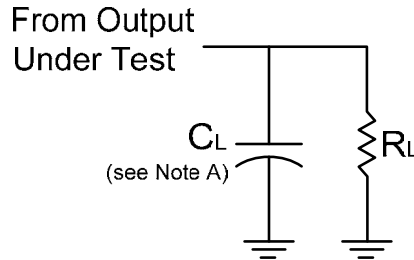
Parameter	From (Input)	TO (OUTPUT)	$V_{CC} = 1.5\text{ V} \pm 0.1\text{ V}$		$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{pd}	A or B	Y	3.1	9	2.1	6.3	1	4.4	0.8	3.8	0.9	3.6	ns

Operating Characteristics

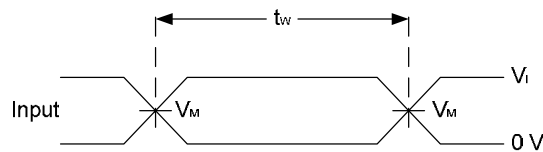
$T_A = 25\text{ }^\circ\text{C}$

Parameter		Test Conditions	$V_{CC} = 1.5\text{ V}$	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	$V_{CC} = 5\text{ V}$	Unit
			TYP	TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance	$f = 10\text{ MHz}$	22	22	22	23	25	pF

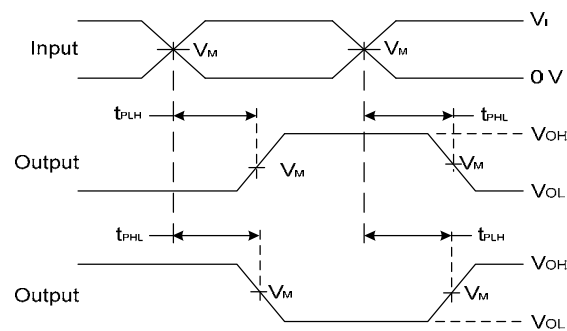
Parameter Measurement Information



V _{CC}	Inputs		V _M	C _L	R _L
	V _I	t _r /t _f			
1.5V±0.10V	V _{CC}	≤2ns	V _{CC} /2	15pF	1MΩ
1.8V±0.15V	V _{CC}	≤2ns	V _{CC} /2	15pF	1MΩ
2.5V±0.2V	V _{CC}	≤2ns	V _{CC} /2	15pF	1MΩ
3.3V±0.3V	3V	≤2.5ns	1.5V	15pF	1MΩ
5V±0.5V	V _{CC}	≤2.5ns	V _{CC} /2	15pF	1MΩ



**Voltage Waveform
Pulse Duration**



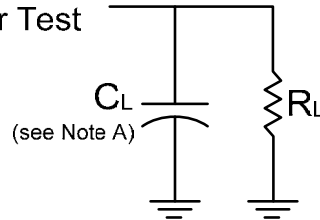
**Voltage Waveform
Propagation Delay Times
Inverting and Non Inverting Outputs**

- Notes:
- Includes test lead and test apparatus capacitance.
 - All pulses are supplied at pulse repetition rate ≤ 10 MHz.
 - Inputs are measured separately one transition per measurement.
 - t_{PLH} and t_{PHL} are the same as t_{PD}.

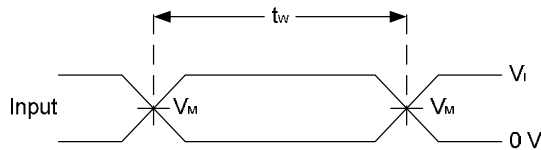
Figure 1. Load Circuit and Voltage Waveforms

Parameter Measurement Information (Continued)

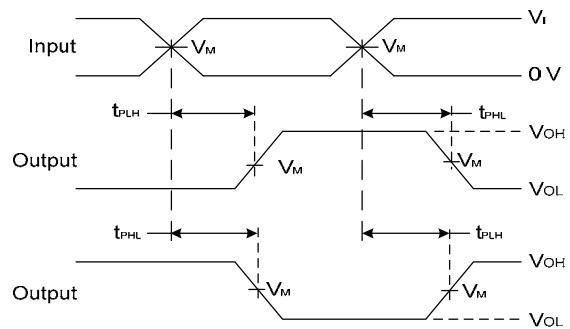
From Output
Under Test



V _{CC}	Inputs		V _M	C _L	R _L
	V _I	t _r /t _f			
1.5V±0.10V	V _{CC}	≤2ns	V _{CC} /2	30pF	1KΩ
1.8V±0.15V	V _{CC}	≤2ns	V _{CC} /2	30pF	1KΩ
2.5V±0.2V	V _{CC}	≤2ns	V _{CC} /2	30pF	500Ω
3.3V±0.3V	3V	≤2.5ns	1.5V	50pF	500Ω
5V±0.5V	V _{CC}	≤2.5ns	V _{CC} /2	50pF	500Ω



**Voltage Waveform
Pulse Duration**



**Voltage Waveform
Propagation Delay Times
Inverting and Non Inverting Outputs**

- Notes:
- A. Includes test lead and test apparatus capacitance.
 - B. All pulses are supplied at pulse repetition rate ≤ 10 MHz.
 - C. Inputs are measured separately one transition per measurement.
 - D. t_{PLH} and t_{PHL} are the same as t_{PD}.

Figure 2. Load Circuit and Voltage Waveforms

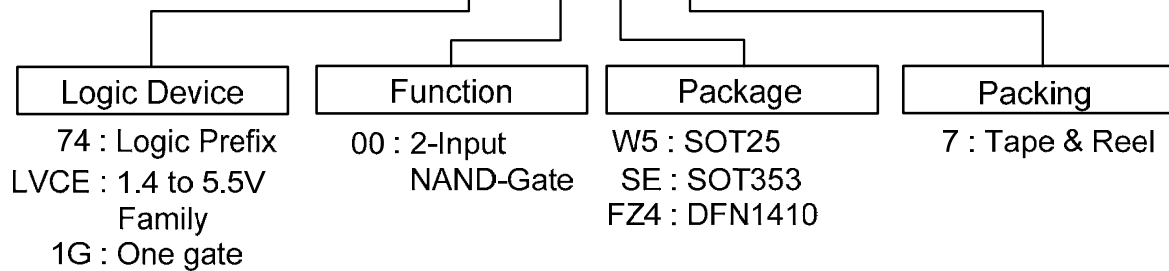


74LVCE1G00

SINGLE 2 INPUT POSITIVE NAND GATE

Ordering Information

74LVCE1G 00 XXX - 7



Device	Package Code	Packaging (Note 5)	7" Tape and Reel	
			Quantity	Part Number Suffix
74LVCE1G00W5-7	W6	SOT25	3000/Tape & Reel	-7
74LVCE1G00SE-7	SE	SOT353	3000/Tape & Reel	-7
74LVCE1G00FZ4-7	FZ4	DFN1410	5000/Tape & Reel	-7

Note: 6. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.

NEW PRODUCT



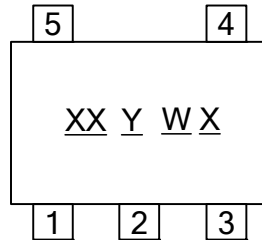
74LVCE1G00

SINGLE 2 INPUT POSITIVE NAND GATE

Marking Information

(1) SOT25 and SOT353

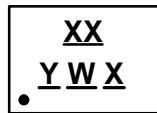
(Top View)

XX : Identification codeY : Year 0~9W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 weekX : A~Z : Internal code

Part Number	Package	Identification Code
74LVCE1G00W5	SOT25	PS
74LVCE1G00SE	SOT353	PS

(3) DFN1410

(Top View)

XX : Identification CodeY : Year : 0~9W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 weekX : A~Z : Internal code

Part Number	Package	Identification Code
74LVCE1G00FZ4	DFN1410	PS

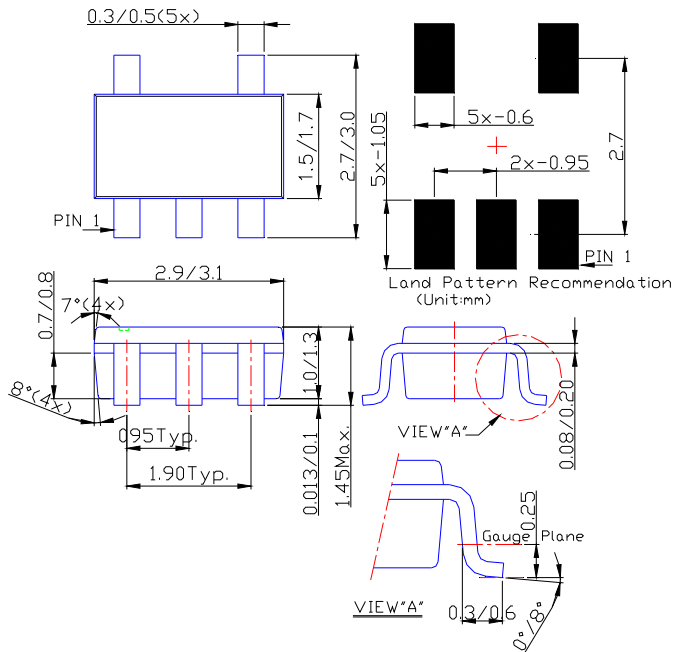


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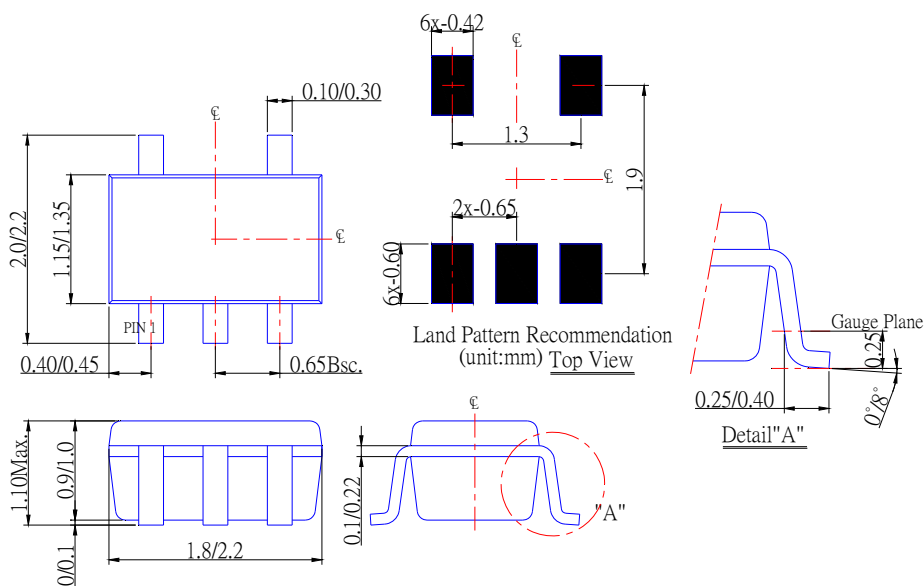
SINGLE 2 INPUT POSITIVE NAND GATE

Package Outline Dimensions (All Dimensions in mm)

(1) Package Type: SOT25



(2) Package Type: SOT353



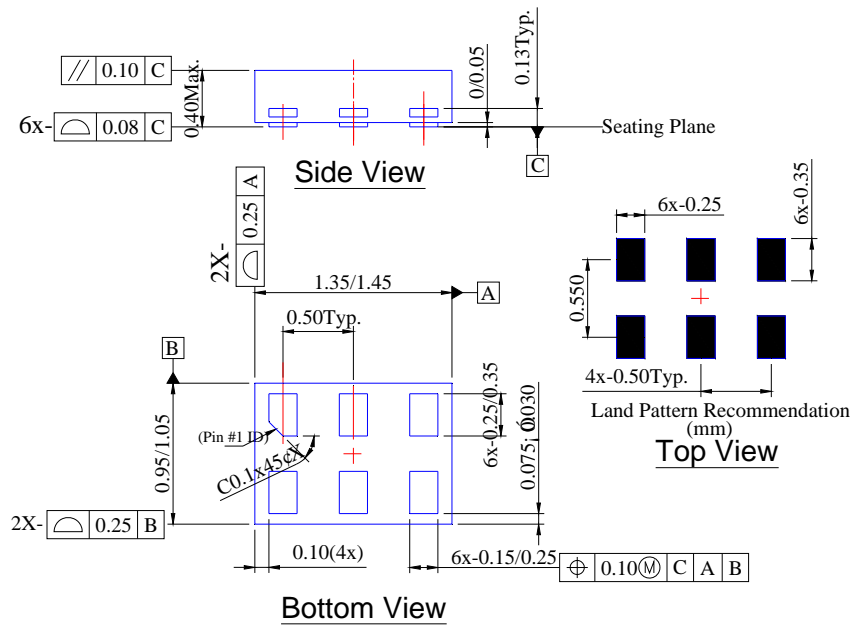


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SINGLE 2 INPUT POSITIVE NAND GATE

Package Outline Dimensions (Continued)

(3) Package Type: DFN1410



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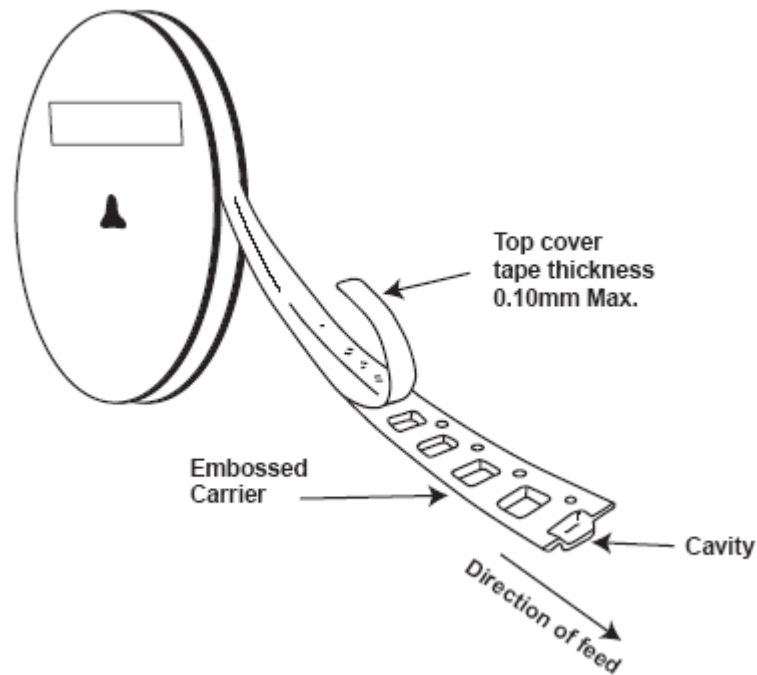
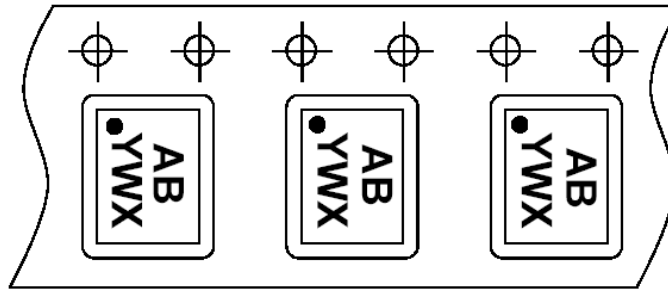


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Taping Orientation (Note 7)

For DFN1410



Note: 7. The taping orientation of the other package type can be found on our website at <http://www.diodes.com/datasheets/ap02007.pdf>



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SINGLE 2 INPUT POSITIVE NAND GATE

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