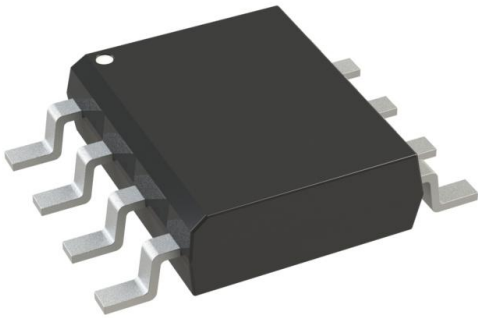


DMP4025LSS-13 Datasheet

www.digi-electronics.com



<https://www.DiGi-Electronics.com>

| | |
|------------------------------|--|
| DiGi Electronics Part Number | DMP4025LSS-13-DG |
| Manufacturer | Diodes Incorporated |
| Manufacturer Product Number | DMP4025LSS-13 |
| Description | MOSFET P-CH 40V 6A 8SO |
| Detailed Description | P-Channel 40 V 6A (Ta) 1.52W (Ta) Surface Mount 8-SO |



Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

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Purchase and inquiry

Manufacturer Product Number:

DMP4025LSS-13

Series:

-

FET Type:

P-Channel

Drain to Source Voltage (Vdss):

40 V

Drive Voltage (Max Rds On, Min Rds On):

4.5V, 10V

Vgs(th) (Max) @ Id:

1.8V @ 250 μ A

Vgs (Max):

\pm 20V

FET Feature:

-

Operating Temperature:

-55°C ~ 150°C (Tj)

Supplier Device Package:

8-SO

Base Product Number:

DMP4025

Manufacturer:

Diodes Incorporated

Product Status:

Active

Technology:

MOSFET (Metal Oxide)

Current - Continuous Drain (Id) @ 25°C:

6A (Ta)

Rds On (Max) @ Id, Vgs:

25mOhm @ 3A, 10V

Gate Charge (Qg) (Max) @ Vgs:

33.7 nC @ 10 V

Input Capacitance (Ciss) (Max) @ Vds:

1640 pF @ 20 V

Power Dissipation (Max):

1.52W (Ta)

Mounting Type:

Surface Mount

Package / Case:

8-SOIC (0.154", 3.90mm Width)

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8541.29.0095

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

40V P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

| $V_{(BR)DSS}$ | $R_{DS(on) \max}$ | $I_D \max (A)$ $T_A = 25^\circ C$ (Notes 6) |
|---------------|---------------------------------|---|
| -40V | 25m Ω @ $V_{GS} = -10V$ | -8.0 |
| | 45m Ω @ $V_{GS} = -4.5V$ | -6.0 |

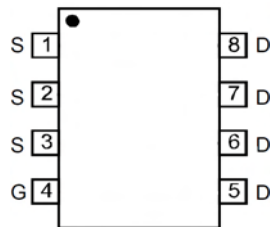
Description and Applications

This MOSFET has been designed to minimize the on-state resistance and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

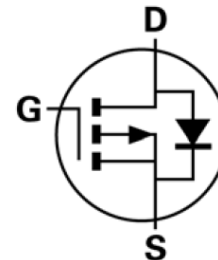
- Motor control
- Backlighting
- DC-DC Converters
- Printer equipment



Top View



Pin-Out Top View



Device symbol

Features and Benefits

- Low $R_{DS(on)}$ – Minimizes conduction losses
- Fast switching speed – Minimizes switching losses
- **Totally Lead-Free & Fully RoHS compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

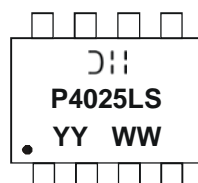
- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0 (Note 1)
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208
- Weight: 0.074 grams (approximate)

Ordering Information (Note 4)

| Product | Marking | Reel size (inches) | Tape width (mm) | Quantity per reel |
|---------------|---------|--------------------|-----------------|-------------------|
| DMP4025LSS-13 | P4025LS | 13 | 12 | 2,500 |

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See <http://www.diodes.com> for more information about Diodes Incorporated's definitions of Halogen and Antimony free, "Green" and Lead-Free.
 3. Halogen and Antimony free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com>

Marking Information



- = Manufacturer's Marking
 P4025LS = Product Type Marking Code
 YYWW = Date Code Marking
 YY = Year (ex: 10 = 2010)
 WW = Week (01 - 53)


Maximum Ratings @ $T_A = 25^\circ\text{C}$ unless otherwise specified

| Characteristic | | | Symbol | Value | Units |
|--|------------------------|------------------------------------|-----------|----------|-------|
| Drain-Source Voltage | | | V_{DSS} | -40 | V |
| Gate-Source Voltage | | | V_{GSS} | ± 20 | |
| Continuous Drain Current | $V_{GS} = -10\text{V}$ | (Notes 6) | I_D | -8.0 | A |
| | | $T_A = 70^\circ\text{C}$ (Notes 6) | | -6.9 | |
| | | (Notes 5) | | -6.0 | |
| Pulsed Drain Current | $V_{GS} = -10\text{V}$ | (Notes 7) | I_{DM} | -30 | |
| Continuous Source Current (Body diode) | | | (Notes 7) | I_S | |
| Pulsed Source Current (Body diode) | | | (Notes 7) | I_{SM} | -30 |

Thermal Characteristics @ $T_A = 25^\circ\text{C}$ unless otherwise specified

| Characteristic | | | Symbol | Value | Unit |
|---|-----------|-----------------|----------------|-------------|--------------------|
| Power Dissipation | (Notes 5) | P_D | | 1.52 | W |
| | (Notes 6) | | | 2.4 | |
| Thermal Resistance, Junction to Ambient | (Notes 5) | $R_{\theta JA}$ | | 82 | $^\circ\text{C/W}$ |
| | (Notes 6) | | | 52 | |
| Thermal Resistance, Junction to Lead | (Notes 8) | $R_{\theta JL}$ | | 48.85 | |
| Operating and Storage Temperature Range | | | T_J, T_{STG} | -55 to +150 | $^\circ\text{C}$ |

- Notes:
5. For a device surface mounted on minimum recommended FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
 6. Same as note (2), except the device is surface mounted on 25mm X 25mm X 1.6mm FR4 PCB.
 7. Repetitive rating on 25mm X 25mm FR4 PCB, $D=0.02$, pulse width 300 μs – pulse width by maximum junction temperature.
 8. Thermal resistance from junction to solder-point (at the end of the drain lead).

Thermal Characteristics

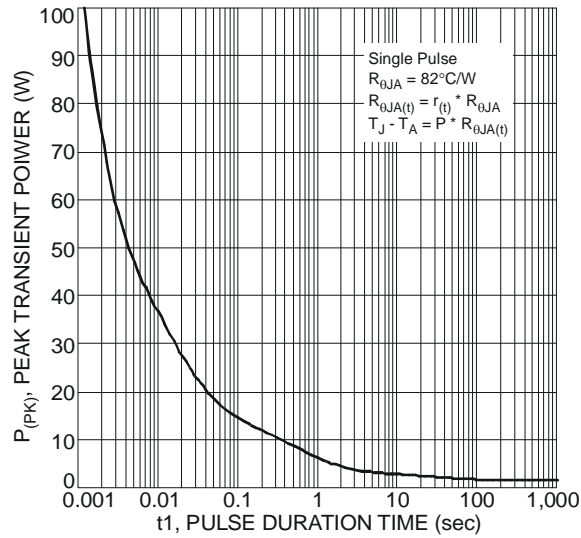


Fig. 1 Single Pulse Maximum Power Dissipation

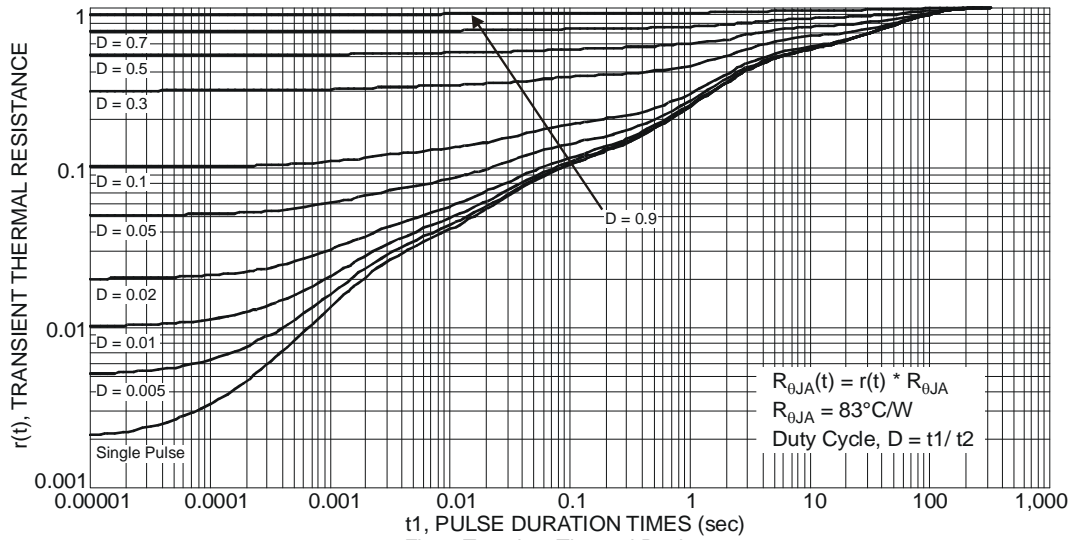


Fig. 2 Transient Thermal Resistance



DMP4025LSS

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise specified

| Characteristic | Symbol | Min | Typ | Max | Unit | Test Condition |
|--|--------------|------|------|-----------|---------------|---|
| OFF CHARACTERISTICS | | | | | | |
| Drain-Source Breakdown Voltage | BV_{DS} | -40 | — | — | V | $I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$ |
| Zero Gate Voltage Drain Current | I_{DSS} | — | — | -1.0 | μA | $V_{DS} = -40\text{V}, V_{GS} = 0\text{V}$ |
| Gate-Source Leakage | I_{GSS} | — | — | ± 100 | nA | $V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$ |
| ON CHARACTERISTICS | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | -0.8 | -1.3 | -1.8 | V | $I_D = -250\mu\text{A}, V_{DS} = V_{GS}$ |
| Static Drain-Source On-Resistance (Note 9) | $R_{DS(ON)}$ | — | 18 | 25 | m Ω | $V_{GS} = -10\text{V}, I_D = -3\text{A}$ |
| | | | 30 | 45 | | $V_{GS} = -4.5\text{V}, I_D = -3\text{A}$ |
| Forward Transconductance (Notes 9 & 10) | g_{fs} | — | 16.6 | — | S | $V_{DS} = -5\text{V}, I_D = -3\text{A}$ |
| Diode Forward Voltage (Note 9) | V_{SD} | — | -0.7 | -1.0 | V | $I_S = -1\text{A}, V_{GS} = 0\text{V}$ |
| DYNAMIC CHARACTERISTICS (Note 10) | | | | | | |
| Input Capacitance | C_{iss} | — | 1640 | — | pF | $V_{DS} = -20\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$ |
| Output Capacitance | C_{oss} | — | 179 | — | | |
| Reverse Transfer Capacitance | C_{rss} | — | 128 | — | | |
| Gate Resistance | R_g | — | 6.43 | — | Ω | $V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$ |
| Total Gate Charge (Note 11) | Q_g | — | 14.0 | — | nC | $V_{GS} = -4.5\text{V}$ $V_{DS} = -20\text{V}$ $I_D = -3\text{A}$ |
| Total Gate Charge (Note 11) | Q_{g1} | — | 33.7 | — | | |
| Gate-Source Charge (Note 11) | Q_{gs} | — | 5.5 | — | | |
| Gate-Drain Charge (Note 11) | Q_{gd} | — | 7.3 | — | | |
| Turn-On Delay Time (Note 11) | $t_{D(on)}$ | — | 6.9 | — | ns | $V_{DD} = -20\text{V}, V_{GS} = -10\text{V}$ $I_D = -3\text{A}$ |
| Turn-On Rise Time (Note 11) | t_r | — | 14.7 | — | | |
| Turn-Off Delay Time (Note 11) | $t_{D(off)}$ | — | 53.7 | — | | |
| Turn-Off Fall Time (Note 11) | t_f | — | 30.9 | — | | |

Notes: 9. Measured under pulsed conditions. Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$
 10. For design aid only, not subject to production testing.
 11. Switching characteristics are independent of operating junction temperatures.

Typical Characteristics

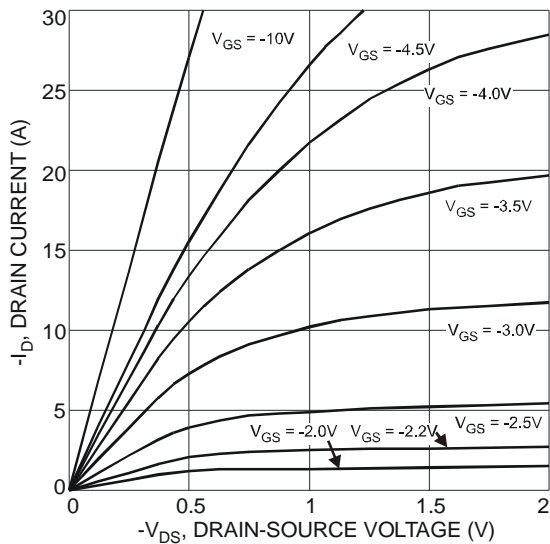


Fig. 3 Typical Output Characteristic

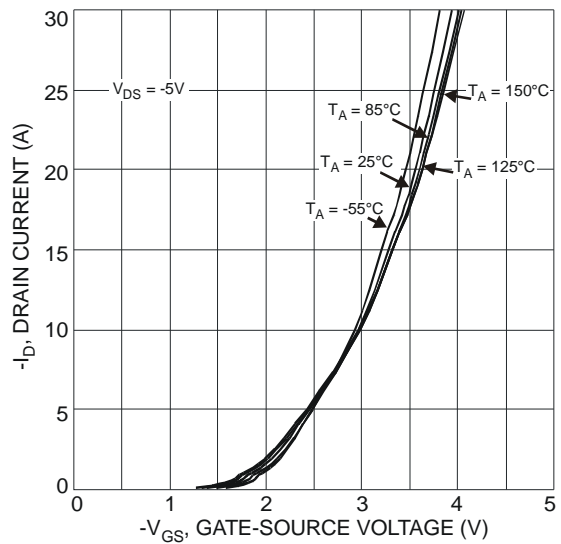


Fig. 4 Typical Transfer Characteristic



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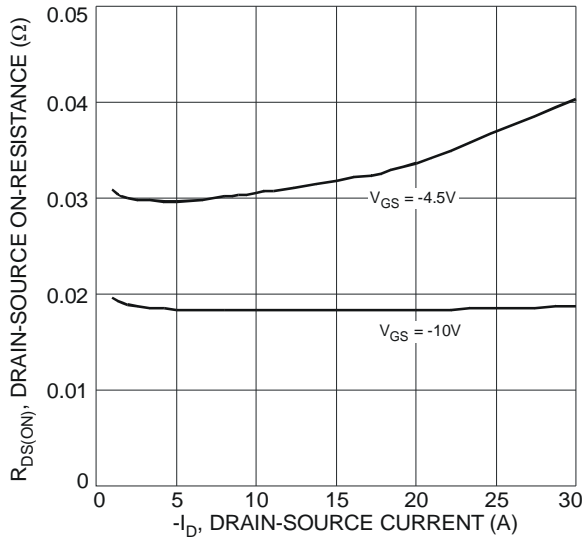


Fig. 5 Typical On-Resistance vs. Drain Current and Gate Voltage

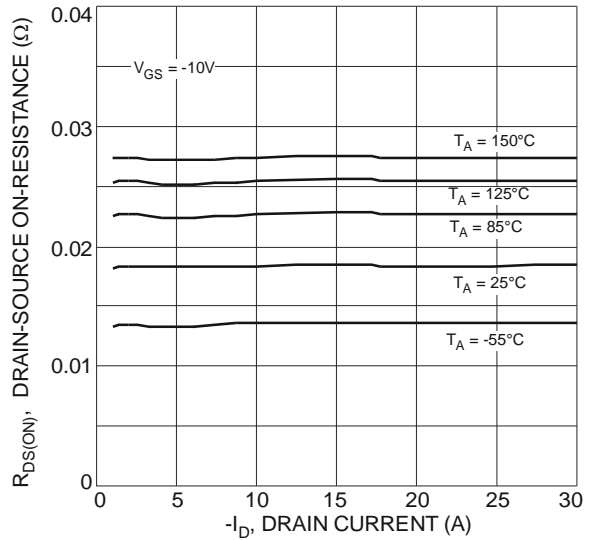


Fig. 6 Typical On-Resistance vs. Drain Current and Temperature

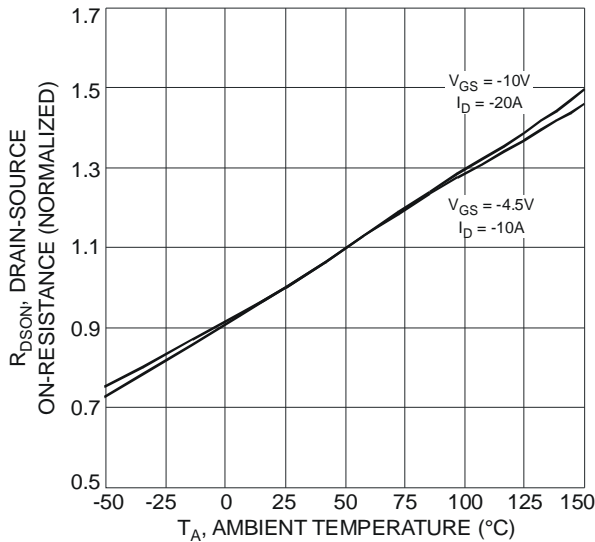


Fig. 7 On-Resistance Variation with Temperature

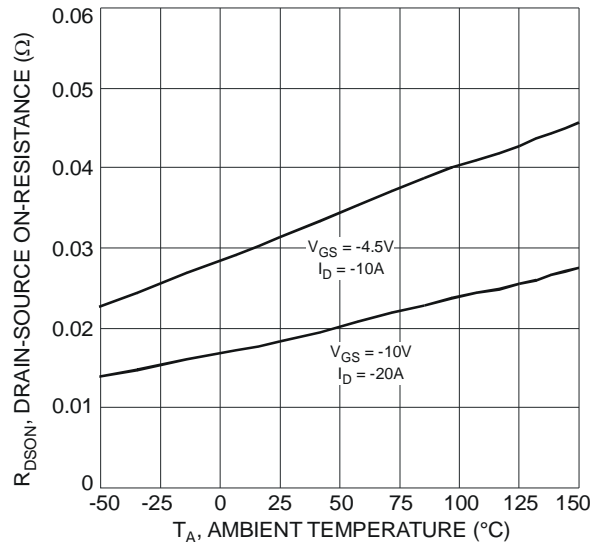


Fig. 8 On-Resistance Variation with Temperature

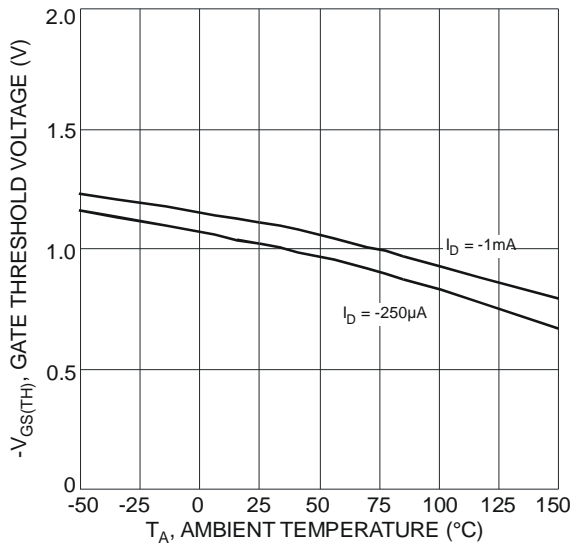


Fig. 9 Gate Threshold Variation vs. Ambient Temperature

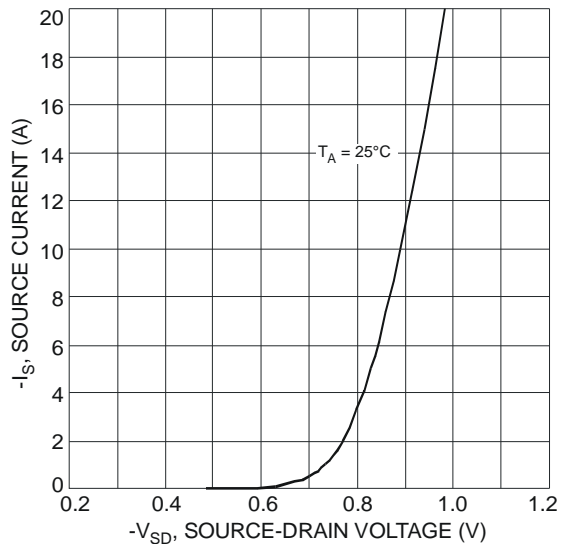
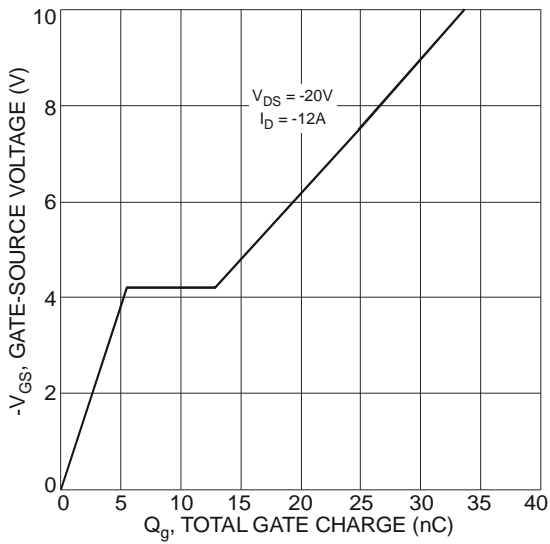
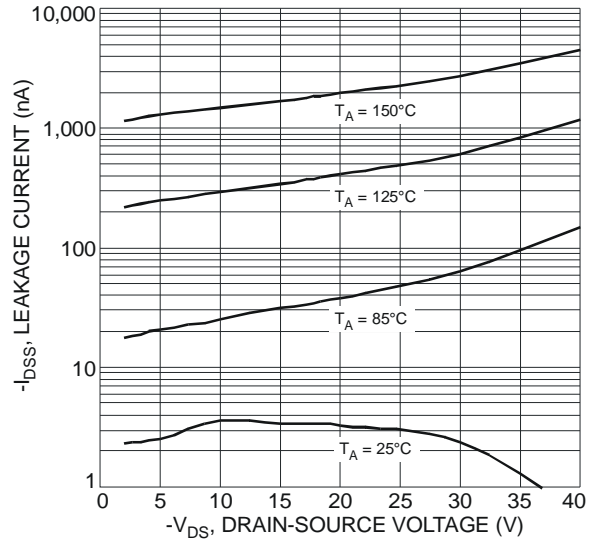
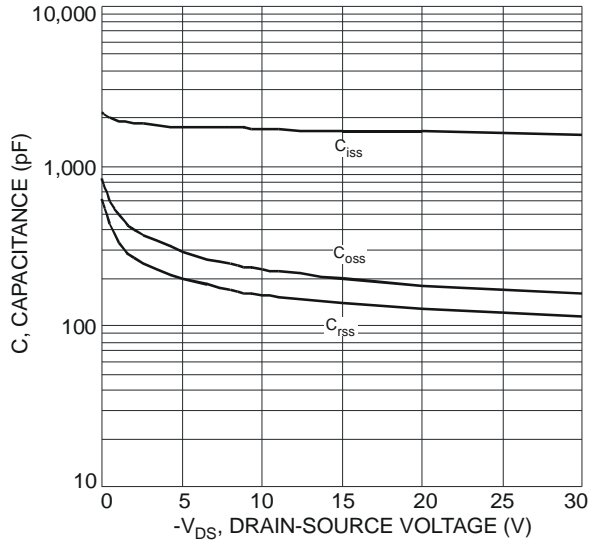


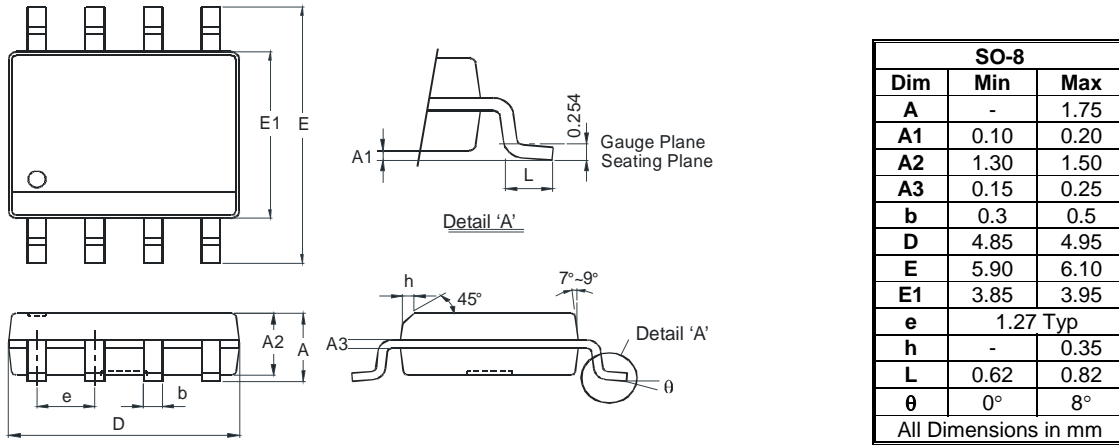
Fig. 10 Diode Forward Voltage vs. Current

DMP4025LSS

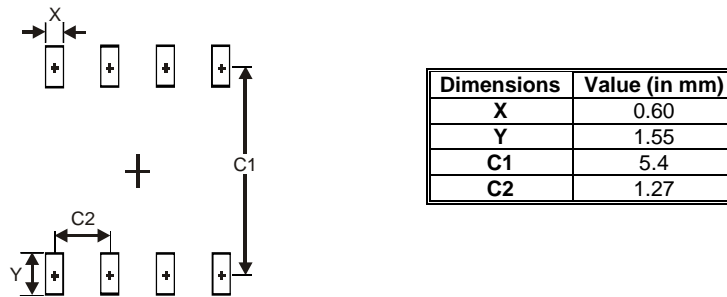


DMP4025LSS

Package Outline Dimensions



Suggested Pad Layout



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