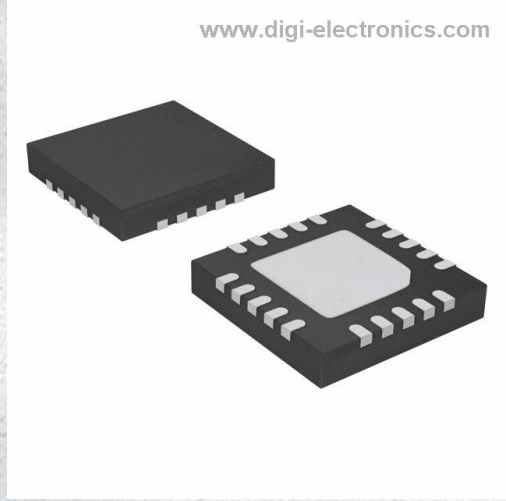
PAM8019KGR Datasheet



DiGi Electronics Part Number	PAM8019KGR-DG
Manufacturer	Diodes Incorporated
Manufacturer Product Number	PAM8019KGR
Description	IC AMP D/AB STER 3W U-QFN4040-20
Detailed Description	Amplifier IC 2-Channel (Stereo) with Stereo Headphones Class D, Class AB U-QFN4040-20

https://www.DiGi-Electronics.com

Tel: +00 852-30501935

RFQ Email: Info@DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
PAM8019KGR	Diodes Incorporated
Series:	Product Status:
-	Active
Type:	Output Type:
Class D, Class AB	2-Channel (Stereo) with Stereo Headphones
Max Output Power x Channels @ Load:	Voltage - Supply:
3W x 2 @ 4Ohm	2.8V ~ 5.5V
Features:	Mounting Type:
Mute, Short-Circuit and Thermal Protection	Surface Mount
Operating Temperature:	Supplier Device Package:
-40°C ~ 85°C (TA)	U-QFN4040-20
Package / Case:	Base Product Number:
20-UFQFN Exposed Pad	PAM8019

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	1 (Unlimited)
REACH Status:	ECCN:
REACH Unaffected	EAR99
HTSUS:	
8542.33.0001	

THE PAM8019 IS NOT RECOMMENDED FOR NEW DESIGNS. PLEASE USE THE PAM8019E.

Lead-free Green

PAM8019

3W STEREO CLASS-D AUDIO AMPLIFIER AND CLASS AB HEADPHONE DRIVER WITH DC VOLUME CONTROL, NON-CLIP POWER LIMIT AND UVP

Description

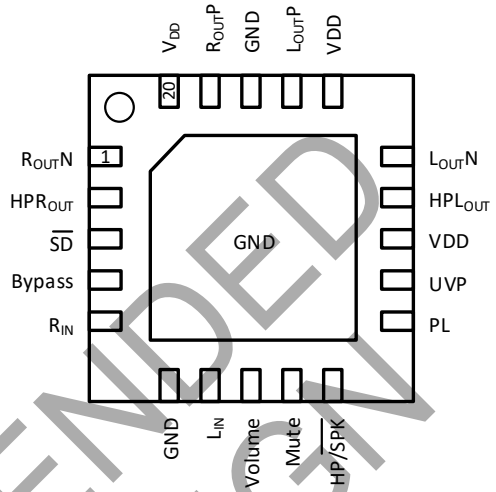
The PAM8019 is a Stereo 3W Class D audio power amplifier for driving bridged-tied speakers and includes a Stereo Class AB amplifier for driving headphones. The advanced 64 step DC volume control minimizes external components allowing simple and accurate volume control over the gain range of +20dB (Volume = 0V) to -60dB (Volume = 5V).

Integrated non-clip power limit technology suppresses output automatically with programmable power limit, improving the sound quality and helping to protect the speakers. Programmable undervoltage protection (UVP) can be used to shut down the PAM8019 at a pre-determined voltage level helping to eliminate speaker pop by shutting down before the power supply collapses.

The PAM8019 is available in the power efficient and space saving U-QFN4040-20 package.

Pin Assignments

Top View



Features

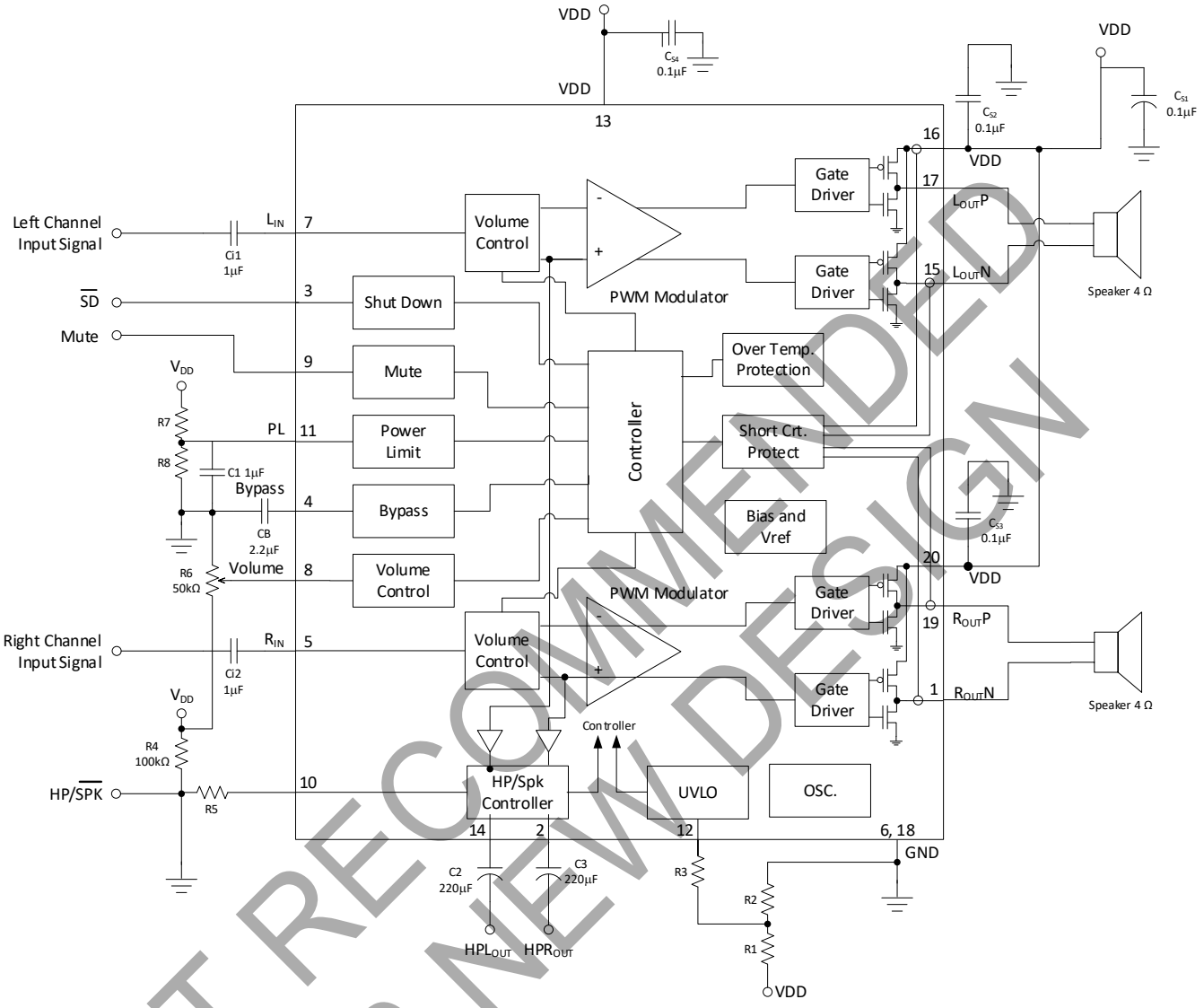
- 3W Stereo Class D Amplifier with Class AB Headphone Amplifier
- Filter Free and Low EMI Architecture
- Operating Voltage: 2.8V to 5.5V
- Low Quiescent Current of 7mA at a V_{DD} of 5V
- 64 Step DC Volume Control with Hysteresis from -60dB to +20dB
- Output Power
  - Class D Amplifier THD+N = 1%
    V_{DD} = 5V, Load = 4Ω; P_O = 2.4W / Load = 8Ω; P_O = 1.4W
  - Class D Amplifier THD+N = 10%
    V_{DD} = 5V, Load = 4Ω; P_O = 3.0W / Load = 8Ω; P_O = 1.7W
  - Class AB Headphone Amplifier
    V_{DD} = 5V, Load = 32Ω; P_O = 60mW
- Speaker or Headphone Select
- Non-Clip Power Limit (NCPL) Function
- OVP and Programmable UVP Protection
- Thermal and Overcurrent Protection with Auto-Recovery
- Power Enhance Package U-QFN4040-20
- Lead Free and Green Devices Available (RoHS Compliant)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Applications

- LCD monitors and TVs
- Projectors/All-in-one computers
- Portable/active speakers
- Portable DVD players/Game machines

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

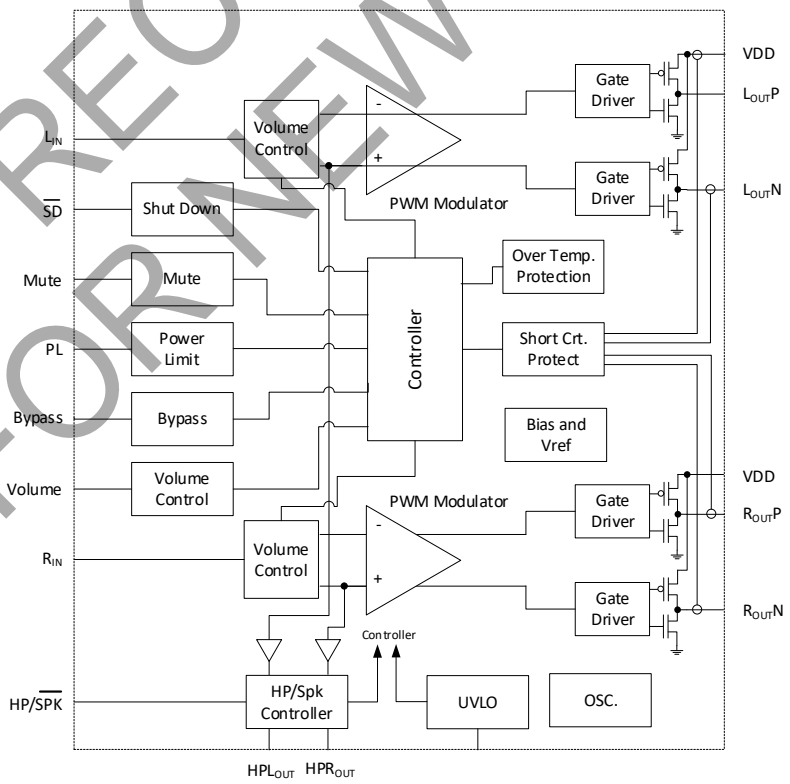
Typical Applications Circuit



Pin Descriptions

Pin Number	Pin Name	Function
3	$\overline{SD}$	Full Chip Shutdown Control Input (Active Low)
4	Bypass	Bias Voltage for Power Amplifier
5	R_{IN}	Negative Input of Right Channel Power Amplifier
6, 18	GND	Ground Connection
7	L_{IN}	Negative Input of Left Channel Power Amplifier
8	Volume	Internal Gain Setting Input Connect to VDD which Set Max. Gain = +20dB
9	Mute	Mute Control Signal Input (Active High)
10	HP/$\overline{SPK}$	Output Mode Control Input High for Headphone Mode and Low for Speaker Mode
11	PL	Power Limit Reference Voltage, see *Application Information* section for further details
12	UVP	Undervoltage Protection Input See *Application Information* section for further details
13, 16, 20	VDD	Supply Voltage
14	HPL_{OUT}	Headphone – Left Channel Output
2	HPR_{OUT}	Headphone – Right Channel Output
15	$L_{OUT}N$	Power Amplifier – Left Channel Negative Output
17	$L_{OUT}P$	Power Amplifier – Left Channel Positive Output
19	$R_{OUT}P$	Power Amplifier – Right Channel Negative Output
1	$R_{OUT}N$	Power Amplifier – Right Channel Positive Output
PAD	GND	Connect to ground (recommended) or No Connect.

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.) (Note 4)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage V_{DD}	-0.3 to 6.0	V
V_{IN}	Input Voltage L_{IN}, R_{IN}, $\overline{SD}$, Mute, HP/$\overline{SPK}$	-0.3 to V_{DD} + 0.3	
T_J	Maximum Junction Temperature	+150	°C
T_{STG}	Storage Temperature Range	- 65 to +150	
T_{SDR}	Maximum Soldering Temperature Range, 5 Seconds	+300	

Note: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability.

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter		Max	Unit
V_{DD}	Supply Voltage Range		2.8 to 5.5	V
V_{IH}	High-Level Threshold Voltage	$\overline{SD}$, Mute	2 to V_{DD}	V
		HP/$\overline{SPK}$	0.8 x V_{DD} to V_{DD}	V
V_{IL}	Low-Level Threshold Voltage	$\overline{SD}$, Mute	0 to 0.8	V
		HP/$\overline{SPK}$	0 to 1.0	V
V_{ICM}	Common Mode Input Voltage		1 to V_{DD} - 1	V
T_A	Ambient Operation Temperature Range		-40 to +85	°C
T_J	Junction Temperature Range		-40 to +125	

Thermal Information (@T_A = +25°C, unless otherwise specified.)

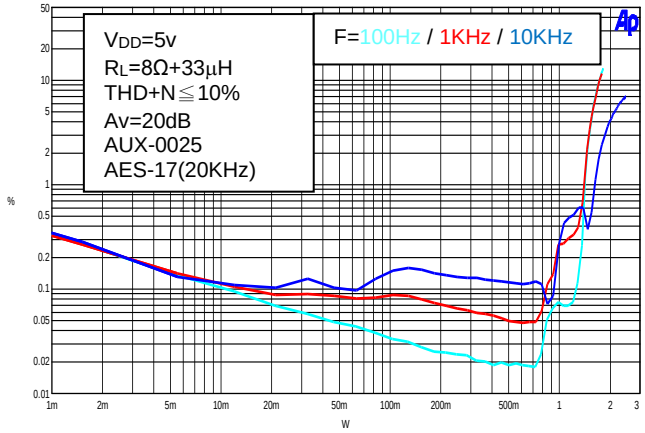
Symbol	Parameter		Typical Value	Unit
θ_{JA}	Thermal Resistance – Junction to Ambient	U-QFN4040-20	45	°C/W
θ_{JC}	Ambient Operation Temperature Range	U-QFN4040-20	7	°C/W

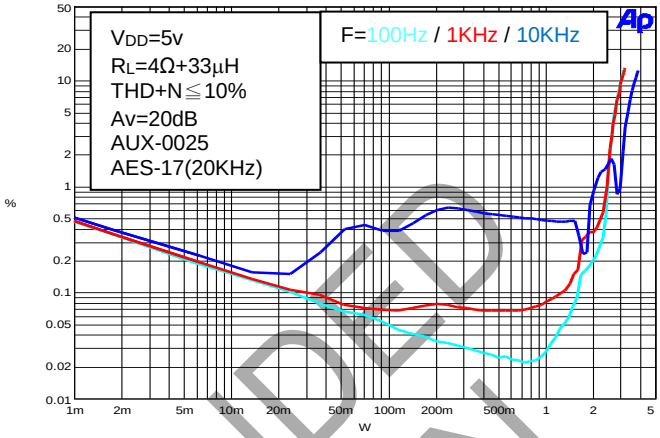
Electrical Characteristics (@T_A = +25°C, V_{DD} = 5V, Gain = Max., R_L = 8Ω, unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD}	Supply Voltage Range	—	2.8	—	5.5	V
Speaker Mode						
I_Q	Quiescent Current (BTL)	V_{MUTE} = 0, V_{SD} = 5V, No Load	—	7	—	mA
I_Q	Quiescent Current (SE)	V_{MUTE} = 0, V_{SD} = 5V, No Load	—	4	—	mA
I_{MUTE}	Mute Current (BTL)	V_{MUTE} = 0, V_{SD} = 5V, No Load	—	3	—	mA
I_{MUTE}	Mute Current (SE)	V_{MUTE} = 0, V_{SD} = 5V, No Load	—	4	—	mA
I_{SD}	Shutdown Current	V_{MUTE} = 0, V_{SD} = 0V, No Load	—	—	1	μA
f_{OSC}	Oscillator Frequency	—	200	250	300	kHz
RI	Input Resistance (BTL)	Gain = 20dB	—	—	33	kΩ
RI	Input Resistance (SE)	Gain = 3.5dB	—	—	56	kΩ
V_{OS}	Output Offset Voltage	No load	—	10	—	mV
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{DD} = 5.5V, I_{DS} = 0.8A P MOSFET	—	0.26	—	Ω
		V_{DD} = 5.5V, I_{DS} = 0.8A N MOSFET	—	0.19	—	
		V_{DD} = 4.5V, I_{DS} = 0.6A P MOSFET	—	0.28	—	
		V_{DD} = 4.5V, I_{DS} = 0.6A N MOSFET	—	0.21	—	
		V_{DD} = 3.6V, I_{DS} = 0.4A P MOSFET	—	0.29	—	
		V_{DD} = 3.6V, I_{DS} = 0.4A N MOSFET	—	0.21	—	
$t_{START\ UP}$	Startup Time from Shutdown	Bypass Capacitor, C_B = 2.2μF	—	1.72	—	s
P_O	Output Power	THD+N = 10%, f = 1kHz, Rl = 8Ω	1.5	1.7	—	W
		THD+N = 10%, f = 1kHz, Rl = 4Ω	2.8	3.0	—	
THD+N	Total Harmonic Distortion Plus Noise	Rl = 8Ω, Po = 0.8W, f = 1kHz	—	0.08	—	%
		Rl = 4Ω, Po = 1.6W, f = 1kHz	—	0.08	—	
PSRR	Power Supply Ripple Rejection	Input AC-GND, f = 1kHz, V_{PP} = 200mV	—	- 61	—	dB
CS	Channel Separation	V_{DD} = 1W, f = 1kHz	—	-82	—	dB
η	Efficiency	P_O = 1.7W, f = 1kHz, Rl = 8Ω	85	90	—	%
		P_O = 3W, f = 1kHz, Rl = 4Ω	80	88	—	
V_N	Noise	Input AC-GND, A-weighting	—	180	—	μV
		Non A-weighting	—	270	—	μV
SNR	Signal Noise Ratio	f = 20 to 20kHz, THD = 1%	—	83	—	dB
Head Phone Mode						
V_{OS}	Output Offset Voltage	No load	—	2.5	—	V
P_O	Output Power	THD+N = 1%, Rl = 32Ω, f = 1kHz	—	60	—	mW
THD+N	Total Harmonic Distortion Plus Noise	Rl = 32Ω, Po = 50mW, f = 1kHz	—	0.02	—	%
PSRR	Power Supply Ripple Rejection	Input AC-GND, f = 1kHz, V_{PP} = 200mV	—	75	—	dB
CS	Channel Separation	P_O = 1W, f = 1kHz	—	-87	—	dB
V_N	Noise	Input AC-GND, A-weighting	—	74	—	μV
		Non A-weighting	—	58	—	μV
SNR	Signal Noise Ratio	f = 20 to 20kHz, THD = 1%	—	89	—	dB
Control Section						
V_{IH}	$\overline{SD}$ Input High	—	1.4	—	—	V
V_{IL}	$\overline{SD}$ Input Low	—	—	—	0.6	V
V_{MH}	Mute Input High	—	1.4	—	—	V
V_{ML}	Mute Input Low	—	—	—	0.6	V
OTP	Overtemperature Protection	—	—	+150	—	°C
OTH	Overtemperature Hysteresis	—	—	+108	—	°C

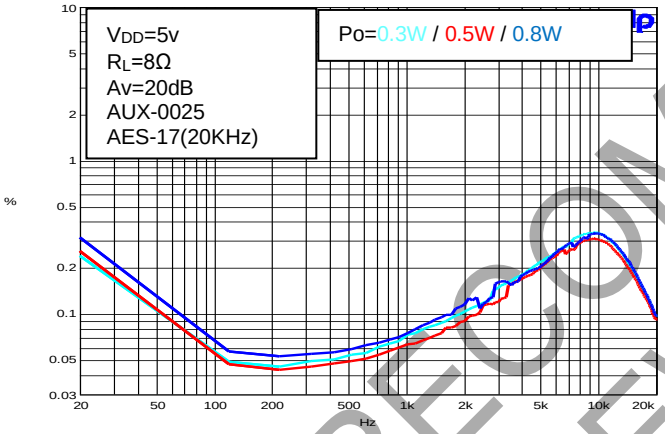
Typical Performance Characteristics

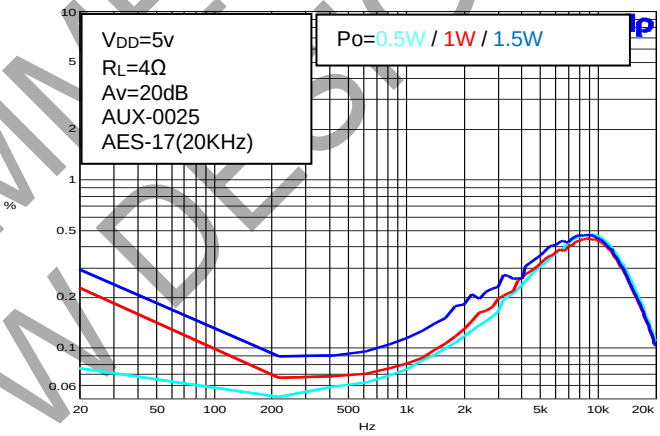
THD+N vs. Output Power - Speaker



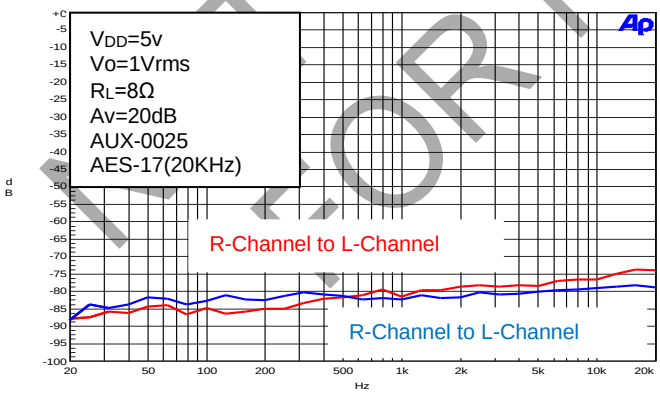


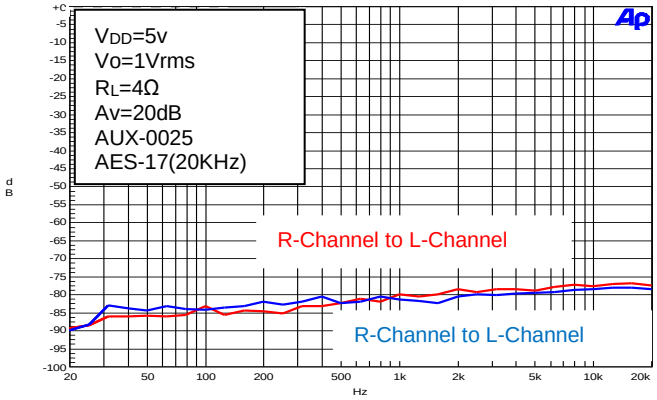
THD+N vs. Frequency - Speaker





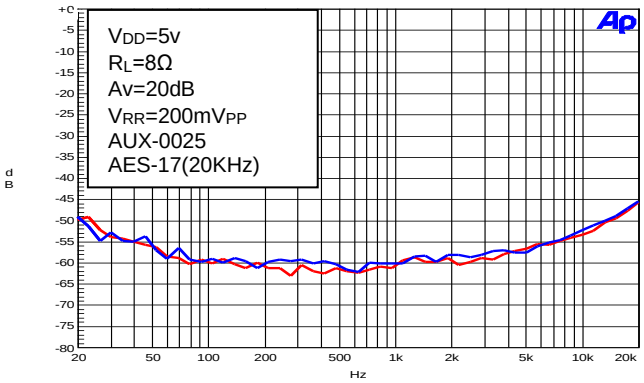
Crosstalk vs. Frequency - Speaker

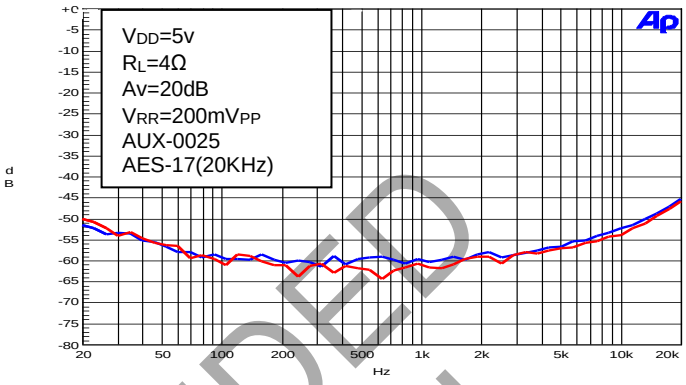




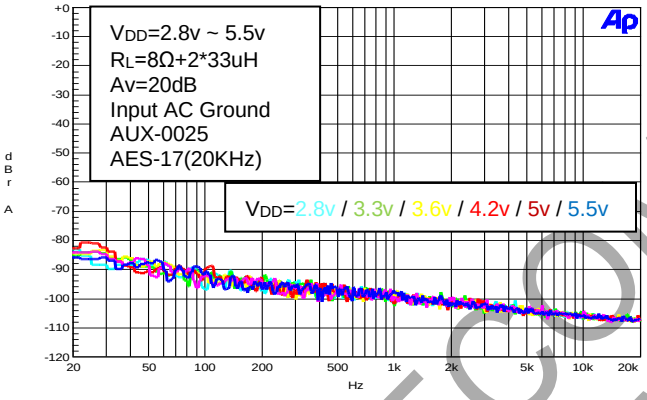
Typical Performance Characteristics (continued)

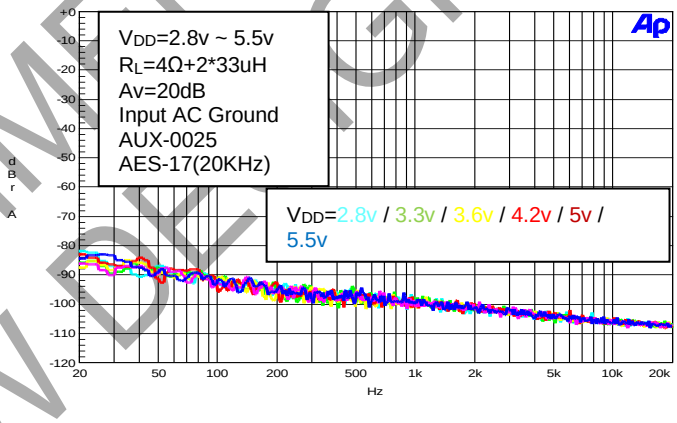
PSRR vs. Frequency





Output Noise vs. Frequency – Speaker





Typical Performance Characteristics (continued)

Table 1. DC Volume Control

Step	DC Volume (V)	Power Amp Gain (dB)	Head Phone Amp Gain (dB)	Step	DC Volume (V)	Power Amp Gain (dB)	Head Phone Amp Gain (dB)
1	0.000 to 0.201	20	3.51	33	2.462 to 2.533	6.7	-7.11
2	0.202 to 0.275	19.6	3.22	34	2.534 to 2.605	6.4	-7.43
3	0.276 to 0.347	19.2	2.94	35	2.606 to 2.678	6	-7.76
4	0.348 to 0.419	18.8	2.66	36	2.679 to 2.751	5.7	-8.09
5	0.420 to 0.491	18.4	2.39	37	2.752 to 2.823	5.3	-8.42
6	0.492 to 0.563	18	2.12	38	2.824 to 2.897	4.9	-8.76
7	0.564 to 0.633	17.6	1.85	39	2.898 to 2.969	4.6	-9.09
8	0.634 to 0.701	17.1	1.46	40	2.970 to 3.043	4.2	-9.43
9	0.702 to 0.771	16.6	1.07	41	3.044 to 3.114	3.8	-9.77
10	0.772 to 0.849	16.1	0.69	42	3.115 to 3.186	3.5	-10.1
11	0.850 to 0.929	15.6	0.32	43	3.187 to 3.259	3.1	-10.46
12	0.930 to 1.005	15.1	-0.05	44	3.260 to 3.332	2.7	-10.81
13	1.006 to 1.079	14.6	-0.41	45	3.333 to 3.403	2.3	-11.16
14	1.080 to 1.153	14.2	-0.77	46	3.404 to 3.476	2	-11.52
15	1.154 to 1.225	13.7	-1.12	47	3.477 to 3.551	1.6	-11.88
16	1.226 to 1.297	13.3	-1.47	48	3.552 to 3.621	1.2	-12.24
17	1.298 to 1.371	12.9	-1.82	49	3.622 to 3.695	0.8	-12.62
18	1.372 to 1.443	12.5	-2.16	50	3.696 to 3.767	0.4	-12.99
19	1.444 to 1.517	12	-2.5	51	3.768 to 3.839	0	-13.38
20	1.518 to 1.589	11.6	-2.84	52	3.840 to 3.909	-1	-14.37
21	1.590 to 1.661	11.2	-3.18	53	3.910 to 3.979	-2.1	-15.42
22	1.662 to 1.733	10.8	-3.51	54	3.980 to 4.045	-3	-16.3
23	1.734 to 1.807	10.5	-3.84	55	4.046 to 4.116	-5	-18.23
24	1.808 to 1.879	10.1	-4.17	56	4.117 to 4.195	-7	-20.16
25	1.880 to 1.951	9.7	-4.5	57	4.196 to 4.273	-9	-22.08
26	1.952 to 2.025	9.3	-4.82	58	4.274 to 4.347	-10.9	-23.96
27	2.026 to 2.097	8.9	-5.16	59	4.348 to 4.421	-17	-30.01
28	2.098 to 2.169	8.6	-5.48	60	4.422 to 4.493	-22.8	-35.83
29	2.170 to 2.243	8.2	-5.8	61	4.494 to 4.565	-29	-41.98
30	2.244 to 2.315	7.8	-6.13	62	4.566 to 4.637	-33.5	-46.46
31	2.316 to 2.389	7.5	-6.45	63	4.638 to 4.708	-39.5	-52.58
32	2.390 to 2.461	7.1	-6.78	64	4.709 to 5.000	-60	-92.95

Application Information

Non-Clip Power Limit (NCPL) Function

When output reaches the maximum power setting value, the NCLP circuits will decrease the gain to prevent the output waveform from clipping helping to prevent speaker damage and maximizing audio performance. The PL pin is used to set and control the NCPL function.

Table 2. NCPL Setting Threshold vs. Output

AGC Function	Output Power
V_{DD} to V_{DD} x 0.45 or PL pin floating	NCPL function disabled
V_{DD} x 0.45 to V_{DD} x 0.27	P_O = [[8(1/2 V_{DD} - VPL)^2] / RI] x 0.95
V_{DD} x 0.27 to GND	P_O = 2.3W (Max. output power 4Ω) P_O = 1.2W (Max. output power 8Ω)

Mute Operation

The Mute pin is an input for controlling the Class-D output state of the PAM8019. A logic low on this pin enables the outputs and logic high on this pin disables the outputs. This pin may be used to quickly disable or enable the outputs without a volume fade. Quiescent current is listed in the *Electrical Characteristic* table. The Mute pin can be left floating due to the internal pulldown.

Shutdown Operation

In order to reduce power consumption while not in use, the PAM8019 contains shutdown circuit to turn off the amplifier's bias circuit. The amplifier is turned off when logic low is placed on the $\overline{SD}$ pin. The $\overline{SD}$ pin can be left floating due to the internal pullup.

Undervoltage Protection

External undervoltage detection can be used to shut down the PAM8019 before an input device can generate a pop. The shutdown threshold at the UVP pin is 1.2V. The user selects a resistor divider to obtain the shutdown threshold and hysteresis for the specific application.

The threshold can be determined as below:
With the condition: R3 >> R1//R2

VUVP = [1.2-(6μA x R3)] x (R1+R2) / R2
Hysteresis = 5μA x R3 x (R1+R2) / R2

Power Supply Decoupling

The PAM8019 is a high-performance CMOS audio-amplifier that requires adequate power supply decoupling to ensure the THD and PSRR are as low as possible. Power supply decoupling also prevents oscillation caused by long leads between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. A good Low-Equivalent-Series-Resistance (ESR) ceramic-capacitor of typically 0.1μF is recommended to be placed as close as possible to the V_{DD} pin to filter the higher frequency transients, spikes or digital hash on the line. Filtering lower-frequency noise signals a large capacitor of 10μF or greater should be placed near the audio amplifier.

Input Capacitor (CI)

It is desirable to use a large input capacitor but in applications where the speaker lacks the ability to reproduce signals below 100Hz to 150Hz it may be possible to minimize CI without effecting system performance. Input Capacitor (CI) and Input Resistance (RI) of the amplifier form a high-pass filter with the corner frequency determined equation below:

$$fc = 1 / 2\pi RI \times CI$$

In addition to system cost and size, click and pop performance is affected by the size of the coupling capacitors. A larger in/out coupling capacitor requires more charge to reach its quiescent DC voltage (Normally 1/2 V_{DD}). This charge comes from the internal circuit via the feedback and is more likely to create pops upon device enable. Minimizing the capacitor size based on necessary low frequency response can minimize the turn on pop.

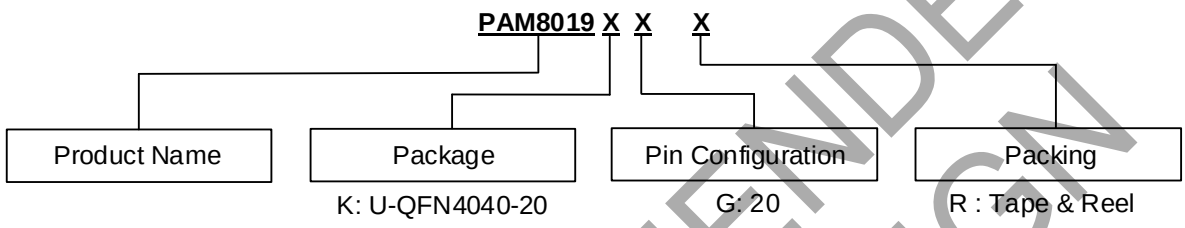
Application Information (continued)

Bypass Capacitor (C_{BYP})

Bypass Capacitor (C_{BYP}) is the most critical capacitor and serves several important functions. During startup or recovery from shutdown mode, C_{BYP} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output signal. The noise is from the internal analog reference to the amplifier, which appears as degraded PSRR and THD+N.

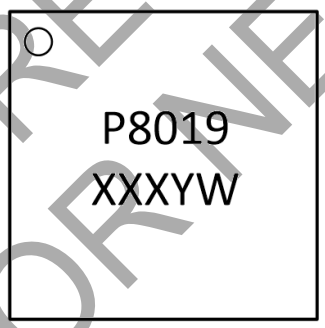
A ceramic bypass capacitor (C_{BYP}) of 0.47µF to 1.0µF is recommended for the best THD and noise performance. Increasing the bypass capacitor reduces clicking and popping noise from power on/off and when entering and leaving shutdown.

Ordering Information



Part Number	Package	Packing	
		Qty.	Carrier
PAM8019KGR	U-QFN4040-20	3000	Tape and Reel

Marking Information

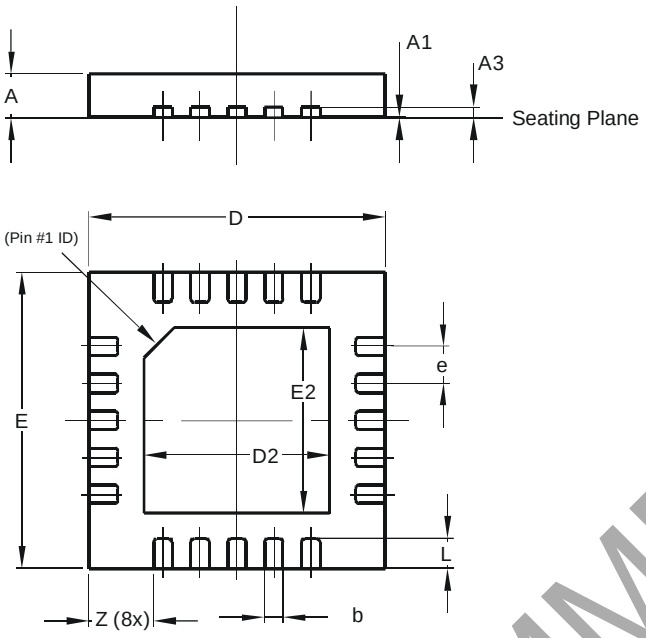


Y: Year
W: Week
X: Internal Code

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-QFN4040-20



U-QFN4040-20			
Dim	**Min**	**Max**	**Typ**
A	0.55	0.65	0.60
A1	0	0.05	0.02
A3	-	-	0.15
b	0.20	0.30	0.25
D	3.95	4.05	4.00
D2	2.40	2.60	2.50
E	3.95	4.05	4.00
E2	2.40	2.60	2.50
e	0.50 BSC		
L	0.35	0.45	0.40
Z	-	-	0.875
All Dimensions in mm			

Suggested Pad Layout

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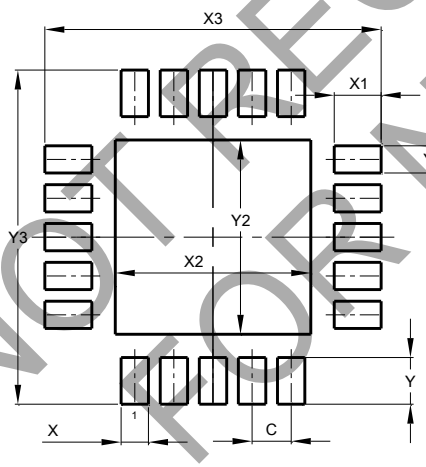

Dimensions	Value (in mm)
C	0.500
X	0.350
X1	0.600
X2	2.500
X3	4.300
Y	0.600
Y1	0.350
Y2	2.500
Y3	4.300

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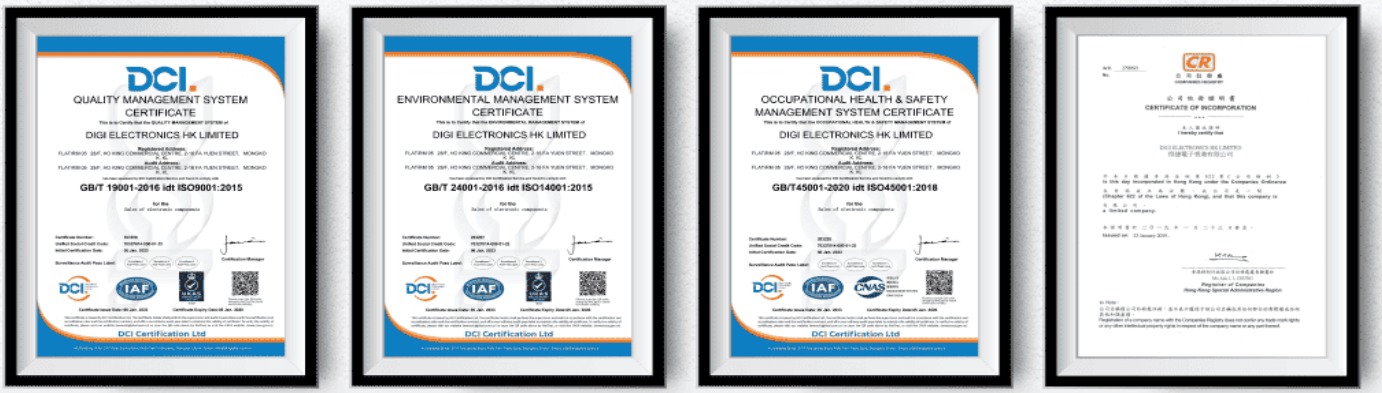

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