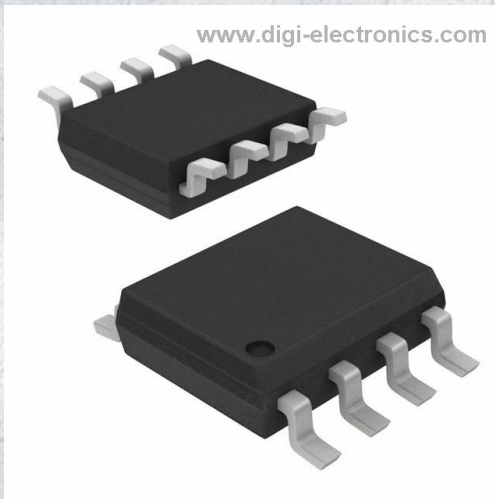


PI6C49X0204BWIE Datasheet



<https://www.DiGi-Electronics.com>

DiGi Electronics Part Number	PI6C49X0204BWIE-DG
Manufacturer	Diodes Incorporated
Manufacturer Product Number	PI6C49X0204BWIE
Description	IC CLK BUFFER 1:4 250MHZ 8SOIC
Detailed Description	Clock Fanout Buffer (Distribution) IC 1:4 250 MHz 8-SOIC (0.154", 3.90mm Width)



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RFQ Email: Info@DiGi-Electronics.com

DiGi is a global authorized distributor of electronic components.

Purchase and inquiry

Manufacturer Product Number:

PI6C49X0204BWIE

Series:

-

Type:

Fanout Buffer (Distribution)

Ratio - Input:Output:

1:4

Input:

LVC MOS, LV TTL

Frequency - Max:

250 MHz

Operating Temperature:

-40°C ~ 85°C (TA)

Package / Case:

8-SOIC (0.154", 3.90mm Width)

Base Product Number:

PI6C49

Manufacturer:

Diodes Incorporated

Product Status:

Active

Number of Circuits:

1

Differential - Input:Output:

No/No

Output:

LVC MOS, LV TTL

Voltage - Supply:

1.6V ~ 3.465V

Mounting Type:

Surface Mount

Supplier Device Package:

8-SOIC

Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99



PI6C49X0204B-A

Low Skew, 1-TO-4 LVC MOS/LVTTL Fanout Buffer

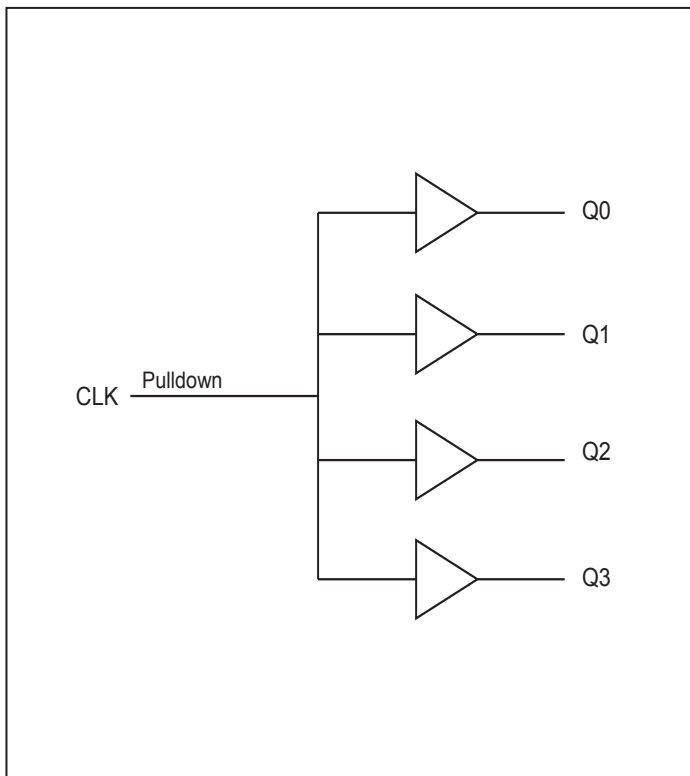
Features

- Four LVC MOS / LVTTL outputs
- LVC MOS / LVTTL clock input
- CLK can accept the following input levels: LVC MOS, LVTTL
- Maximum output frequency: 200MHz
- Additive phase jitter, RMS: 0.06ps (typical) @ 3.3V
- Output skew: 45ps (maximum) @ 3.3V
- Part-to-part skew: 500ps (maximum)
- Small 8 lead SOIC package saves board space
- 3.3V core supply, 3.3V or 2.5V output supply
- 0°C to 70°C ambient operating temperature

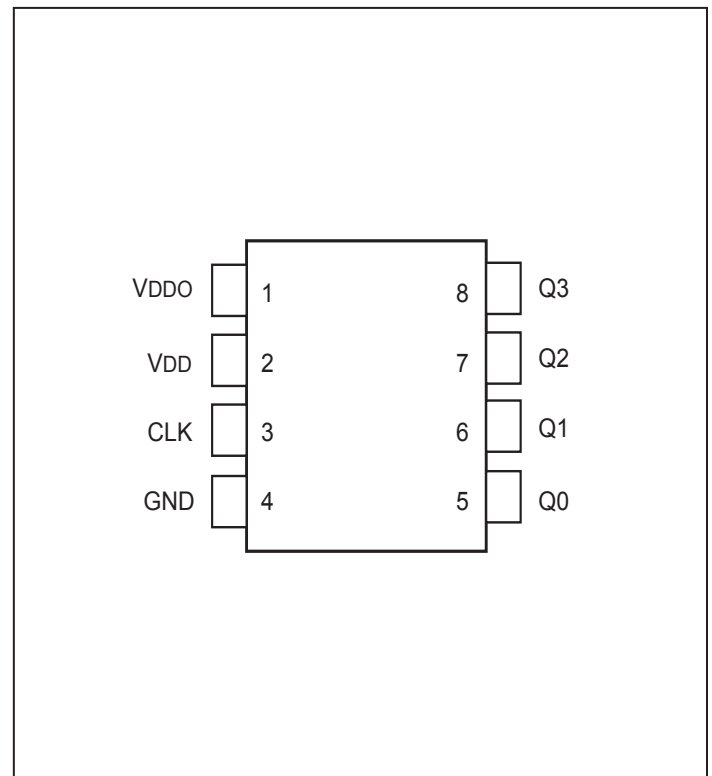
Description

The PI6C49X0204B-A is a low skew, 1-to-4 Fanout Buffer. Guaranteed output and part-to-part skew characteristics make the PI6C49X0204B-A ideal for those clock distribution applications demanding well defined performance and repeatability.

Block Diagram



Pin Assignment



**PI6C49X0204B-A****Low Skew, 1-TO-4 LVCMOS/LVTTL Fanout Buffer****Pin Descriptions**

Pin#	Pin Name	Pin Type		Pin Description
1	V _{DDO}	Power		Output supply pin.
2	V _{DD}	Power		Positive supply pin.
3	CLK	Input	Pulldown	LVCMOS / LVTTL clock input.
4	GND	Power		Power supply ground.
5	Q0	Output		Single clock output. LVCMOS / LVTTL interface levels.
6	Q1	Output		Single clock output. LVCMOS / LVTTL interface levels.
7	Q2	Output		Single clock output. LVCMOS / LVTTL interface levels.
8	Q3	Output		Single clock output. LVCMOS / LVTTL interface levels.

Note: *Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Pin Characteristics

Symbol	Parameter	Test Conditions	Min.	Typical	Max.	Units
C _{IN}	Input Capacitance			4		pF
C _{PD}	Power Dissipation Capacitance (per output)	V _{DD} , V _{DDO} = 3.465V			15	pF
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ
R _{OUT}	Output Impedance	V _{DD} , V _{DDO} >2.5V	5	7	12	Ω

**Maximum Ratings**

(Above which useful life may be impaired. For user guidelines, not tested.)

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Output, V_O	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, θ_{JA}	112.7°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

Note:

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the DC Characteristics or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 3A. Power Supply DC Characteristics, $T_A = 0^\circ\text{C}$ TO 70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD	Core Supply Voltage	3.3V Operation	3.135	3.3	3.465	V
VDDO	Output Power Supply Voltage	3.3V Supply	3.135	3.3	3.465	V
		2.5V Supply	2.375	2.5	2.625	
I_{DD}	Power Supply Current				22	mA
I_{DDO}	Output Supply Current	25MHz			7	mA
		200MHz			45	mA

**PI6C49X0204B-A****Low Skew, 1-TO-4 LVCMOS/LVTTL Fanout Buffer****LVCMOS / LVTTL DC CHARACTERISTICS, $T_A = 0^\circ\text{C}$ to 70°C**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	
V_{IH}	Input High Voltage	VDD = 3.3V	2.3		VDD+0.3	V	
		VDD = 2.5V	1.7		VDD+0.3		
V_{IL}	Input Low Voltage	VDD = 3.3V	-0.3		0.8	V	
		VDD = 2.5V	-0.3		0.8		
I_{IH}	Input High Current	VDD = $V_{IN} = 3.465\text{V}$			150	μA	
I_{IL}	Input Low Current	VDD = 3.465V, $V_{IN} = 0\text{V}$	-5			μA	
V_{OH}	Output High Voltage	VDDO = 3.3V	50 Ω to VDDO /2	2.6			V
			$I_{OH} = -100\mu\text{A}$	2.9			V
		VDDO = 2.5V	50 Ω to VDDO /2	1.8			V
			$I_{OH} = -100\mu\text{A}$	2.2			V
V_{OL}	Output High Voltage	VDDO = 3.3V	50 Ω to VDDO /2			0.5	V
			$I_{OH} = -100\mu\text{A}$			0.2	V
		VDDO = 2.5V	50 Ω to VDDO /2			0.5	V
			$I_{OH} = -100\mu\text{A}$			0.2	V

**AC CHARACTERISTICS**, VDD = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f _{MAX}	Output Frequency	VDDO = 3.3V			200	MHz
		VDDO = 2.5V			200	
t _{pLH}	Propagation Delay, Low-to-High; NOTE 1	VDDO = 3.3V, f ≤ 200MHz	1.9	2.35	2.8	ns
		VDDO = 2.5V, f ≤ 200MHz	2.3		3.3	
t _{sk(o)}	Output Skew; NOTE 2			25	100	ps
t _{sk(pp)}	Part-to-Part Skew; NOTE 3			250	500	ps
t _r	Output Rise Time NOTE 4	VDDO = 3.3V	280		800	ps
		VDDO = 2.5V	280		850	
t _f	Output Fall Time NOTE 4	VDDO = 3.3V	280		800	ps
		VDDO = 2.5V	280		850	
odc	Output Duty Cycle	VDDO = 3.3V, f ≤ 133MHz	45		55	%
		VDDO = 3.3V, 133MHz < f ≤ 200MHz	40		60	%
		VDDO = 2.5V, f ≤ 133MHz	45		55	%
		VDDO = 2.5V, 133MHz < f ≤ 200MHz	40		60	%
t _{jit}	Additive RMS Jitter	156.25MHz (@12kHz to 20MHz)		0.06		ps
		125MHz (@12kHz to 20MHz)		0.04		ps

Parameters measured at f_{MAX} unless otherwise noted.

NOTE 1: Measured from VDD / 2 of the input to VDDO / 2 of the output.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at VDDO / 2.

NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at VDDO / 2.

NOTE 4: Defined from 20% to 80%



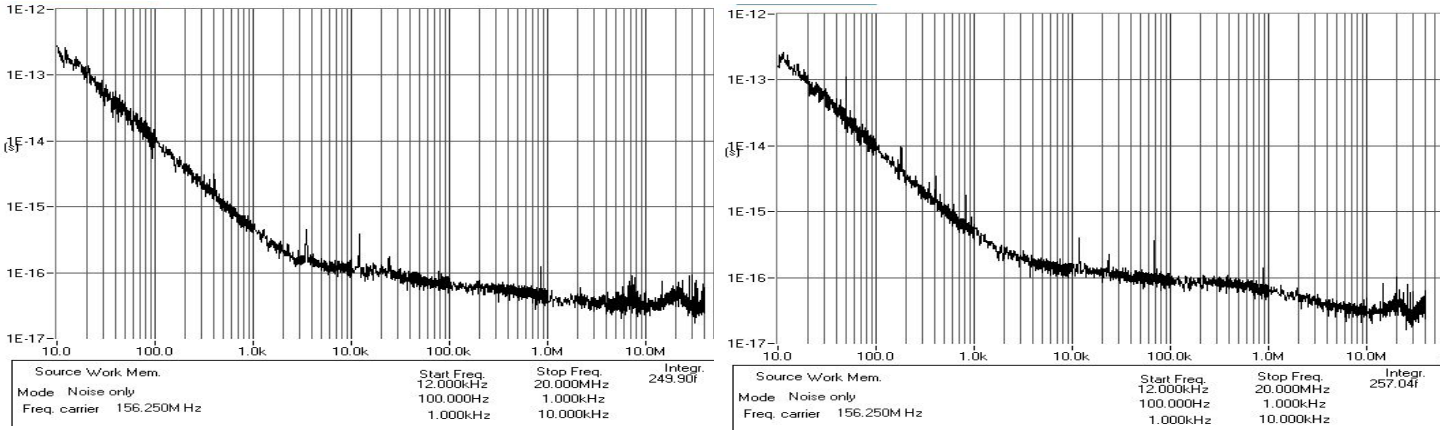
PI6C49X0204B-A

Low Skew, 1-TO-4 LVCMOS/LVTTL Fanout Buffer

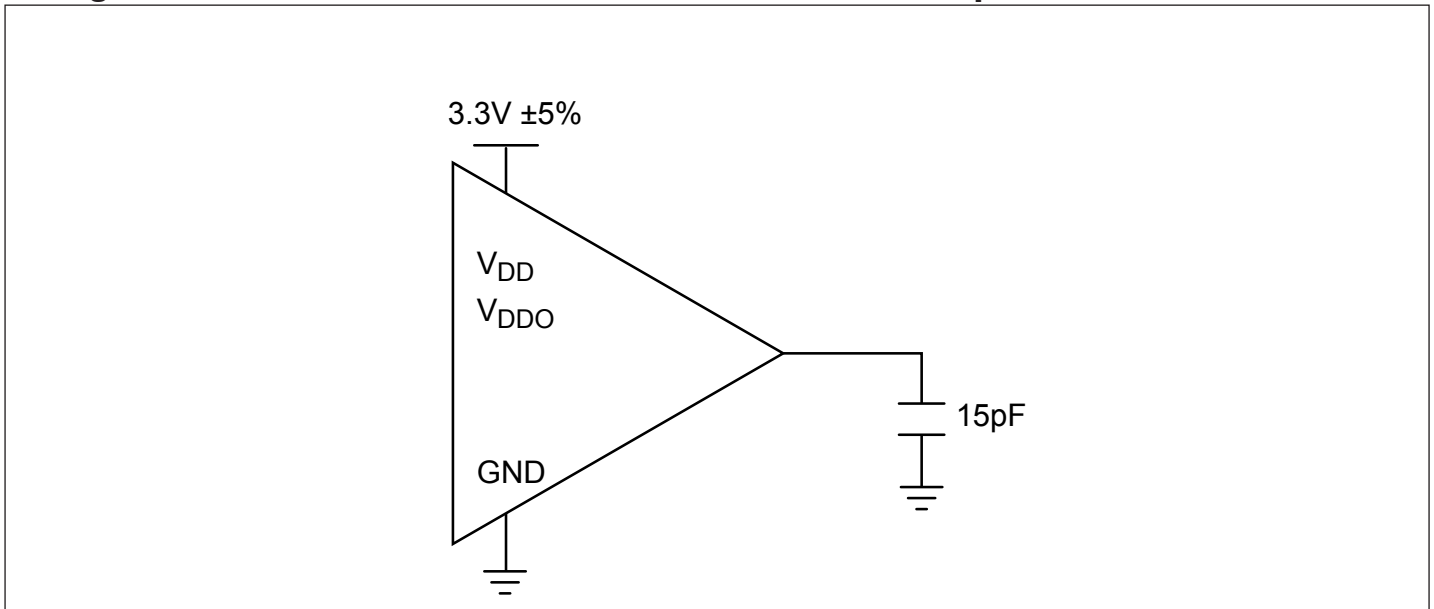
Phase Noise and Additive Jitter

Output phase noise (Right plot) vs Input Phase noise (Left plot)

Additive jitter is calculated at ~60.2fs RMS (12kHz to 20MHz). Additive jitter = $\sqrt{(\text{Output jitter}^2 - \text{Input jitter}^2)}$



Configuration Test Load Board Termination for LVCMOS Outputs



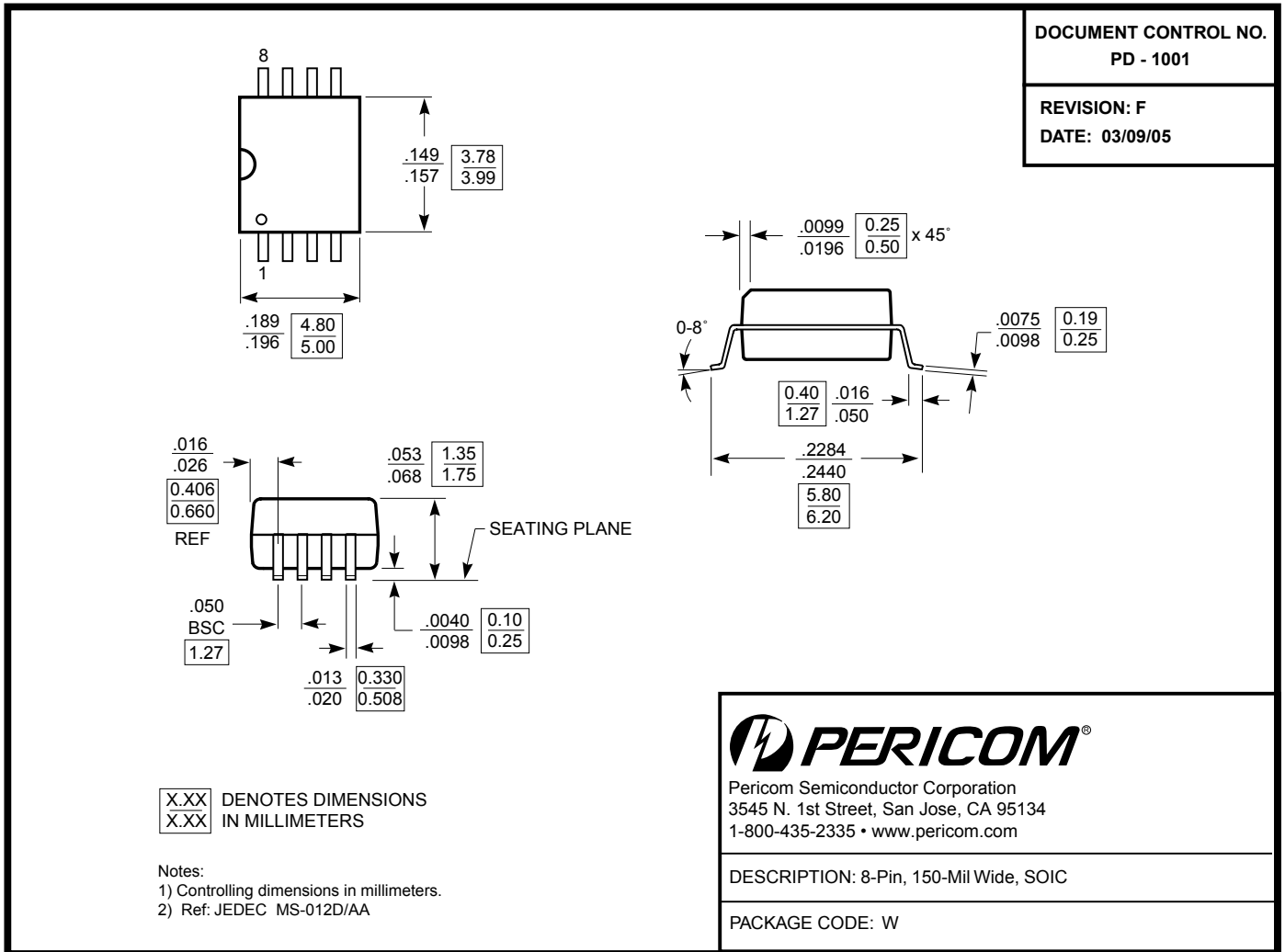
Thermal Information

Symbol	Description	Condition	
θ_{JA}	Junction-to-ambient thermal resistance	Still air	157 °C/W
θ_{JC}	Junction-to-case thermal resistance		42 °C/W



PI6C49X0204B-A

Low Skew, 1-TO-4 LVCMOS/LVTTL Fanout Buffer



Note:

- For latest package info, please check: <http://www.pericom.com/products/packaging/mechanicals.php>

Ordering Information⁽¹⁻³⁾

Ordering Code	Package Code	Package Description
PI6C49X0204B-AWE	W	8-pin, Pb-free & Green, SOIC

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding an X suffix = Tape/Reel

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