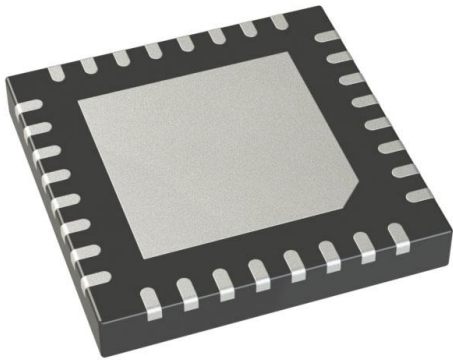


# PI6CG15401ZHIEX Datasheet

[www.digi-electronics.com](http://www.digi-electronics.com)



<https://www.DiGi-Electronics.com>

DiGi Electronics Part Number	PI6CG15401ZHIEX-DG
Manufacturer	<a href="#">Diodes Incorporated</a>
Manufacturer Product Number	PI6CG15401ZHIEX
Description	IC CLOCK GENERATOR 32TQFN
Detailed Description	Clock Generator IC 100MHz 1 32-VFQFN Exposed Pad



Tel: +00 852-30501935

RFQ Email: [Info@DiGi-Electronics.com](mailto:Info@DiGi-Electronics.com)

DiGi is a global authorized distributor of electronic components.

## Purchase and inquiry

Manufacturer Product Number:

PI6CG15401ZHIEX

Series:

-

DiGi-Electronics Programmable:

Not Verified

PLL:

Yes

Output:

CMOS, HCSL

Ratio - Input:Output:

2:8

Frequency - Max:

100MHz

Voltage - Supply:

1.425V ~ 1.575V

Mounting Type:

Surface Mount

Supplier Device Package:

32-TQFN (5x5)

Manufacturer:

Diodes Incorporated

Product Status:

Active

Type:

Clock Generator

Input:

CMOS, Crystal

Number of Circuits:

1

Differential - Input:Output:

No/Yes

Divider/Multiplier:

No/No

Operating Temperature:

-40°C ~ 85°C (TA)

Package / Case:

32-VFQFN Exposed Pad

Base Product Number:

PI6CG15401

## Environmental & Export classification

RoHS Status:

ROHS3 Compliant

REACH Status:

REACH Unaffected

HTSUS:

8542.39.0001

Moisture Sensitivity Level (MSL):

1 (Unlimited)

ECCN:

EAR99

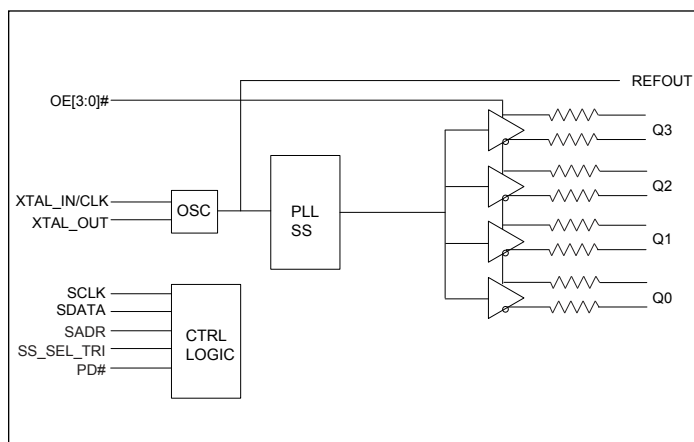

**PI6CG15401**
**Ultra Low Power 4-Output PCIe Clock Generator With On-chip Termination**
**Features**

- 1.5V supply voltage
- Crystal/CMOS input: 25 MHz
- 4 differential low power HCSL outputs with on-chip termination
- Individual output enable
- Reference CMOS output
- Programmable Slew rate and output amplitude for each output
- Differential outputs blocked until PLL is locked
- Selectable 0%, -0.25% or -0.5% spread on differential outputs
- Strapping pins or SMBus for configuration;
- 3.3V tolerant SMBus interface support
- Very low jitter outputs
  - Differential cycle-to-cycle jitter <50ps
  - Differential output-to-output skew <50ps
  - PCIe Gen1/Gen2/Gen3/Gen4 compliant
  - CMOS REFOUT phase jitter is < 1.5ps RMS
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](mailto:contact@diodes.com) or your local Diodes representative.   
<https://www.diodes.com/quality/product-definitions/>
- Packaging (Pb-free & Green):
  - 32-lead 5x5mm TQFN (ZH)

**Description**

The PI6CG15401 is an 4-output ultra low power PCIe Gen1/Gen2/Gen3/Gen4 clock generator. It uses 25MHz crystal or CMOS reference as an input to generate the 100MHz low power differential HCSL outputs with on-chip terminations. The on-chip termination can save 16 external resistors and make layout easier. An additional buffered reference output is provided to serve as a low noise reference for other circuitry.

It uses Diodes proprietary PLL design to achieve very low jitter that meets PCIe Gen1/Gen2/Gen3/Gen4 requirements. It also provides various options such as different slew rate and amplitude through strapping pins or SMBUS so that users can configure the device easily to get the optimized performance for their individual boards. The device also supports selectable spread-spectrum options to reduce EMI for various applications.

**Block Diagram**

**Notes:**

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

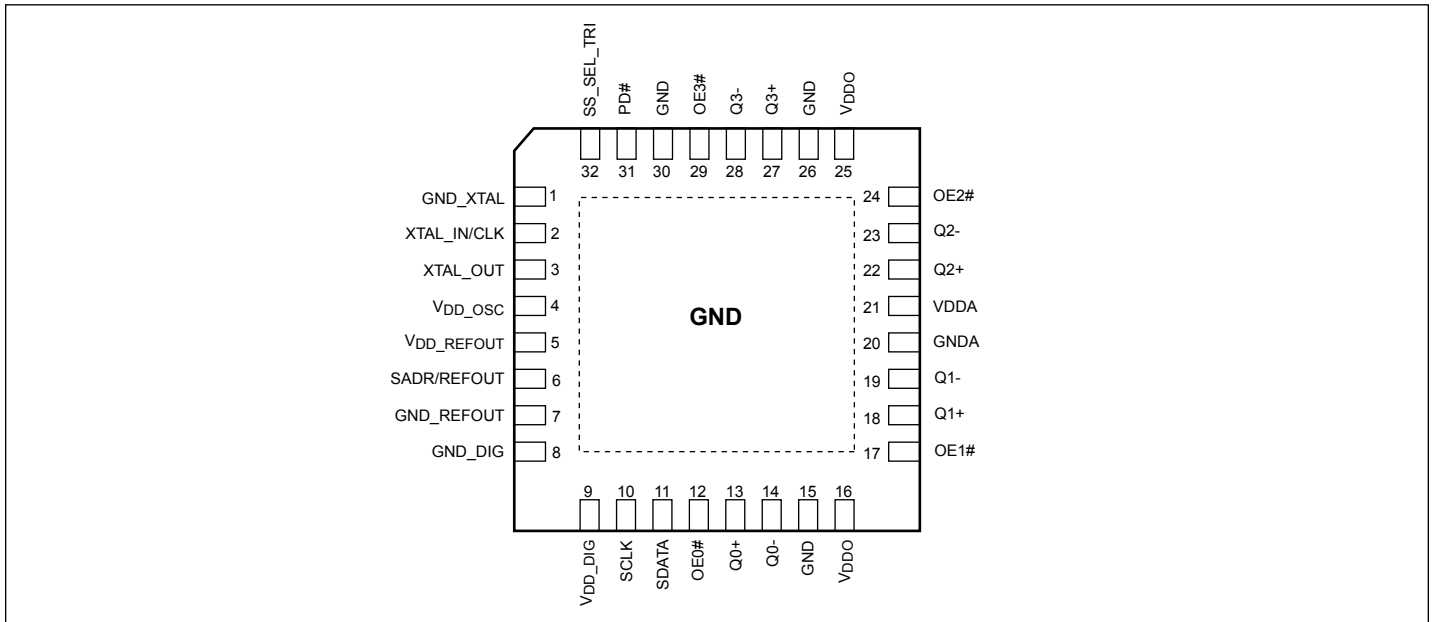


A Product Line of  
Diodes Incorporated



PI6CG15401

## Pin Configuration



## Pin Description

Pin #	Pin Name	Type	Description
1	GND_XTAL	Power	Ground for oscillator circuit
2	XTAL_IN/CLK	Input	Crystal input or CMOS reference input
3	XTAL_OUT	Output	Crystal output
4	VDD_OSC	Power	Power supply for oscillator circuitry, nominal 1.5V
5	VDD_REFOUT	Power	Power supply for buffered CMOS output
6	SADR/REFOUT	Input/ Output	CMOS Latch to select SMBus Address or 1.5V LVCMOS REFOUT. This pin has internal pull-down.
7	GND_REFOUT	Power	Ground for REFOUT
8	GND_DIG	Power	Ground for digital circuitry
9	VDD_DIG	Power	Power supply for digital circuitry, nominal 1.5V
10	SCLK	Input	CMOS SMBUS clock input, 3.3V tolerant
11	SDATA	Input/ Output	CMOS SMBUS Data line, 3.3V tolerant
12	OE0#	Input	CMOS Active low input for enabling Q0 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
13	Q0+	Output	HCSL Differential true clock output
14	Q0-	Output	HCSL Differential complementary clock output
15, 26, 30	GND	Power	Ground
16, 25	VDDO	Power	Power supply for differential outputs



<b>PI6CG15401</b>
-------------------

### Pin Description Cont.

Pin #	Pin Name	Type		Description
17	OE1#	Input	CMOS	Active low input for enabling Q1 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
18	Q1+	Output	HCSL	Differential true clock output
19	Q1-	Output	HCSL	Differential complementary clock output
20	GNDA	Power		Ground for analog circuitry
21	V <sub>DDA</sub>	Power		Power supply for analog circuitry
22	Q2+	Output	HCSL	Differential true clock output
23	Q2-	Output	HCSL	Differential complementary clock output
24	OE2#	Input	CMOS	Active low input for enabling Q2 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
27	Q3+	Output	HCSL	Differential true clock output
28	Q3-	Output	HCSL	Differential complementary clock output
29	OE3#	Input	CMOS	Active low input for enabling Q3 pair. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
31	PD#	Input	CMOS	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.
32	SS_SEL_TRI	Input	Tri-level	Latched select input to select spread spectrum amount at initial power up 1 = -0.5% spread, M = -0.25%, 0 = Spread Off

### SMBus Address Selection Table

	SADR	Address	+Read/Write Bit
State of SADR on first application of PD#	0	1101000	X
	1	1101010	X

### Power Management Table

PD#	SMBus OE bit	OEn#	Qn+	Qn-	REFOUT
0	X	X	Low	Low	HiZ
1	1	0	Running	Running	Running
1	1	1	Low	Low	Low
1	0	X	Low	Low	Low



A Product Line of  
Diodes Incorporated



PI6CG15401

## Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature.....	-65°C to +150°C
Junction Temperature.....	up to +125°C
Supply Voltage to Ground Potential, $V_{DDxx}$ .....	-0.5V to +2.0V
Input Voltage .....	-0.5V to $V_{DD}+0.5V$ , not exceed 2.0V
SMBus, Input High Voltage .....	3.3V
ESD Protection (HBM) .....	2000 V

### Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Operating Conditions

Temperature =  $T_A$ ; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
$V_{DD}, V_{DDA}, V_{DD\_OSC}, V_{DD\_RE-FOUT}, V_{DD\_DIG}$	Power Supply Voltage		1.425	1.5	1.575	V
$V_{DDO}$	Output Power Supply Voltage		1.425	1.5	1.575	V
$I_{DDA}$	Analog Power Supply Current	All outputs active @100MHz		6	9	mA
$I_{DD}$	Power Supply Current	All $V_{DD}$ , except $V_{DDA}$ and $V_{DDO}$ , All outputs active @100MHz		2	4	mA
$I_{DDO}$	Power Supply Current for Outputs	All outputs active @100MHz		21	25	mA
$I_{DDA\_WL}$	Analog Power Supply Wake-on-LAN <sup>(1)</sup> Current	Q outputs off, REF output running		0.4	1	mA
$I_{DD\_WL}$	Power Supply Wake-on-LAN <sup>(1)</sup> Current	All $V_{DD}$ , except $V_{DDA}$ and $V_{DDO}$ , Q outputs off, REF output running		1	2	mA
$I_{DDO\_WL}$	Power Supply Wake-on-LAN <sup>(1)</sup> Current for Outputs	Q outputs off, REF output running		0.04	0.1	mA
$I_{DDA\_PD}$	Analog Power Supply Power Down <sup>(2)</sup> Current	All outputs off		0.4	1	mA
$I_{DD\_PD}$	Power Supply Power Down <sup>(2)</sup> Current	All outputs off		0.4	1	mA
$I_{DDO\_PD}$	Power Supply Current Power Down <sup>(2)</sup> for Outputs	All outputs off			0.1	mA
$T_A$	Ambient Temperature	Industrial grade	-40		85	°C

### Note:

1. Wake-on-LAN mode: PD# = '0' Byte 3, bit 5 = '1'
2. Power down mode: PD# = '0' Byte 3, bit 5 = '0'



A Product Line of  
Diodes Incorporated



PI6CG15401

## Input Electrical Characteristics

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
R <sub>pu</sub>	Internal pull up resistance			120		KΩ
R <sub>dn</sub>	Internal pull down resistance			120		KΩ
C <sub>XTAL</sub>	Internal capacitance on X_IN and X_OUT pins			5		pF
L <sub>PIN</sub>	Pin inductance				7	nH

## Crystal Characteristic

Parameters	Description	Min.	Typ.	Max.	Units
OSCmode	Mode of Oscillation	Fundamental			
FREQ	Frequency		25		MHz
ESR <sup>1</sup>	Equivalent Series Resistance			50	Ω
C <sub>load</sub>	Load Capacitance		8		pF
C <sub>shunt</sub>	Shunt Capacitance			7	pF
	Drive Level			300	uW

### Note:

1. ESR value is dependent upon frequency of oscillation

## SMBus Electrical Characteristics

Temperature = T<sub>A</sub>; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
V <sub>DDSMB</sub>	Nominal bus voltage		1.425		3.3	V
V <sub>IHSMB</sub>	SMBus Input High Voltage	SMBus, V <sub>DDSMB</sub> = 3.3V	2.1		3.3	V
		SMBus, V <sub>DDSMB</sub> < 3.3V	0.65 V <sub>DDSMB</sub>			
V <sub>ILSMB</sub>	SMBus Input Low Voltage	SMBus, V <sub>DDSMB</sub> = 3.3V			0.6	V
		SMBus, V <sub>DDSMB</sub> < 3.3V			0.6	
I <sub>SMBSINK</sub>	SMBus sink current	SMBus, at V <sub>OLSMB</sub>	4			mA
V <sub>OLSMB</sub>	SMBus Output Low Voltage	SMBus, at I <sub>SMBSINK</sub>			0.4	V
f <sub>MAXSMB</sub>	SMBus operating frequency	Maximum frequency			400	kHz
t <sub>RMSB</sub>	SMBus rise time	(Max V <sub>IL</sub> - 0.15) to (Min V <sub>IH</sub> + 0.15)			1000	ns
t <sub>FMSB</sub>	SMBus fall time	(Min V <sub>IH</sub> + 0.15) to (Max V <sub>IL</sub> - 0.15)			300	ns

## Spread Spectrum Characteristic

Temperature = T<sub>A</sub>; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
f <sub>MOD</sub>	SS Modulation Frequency	Triangular modulation	30	31.6	33	kHz



<b>PI6CG15401</b>
-------------------

## LVCMOS DC Electrical Characteristics

Temperature =  $T_A$ ; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
$V_{IH}$	Input High Voltage	Single-ended inputs, except SMBus	0.75 $V_{DD}$		$V_{DD}$ +0.3	V
$V_{IM}$	Input Mid Voltage	SS_SEL_TRI	$0.4V_{DD}$	$0.5V_{DD}$	$0.6V_{DD}$	V
$V_{IL}$	Input Low Voltage	Single-ended inputs, except SMBus	-0.3		0.25 $V_{DD}$	V
$I_{IH}$	Input High Current	Single-ended inputs, $V_{IN} = V_{DD}$			20	$\mu A$
$I_{IL}$	Input Low Current	Single-ended inputs, $V_{IN} = 0V$	-20			$\mu A$
$I_{IH}$	Input High Current	Single-ended inputs with pull up / pull down resistor, $V_{IN} = V_{DD}$			220	$\mu A$
$I_{IL}$	Input Low Current	Single-ended inputs with pull up / pull down resistor, $V_{IN} = 0V$	-220			$\mu A$
$V_{OH}$	Output High Voltage	REFOUT, except SMBus; $I_{OH} = -2mA$	$V_{DD}$ -0.45			V
$V_{OL}$	Output Low Voltage	REFOUT, except SMBus; $I_{OH} = 2mA$			0.45	V
$R_{OUT}$	CMOS Output impedance			20		$\Omega$
$C_{IN}$	Input Capacitance		1.5		5	pF

## LVCMOS AC Characteristics

Temperature =  $T_A$ ; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
$f_{INPUT}$	Input Frequency	XTAL_IN/CLK	23	25	27	MHz
$t_{RIN}$	Input rise time	Single-ended inputs			5	ns
$t_{FIN}$	Input fall time	Single-ended inputs			5	ns
$t_{STAB}$	Clock stabilization	From Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock			1.8	ms
$t_{OELAT}$	Output enable latency	Q start after OE# assertion Q stop after OE# deassertion	1		3	clocks
$t_{PDLAT}$	PD# de-assertion	Differential outputs enable after PD# de-assertion		20	300	us
$t_{PERIOD}$	REFOUT clock period	REFOUT, assume input is at 25MHz		40		ns
$f_{ACC}$	REFOUT frequency accuracy <sup>(1)</sup>	REFOUT, long term accuracy to input		0		ppm
$t_{SLEW}$	REFOUT slew rate <sup>(1)</sup>	Byte 3 = 1F, 20% to 80% of $V_{DDREF}$	0.3	0.7	1.1	V/ns
		Byte 3 = 5F, 20% to 80% of $V_{DDREF}$	0.5	1.0	1.6	V/ns
		Byte 3 = 9F, 20% to 80% of $V_{DDREF}$	0.6	1.3	1.9	V/ns
		Byte 3 = DF, 20% to 80% of $V_{DDREF}$	0.84	1.4	2.0	V/ns



A Product Line of  
Diodes Incorporated

PI6CG15401

## LVCMOS AC Characteristics Cont.

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
t <sub>DC</sub>	REFOUT Duty Cycle <sup>(1)</sup>	V <sub>T</sub> = V <sub>DD</sub> / 2 V, driven by a Xtal	45	50	55	%
t <sub>DCDIS</sub>	REFOUT Duty Cycle Distortion	V <sub>T</sub> = V <sub>DD</sub> / 2 V, driven by an external source	0	2	4	%
t <sub>JITCC</sub>	REFOUT cycle-cycle jitter	V <sub>T</sub> = V <sub>DD</sub> / 2 V, driven by a Xtal		51	250	ps
t <sub>JITPH</sub>	REFOUT phase jitter	12kHz to 5MHz, RMS, driven by a Xtal		1	3	ps
t <sub>JITN</sub>	Noise floor	1kHz offset, driven by a Xtal		-126	-105	dBc
		10kHz offset to Nyquist, driven by a Xtal		-140	-110	dBc

### Note:

1. Guaranteed by design and characterization, not 100% tested in production

## HCSL Output Characteristics

Temperature = T<sub>A</sub>; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
V <sub>OH</sub>	Output Voltage High <sup>(1)</sup>	Statistical measurement on single-ended signal using oscilloscope math function	600	750	900	mV
V <sub>OL</sub>	Output Voltage Low <sup>(1)</sup>		-150		150	mV
V <sub>OMAX</sub>	Output Voltage Maximum <sup>(1)</sup>	Measurement on single ended signal using absolute value		760	1150	mV
V <sub>OMIN</sub>	Output Voltage Minimum <sup>(1)</sup>		-300	20		mV
V <sub>OSWING</sub>	Output Swing Voltage <sup>(1,2,3)</sup>	Scope averaging off	300	1450		mV
V <sub>OC</sub>	Output Cross Voltage <sup>(1,2,4)</sup>		250	400	550	mV
DV <sub>OC</sub>	V <sub>OC</sub> Magnitude Change <sup>(1,2,5)</sup>			14	140	mV

### Note:

1. At default SMBUS amplitude settings

2. Guaranteed by design and characterization, not 100% tested in production

3. Measured from differential waveform

4. This one is defined as voltage where Q+ = Q- measured on a component test board and only applied to the differential rising edge

5. The total variation of all V<sub>cross</sub> measurements in any particular system. This is a subset of V<sub>cross\_min/max</sub> allowed.

## HCSL Output AC Characteristics

Temperature = T<sub>A</sub>; Supply voltages per normal operation conditions; See test circuits for the load conditions

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
f <sub>OUT</sub>	Output Frequency			100		MHz
t <sub>RF</sub>	Slew rate <sup>(1,2,3)</sup>	Scope averaging on fast setting	1.2	2.4	3.6	V/ns
		Scope averaging on slow setting	0.8	1.7	3.0	V/ns
D <sub>tRF</sub>	Slew rate matching <sup>(1,2,4)</sup>	Scope averaging on		3	20	%
t <sub>DC</sub>	Duty Cycle <sup>(1,2)</sup>	Measured differentially, PLL Mode	45	50	55	%
t <sub>SKEW</sub>	Output Skew <sup>(1,2)</sup>	Averaging on, V <sub>T</sub> = 50%		34	50	ps
t <sub>j-c-c</sub>	Cycle to cycle jitter <sup>(1,2)</sup>			15	50	ps
t <sub>STARTUP</sub>	Start up time				10	ms

A Product Line of  
Diodes Incorporated

PI6CG15401

### HC SL Output AC Characteristics Cont.

Symbol	Parameters	Condition	Min.	Typ.	Max.	Units
t <sub>LOCK</sub>	PLL lock time				20	ms
t <sub>JPHASE</sub>	Integrated phase jitter (RMS) (1,5,6)	PCIe Gen 1	27	40	86	ps
		PCIe Gen 2 Low Band, 10kHz < f < 1.5MHz	1.0	1.3	3.0	ps
		PCIe Gen 2 High Band, 1.5MHz < f < Nyquist (50MHz)	1.9	2.2	3.1	ps
		PCIe Gen 3 Common Clock Architecture (PLL BW of 2-4 or 2-5MHz, CDR =10MHz)	0.4	0.6	1.0	ps
		PCIe Gen 3 Separate Reference No Spread (PLL BW of 2-4 or 2-5MHz, CDR =10MHz)	0.4	0.7	0.7	ps
		PCIe Gen 4 (PLL BW of 2-4 or 2-5MHz, CDR =10MHz)	0.3	0.4	0.5	ps

**Note:**

1. Guaranteed by design and characterization, not 100% tested in production
2. Measured from differential waveform
3. Slew rate is measured through the Vswing voltage range centered around differential 0V, within +/-150mV window
4. Slew rate matching is measured using a +/-75mV window centered at differential zero
5. See <http://www.pcisig.com> for complete specs
6. Sample size of at least 100k cycles. This can be extrapolated to 108ps pk-pk @ 1M cycles for a BER of 10<sup>-12</sup>

### Differential Output Clock Periods - Spread Spectrum Disabled

Center Freq. MHz	Measurement Window							Units
	1 clock	1 us	0.1 s	0.1 s	0.1 s	1 us	1 clock	
	-c2c jitter AbsPer Min	- SSC Short-term Avg. Min	-ppm Long-term Avg. min	0 ppm Period Nominal	+ppm Long-term Avg. max	+ SSC Short-term Avg. Max	-c2c jitter AbsPer Max	
100.00	9.94900		9.99900	10.00000	10.00100		10.05100	ns

### Differential Output Clock Periods - Spread Spectrum Enabled

Center Freq. MHz	Measurement Window							Units
	1 clock	1 us	0.1 s	0.1 s	0.1 s	1 us	1 clock	
	-c2c jitter AbsPer Min	- SSC Short-term Avg. Min	-ppm Long-term Avg. min	0 ppm Period Nominal	+ppm Long-term Avg. max	+ SSC Short-term Avg. Max	-c2c jitter AbsPer Max	
99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns

**Note:**

1. Guaranteed by design and characterization, not 100% tested in production
2. All long term accuracy and clock period specifications are guaranteed assuming REF is trimmed to 25.00MHz



<b>PI6CG15401</b>
-------------------

## SMBus Serial Data Interface

PI6CG15401 is a slave only device that supports block read and block write protocol using a single 7-bit address and read/write bit as shown below.

Read and write block transfers can be stopped after any complete byte transfer.

### Address Assignment

A6	A5	A4	A3	A2	A1	A0	R/W
1	1	0	1	0	SADR	0	1/0

Note: SMBus address is latched on SADR pin

### How to Write

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit		8 bits	1 bit	1 bit
Start bit	Add.	W(0)	Ack	Beginning Byte location = N	Ack	Data Byte count = X	Ack	Beginning Data Byte (N)	Ack	.....	Data Byte (N+X-1)	Ack	Stop bit

### How to Read

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit
Start bit	Address	W(0)	Ack	Beginning Byte location = N	Ack	Repeat Start bit	Address	R(1)	Ack	Data Byte count = X	Ack	Beginning Data Byte (N)	Ack

	8 bits	1 bit	1 bit
.....	Data Byte (N+X-1)	NAck	Stop bit



A Product Line of  
Diodes Incorporated



PI6CG15401

### Byte 0: Output Enable Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			1		
6	Reserved			1		
5	Reserved			1		
4	Reserved			1		
3	Q3_OE	Q3 output enable	RW	1	Low/Low	Enabled
2	Q2_OE	Q2 output enable	RW	1	Low/Low	Enabled
1	Q1_OE	Q1 output enable	RW	1	Low/Low	Enabled
0	Q0_OE	Q0 output enable	RW	1	Low/Low	Enabled

**Note:**

1. A low on these bits will override the OE# pins and force the differential outputs to Low/Low states

### Byte 1: SS Readback and Control Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	SSENRB1	SS Enable Readback Bit1	R	Latch	'00' for SS_SEL_TRI = '0', '01' for SS_SEL_TRI = 'M', '11' for SS_SEL_TRI = '1'	
6	SSENRB0	SS Enable Readback Bit0	R	Latch		
5	SSEN_SWCTR	Enable SW control of SS	RW	0	Values in B1[7:6] control SS amount	Values in B1[4:3] control SS amount
4	SSENSW1	SS enable SW control Bit1	RW <sup>1</sup>	0	'00' = SS off, '01' = -0.25% SS, '10' = Reserved, '11' = -0.5% SS	
3	SSENSW0	SS enable SW control Bit0	RW <sup>1</sup>	0		
2	Reserved			1		
1	Amplitude1	Control output amplitude	RW	1	'00' = 0.55V, '01' = 0.65V, '10' = 0.7V, '11' = 0.8V	
0	Amplitude0		RW	0		

**Note:**

1. B1[5] must be set to a 1 for these bits to have any effect on the part.



A Product Line of  
Diodes Incorporated



<b>PI6CG15401</b>
-------------------

### Byte 2: Differential Output Slew Rate Control Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			1		
6	Reserved			1		
5	Reserved			1		
4	Reserved			1		
3	SLEWRATECTR_Q3	Control slew rate of Q3	RW	1	Slow setting	Fast setting
2	SLEWRATECTR_Q2	Control slew rate of Q2	RW	1	Slow setting	Fast setting
1	SLEWRATECTR_Q1	Control slew rate of Q1	RW	1	Slow setting	Fast setting
0	SLEWRATECTR_Q0	Control slew rate of Q0	RW	1	Slow setting	Fast setting

### Byte 3: REF Control Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	REFSLEWRATE	Slew rate control for REF	RW	0	'00' = Slowest '01' = Slow '10' = Fast, '11' = Faster	
6			RW	1		
5	REF_PDSTATE	Wake-on-Lan enable for REF	RW	0	REF = 'Low'	REF = running
4	REF_OE	Output enable for REF	RW	1	REF = "Low"	REF = running
3	Reserved			1		
2	Reserved			1		
1	Reserved			1		
0	Reserved			1		

### Byte 4: Reserved

Bit	Control Function	Description	Type	Power Up Condition	0	1
7:0	Reserved					



A Product Line of  
Diodes Incorporated



PI6CG15401

### Byte 5: Revision and Vendor ID Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	RID3	Revision ID	R	0	rev = 0000	
6	RID2		R	0		
5	RID1		R	0		
4	RID0		R	0		
3	PVID3	Vendor ID	R	0	Diodes = 0011	
2	PVID2		R	0		
1	PVID1		R	1		
0	PVID0		R	1		

### Byte 6: Device Type/Device ID Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	DTYPE1	Device type	R	0	'00' = CG, '01' = ZDB, '10' = Reserve, '11' = ZDB	
6	DTYPE0		R	0		
5	DID5	Device ID	R	0	000100 binary, 04Hex	
4	DID4		R	0		
3	DID3		R	0		
2	DID2		R	1		
1	DID1		R	0		
0	DID0		R	0		

### Byte 7: Byte Count Register

Bit	Control Function	Description	Type	Power Up Condition	0	1
7	Reserved			0		
6	Reserved			0		
5	Reserved			0		
4	BC4	Byte count programming	RW	0	Writing to this register will configure how many bytes will be read back, default is 8 bytes	
3	BC3		RW	1		
2	BC2		RW	0		
1	BC1		RW	0		
0	BC0		RW	0		



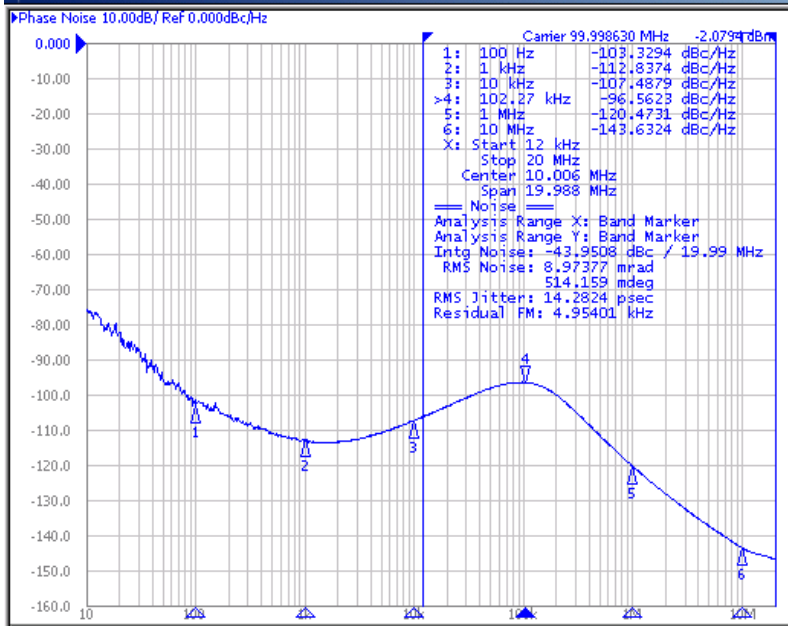
A Product Line of  
Diodes Incorporated



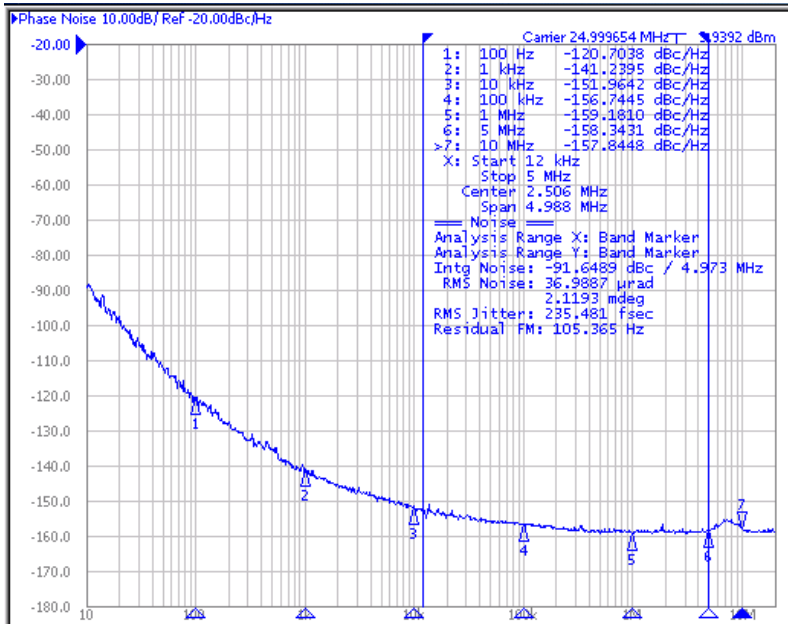
**PI6CG15401**

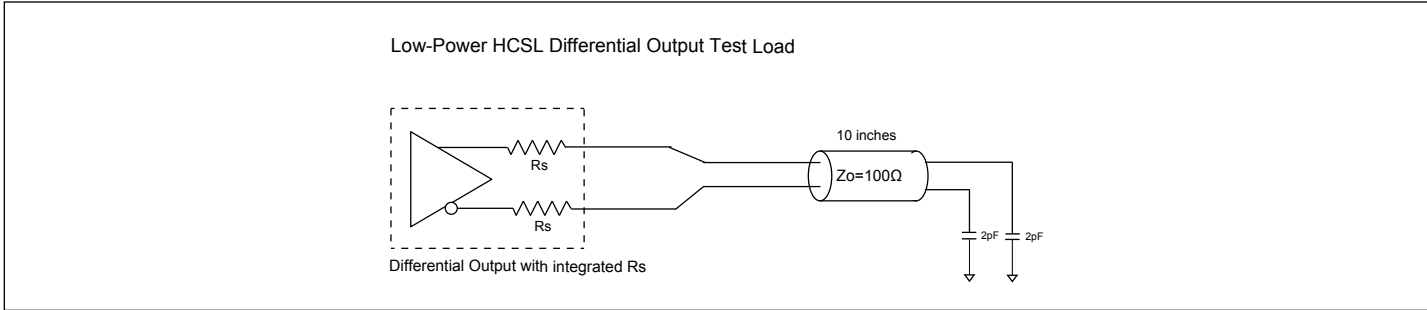
**Plots**

**100MHz HCSL Clock**

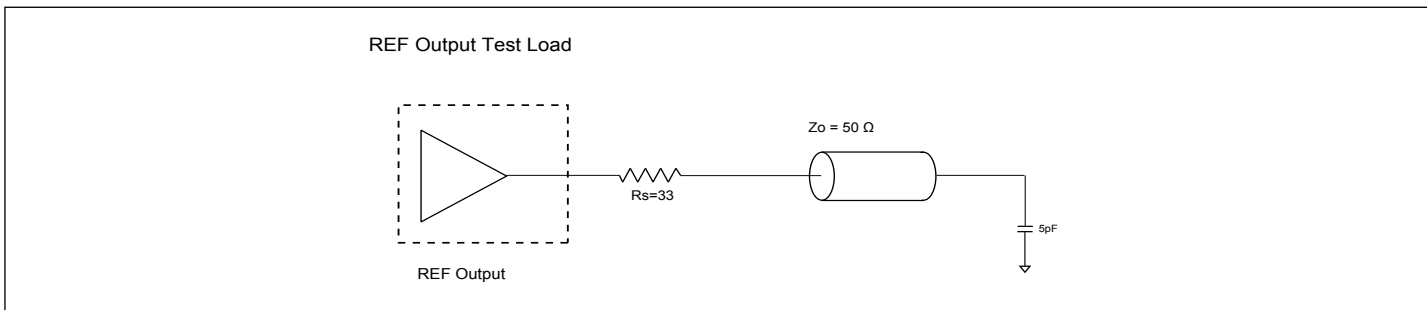


**25MHz CMOS Clock**

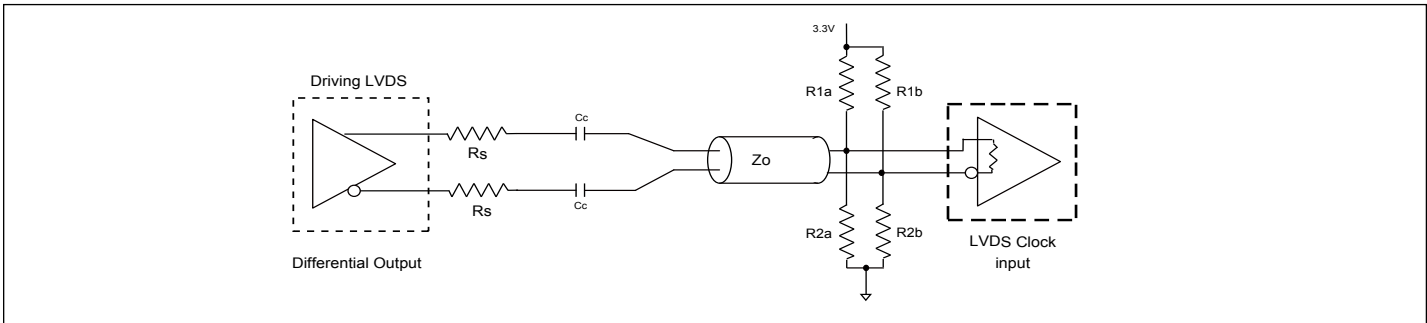




**Figure 1. Low Power HCSL Test Circuit**



**Figure 2. CMOS REF Test Circuit**



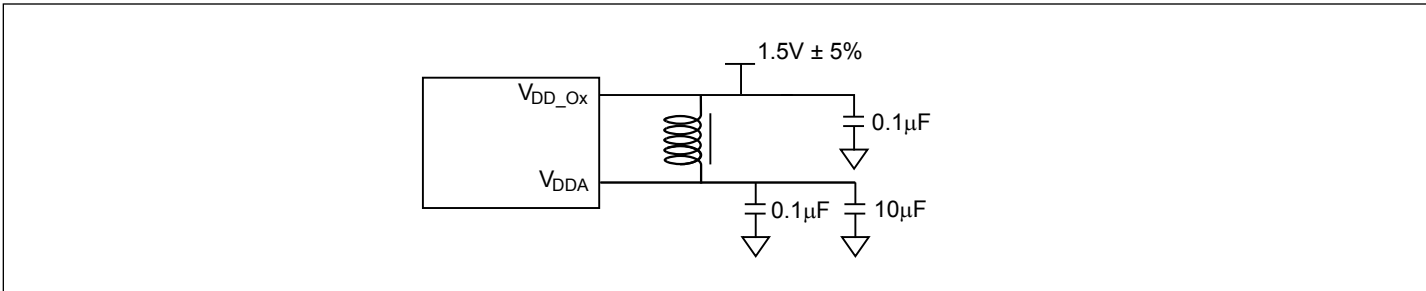
**Figure 3. Differential Output driving LVDS**

**Alternate Differential Output Terminations**

Component	Receiver with termination	Receiver without termination	Unit
$R_{1a}, R_{1b}$	10,000	140	$\Omega$
$R_{2a}, R_{2b}$	5,600	75	$\Omega$
$C_C$	0.1	0.1	$\mu F$
$V_{CM}$	1.2	1.2	V



**PI6CG15401**

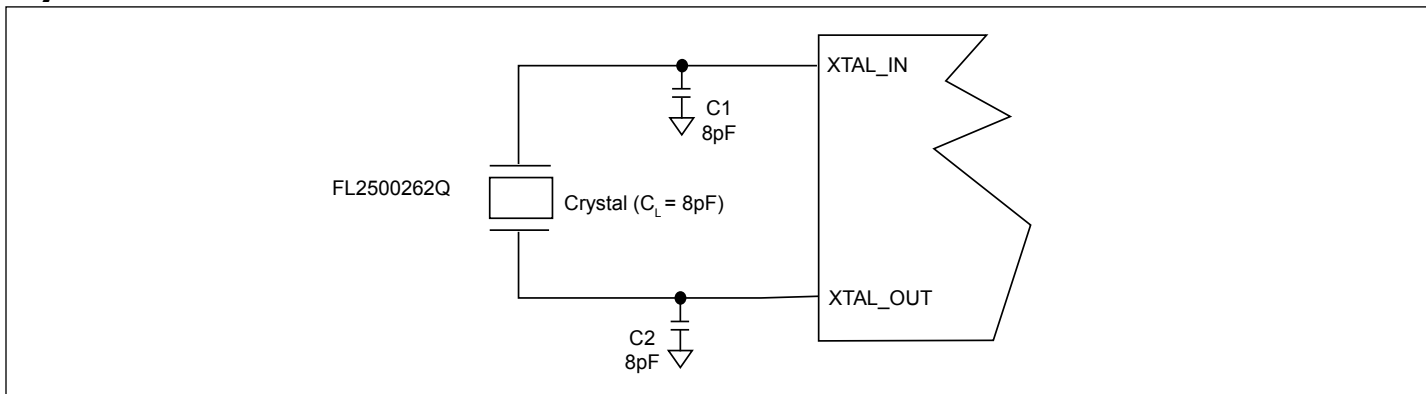


**Figure 4. Power Supply Filter**

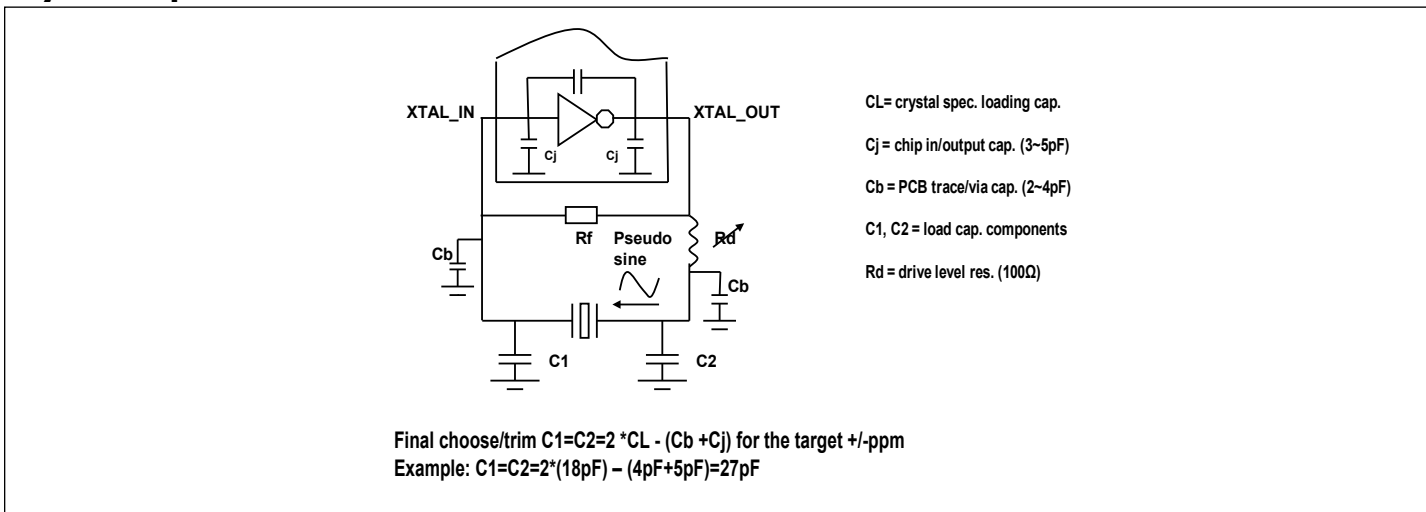
### Crystal Circuit Connection

The following diagram shows PI6CG15401 crystal circuit connection with a parallel crystal. For the  $C_L=8\text{pF}$  crystal, it is suggested to use  $C1=8\text{pF}$ ,  $C2=8\text{pF}$ .  $C1$  and  $C2$  can be adjusted to fine tune to the target ppm of crystal oscillator according to different board layouts based on the following formular in the Crystal Capacitor Calculation diagram.

### Crystal Oscillator Circuit



### Crystal Capacitor Calculation





A Product Line of  
Diodes Incorporated



PI6CG15401

## Recommended Crystal Specification

### Diodes Recommends:

- a) FL2500217, SMD 3.2x2.5(4P), 25MHz, CL=8pF, +/-20ppm, <http://www.Diodes.com/pdf/datasheets/se/FL.pdf>

## Part Marking

PI6CG15  
401ZHIE  
ZYYWWXX



Z: Die Rev  
YYWW: Year & Workweek  
1st X: Assembly Code  
2nd X: Fab Code



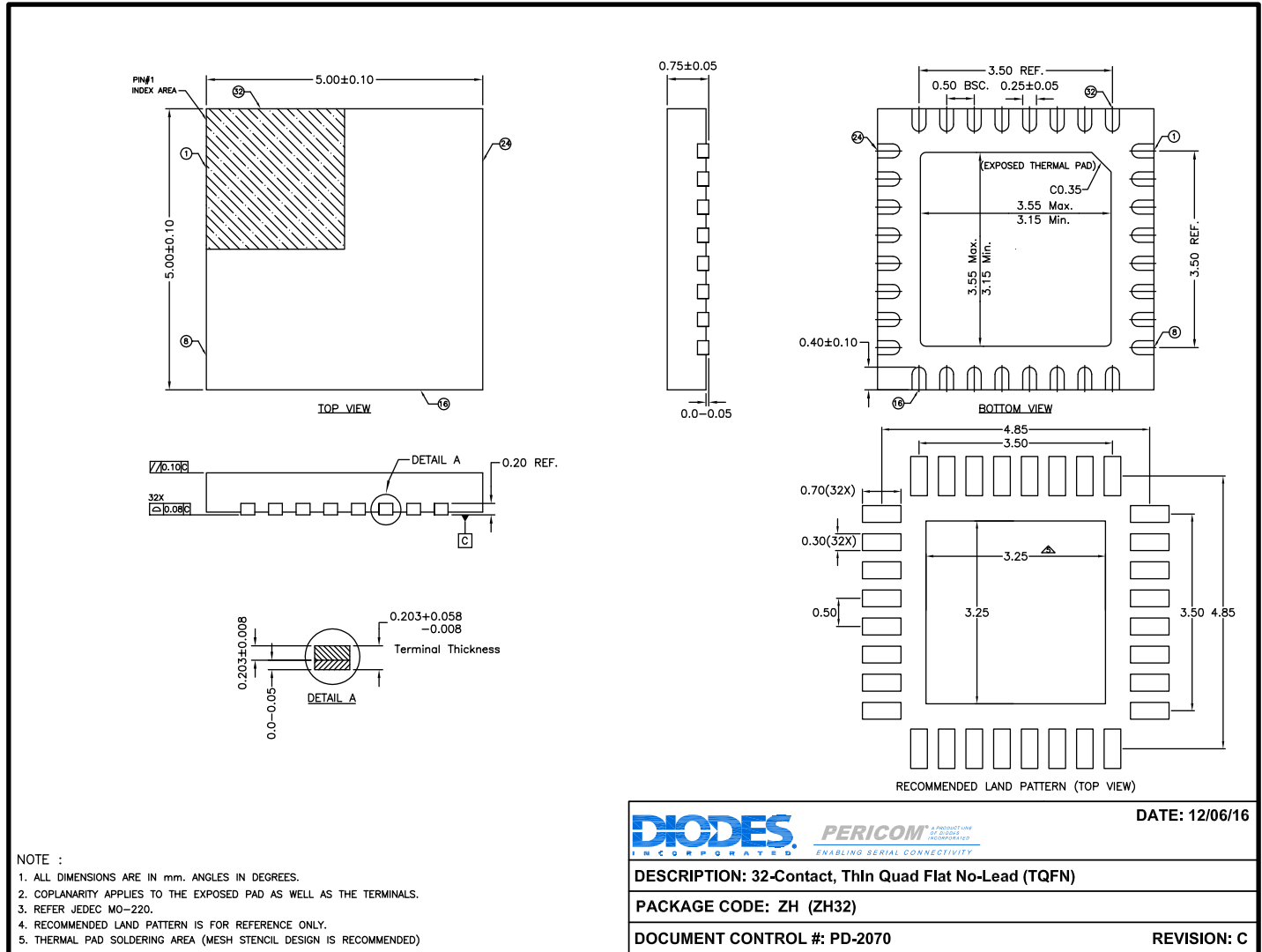
A Product Line of  
Diodes Incorporated



**PI6CG15401**

## Packaging Mechanical

### 32-TQFN (ZH)



**NOTE :**

1. ALL DIMENSIONS ARE IN mm, ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220.
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED)

<b>DIODES</b> INCORPORATED	<b>PERICOM</b> A PRODUCT LINE OF DIODES INCORPORATED ENABLING SERIAL CONNECTIVITY	<b>DATE: 12/06/16</b>
<b>DESCRIPTION: 32-Contact, Thin Quad Flat No-Lead (TQFN)</b>		
<b>PACKAGE CODE: ZH (ZH32)</b>		
<b>DOCUMENT CONTROL #: PD-2070</b>		<b>REVISION: C</b>

17-0570

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

## Ordering Information

Ordering Code	Package Code	Package Description	Operating Temperature
PI6CG15401ZHIEX	ZH	32-Contact, Very Thin Quad Flat No-Lead (TQFN)	Industrial

**Notes:**

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. I = Industrial
5. E = Pb-free and Green
6. X suffix = Tape/Reel



A Product Line of  
Diodes Incorporated



**PI6CG15401**

#### IMPORTANT NOTICE

1. DIODES INCORPORATED AND ITS SUBSIDIARIES (“DIODES”) MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO ANY INFORMATION CONTAINED IN THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

2. The Information contained herein is for informational purpose only and is provided only to illustrate the operation of Diodes products described herein and application examples. Diodes does not assume any liability arising out of the application or use of this document or any product described herein. This document is intended for skilled and technically trained engineering customers and users who design with Diodes products. Diodes products may be used to facilitate safety-related applications; however, in all instances customers and users are responsible for (a) selecting the appropriate Diodes products for their applications, (b) evaluating the suitability of the Diodes products for their intended applications, (c) ensuring their applications, which incorporate Diodes products, comply the applicable legal and regulatory requirements as well as safety and functional-safety related standards, and (d) ensuring they design with appropriate safeguards (including testing, validation, quality control techniques, redundancy, malfunction prevention, and appropriate treatment for aging degradation) to minimize the risks associated with their applications.

3. Diodes assumes no liability for any application-related information, support, assistance or feedback that may be provided by Diodes from time to time. Any customer or user of this document or products described herein will assume all risks and liabilities associated with such use, and will hold Diodes and all companies whose products are represented herein or on Diodes’ websites, harmless against all damages and liabilities.

4. Products described herein may be covered by one or more United States, international or foreign patents and pending patent applications. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks and trademark applications. Diodes does not convey any license under any of its intellectual property rights or the rights of any third parties (including third parties whose products and services may be described in this document or on Diodes’ website) under this document.

5. Diodes products are provided subject to Diodes’ Standard Terms and Conditions of Sale (<https://www.diodes.com/about/company/terms-and-conditions/terms-and-conditions-of-sales/>) or other applicable terms. This document does not alter or expand the applicable warranties provided by Diodes. Diodes does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

6. Diodes products and technology may not be used for or incorporated into any products or systems whose manufacture, use or sale is prohibited under any applicable laws and regulations. Should customers or users use Diodes products in contravention of any applicable laws or regulations, or for any unintended or unauthorized application, customers and users will (a) be solely responsible for any damages, losses or penalties arising in connection therewith or as a result thereof, and (b) indemnify and hold Diodes and its representatives and agents harmless against any and all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim relating to any noncompliance with the applicable laws and regulations, as well as any unintended or unauthorized application.

7. While efforts have been made to ensure the information contained in this document is accurate, complete and current, it may contain technical inaccuracies, omissions and typographical errors. Diodes does not warrant that information contained in this document is error-free and Diodes is under no obligation to update or otherwise correct this information. Notwithstanding the foregoing, Diodes reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes.

8. Any unauthorized copying, modification, distribution, transmission, display or other use of this document (or any portion hereof) is prohibited. Diodes assumes no responsibility for any losses incurred by the customers or users or any third parties arising from any such unauthorized use.

Copyright © 2022 Diodes Incorporated

[www.diodes.com](http://www.diodes.com)

## OUR CERTIFICATE

DiGi provide top-quality products and perfect service for customer worldwide through standardization, technological innovation and continuous improvement. DiGi through third-party certification, we stricly control the quality of products and services. Welcome your RFQ to

Email: [Info@DiGi-Electronics.com](mailto:Info@DiGi-Electronics.com)



Tel: +00 852-30501935

RFQ Email: [Info@DiGi-Electronics.com](mailto:Info@DiGi-Electronics.com)

DiGi is a global authorized distributor of electronic components.