# PT7C4512WEX Datasheet

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|---|---|
| DiGi Electronics Part Number | PT7C4512WEX-DG |
| Manufacturer | Diodes Incorporated |
| Manufacturer Product Number | PT7C4512WEX |
| Description | PLL CLOCK MULTIPLIER |
| Detailed Description | IC |

## Purchase and inquiry

| Manufacturer Product Number: | Manufacturer: |
|---|---|
| PT7C4512WEX | Diodes Incorporated |
| Series: | Product Status: |
| * | Obsolete |
| DiGi-Electronics Programmable: | Base Product Number: |
| Not Verified | PT7C4512 |

## Environmental & Export classification

| RoHS Status: | Moisture Sensitivity Level (MSL): |
|---|---|
| ROHS3 Compliant | 1 (Unlimited) |
| REACH Status: | ECCN: |
| REACH Unaffected | EAR99 |
| HTSUS: | |
| 8542.39.0001 | |

A Product Line of
Diodes Incorporated

# PT7C4512

## PLL Clock Multiplier

## Features

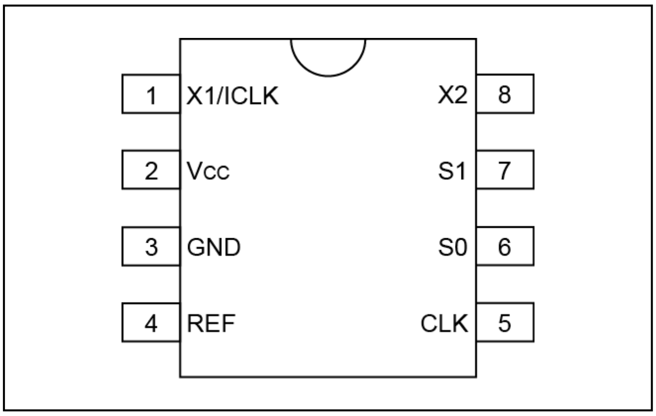
- ➔ Zero ppm multiplication error
- ➔ Input crystal frequency of 5 - 40 MHz
- ➔ Input clock frequency of 4 - 50 MHz
- ➔ Output clock frequencies up to 200 MHz
- ➔ Low period jitter 80ps (100~200MHz)
- ➔ Duty cycle of 45/55% of output clock up to 160MHz
- ➔ 9 selectable frequencies controlled by S0, S1 pins
- ➔ Operating voltages of 3.0 to 5.5V
- ➔ Lead free SOIC-8 package

## Description

This Clock Multiplier is the most cost-effective way to generate a high quality, high frequency clock outputs from lower frequency crystal or clock input. It is designed to replace crystal oscillators in most electronic systems, clock multipliers and frequency translation devices with low output jitter. The device implements a standard fundamental mode using PLL techniques and inexpensive crystal to produce output clocks up to 200 MHz.

The internal Logic divider is to generate nine different popular multiplication factors, allowing one chip to output many common frequencies.

## Pin Configuration




## Pin Description

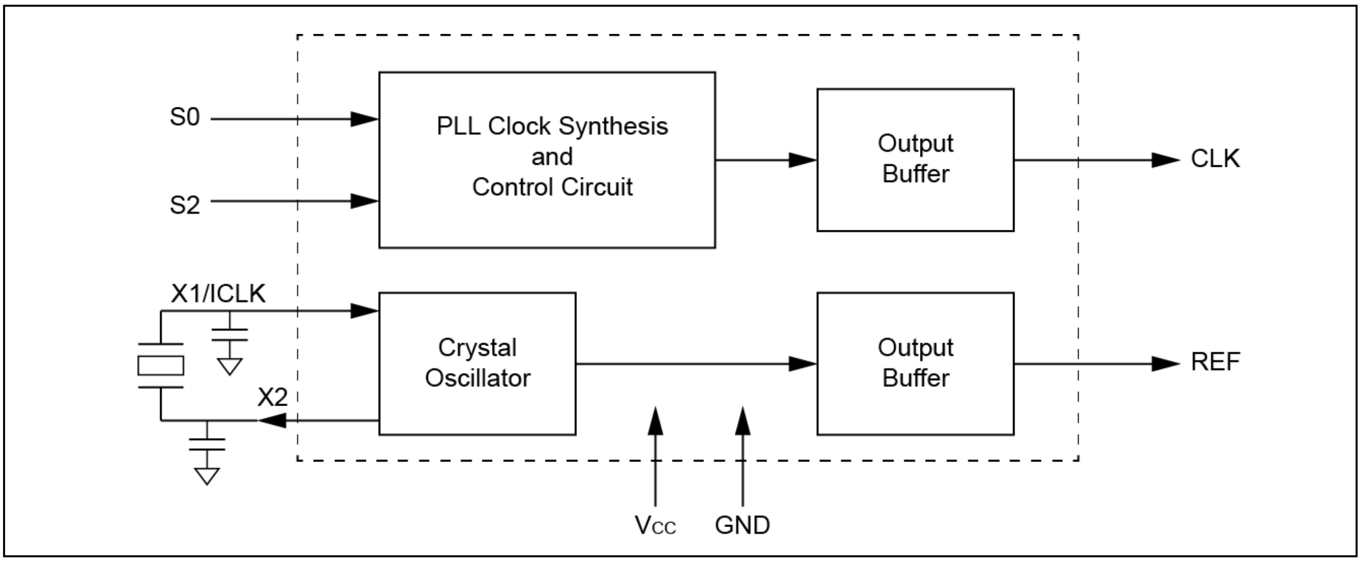
| Pin# | Name | Type | Description |
|---|---|---|---|
| 1 | X1/ICLK | X1 | Crystal connection or clock input |
| 2 | VCC | P | Connect to +3.3V or +5V |
| 3 | GND | P | Connect to ground |
| 4 | REF | O | Buffered crystal oscillator output clock |
| 5 | CLK | O | Clock output per Clock Output Table |
| 6 | S0 | T1 | Multiplier select pin 0, connect to GND or $V_{CC}$ or floating (no connection) |
| 7 | S1 | T1 | Multiplier select pin 1, connect to GND or Vcc or floating (no connection) |
| 8 | X2 | ZO | Crystal connection. Leave unconnected for clock input |

## Clock Output Table

| S1 | S0 | CLK |
|---|---|---|
| 0 | 0 | X4[1] |
| 0 | M[2] | X(16/3) |
| 0 | 1 | X5 |
| M | 0 | X2.5 |
| M | M | X2 |
| M | 1 | X(10/3) |
| 1 | 0 | X6 |
| 1 | M | X3 |
| 1 | 1 | X8 |

**Note:**
1. CLK output frequency = ICLK X 4
2. M = Leave unconnected (self-biases to $V^{CC}$/2)

## Block Diagram




## External Components

**Decoupling Capacitor**

As with any high-performance mixed-signal IC, the PT7C4512 must be isolated from system power supply noise to perform optimally. A decoupling capacitor of 0.01μF or 0.1uF must be connected between VCC and the GND. It must be connected close to the PT7C4512 to minimize lead inductance. No external power supply filtering is required for the PT7C4512.

**Series Termination Resistor**

A 33Ω terminating resistor can be used next to the CLK pin for trace lengths over one inch.

**Crystal Load Capacitors**

There is no on-chip capacitance build-in chip. A parallel resonant, fundamental mode crystal should be used. The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors, if needed, must be connected from each of the pins X1 and X2 to ground. The value (in pF) of these crystal caps should equal CL*2. In this equation, CL= crystal load capacitance in pF. Example: For a crystal with a 15 pF load capacitance, each crystal capacitor would be 30pF.

## Maximum Rating

Storage Temperature………………………………….-60°C to +150°C
Junction Temperature……………………………...……+125°C Max
Supply Voltage to Ground Potential ($V_{CC}$)……………..-0.3V to +7.0V
Inputs (Referenced to GND) ………………………-0.5V to $V_{CC}$+0.5V
Clock Output (Referenced to GND)… …………… -0.5V to $V_{CC}$+0.5V
Soldering Temperature (Max of 10 seconds)… …….260°C (Max. 10s)

**Note:**
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Recommended Operating Conditions

| Sym | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 3.0 | | 5.5 | V |
| $T_A$ | Operating Temperature | | -40 | | +85 | °C |

### DC Electrical Characteristics

($V_{CC}$ = 3.3±0.3V, $T_A$ = -40~85°C, unless otherwise noted)

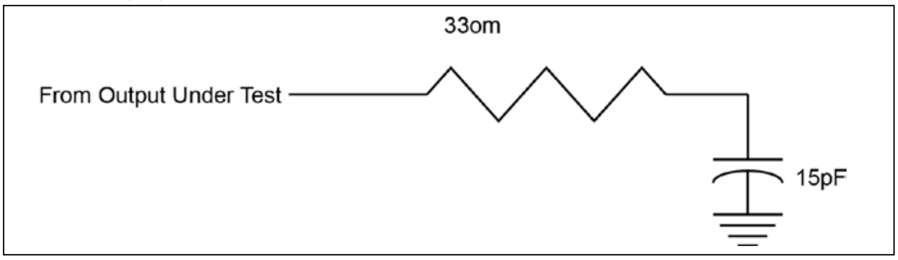
| Sym | Parameter | Test Condition | Pin | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | VCC | 3 | 3.3 | 3.6 | V |
| $I_{CC}$ | Supply Current | No load, 20MHz crystal, 100MHz output | VCC | | 12 | 20 | mA |
| $V_{IH}$ | Input Logic High | | ICLK | ($V_{CC}$/2)+1 | $V_{CC}$/2 | | V |
| $V_{IL}$ | Input Logic Low | | ICLK | | $V_{CC}$/2 | ($V_{CC}$/2)-1 | V |
| $V_{IH}$ | Input Logic High | | S0, S1 | $V_{CC}$-0.5 | | | V |
| $V_{IM}$ | Input Mid-level | | S0, S1 | | $V_{CC}$/2 | | V |
| $V_{IL}$ | Input Logic Low | | S0, S1 | | | 0.5 | V |
| $V_{OH}$ | High-level Output Voltage | IOH = -12mA | CLK | 2.4 | | | V |
| $V_{OL}$ | Low-level Output Voltage | IOL = 12 mA | CLK | | | 0.4 | |
| $I_S$ | Short Circuit Current | | CLK | | ±30 | | mA |

($V_{CC}$ = 5.0±0.5V, $T_A$ = -40~85°C, unless otherwise noted)

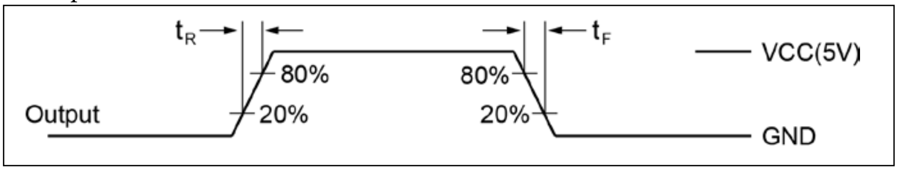
| Sym | Parameter | Test Condition | Pin | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | VCC | 4.5 | 5.0 | 5.5 | V |
| $I_{CC}$ | Supply Current | No load, 20MHz crystal, 100MHz output | VCC | | 20 | 30 | mA |
| $V_{IH}$ | Input Logic High | | ICLK | ($V_{CC}$/2)+1 | $V_{CC}$/2 | | V |
| $V_{IL}$ | Input Logic Low | | ICLK | | $V_{CC}$/2 | ($V_{CC}$/2)-1 | V |
| $V_{IH}$ | Input Logic High | | S0, S1 | $V_{CC}$-0.4 | | | V |
| $V_{IM}$ | Input Mid-level | | S0, S1 | | $V_{CC}$/2 | | V |
| $V_{IL}$ | Input Logic Low | | S0, S1 | | | 0.4 | V |
| $V_{OH}$ | High-level Output Voltage | IOH = -12mA | CLK | $V_{CC}$-0.5 | | | V |
| $V_{OL}$ | Low-level Output Voltage | IOL = 12 mA | CLK | | | 0.4 | |
| $I_S$ | Short Circuit Current | | CLK | | ±70 | | mA |

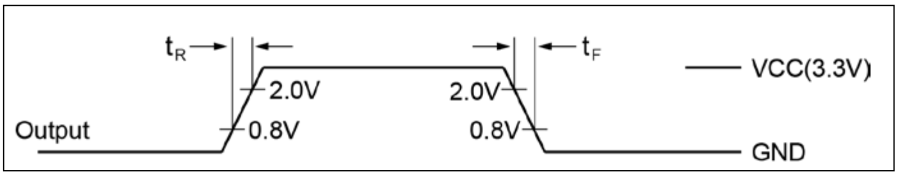
## Test Circuits

1>Load circuit for output clock duty cycle, rise and fall time Measurement




2> Timing Definitions for output clock rise and fall time Measurement



## AC Electrical Characteristics

($V_{CC}$ = 3.3±0.3V, $T_A$ = -40~85°C, unless otherwise noted)

| Sym | Parameter | Test Condition | Pin | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $F_{IN}$ | Input Frequency | Crystal | ICLK | 5 | | 40 | MHz |
| | | Clock | ICLK | 4 | | 50 | MHz |
| $F_{OUT}$ | Output Frequency (2) | $V_{CC}$: 3.0 to 3.6V | CLK | 20 | | 180 | MHz |
| $t_R$ | Output Clock Rise Time | 0.8 to 2.0V, with 15pF load | CLK | | 1 | | Ns |
| $t_F$ | Output Clock Fall Time | 2.0 to 0.8V, with 15pF load | CLK | | 1 | | Ns |
| Duty | Output Clock Duty Cycle | At $V_{CC}$/2, below 160MHz | CLK | 45 | 50 | 55 | % |
| | | At $V_{CC}$/2, 160MHz to 180MHz | CLK | 40 | | 60 | % |
| | PLL Bandwidth (1) | | | 10 | | | kHz |
| | Period Jitter | 70MHz~160MHz, 25C | CLK | | | 120 | ps |

**Note:**
1. Only reference for design
2. The phase relationship between input and output clocks can change at power up

($V_{CC}$ = 5.0±0.5V, $T_A$ = -40~85°C, unless otherwise noted)

| Sym | Parameter | Test Condition | Pin | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $F_{IN}$ | Input Frequency | Crystal | ICLK | 5 | | 40 | MHz |
| | | Clock | ICLK | 4 | | 50 | MHz |
| $F_{OUT}$ | Output Frequency (2) | $V_{CC}$: 4.5 to 5.5V | CLK | 20 | | 200 | MHz |
| $t_R$ | Output Clock Rise Time | 20%$V_{CC}$ to 80%$V_{CC}$, with 15pF load | CLK | | 1.2 | | Ns |
| $t_F$ | Output Clock Fall Time | 80%$V_{CC}$ to 20%$V_{CC}$, with 15pF load | CLK | | 1.2 | | Ns |
| Duty | Output Clock Duty Cycle | At $V_{CC}$/2, below 160MHz | CLK | 45 | 50 | 55 | % |
| | | At $V_{CC}$/2, 160MHz to 200MHz | CLK | 40 | | 60 | % |
| | PLL Bandwidth (1) | | | 10 | | | kHz |
| | Period Jitter | 70MHz~160MHz, 25C | CLK | | | 120 | ps |

**Note:**
1. Only reference for design
2. The phase relationship between input and output clocks can change at power up

## Part Marking

W Package


*: Die Rev
YW: Date Code (Year & Workweek)
1st X: Assembly Site Code
2nd X: Wafer Fab Site Code
Bar above “T” means Fab3 of MGN
Bar above fabe code means Cu wire

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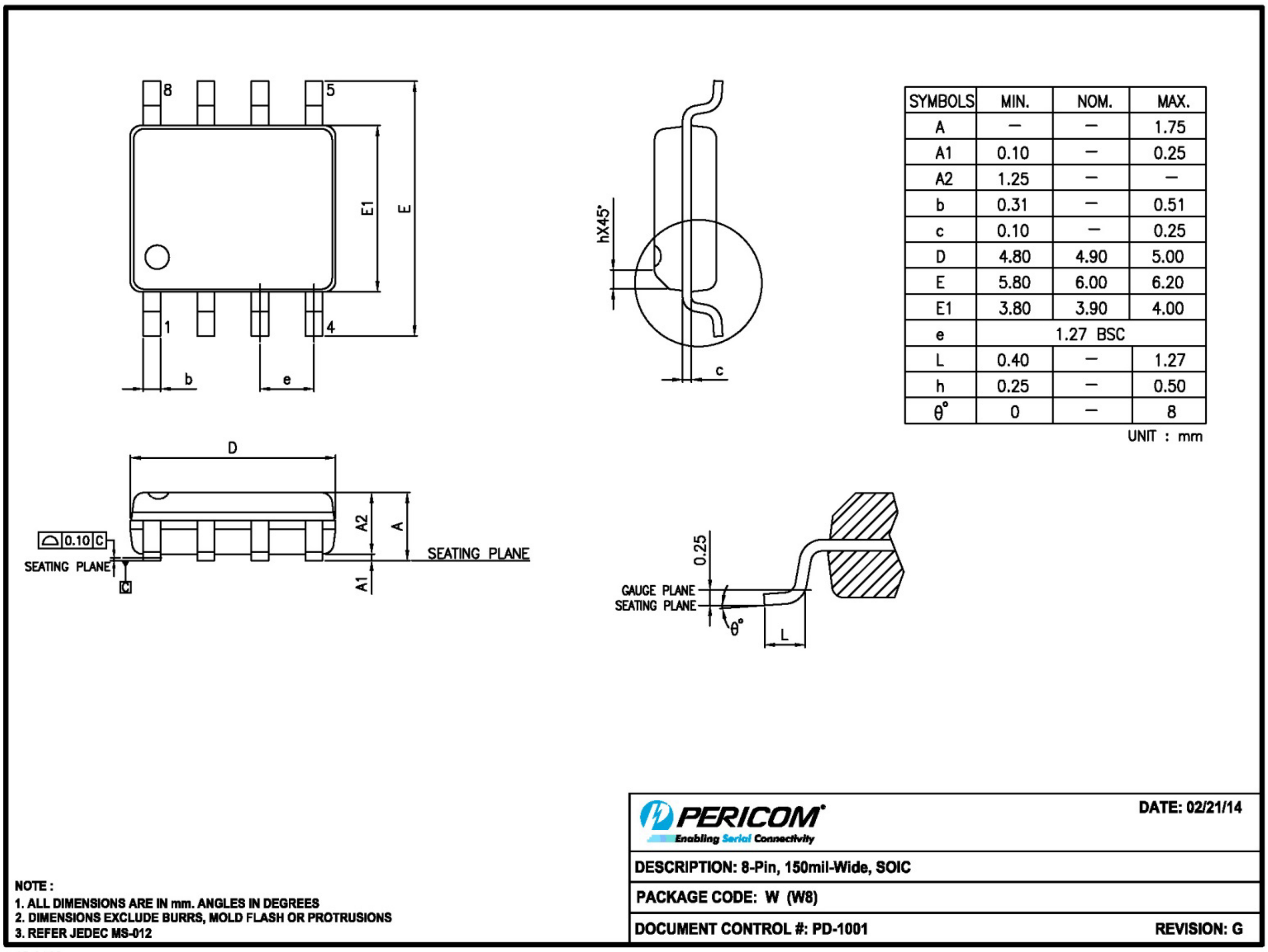
PT7C4512

## Packaging Mechanical

8-SOIC (W)




| SYMBOLS | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | – | – | 1.75 |
| A1 | 0.10 | – | 0.25 |
| A2 | 1.25 | – | – |
| b | 0.31 | – | 0.51 |
| c | 0.10 | – | 0.25 |
| D | 4.80 | 4.90 | 5.00 |
| E | 5.80 | 6.00 | 6.20 |
| E1 | 3.80 | 3.90 | 4.00 |
| e | | 1.27 BSC | |
| L | 0.40 | – | 1.27 |
| h | 0.25 | – | 0.50 |
| θ° | 0 | – | 8 |

UNIT : mm

15-0103

**For latest package info.**

please check: http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/

## Ordering Information

| Part Number | Package Code | Description |
|---|---|---|
| PT7C4512WEX | W | 8-Pin, 150mil-Wide (SOIC) |

**Notes:**

1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See http://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
4. E = Pb-free and Green
5. X suffix = Tape/Reel

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