PEX8649-AA50RBCG Datasheet

DiGi Electronics Part Number	PEX8649-AA50RBCG-DG
Manufacturer	Broadcom Limited
Manufacturer Product Number	PEX8649-AA50RBCG
Description	PEX8649-AA50RBC G
Detailed Description	PCI Express® Switch IC 48 Channel 676-FCBGA (27x27)

https://www.DiGi-Electronics.com

Purchase and inquiry

Manufacturer Product Number:	Manufacturer:
PEX8649-AA50RBCG	Broadcom Limited
Series:	Product Status:
ExpressLane™	Active
Applications:	Multiplexer/Demultiplexer Circuit:
PCI Express®	-
Switch Circuit:	Number of Channels:
-	48
On-State Resistance (Max):	Voltage - Supply, Single (V+):
-	0.95V ~ 1.05V
Voltage - Supply, Dual (V±):	-3db Bandwidth:
-	-
Features:	Operating Temperature:
Configurable	-5°C ~ 85°C
Package / Case:	Supplier Device Package:
676-BGA, FCBGA	676-FCBGA (27x27)

ExpressLane PEX 8649-AA 48-Lane, 12-Port PCI Express Gen 2 Multi-Root Switch Data Book

Version	1.5
January	**2013**
Website	www.plxtech.com
Technical Support	www.plxtech.com/support
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Revision History

Version	Date	Description of Changes
1.1	December, 2009	Production release, Silicon Revision AA.
1.2	January, 2010	Production update, Silicon Revision AA. Updated register offsets 80h[2:0] and A30h[4]. Rewrote Section 14.1.4.2. Applied miscellaneous corrections and enhancements throughout the data book.
1.3	March, 2010	Production update, Silicon Revision AA. Updated Section 10.9.2, re: 16-bit I/O Expanders. Updated register offset A30h[4]. Added Extended Temperature-related thermal content to Table 18-1 and Section 19.1.1. Applied miscellaneous corrections and enhancements throughout the data book.
1.4	November, 2010	Production update, Silicon Revision AA. Applied miscellaneous corrections and enhancements throughout the data book.
1.5	January, 2013	Production update, Silicon Revision AA. Corrected VS*x*_PERST# in Table 3-11 to be identified as an input. Updated ordering part number in Appendix A to include Enhanced Noise Immunity support.

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Document Number: 8649-AA-SIL-DB-P1-1.5

Preface

The information in this data book is subject to change without warning. This PLX data book to be updated periodically as new information is made available.

Audience

This data book provides functional details of PLX Technology’s ExpressLane PEX 8649-AA 48-Lane, 12-Port PCI Express Gen 2 Multi-Root Switch, for hardware designers and software/firmware engineers.

Supplemental Documentation

This data book assumes that the reader is familiar with the following documents:

- PLX Technology, Inc., www.plxtech.com

  The PLX PEX 8649 Toolbox includes this data book and other supporting documentation, *such as* errata, and design and application notes, as well as the migration document from the PEX 8648.
- The Institute of Electrical and Electronics Engineers, Inc. (IEEE), www.ieee.org
  - *IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture*
  - *IEEE Standard 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*
  - *IEEE Standard 1149.1-1994, Specifications for Vendor-Specific Extensions*
  - *IEEE Standard 1149.6-2003, IEEE Standard Test Access Port and Boundary-Scan Architecture Extensions*
- Intel Corporation, www.intel.com
  - *PHY Interface for the PCI Express Architecture, Version 2.00*
- NXP Semiconductors, www.standardics.nxp.com
  - *The I2C-Bus Specification, Version 2.1*
- PCI Special Interest Group (PCI-SIG), www.pcisig.com
  - *PCI Local Bus Specification, Revision 3.0*
  - *PCI Bus Power Management Interface Specification, Revision 1.2*
  - *PCI to PCI Bridge Architecture Specification, Revision 1.2*
  - *PCI Express Base Specification, Revision 1.1*
  - *PCI Express Base Specification, Revision 2.0*
  - *PCI Express Base Specification, Revision 2.0 Errata*
  - *PCI Express Card Electromechanical Specification, Revision 2.0*
  - *PCI Express Mini Card Electromechanical Specification, Revision 1.1*
  - *PCI Express Architecture PCI Express Jitter and BER White Paper, Revision 1.0*
- Personal Computer Memory Card International Association (PCMCIA), www.pcmcia.org
  - *ExpressCard Standard Release 1.0*
- PXI System Alliance (PXI), www.pxisa.org
  - *PXI-5 PXI Express Hardware Specification, Revision 1.0*
- SBS Implementers Forum, smbus.org
  - *System Management Bus (SMBus) Specification, Version 2.0*

Note: *In this data book, shortened titles are associated with the previously listed documents. The following table lists these abbreviations.*

Abbreviation	Document
PCI r3.0	*PCI Local Bus Specification, Revision 3.0*
PCI Power Mgmt. r1.2	*PCI Bus Power Management Interface Specification, Revision 1.2*
PCI-to-PCI Bridge r1.2	*PCI to PCI Bridge Architecture Specification, Revision 1.2*
PCI Express Base r1.1	*PCI Express Base Specification, Revision 1.1*
PCI Express Base r2.0	*PCI Express Base Specification, Revision 2.0*
PCI ExpressCard CEM r2.0	*PCI Express Card Electromechanical Specification, Revision 2.0*
PCI ExpressCard Mini CEM r1.1	*PCI Express Mini Card Electromechanical Specification, Revision 1.1*
IEEE Standard 1149.1-1990	*IEEE Standard Test Access Port and Boundary-Scan Architecture*
IEEE Standard 1149.6-2003	*IEEE Standard Test Access Port and Boundary-Scan Architecture Extensions*
I^2C Bus v2.1 *I2C Bus v2.1*[a]	*The I^2C-Bus Specification, Version 2.1*
SMBus v2.0	*System Management Bus (SMBus) Specification, Version 2.0*

a. *Due to formatting limitations, the specification name may appear without the superscripted "2" in its title.*

Terms and Abbreviations

The following table lists common terms and abbreviations used in this data book. Terms and abbreviations defined in the *PCI Express Base r2.0* are generally not included in this table.

Terms and Abbreviations	Definitions
8b/10b	Data-encoding scheme used on data transferred across a Link that is operating at either Gen 1 or Gen 2 Link speed (2.5 or 5.0 GT/s, respectively).
ACK	Acknowledge Control Packet. A control packet used by a destination to acknowledge data packet receipt. A signal that acknowledges signal receipt.
ARI	Alternative Routing-ID Interpretation.
ARP	Address Resolution Protocol.
BAR	Base Address register.
BER	Bit error rate.
BIST	Built-In Self Test.
CDR	Clock/Data Recovery circuit.
CRC	Cyclic Redundancy Check.
CSR	Configuration Space register.
Data Beat	Single data transfer in a single clock period.
DLL	Data Link Layer.
DMA	Direct Memory Access.
Downstream Device	Device that is connected to a downstream Port.
Downstream Port	Port that is used to communicate with a device below it in the system hierarchy. A switch can have one or more downstream Ports.
DRI	Data Rate Identifier field in Training Sets.
ECC	Error-Correcting Code.
ECRC	End-to-end Cyclic Redundancy Check.
EIES	Electrical Idle Exit Sequence.
EIOS	Electrical Idle Ordered-Set.
Electrical Idle	Transmitter is in a High-Impedance state (+ and - are both at common mode voltage).
EP	Endpoint.
FC	Flow Control.
Field	Multiple register bits that are combined for a single function.
FTS	Fast Training Sequence.
Gen 1	*PCI Express Base r1.1* and below. Link transfer rate of 2.5 GT/s.
Gen 2	*PCI Express Base r2.0*. Link transfer rate of 5.0 GT/s.
GPIO	General-Purpose Input/Output.
GT/s	Giga-Transfers per second.
INCH	Ingress Credit Handler.
ISR	Interrupt Service Routine.

Terms and Abbreviations	Definitions
Lane	Bidirectional pair of differential PCI Express I/O signals.
LCRC	Link Cyclic Redundancy Check.
LFSR	Linear Feedback Shift register.
Link	Active connection between two Ports.
Link Interface	Primary side of the NT Port, connects to external device pins. The secondary side of the NT Port is referred to as the *NT Port Virtual Interface*, and connects to the internal virtual PCI Express interface.
Local	Reference to PCI Express attributes (*such as* credits) that belong to the PCI Express Station.
LTSSM	Link Training and Status State Machine.
LUT	Lookup Table.
MPS	Maximum Payload Size.
MR-IOV	Multi-Root I/O Virtualization.
MRL	Manually operated Retention Latch.
NACK	Negative Acknowledge. Used in the SMBus-related content.
NAK	Negative Acknowledge.
N_FTS	Number of Fast Training Sequences field in Training Sets.
NOP	No Operation.
NT	Non-Transparent. A bridging technique used in the PCI Express Switch to isolate Memory spaces by presenting the processor as an endpoint rather than another memory system. The PEX 8649 supports one NT Port.
OS	Ordered-Set.
P2P	Peer-to-Peer or PCI-to-PCI (as identified at point of use).
PCI Express Station	Functional unit that provides the PCI Express conforming system interface. Includes the Serializer/De-Serializer (SerDes) hardware interface modules and PCI Express interface, which provides the Physical Layer (PHY), Data Link Layer (DLL), and Transaction Layer (TL) logic.
PEC	Packet Error Code.
PEX	PCI Express.
PHY	Physical Layer.
PIPE	PHY Interface for PCI Express architecture.
PLL	Phase-Locked Loop.
PM	Power Management.
PME	Power Management Event.
PN	Port Number.
Port	Interface to a group of SerDes and supporting logic that is capable of creating a Link, for communication with another Port.
Port ID	Number, assigned in hardware, that associates a SerDes with a Port.
P-P	PCI-to-PCI.
PRBS	Pseudo-Random Bit Sequence.

Terms and Abbreviations	Definitions
QoS	Quality of Service.
RAS	Reliability, Availability, and Serviceability.
RoHS	Restrictions on the use of certain Hazardous Substances (RoHS) Directive.
RR	Round-Robin scheduling.
Rx	Receiver.
SerDes	Serializer/De-Serializer. A high-speed differential-signaling parallel-to-serial and serial-to-parallel conversion logic attached to Lane pads.
SMBus	System Management Bus.
SN	SerDes Number.
SPI	Serial Peripheral Interface.
SRA	Shadow Register Access.
Station	Logic block that implements the PCI Express function, bounded by the external pins of the differential Transceivers and the interface to the internal switch fabric.
Sticky Bits	Register bits in which the current values are unchanged by a Hot Reset, Link Down event or a Secondary Bus Reset, while the switch is powered. Sticky bits are reset to default values by a Fundamental Reset. HwInit, ROS, RW1CS, and RWS CSR types. (Refer to Table 13-4, “Register Types, Grouped by User Accessibility,” for CSR type definitions.)
Sticky State	Condition that causes a state machine to be stuck in a particular state, unable to make forward progress.
TC	Traffic Class.
TCB	Training Control Bit field in Training Sets.
TL	Transaction Layer.
TLC	Transaction Layer Control. The module performing PCI Express Transaction Layer functions.
TLP	Transaction Layer Packet. PCI Express packet formation and organization.
Transparent	Refers to standard PCI Express upstream-to-downstream routing protocol.
TS1	Type 1 Training Sequence Ordered-Set.
TS2	Type 2 Training Sequence Ordered-Set.
Tx	Transceiver.
UDID	Unique Device Identifier.
UI	Unit Interval – 400 ps at 2.5 GT/s, 200 ps at 5.0 GT/s.
Upstream Device	Device that is connected to the upstream Port(s).
Upstream Port	Port that is used to communicate with a device above it in the system hierarchy.
UTP	User Test Pattern.
VC	Virtual Channel.
VC&T	Virtual Channel and Type.
Vector	Address and data.
Virtual Interface	Secondary side of the NT Port, connects to the internal virtual PCI Express interface.
VS	Virtual Switch.
WRR	Weighted Round-Robin scheduling.

Data Book Notations and Conventions

Notation / Convention	Description
Blue text	Indicates that the text is hyperlinked to its description elsewhere in the data book. Left-click the blue text to learn more about the hyperlinked information. This format is often used for register names, register bit and field names, register offsets, chapter and section titles, figures, and tables.
PEX_XXXn[*x*] PEX_XXXp[*x*]	When the signal name appears in all CAPS, with the primary Port description listed first, field [*x*] indicates the number associated with the signal balls/pads assigned to a specific SerDes module/Lane. The lowercase "n" (negative) or "p" (positive) suffix indicates the differential pair of signals, which are always used together.
# = Active-Low signals	Unless specified otherwise, Active-Low signals are identified by a "#" appended to the term (*for example*, PEX_PERST#).
`Program/code samples`	`Monospace font` (*`program or code samples`*) is used to identify code samples or programming references. These code samples are case-sensitive, unless specified otherwise.
`command_done`	Interrupt format.
Command/Status	Register names.
Parity Error Detected	Register parameter [bit or field] or control function.
Upper Base Address[31:16]	Specific Function in 32-bit register bounded by bits [31:16].

Number multipliers	k = 1,000 (10^3) is generally used with frequency response.
	K = 1,024 (2^{10}) is used for Memory size references.
	KB = 1,024 bytes.
	M = meg.
	= 1,000,000 when referring to frequency (decimal notation)
	= 1,048,576 when referring to Memory sizes (binary notation)

255d	d = Suffix that identifies decimal values.
1Fh	h = Suffix that identifies hex values. Each prefix term is equivalent to a 4-bit binary value (Nibble). Legal prefix terms are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F.
1010b	b = suffix which identifies binary notation (*for example*, 01b, 010b, 1010b, and so forth). Not used with single-digit values of 0 nor 1.
0 through 9	Decimal numbers, or single binary numbers.
byte	5/20/09: Add period. D, S, C Eight bits – abbreviated to "B" (*for example*, 4B = 4 bytes).
LSB	Least-Significant Byte.
lsb	Least-significant bit.
MSB	Most-Significant Byte.
msb	Most-significant bit.
DWord or DW	Double-Word (32 bits) is the primary register size in these devices.
QWord	Quad-Word (64 bits).
Reserved	Do not modify ***reserved*** bits and words. Unless specified otherwise, these bits read as 0 and must be written as 0.
word	16 bits.

Contents

Registers

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NT Port Virtual Interface Registers – Base Mode Only

NT Port Link Interface Registers – Base Mode Only

Chapter 1 Introduction

1.1 Overview

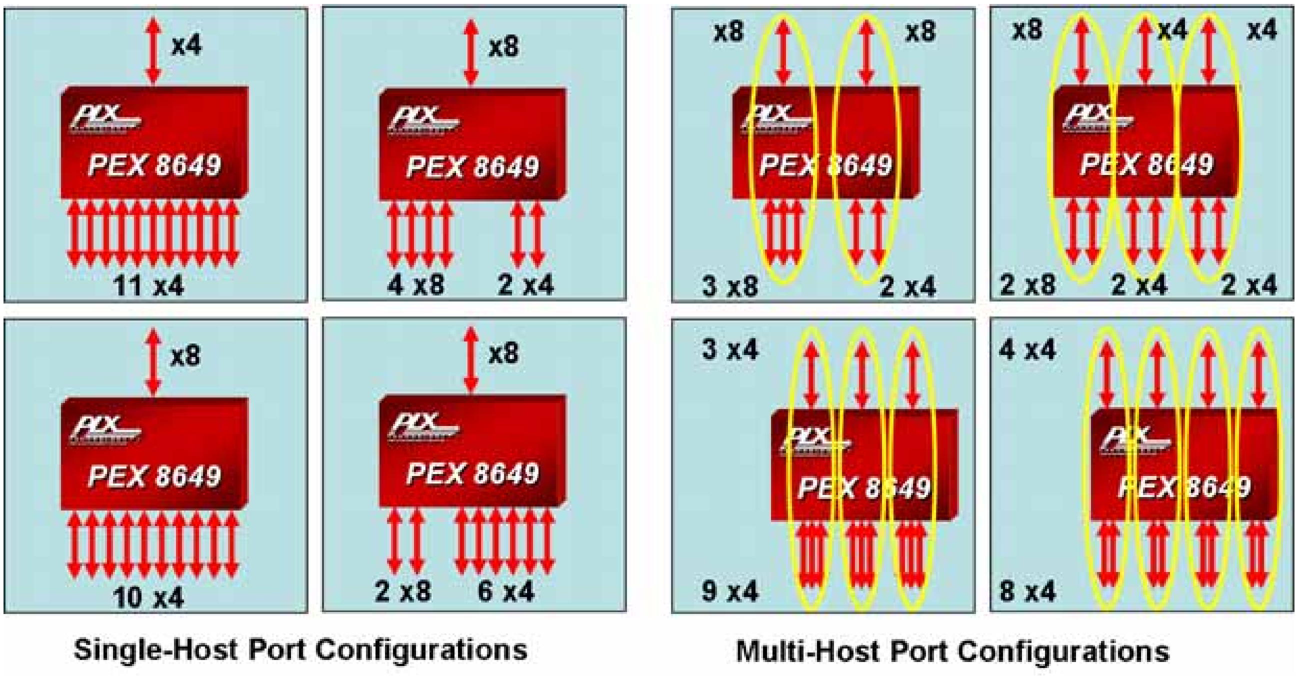
This data book describes PLX Technology’s ExpressLane^{TM} PEX 8649, a fully non-blocking, low-latency, low-cost, and low-power 48-Lane, 12-Port PCI Express Gen 2 Multi-Root switch. Conforming to the *PCI Express Base r2.0*, the PEX 8649 enables users to add high-bandwidth I/O to various products, including servers, storage systems, and communications platforms. The PEX 8649’s flexible hardware configuration and software programmability allows the switch to be tailored for a wide variety of application requirements.

The PEX 8649 is well-suited for fan-in/out applications, as well as for applications requiring peer-to-peer communication. The PEX 8649 supports two functional modes – *Base* and *Virtual Switch*:

- In Base mode, the PEX 8649 acts as a standard PCI Express switch, supporting one Host hierarchy
- In Virtual Switch mode, the PEX 8649 supports up to four Hosts, creating up to four virtual switches within the PEX 8649 – each with its own virtual hierarchy

Figure 1-1 illustrates several of the possible PEX 8649 Port configurations, using various Link widths. The PEX 8649 can also support Link widths of x1 and x2, by auto-negotiating its Ports to the Link width of the PCI Express device with which it is interfacing.

Figure 1-1. Common Port Configurations



1.2 Features

The PEX 8649 supports the following features:

- 12-Port PCI Express switch
  - – 48 Lanes with integrated on-chip SerDes
  - – Low-power SerDes (under 90 mW per Lane)
  - – Fully Non-Blocking Switch architecture
  - – Relaxed Ordering
  - – Port configuration
    - 12 independent Ports
    - Choice of Link width (quantity of Lanes) per unique Link/Port – x4, x8, or x16; Link widths of x1 and x2 are also supported
    - Configurable with serial EEPROM, I^2C, SMBus, and/or Host software
    - Designate any Port as the *upstream Port* (Port 0 is recommended in Base mode)
- Multi-Root support
  - – Up to four upstream Ports supported
  - – 1+1 Failover (one active and one backup)
  - – *N*+1 Failover (*N* active and one backup)
- High Performance
  - – 480 GT/s aggregate bandwidth (5.0 GT/s/Lane x 48 SerDes x 2 (full duplex))
  - – Integrated 5.0 GT/s SerDes speed negotiation, for each Port
  - – Non-Blocking Internal architecture
  - – Full line rate on all Ports
  - – Cut-Thru packet latency of less than 150 ns between symmetric (x16 to x16) ingress and egress Ports
  - – Non-blocking Crossbar Switch interface supports TLP bandwidth capacity of each x16 Link
  - – Maximum Payload Size – 2,048 bytes
- *performance*PAK™
  - – Read Pacing™ (intelligent bandwidth allocation)
  - – Multicast (supported in all modes except Legacy NT)
  - – Dynamic Buffer Pool Architecture for faster credit updates
- *vision*PAK™
  - – Performance Monitoring
    - Per-Port Payload and Header Counters
    - Per-traffic type (Write, Read, Completion) Counters
  - – Error Injection and Pseudo-Random Bit Sequence (PRBS)
  - – SerDes Loopback
  - – SerDes Eye Capture
- Access Control Services (ACS) – Protection mechanisms for added data integrity in peer-to-peer transactions
- Alternative Routing-ID Interpretation (ARI) – Enables virtualized systems and/or highly integrated multi-function devices

- Quality of Service (QoS) support
  - All Ports support one, full-featured Virtual Channel (VC0)
  - All Ports support eight Traffic Class (TC[7:0]) mapping, independently of the other Ports
  - Round-Robin (RR) and Weighted Round-Robin (WRR) Port arbitration
- Non-Transparent Bridging (NT mode, supported in Base mode)
  - Program any one downstream Port as the *upstream Non-Transparent (NT) Port*
  - Enables Dual-Host, Dual-Fabric, Host-Failover applications
  - Moveable *upstream Port*
  - Cross-link Port capability
- Reliability, Availability, Serviceability (RAS) features
  - PCI Express Standard Hot Plug Controller for two Ports, including optional usage models for Manually operated Retention Latch, by way of Manually operated Retention Latch (MRL) Sensor and Attention Button support
  - Serial Hot Plug, by way of I^{2}C, for Hot Plug capability on all Transparent downstream Ports
  - End-to-end Cyclic Redundancy Check (ECRC) and Poison bit support
  - Data path protection
  - Memory (RAM) error correction
  - Electromechanical Interlock supported with Power Enable output
  - Baseline and Advanced Error Reporting capability
  - Port (Link) Status bits and GPIO available
  - Per-Port error diagnostics
  - Joint Test Action Group (JTAG) AC/DC boundary scan
- INTA# (PEX_INTA# and VS*x*_PEX_INTA#) and FATAL ERROR (FATAL_ERR# and VS*x*_FATAL_ERR#) (Conventional PCI SERR# equivalent) ball support
- 20 General-Purpose Input/Output (GPIO) balls (Port Status (PEX_PORT_GOOD*x*#) and GPIO*x*), which can be used for Link Status LEDs, GPIO, and/or Interrupt inputs
- Other PCI Express Capabilities
  - Lane reversal
  - Polarity reversal
  - Conventional PCI-compatible Link Power Management states – L0, L0s, L1, L2/L3 Ready, and L3 (with Vaux ***not supported***)
  - Conventional PCI-compatible Device Power Management states – D0 and D3hot
  - Active State Power Management (ASPM)
  - Dynamic speed (2.5 or 5.0 GT/s) negotiation, for each Port
  - Dynamic Link width negotiation
- Out-of-Band Initialization options
  - Serial EEPROM
  - I^{2}C and SMBus (7-bit Slave address with 100 Kbps)
- Testability – JTAG support for DC
- 27 x 27 mm^2, 676-ball Flip-Chip Ball Grid Array (FCBGA) package with Heat Spreader
- Typical power – 6.74W
- ***Microsoft Vista***®-compliant

- Compliant to the following specifications:
  - *PCI Local Bus Specification, Revision 3.0 (PCI r3.0)*
  - *PCI Bus Power Management Interface Specification, Revision 1.2 (PCI Power Mgmt. r1.2)*
  - *PCI to PCI Bridge Architecture Specification, Revision 1.2 (PCI-to-PCI Bridge r1.2)*
  - *PCI Express Base Specification, Revision 1.1 (PCI Express Base r1.1)*
  - *PCI Express Base Specification, Revision 2.0 (PCI Express Base r2.0)*
  - *PCI Express Base Specification, Revision 2.0 Errata*
  - *PCI Express Card Electromechanical Specification, Revision 2.0 (PCI ExpressCard CEM r2.0)*
  - *PCI Express Mini Card Electromechanical Specification, Revision 1.1 (PCI ExpressCard Mini CEM r1.1)*
  - *IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (IEEE Standard 1149.1-1990)*
  - *IEEE Standard 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*
  - *IEEE Standard 1149.1-1994, Specifications for Vendor-Specific Extensions*
  - *IEEE Standard 1149.6-2003, IEEE Standard Test Access Port and Boundary-Scan Architecture Extensions (IEEE Standard 1149.6-2003)*
  - *The I^{2}C-Bus Specification, Version 2.1 (I^{2}C Bus v2.1)*
  - *PHY Interface for the PCI Express Architecture, Version 2.00*
  - *System Management Bus Specification, Version 2.0* (*SMBus v2.0*)

Chapter 2 Features and Applications

2.1 Flexible and Feature-Rich 48-Lane, 12-Port Switch

2.1.1 Highly Flexible Port Configurations

The PLX ExpressLane PEX 8649 PCI Express Gen 2 Multi-Root Switch offers a maximum of 12 configurable Ports.

Link widths can be individually configured as any power-of-two, from x1 to x16 to support specific bandwidth needs. Additionally, Link widths can be individually configured for each Port, through auto-negotiation, hardware strapping, an optional serial EEPROM, and/or the I^{2}C Slave interface.

The PEX 8649 supports several Port configurations. *For example*, the PEX 8649 can be used in a fan-out application, where any Port can be designated as the upstream Port and the remaining available Lanes are divided among up to 11 downstream Ports, of varying Link widths. Any one Port can be designated as, or dynamically changed to be, the upstream Port (Port 0 is recommended in Base mode).

Flexible buffer allocation, along with the PEX 8649's flexible packet flow control, maximizes throughput for applications where more traffic flows in the downstream, rather than upstream, direction. Figure 1-1 illustrates some of the PEX 8649's common Port configurations in Conventional PCI mode (Base mode).

The PEX 8649 can also be configured in Virtual Switch mode, where users can choose up to four Ports as Host/upstream Ports and assign a specific quantity of downstream Ports to each Host. In this mode, a virtual switch is created for each Host Port and its associated downstream Ports within the switch. The traffic between the Ports of a virtual switch is completely isolated from the traffic in other virtual switches. In addition to Base mode configurations, Figure 1-1 also illustrates common Port configurations in Virtual Switch mode, where each ellipse represents a virtual switch within the PEX 8649.

2.1.2 Non-Blocking Crossbar Switch Architecture

The Non-Blocking Crossbar Switch architecture is an on-chip interconnect switching fabric, which is built upon the existing PLX Switch Fabric Architecture technology. In addition to addressing simultaneous multiple flows, the Crossbar Switch architecture incorporates functions required to support an efficient PCI Express switch fabric, including:

- Deadlock avoidance
- Priority preemption
- PCI Express Ordering rules
- Packet fair queuing
- Oldest first scheduling

The Crossbar Switch interconnect physical topology is that of a packet-based Crossbar Switch fabric (internal fabric) designed to simultaneously connect multiple on-chip Stations. The Crossbar Switch protocol is sufficiently flexible and robust to support a variety of embedded system requirements. The protocol is specifically designed to ease chip integration, by strongly enforcing Station boundaries and standardizing communication between Stations. The Crossbar Switch architecture basic features include:

- Multiple concurrent Data transfers
- Global ordering within the PEX 8649
- Three types of transactions – Posted, Non-Posted, and Completion (P, NP, and Cpl, respectively) – meet PCI and PCI Express Ordering and Deadlock Avoidance rules
- Optional weighting of source Ports, to support Source Port arbitration

2.1.3 Multi-Host Architecture

The PEX 8649 allows users to configure the switch in Conventional PCI mode (Base mode), or in Virtual Switch mode with up to four Host Ports capable of 1+1 (one active and one backup) or *N*+1 (*N* active and one backup) Host Failover. This powerful architectural enhancement enables users to build PCI Express-based systems that support high-availability, failover, redundant, and clustered systems.

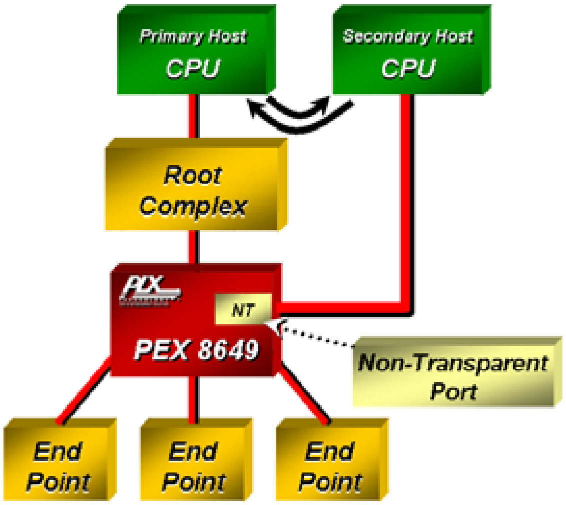
2.1.3.1 Dual-Host and Failover Support – NT Mode Only

Note: *NT mode is available only in Base mode.*

In Base mode, the PEX 8649 supports a Non-Transparent (NT) Port (Figure 2-1), which enables the implementation of dual-Host systems for redundancy and Host failover capability. The NT Port allows systems to isolate Host memory domains, by presenting the processor subsystem as an endpoint, rather than as another memory system:

- **Base Address** registers (BARs) are used to translate addresses
- **Doorbell** registers are used to signal interrupts between the address domains
- **Scratchpad** registers are accessible from both address domains, to allow inter-processor communication

Figure 2-1. NT Port – NT Mode Only



2.1.3.2 Virtual Switch Mode (Multi-Host) and Failover Support

In Virtual Switch mode, the PEX 8649 can be configured with up to four upstream Host Ports, each with its own dedicated downstream Ports. The PEX 8649 can be configured for 1+1 or *N*+1 redundancy. The PEX 8649 allows the Hosts to communicate their status to one another, using special **Doorbell** registers.

In Failover mode, if a Host fails, the Host designated for failover disables the upstream Port attached to the failing Host, then programs the downstream Ports of that Host to its own domain. Figure 2-2a illustrates a two-Host system in Virtual Switch mode, with two virtual switches within the PEX 8649. Figure 2-2b illustrates Host 1 as being disabled after failing, and Host 2 having taken over all of Host 1's endpoints.

Figure 2-2. Virtual Switch Mode (Multi-Host) and Failover Support

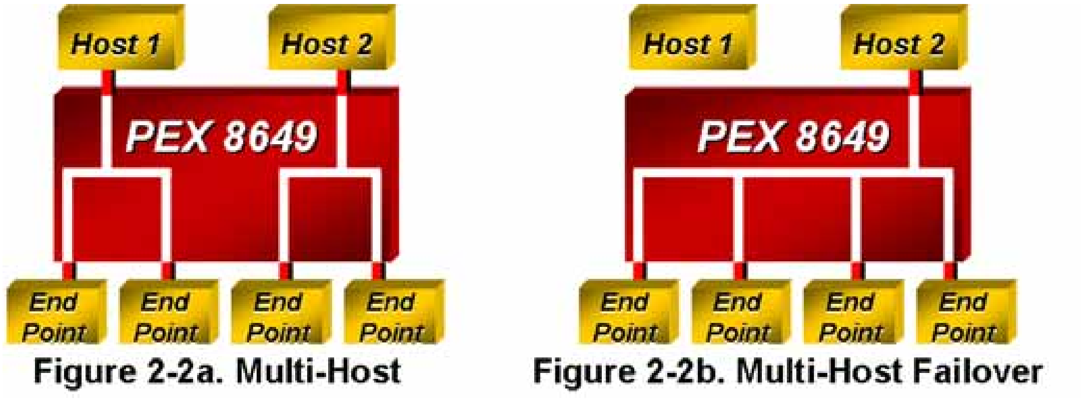


Figure 2-2a. Multi-Host

Figure 2-2b. Multi-Host Failover

2.1.4 Low Packet Latency and High Performance

The PEX 8649 architecture supports packet **Cut-Thru with a maximum latency of 150 ns** between **symmetric (x16 to x16)** ingress and egress Ports. This, combined with large Packet memory, flexible common buffer/Flow Control (FC) credit pool, and Non-Blocking Internal Switch architecture, provides full line rate on all Ports for performance-hungry applications, *such as* servers and switch fabrics. The low latency enables applications to achieve high throughput and performance. In addition to low latency, the PEX 8649 supports a Packet Payload size of up to 2,048 bytes, enabling users to achieve even higher throughput.

2.1.4.1 Data Payloads

The Data Payloads are variable length with a maximum of 2,048 bytes, as defined by the *Maximum Payload Size* field (available sizes are 128, 256, 512, 1,024, and 2,048, depending upon the quantity of enabled Ports). Read Requests ***do not*** include a Data Payload.

Note: *Refer to the* ***Device Control*** *register Maximum Payload Size field (offset 70h[7:5]) for Maximum Payload Size Port limitations.*

2.1.4.2 Cut-Thru Mode

Cut-Thru mode can reduce latency, especially for longer packets, because the entire packet does not need to be stored before being forwarded. Instead, after the Header is decoded, the packet can be immediately forwarded. The PEX 8649 is designed to cut through TLPs, to and from every Port. By default, all Ports are enabled for Cut-Thru. Cut-Thru mode can be disabled for all Ports, by Clearing the **Debug Control** register *Cut-Thru Enable* bit (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 350h[11]).

Cut-Thru mode, if enabled, is supported for the PEX 8649's NT Port Link Interface, if the PEX 8649 is configured for NT mode (Base mode only).

Note: *The* ***Debug Control*** *register Cut-Thru Enable bit affects the entire switch. If Cut-Thru is enabled, all Ports use Cut-Thru. If Cut-Thru is* ***not*** *enabled, no Ports use Cut-Thru.*

Caution: One of the drawbacks to using Cut-Thru mode is that the TLP is not known to be good until the last byte. If the TLP proves to be bad, the Cut-Thru packet must be discarded. If the TLP has already been forwarded to another device, that TLP will be framed with an EDB (End Data Bad), as opposed to the standard END.

2.1.5 Virtual Channel and Traffic Classes

The PEX 8649 supports one Virtual Channel (VC0) and eight Traffic Classes (TC[7:0]). VC0 and TC0 are required by the *PCI Express Base r2.0*, and configured at device start-up.

2.1.6 Data Integrity

To enable designs that require **guaranteed error-free packets**, the PEX 8649 provides **End-to-end Cyclic Redundancy Check** (ECRC) protection and **Poison** bit support, as well as **Error-Correcting Code** (ECC) protection on the internal data paths and memory (RAM). ECC maintains packet integrity through the PEX 8649, by providing automatic correction of any 1-bit errors. These features are optional in the *PCI Express Base r2.0*; however, PLX provides them across its entire ExpressLane PCI Express Gen 2 switch product line.

2.1.7 Configuration Flexibility

The PEX 8649 provides several ways to configure its operations. *For example*, the PEX 8649 can be configured through Strapping balls, Host software, an optional serial EEPROM, or the I^{2}C Slave interface. Additionally, the I^{2}C Slave interface allows for easy debug during the Development phase, performance monitoring during the Operation phase, and driver or software upgrade.

2.1.8 Interoperability

The PEX 8649 is designed to be fully compliant with the *PCI Express Base r2.0*, and is backward-compatible to the *PCI Express Base r1.1* and *PCI Express Base r1.0a*. Additionally, the switch supports **auto-negotiation**, **Lane reversal**, and **polarity reversal**, for maximum board design and board layout flexibility. Furthermore, the PEX 8649 is designed to be interoperable with many popular motherboards and server boards with PCI Express connections, and PCI Express endpoints (Ethernet, RAID Controllers), as well as PLX's family of PCI Express switches and bridges. All PLX ExpressLane devices undergo thorough interoperability testing at PLX's **Interoperability Lab** and compliance testing at the **PCI-SIG Compliance Workshop**, to ensure compatibility with PCI Express devices in the market.

2.1.9 Low Power with Granular SerDes Control

The PEX 8649 provides **low-power** capability that is fully compliant with the *PCI Express Base r2.0* and *PCI Power Mgmt. r1.2* Power Management (PM) specifications. Unused SerDes can be automatically powered down, to further reduce power consumption.

The PEX 8649 supports **SerDes output software control**, to allow power and signal strength optimization within a system. The PLX SerDes implementation supports four power levels – *Off*, *Low*, *Typical*, and *High*. The SerDes block also supports **Loopback modes** and **Advanced Error Reporting**, which enables efficient system debug and management.

2.1.10 Dynamic Lane Reversal

The PEX 8649 supports dynamic Lane reversal during the Link training process. Lane reversal capability allows flexibility in determining board routing, so that PCI Express components can be connected without having to crisscross wires. If the wiring of Lanes to a device is reversed (on both Transmitters and Receivers), only one of the two connected devices must support Lane reversal.

Either of the outside Lanes (Transmitter and Receiver pairs) of the PEX 8649 programmed Link width must be identified as being Lane 0. During Link training, both devices on the Link negotiate the Lane numbering. During the Link Training and Status State Machine (LTSSM)'s *Configuration* state, the upstream device sends TS1 Ordered-Sets, in which each connected Lane is identified by a consecutive Lane Number, starting with Lane 0 corresponding to the physical Lane Number of the Port.

The Port reverses its Lane Numbers and attempts to re-train when any of the following conditions occur:

- No Receiver is detected on preferred Lane 0
- No valid Training Sets are received on preferred Lane 0 during the LTSSM's *Polling* state
- TS1 with a non-zero Lane Number Port is received on the Port's Lane 0

To confirm successful Lane Number negotiation, both devices exchange TS2 Ordered-Sets with identical Lane Numbers on each connected Lane.

2.1.11 Hot Plug for High Availability

Hot Plug capability allows users to replace hardware modules and perform maintenance, without having to power down the system. The PEX 8649 Hot Plug Capability and Advanced Error Reporting features make the switch suitable for High-Availability (HA) applications. The PEX 8649 supports both Parallel and Serial Hot Plug. Parallel Hot Plug is supported on any of two Transparent downstream Ports, and/or Serial Hot Plug is supported on a maximum of 11 downstream Ports.

For further details, refer to Chapter 10, "Hot Plug Support."

2.1.12 Fully Compliant Power Management

The PEX 8649 supports Link (L0, L0s, L1, L2/L3 Ready, and L3) and Device (D0 and D3hot) PM states, in compliance with the *PCI Express Base r2.0* and *PCI Power Mgmt. r1.2* PM specifications.

For further details, refer to Chapter 11, "Power Management."

2.1.13 General-Purpose Input/Output Signals

The PEX 8649 contains 20 General-Purpose Input/Output (GPIO) balls and associated registers, that can be programmed to function as GPIO, Link Status (PORT_GOOD) indicators, and/or Interrupt inputs. Default functionality is GPIO input; however, serial EEPROM, I^{2}C/SMBus, and/or software can program the GPIO registers to define functionality for each I/O. Default functionality can also be modified by the logical value of the STRAP_TESTMODE[3:0] inputs, sampled at Fundamental Reset. Because typical designs implement PORT_GOOD functionality for enabled Ports, GPIO[11:0] are renamed as PEX_PORT_GOOD[23:16, 3:0]# outputs, respectively.

For further details, refer to the GPIO[31:24], PEX_PORT_GOOD*x*#, and STRAP_TESTMODE[3:0] signal descriptions in Section 3.4.7, "Device-Specific Signals," Section 3.4.4, "Strapping Signals," and Section 9.5, "General-Purpose Input/Output."

2.1.14 *performance*PAK

Exclusive to PLX, *performance*PAK is a suite of unique and innovative performance features that enable PLX’s Gen 2 switches to be the highest-performing Gen 2 switches available in the market today. The *performance*PAK features consist of Read Pacing, Multicast, and Dynamic Buffer Pool.

2.1.14.1 Read Pacing

The Read Pacing feature allows users to throttle the number of Read Requests being made by downstream devices. When a downstream device requests several long Reads back-to-back, the Root Complex services the Read Requests from this downstream Port in a sequential order. If this Port has a narrow Link and is therefore slow in receiving these Read packets from the Root Complex, other downstream Ports may become starved, thus negatively impacting performance. The feature enhances performance by allowing for the adequate servicing of all downstream devices, by intelligent handling of Read Requests.

For further details, refer to Section 8.5, “Read Pacing.”

2.1.14.2 Multicast – All Modes Except Legacy NT

Multicast (MC) allows programs to concurrently write the same data to a group of multiple destinations. When Posted Memory Write and/or Address Routed Message TLPs entering the PEX 8649 are addressed to the MC Address range (*MC BARs*), the PEX 8649 automatically generates and transmits, if enabled, a copy of the original TLP (referred to as the *MC Copy TLP*) to the destination Ports. The MC Address space is divided into *MC Groups (MCG)*, defined by using *MC Base Address* and *MC Index Position*. Each PEX 8649 Port can elect to receive an MC Copy TLP by belonging to an *MCG*, by Setting the corresponding *MC Receive* bit. An MC TLP can be blocked using the *MC Block All* bit, if required. *MC Overlay Bar* can be used to replace the original MC TLP’s address to a Unicast Address space, if the endpoint does not support MC.

For further details, refer to Section 8.6, “Multicast – All Modes Except Legacy NT.”

2.1.14.3 Dynamic Buffer Pool

The PEX 8649 uses a dynamic buffer pool for FC management, which uses a common pool of FC Credits that is shared among other Ports within a Station. This shared buffer pool is user-programmable, so FC credits can be allocated among the enabled Ports, as needed. Not only does this prevent wasted buffers and inappropriate buffer assignments, any un-allocated buffers remain in the common buffer pool, which can then be used by other Ports within the same Station, for faster FC credit updates.

2.1.15 *vision*PAK

Another PLX exclusive, *vision*PAK is a debug diagnostics suite of integrated hardware and software instruments that users can use to help bring their systems to market faster. *vision*PAK features consist of Performance Monitoring, Error Injection, SerDes Loopback, SerDes Eye Capture, and more.

2.1.15.1 Performance Monitoring

The PEX 8649's real-time performance monitoring allows users to literally "see" ingress and egress performance on each Port as traffic passes through the switch, using PLX's Software Development Kit (SDK). The monitoring is completely passive, and therefore, has no effect on overall system performance. Internal counters provide extensive granularity down to traffic and packet type, and even allow for the filtering of traffic (*that is*, count only Memory Writes).

2.1.15.2 Error Injection

Using the PEX 8649's Error Injection feature, users can inject malformed packets and/or Fatal errors into their system, then evaluate the system's ability to detect and recover from such errors.

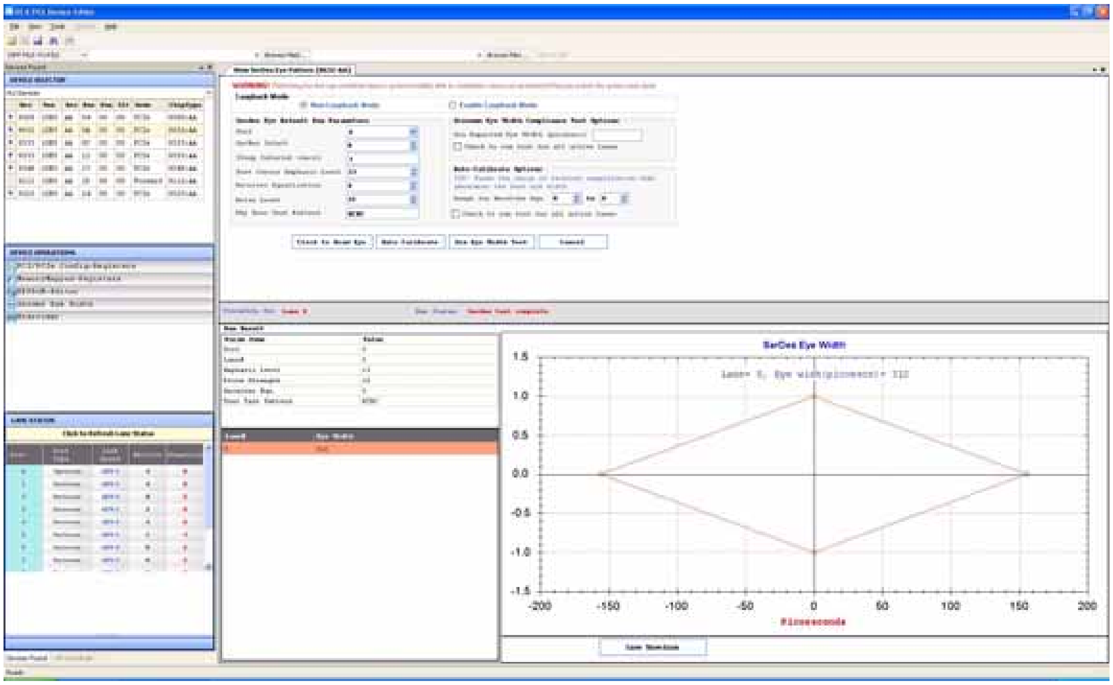
2.1.15.3 SerDes Loopback

The PEX 8649 supports External Tx, Recovered Clock, and Recovered Data Loopback modes.

2.1.15.4 SerDes Eye Capture

Users can evaluate their system's signal integrity at the Physical Layer (PHY), using the PEX 8649's SerDes Eye Capture feature. Using PLX's SDK, users can view the Receiver eye width of any Lane on the PEX 8649. Users can then modify SerDes settings and see the impact on the Receiver eye. Figure 2-3 presents a screen shot of the SDK's SerDes Eye Capture feature.

Figure 2-3. PLX SDK SerDes Eye Capture Feature



2.2 Applications

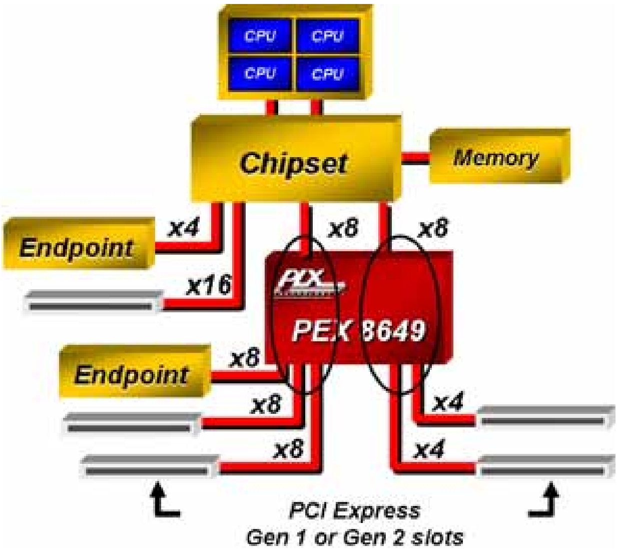
Suitable for **Host-centric** and **peer-to-peer traffic**, the PEX 8649 can be configured for a wide variety of form factors and applications.

2.2.1 Host-Centric Fan-Out

The PEX 8649, with its versatile symmetric or asymmetric Lane configuration capability, allows user-specific tuning to a variety of Host-centric applications.

Figure 2-4 illustrates a typical **server** design where, in a quad- or multi-processor system, users can assign endpoints/slots to CPU cores, to distribute the system load. The packets directed to different CPU cores go to different (user-assigned) PEX 8649 upstream Port(s), providing better queuing and load-balancing capability, for higher performance. Conversely, the PEX 8649 can also be used in Base mode, to simply fan-out to endpoints.

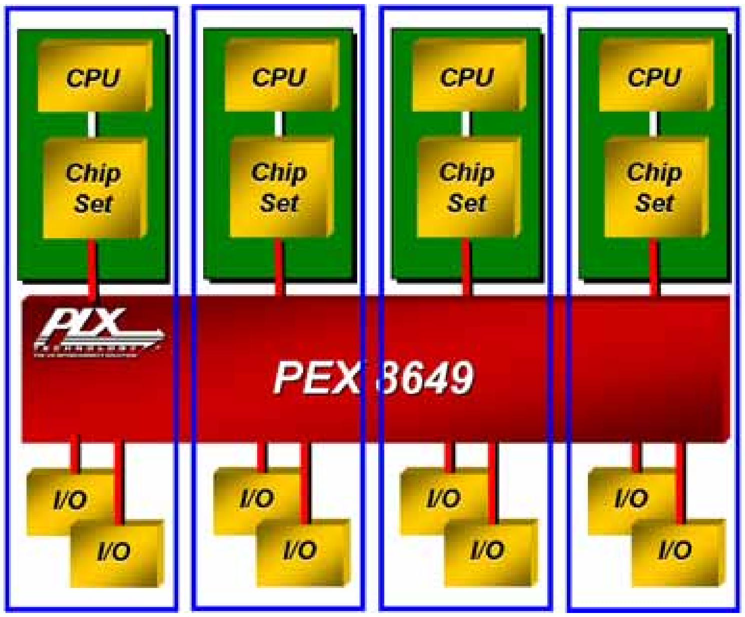
Figure 2-4. Host-Centric, Dual-Upstream



2.2.2 Multi-Host Systems

In Multi-Host mode, the PEX 8649 can concurrently support up to four Hosts. By creating up to four virtual switches, the PEX 8649 allows up to four Hosts to fan-out to their respective endpoints. This reduces the number of switches required for fan-out, saving precious board space and power consumption. In Figure 2-5, the PEX 8649 is shared by four different servers (Hosts), with each server running its own applications (I/Os). The PEX 8649 assigns the endpoints to the appropriate Host, and isolates them from the other Hosts.

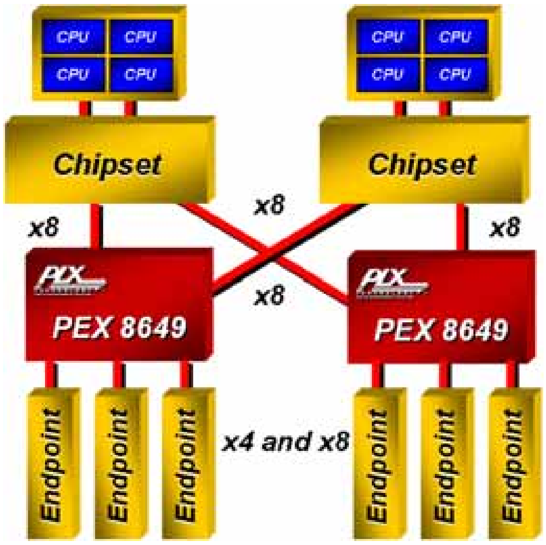
Figure 2-5. Multi-Host Systems



2.2.3 Host Failover

The PEX 8649 can also be used in applications where Host Failover is required. In the application illustrated in Figure 2-6, two Hosts can be simultaneously active and controlling their own domains, while exchanging status information through **Doorbell** registers or the I^{2}C Slave interface. The devices can be programmed to trigger failover if the heartbeat information is not provided. In the event of a failure, the surviving device will reset the endpoints connected to the failing CPU, then enumerate them within its own domain, without impacting the operation of endpoints already within its domain.

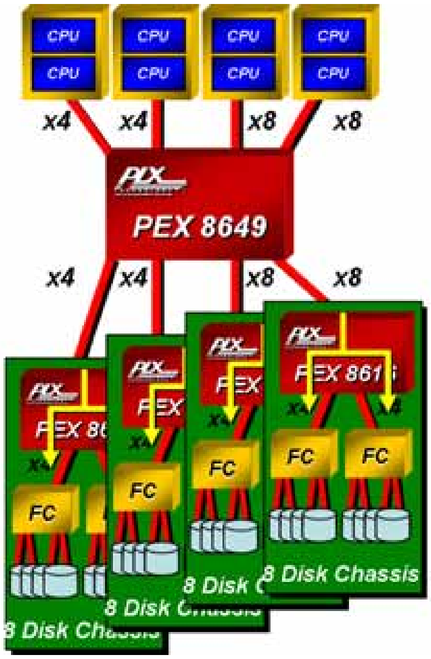
Figure 2-6. Host Failover



2.2.4 *N*+1 Failover in Storage Systems

The PEX 8649's Multi-Host feature can also be used to develop storage array clusters, where each Host manages a set of storage devices, independent of the other Hosts. Users can designate one of the Hosts as the Failover Host for all the other Hosts, while actively managing its own endpoints. The Failover Host communicates with the other Hosts for status/heartbeat information, and executes a Failover event if/when a Failover event is triggered. (Refer to Figure 2-7.)

Figure 2-7. *N*+1 Failover



2.3 Software Usage Model

From the system model viewpoint, each PCI Express Port is a virtual PCI-to-PCI bridge, with its own set of PCI Express Configuration registers. The recommended upstream Port in Base mode is Port 0; however, any Port can be configured as the upstream Port through optional configuration, by way of a serial EEPROM, the I^{2}C Slave interface, and/or Strapping balls. The BIOS and/or Host can configure the other Ports, by way of the upstream Port, using Conventional PCI enumeration. In Virtual Switch mode, any Port within the same virtual hierarchy can be designated as the upstream Port for that particular hierarchy.

2.3.1 System Configuration

The virtual PCI-to-PCI bridges within the PEX 8649 are compliant to the PCI and PCI Express system models. The Configuration Space registers (CSRs) in a virtual primary/secondary PCI-to-PCI bridge are accessible by Type 0 or Type 1 Configuration Requests, through the virtual primary bus interface (matching Bus Number, Device Number, and Function Number). Assuming the Bus Number for the upstream Port is 1, the PEX 8649's BDF (Bus, Device, Function) for F0 and F1 is 1/0/0 and 1/0/1, respectively.

2.3.2 Interrupt Sources and Events

The PEX 8649 supports the INT*x* Interrupt Message type (compatible with *PCI r3.0* Interrupt signals) or Message Signaled Interrupts (MSIs), when enabled. The PEX 8649 generates interrupts/Messages for the following:

- Hot Plug or Link State events
- Device-Specific errors
- GPIO-generated events
- NT Doorbell-generated events (Base mode only)
- Management Port Doorbell events (Transparent Ports and NT Port Virtual Interface only)
- Management Link Status event (Transparent Ports and NT Port Virtual Interface only)
- Baseline and Advanced Error Reporting

Internally generated interrupts and interrupts forwarded from downstream Ports are re-mapped and collapsed at the upstream Port(s).

Chapter 3 Signal Ball Description

3.1 Introduction

This chapter provides descriptions of the 676 PEX 8649 signal balls. The signal name, type, location, and a brief description are provided for each signal ball. A map of the PEX 8649's physical layout is also provided.

3.2 Abbreviations

The following abbreviations are used in the signal tables provided in this chapter.

Table 3-1. Ball Assignment Abbreviations

Abbreviation	Description
#	Active-Low signal
A	Analog Input signal
APWR	Power (VDD10A) balls for SerDes Analog circuits
CMLCLKn[a]	Differential low-voltage, high-speed, CML negative Clock inputs
CMLCLKp[a]	Differential low-voltage, high-speed, CML positive Clock inputs
CMLRn	Differential low-voltage, high-speed, CML negative Receiver inputs
CMLRp	Differential low-voltage, high-speed, CML positive Receiver inputs
CMLTn	Differential low-voltage, high-speed, CML negative Transmitter outputs
CMLTp	Differential low-voltage, high-speed, CML positive Transmitter outputs
CPWR	1.0V Power (VDD10) balls for low-voltage Core circuits
GND	Common Ground (VSS) for all circuits
I	Input
I/O	Bidirectional (Input or Output)
I/OPWR	2.5V Power (VDD25) balls for Input and Output interfaces
O	Output
OD	Open Drain output
PD	Weak internal pull-down resistor
PLLPWR	2.5V Power (VDD25A) balls for Phase-Locked Loop (PLL) circuits
PU	Weak internal pull-up resistor
SerDes	Serializer/De-Serializer differential low-voltage, high-speed, I/O signal pairs (negative and positive)
STRAP	Signals used for PEX 8649 configuration, operational mode setting, and ***Factory Test***; these signals generally are not toggled at runtime

[a] *For REFCLK input, CML source is recommended; however, LVDS source is supported.*

3.3 Internal Pull-Up/Pull-Down Resistors

The PEX 8649 contains I/O buffers that have weak internal pull-up or pull-down resistors, indicated in this chapter by PU or PD, respectively, in the signal ball tables (**Type** column). If a signal with this notation is used and no board trace is connected to the ball, the internal resistor is usually sufficient to keep the signal from toggling. However, if a signal with this notation is not used, but is connected to a board trace and is not used nor driven by an external source at all times, the internal resistors might not be strong enough to hold the signal in the inactive state. In cases such as these, it is recommended that the signal be pulled or tied High to VDD25 or Low to VSS (GND), as appropriate, through a 3KΩ to 10KΩ resistor.

Table 3-2 lists the internal pull-up and pull-down resistor values.

Table 3-2. Internal Resistor Values

Internal Resistor	Minimum	Typical	Maximum	Units
PU	74K	111K	178K	Ω
PD	62K	99K	179K	Ω

3.4 Signal Ball Descriptions

Note: *If there is more than one ball per signal name that includes a numbered range, the locations are listed in the same sequence in which the range is listed, starting at the top row, from left to right. For example, PEX_PERn15 is located at AC22, PEX_PERn14 is located at AC17, and so forth.*

If there is more than one ball per signal name that does not include a numbered range (such as VDD10), the locations are listed in ascending alphanumeric order.

The PEX 8649 signals are divided into the following groups:

- PCI Express Signals
- Hot Plug Signals
  - Parallel Hot Plug Signals
  - Serial Hot Plug Signals
- Serial EEPROM Signals
- Strapping Signals
- JTAG Interface Signals
- I^{2}C/SMBus Slave Interface Signals
- Device-Specific Signals
- External Resistor Signals
- No Connect Signals
- Power and Ground Signals

3.4.1 PCI Express Signals

Table 3-3 defines the PCI Express SerDes and Control signals.

Table 3-3. PCI Express Signals – 195 Balls

Signal Name	Type	Location	Description
PEX_PERn[15:0]	CMLRn	AC22, AC21, AC20, AC19, AC17, AC16, AC15, AC14, AC13, AC12, AC11, AC10, AC8, AC7, AC6, AC5	**Negative Half of PCI Express Receiver Differential Signal Pairs for Station 0 (16 Balls)**
PEX_PERn[31:16]	CMLRn	D13, D12, D11, D10, D8, D7, D6, D5, J4, K4, L4, M4, P4, R4, T4, U4	**Negative Half of PCI Express Receiver Differential Signal Pairs for Station 5 (16 Balls)**
PEX_PERn[47:32]	CMLRn	D14, D15, D16, D17, D19, D20, D21, D22, J23, K23, L23, M23, P23, R23, T23, U23	**Negative Half of PCI Express Receiver Differential Signal Pairs for Station 4 (16 Balls)**
PEX_PERp[15:0]	CMLRp	AB22, AB21, AB20, AB19, AB17, AB16, AB15, AB14, AB13, AB12, AB11, AB10, AB8, AB7, AB6, AB5	**Positive Half of PCI Express Receiver Differential Signal Pairs for Station 0 (16 Balls)**
PEX_PERp[31:16]	CMLRp	E13, E12, E11, E10, E8, E7, E6, E5, J5, K5, L5, M5, P5, R5, T5, U5	**Positive Half of PCI Express Receiver Differential Signal Pairs for Station 5 (16 Balls)**
PEX_PERp[47:32]	CMLRp	E14, E15, E16, E17, E19, E20, E21, E22, J22, K22, L22, M22, P22, R22, T22, U22	**Positive Half of PCI Express Receiver Differential Signal Pairs for Station 4 (16 Balls)**
PEX_PERST#	I PU	AC1	**PCI Express Reset** Used to cause a Fundamental Reset. **Base Mode** Refer to Section 5.1, “Resets – Base Mode,” for further details. **Virtual Switch Mode** In Virtual Switch mode, PEX_PERST# assertion resets all virtual switches. Refer to Section 5.2, “Resets – Virtual Switch Mode,” for further details. ***Note:*** *VSx_PERST# signals, defined in Table 3-11, are the Reset inputs for individual virtual switches.*

Table 3-3. PCI Express Signals – 195 Balls *(Cont.)*

Signal Name	Type	Location	Description
PEX_PETn[15:0]	CMLTn	AF22, AF21, AF20, AF19, AF17, AF16, AF15, AF14, AF13, AF12, AF11, AF10, AF8, AF7, AF6, AF5	**Negative Half of PCI Express Transmitter Differential Signal Pairs for Station 0 (16 Balls)**
PEX_PETn[31:16]	CMLTn	A13, A12, A11, A10, A8, A7, A6, A5, J1, K1, L1, M1, P1, R1, T1, U1	**Negative Half of PCI Express Transmitter Differential Signal Pairs for Station 5 (16 Balls)**
PEX_PETn[47:32]	CMLTn	A14, A15, A16, A17, A19, A20, A21, A22, J26, K26, L26, M26, P26, R26, T26, U26	**Negative Half of PCI Express Transmitter Differential Signal Pairs for Station 4 (16 Balls)**
PEX_PETp[15:0]	CMLTp	AE22, AE21, AE20, AE19, AE17, AE16, AE15, AE14, AE13, AE12, AE11, AE10, AE8, AE7, AE6, AE5	**Positive Half of PCI Express Transmitter Differential Signal Pairs for Station 0 (16 Balls)**
PEX_PETp[31:16]	CMLTp	B13, B12, B11, B10, B8, B7, B6, B5, J2, K2, L2, M2, P2, R2, T2, U2	**Positive Half of PCI Express Transmitter Differential Signal Pairs for Station 5 (16 Balls)**
PEX_PETp[47:32]	CMLTp	B14, B15, B16, B17, B19, B20, B21, B22, J25, K25, L25, M25, P25, R25, T25, U25	**Positive Half of PCI Express Transmitter Differential Signal Pairs for Station 4 (16 Balls)**
PEX_REFCLKn	CMLCLKn	AF9	**Negative Half of 100-MHz PCI Express Reference Clock Input Signal Pair** PEX_REFCLKn must be AC-coupled. Use a 0.01 to 0.1 µF capacitor.
PEX_REFCLKp	CMLCLKp	AE9	**Positive Half of 100-MHz PCI Express Reference Clock Input Signal Pair** PEX_REFCLKp must be AC-coupled. Use a 0.01 to 0.1 µF capacitor.

3.4.2 Hot Plug Signals

The PEX 8649 includes signals for both Parallel and Serial Hot Plug support.

Parallel Hot Plug can be implemented on any of two Transparent downstream Ports, as selected by the **Parallel Hot Plug Control** register (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 3A4h[15:8 and 23:16] for Parallel Hot Plug Controllers B and C, respectively).

Serial Hot Plug can be implemented on any Transparent downstream Port. If a Transparent downstream Port is both Parallel- and Serial Hot Plug-capable, the Serial Hot Plug Controller is used, by default, unless the Port's **Power Management Hot Plug User Configuration** register *Serial Hot Plug Override Parallel Disable* bit (offset F70h[19]) is Set.

Hot Plug signals are enabled, configured, and accessed through the **Slot Capability** and **Slot Status and Control** registers (Downstream Ports, offsets 7Ch and 80h, respectively). Also, each Port's **Power Management Hot Plug User Configuration** register provides additional Device-Specific configuration and control, for both Parallel and Serial Hot Plug implementations.

Both signal types are discussed in the sections that follow.

3.4.2.1 Parallel Hot Plug Signals

The PEX 8649 includes 10 signal balls per Hot Plug-capable Port that supports the Parallel Hot Plug Controller (HP_), as defined in Table 3-4. These signals are active only for Hot Plug-capable Transparent downstream Ports configured at start-up.

For further details regarding Hot Plug, refer to Chapter 10, "Hot Plug Support."For a list of the default Parallel Hot Plug Ports, refer to Section 10.8.2, "Default Parallel Hot Plug Ports – Virtual Switch Mode."

Notes: *All Parallel Hot Plug signals are I/O; however, their logical operation is either input or output, as described for each signal.*

All Parallel Hot Plug signals are duplicated for each Hot Plug-capable Port, as B and C signals, which map to any Transparent downstream Port, as selected by the ***Parallel Hot Plug Control*** *register (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 3A4h[15:8 and 23:16] for Parallel Hot Plug Controllers B and C, respectively).*

Table 3-4. Parallel Hot Plug Signals[a] for Ports C, B – 20 Balls

Signal Name	Type	Location	Description
HP_ATNLED_[C, B]#	I/O PU	B25, AB1	**Hot Plug Attention LED Outputs (2 Balls)** Active-Low Slot Control Logic output that is used to drive the Attention Indicator. Output is asserted Low to turn On (illuminate) the LED. Enabled when the **Slot Capability** register *Attention Indicator Present* bit (Downstream Ports, offset 7Ch[3]) is Set and controlled by the **Slot Control** register *Attention Indicator Control* field (Downstream Ports, offset 80h[7:6]). When software writes to the *Attention Indicator Control* field, a Command Completed interrupt can be generated to notify the Host that the command has been executed. When the following conditions exist: • **Slot Capability** register *Attention Indicator Present* bit (Downstream Ports, offset 7Ch[3]) is Set, and • **Slot Control** register *Command Completed Interrupt Enable* bit is not masked (Downstream Ports, offset 80h[4] is Set), and • **Slot Control** register *Hot Plug Interrupt Enable* bit (Downstream Ports, offset 80h[5]) is Set, an interrupt (MSI, INT*x* Message, or PEX_INTA# and/or VS*x*_PEX_INTA# output, all mutually exclusive, on a per-Port basis) can be generated to the Host. **If HP_ATNLED_*x*# are used, each requires an external current-limiting resistor.** ***Note:*** *Although this is an I/O signal, its logical operation is output.*

Table 3-4. Parallel Hot Plug Signals[a] for Ports C, B – 20 Balls *(Cont.)*

Signal Name	Type	Location	Description
HP_BUTTON_[C, B]#	I/O PU	C25, AB3	**Hot Plug Attention Button Inputs (2 Balls)** Active-Low Slot Control Logic input that is connected directly to the Attention Button, with input assertion status latched in the **Slot Status** register *Attention Button Pressed* bit (Downstream Ports, offset 80h[16]). Enabled when the **Slot Capability** register *Attention Button Present* bit (Downstream Ports, offset 7Ch[0]) is Set. When the following conditions exist: • HP_BUTTON_*x*# is not masked (**Slot Control** register *Attention Button Pressed Enable* bit (Downstream Ports, offset 80h[0]) is Set), and • **Slot Capability** register *Hot Plug Capable* bit (Downstream Ports, offset 7Ch[6]) is Set, and • **Slot Control** register *Hot Plug Interrupt Enable* bit (Downstream Ports, offset 80h[5]) is Set, an interrupt (MSI, INT*x* Message, or PEX_INTA# and/or VS*x*_PEX_INTA# output, all mutually exclusive, on a per-Port basis) can be generated, to notify the Host of intended board insertion or removal. ***Notes:*** *HP_BUTTON_x# is internally de-bounced, but must remain stable for at least 10 ms.* *Although this is an I/O signal, its logical operation is input.*
HP_CLKEN_[C, B]#	I/O PU	F24, AE1	**Hot Plug Reference Clock Enable Outputs (2 Balls)** Active-Low Slot Control Logic output that, when enabled, controls the connection of the external REFCLK to the slot. Enabled when the **Slot Capability** register *Power Controller Present* bit (Downstream Ports, offset 7Ch[1]) is Set, and controlled by the **Slot Control** register *Power Controller Control* bit (Downstream Ports, offset 80h[10]). The time delay from HP_PWREN_*x* output assertion to HP_CLKEN_*x*# output assertion is programmable (through serial EEPROM load) from 128 to 512 ms, in the *HPC* T_{pepv} field (offset F70h[4:3]). When this register field is programmed to 00b (default), HP_PWR_GOOD_*x* input assertion controls the time delay from HP_PWREN_*x* output assertion to HP_CLKEN_*x*# output assertion. ***Note:*** *Although this is an I/O signal, its logical operation is output.*

Table 3-4. Parallel Hot Plug Signals[a] for Ports C, B – 20 Balls *(Cont.)*

Signal Name	Type	Location	Description
HP_MRL_[C, B]#	I/O PU	G21, AB2	**Hot Plug Manually Operated Retention Latch Sensor Inputs (2 Balls)** Active-Low Slot Control Logic input that is connected directly to an optional Manually operated Retention Latch (MRL) Sensor that is logic Low when the latch is closed. Enabled when the **Slot Capability** register *MRL Sensor Present* bit (Downstream Ports, offset 7Ch[2]) is Set. When enabled, HP_MRL_*x*# input assertion enables Hot Plug output sequencing to turn On the slot's power (HP_PWREN_*x* and HP_PWRLED_*x*#) and clock (HP_CLKEN_*x*#), and de-assert Reset (HP_PERST_*x*#) after reset, as illustrated in Figure 10-2, "Hot Plug Outputs When Power Controller Present and Power Controller Control Bits Are Cleared," or under software control. A change in the HP_MRL_*x*# signal state is latched in the **Slot Status** register *MRL Sensor Changed* bit (Downstream Ports, offset 80h[18]), and the state change can assert an interrupt to notify the Host of a change in the MRL Sensor state. When the following conditions exist: • HP_MRL_*x*# is not masked (**Slot Control** register *MRL Sensor Changed Enable* bit (Downstream Ports, offset 80h[2]) is Set), and • **Slot Control** register *Hot Plug Interrupt Enable* bit (Downstream Ports, offset 80h[5]) is Set, an interrupt (MSI, INT*x* Message, or PEX_INTA# and/or VS*x*_PEX_INTA# output, all mutually exclusive, on a per-Port basis) can be generated. If the associated Hot Plug-capable Transparent downstream Port connects to a PCI Express board slot that does not implement an MRL Sensor, HP_MRL_*x*# is typically connected to HP_PRSNT_*x*# and a pull-up resistor, with the common node connected to the PRSNT2# signal(s) at the slot. If the associated Hot Plug-capable Transparent downstream Port instead connects directly to a device, and Hot Plug signals (such as HP_PERST_*x*#) are used, pull HP_MRL_*x*# Low to enable the automatic Hot Plug output sequencing following switch Reset (PEX_PERST# or Hot Reset) de-assertion. Otherwise, if Hot Plug signals are not used, pull HP_MRL_*x*# High, to hold the Hot Plug outputs in their inactive states. When HP_MRL_*x*# is enabled and the input is sampled High on a powered slot, REFCLK to the slot is automatically disconnected and the slot power is automatically turned Off, as illustrated in Figure 10-3, "Hot Plug Automatic Power-Down Sequence." ***Notes:*** *HP_MRL_x# is internally de-bounced, but must remain stable for at least 10 ms. HP_MRL_x#, if enabled, is not de-bounced when sampled immediately after reset.* *Although this is an I/O signal, its logical operation is input.*

Table 3-4. Parallel Hot Plug Signals[a] for Ports C, B – 20 Balls *(Cont.)*

Signal Name	Type	Location	Description
HP_PERST_[C, B]#	I/O PU	G22, AD1	**Hot Plug Reset Outputs (2 Balls)** Active-Low Slot Control Logic output that is used to reset the slot. When the **Slot Capability** register *Power Controller Present* bit (Downstream Ports, offset 7Ch[1]) is Set, the HP_PERST_*x*# output state can be controlled by software, using the **Slot Control** register *Power Controller Control* bit (Downstream Ports, offset 80h[10]). ***Note:*** *Although this is an I/O signal, its logical operation is output.*
HP_PRSNT_[C, B]#	I/O PU	D25, W5	**Hot Plug PRSNT2# Inputs (2 Balls)** Active-Low Slot Control Logic input that connects to the slot's PRSNT2# signal, which on the add-in board connects to the slot's PRSNT1# signal, which is typically grounded on the motherboard. A change in the HP_PRSNT_*x*# input state is latched in the **Slot Status** register *Presence Detect Changed* bit (Downstream Ports, offset 80h[19]), and the state change can assert an interrupt to notify the Host of board presence or absence. When the following conditions exist: • HP_PRSNT_*x*# is not masked (**Slot Control** register *Presence Detect Changed Enable* bit (Downstream Ports, offset 80h[3], is Set), and • **Slot Control** register *Hot Plug Interrupt Enable* bit (Downstream Ports, offset 80h[5]) is Set, an interrupt (MSI, INT*x* Message, or PEX_INTA# and/or VS*x*_PEX_INTA# output, all mutually exclusive, on a per-Port basis) can be generated. ***Notes:*** *HP_PRSNT_x# is internally de-bounced, but must remain stable for at least 10 ms.* *Although this is an I/O signal, its logical operation is input.*

Table 3-4. Parallel Hot Plug Signals[a] for Ports C, B – 20 Balls *(Cont.)*

Signal Name	Type	Location	Description
HP_PWREN_[C, B]	I/O PD	D24, AC2	**Hot Plug Power Enable Outputs (2 Balls)** Active-High Slot Control Logic output that controls the slot power state. When this output is High, power is enabled to the slot. Enabled when the **Slot Capability** register *Power Controller Present* bit (Downstream Ports, offset 7Ch[1]) is Set. When software turns the slot's Power Controller On or Off (**Slot Control** register *Power Controller Control* bit (Downstream Ports, offset 80h[10])), a Command Completed interrupt can be generated to notify the Host that the command has been executed. When the following conditions exist: • **Slot Control** register *Command Completed Interrupt Enable* bit is not masked (Downstream Ports, offset 80h[4], is Set), and • **Slot Control** register *Hot Plug Interrupt Enable* bit (Downstream Ports, offset 80h[5]) is Set, an interrupt (MSI, INT*x* Message, or PEX_INTA# and/or VS*x*_PEX_INTA# output, all mutually exclusive, on a per-Port basis) can be generated to the Host. When HP_MRL_*x*# is enabled (**Slot Capability** register *MRL Sensor Present* bit (Downstream Ports, offset 7Ch[2]) is Set), HP_MRL_*x*# input assertion enables Hot Plug output sequencing to turn On the slot's power, by asserting HP_PWREN_*x* after reset, as illustrated in Figure 10-2, "Hot Plug Outputs When Power Controller Present and Power Controller Control Bits Are Cleared," or under software control. ***Notes:*** *HP_PWREN_x polarity is inverted with respect to HP_PWRENx# functionality in PLX ExpressLane Gen 1 switches.* *Although this is an I/O signal, its logical operation is output.*
HP_PWRFLT_[C, B]#	I/O PU	B26, AC3	**Hot Plug Power Fault Inputs (2 Balls)** Active-Low Slot Control Logic input that, when asserted Low, indicates that the slot's external Power Controller detected a power fault on one or more supply rails. Enabled when the **Slot Capability** register *Power Controller Present* bit (Downstream Ports, offset 7Ch[1]) is Set, and input assertion status is latched in the **Slot Status** register *Power Fault Detected* bit (Downstream Ports, offset 80h[17]). When the following conditions exist: • HP_PWRFLT_*x*# is not masked (**Slot Control** register *Power Fault Detector Enable* bit (Downstream Ports, offset 80h[1]) is Set), and • **Slot Control** register *Hot Plug Interrupt Enable* bit (Downstream Ports, offset 80h[5]) is Set, an interrupt (MSI, INT*x* Message, or PEX_INTA# and/or VS*x*_PEX_INTA# output, all mutually exclusive, on a per-Port basis) can be generated, to notify the Host of a power fault. ***Notes:*** *If HP_PWREN_x and HP_CLKEN_x# are not used, HP_PWRFLT_x# can be used as a general-purpose input with status reflected in the* ***Slot Status*** *register Power Fault Detected bit (Downstream Ports, offset 80h[17]), provided that the* ***Slot Capability*** *register Power Controller Present bit (Downstream Ports, offset 7Ch[1]) is Set.* *Although this is an I/O signal, its logical operation is input.*

Table 3-4. Parallel Hot Plug Signals[a] for Ports C, B – 20 Balls *(Cont.)*

Signal Name	Type	Location	Description
HP_PWR_GOOD_[C, B]	I/O PD	F25, Y3	**Hot Plug Power Good Inputs (2 Balls)** Active-High (default) input that, when enabled (default), causes the Slot Control Logic to delay HP_CLKEN_*x*# output assertion to turn On REFCLK to the slot, until HP_PWR_GOOD_*x* input is asserted to indicate that the installed module's power supplies are active and stable. Signal polarity can be changed to Active-Low, by programming the serial EEPROM to Set the Port's *HP_PWR_GOOD_x Active-Low Enable* bit (offset F70h[6]). Polarity must not be changed by I^2C, because that is too slow for initialization. HP_PWR_GOOD_*x* is disabled when the Port's *HPC* T_{pepv} field (offset F70h[4:3]) is programmed to a value other than 00b, to cause HP_CLKEN_*x*# output assertion to follow HP_PWREN_*x* assertion, by a fixed delay (128, 256, or 512 ms). ***Note:*** *Although this is an I/O signal, its logical operation is input.*
HP_PWRLED_[C, B]#	I/O PU	D26, AD2	**Hot Plug Power LED Outputs (2 Balls)** Active-Low Slot Control Logic output that is used to drive the Power Indicator. This output is asserted Low to turn On (illuminate) the LED. Enabled when the **Slot Capability** register *Power Indicator Present* bit (Downstream Ports, offset 7Ch[4]) is Set, and controlled by the **Slot Control** register *Power Indicator Control* field (Downstream Ports, offset 80h[9:8]). When software writes to the *Power Indicator Control* field, a Command Completed interrupt can be generated to notify the Host that the command has been executed. When the following conditions exist: • **Slot Capability** register *Power Indicator Present* bit (Downstream Ports, offset 7Ch[4]) is Set, and • **Slot Control** register *Command Completed Interrupt Enable* bit is not masked (Downstream Ports, offset 80h[4], is Set), and • **Slot Control** register *Hot Plug Interrupt Enable* bit (Downstream Ports, offset 80h[5]) is Set, an interrupt (MSI, INT*x* Message, or PEX_INTA# and/or VS*x*_PEX_INTA# output, all mutually exclusive, on a per-Port basis) can be generated to the Host. **If HP_PWRLED_*x*# are used, each requires an external current-limiting resistor.** ***Note:*** *Although this is an I/O signal, its logical operation is output.*

[a] If Hot Plug outputs (including HP_PERST_x#) are used and HP_MRL_x# input is not used, pull HP_MRL_x# input Low so that Hot Plug outputs (including HP_PERST_x#) will properly sequence if the serial EEPROM is blank or missing. Default register values enable HP_MRL_x#, which must then be asserted to cause Hot Plug outputs to toggle (for example, to de-assert HP_PERST_x# and assert HP_PWRLED_x#).

3.4.2.2 Serial Hot Plug Signals

Transparent downstream Ports can implement Hot Plug, by using external I^{2}C I/O Expanders (one 16-pin Maxim MAX7311, NXP PCA9555, or TI PCA9555 per slot –or– one 40-pin NXP PCA9698 per two slots). All Ports implementing Serial Hot Plug can concurrently use either type of I/O Expander (16- or 40-pin). The Serial Hot Plug Controller queries each I/O Expander for its Device ID. 40-Pin I^{2}C I/O Expanders implement Device ID, and 16-pin I/O Expanders do not. If the device responds to the PEX 8649's Device ID query, the Serial Hot Plug Controller assumes that the I/O Expander is a 40-pin device. The query can be disabled, by Setting the **Power Management Hot Plug User Configuration** register *40-Pin I/O Expander Scan Disable* bit (offset F70h[17]).

Table 3-4 defines the three signal balls that support Serial Hot Plug. Additionally, the PEX 8649 supports external Serial Hot Plug signals on the external I^{2}C I/O Expanders. (Refer to Section 10.9.2, "External I^{2}C I/O Expander Parts Selection and Pin Definition.")

These signals are active only for Serial Hot Plug-capable Ports configured at start-up. For further details regarding Hot Plug, refer to Chapter 10, "Hot Plug Support."

Table 3-5. Serial Hot Plug Signals – 3 Balls

Signal Name	Type	Location	Description
I2C_SCL1	OD	AC25	**I^{2}C Serial Clock Line for Serial Hot Plug Support** I^{2}C Clock source. Used with the external I^{2}C I/O Expander, and must be bused to each I/O Expander's Clock (SCL) pin. In combination with I2C_SDA1, forms the PEX 8649 I^{2}C Master interface. **I2C_SCL1 requires an external pull-up resistor.**
I2C_SDA1	OD	AE25	**I^{2}C Serial Data Output for Serial Hot Plug Support** Transmits and receives I^{2}C data. Used with the external I^{2}C I/O Expander, and must be bused to each I/O Expander's Data (SDA) pin. In combination with I2C_SCL1, forms the PEX 8649 I^{2}C Master interface. **I2C_SDA1 requires an external pull-up resistor.**
SHPC_INT#	I/O PU	B3	**Serial Hot Plug Controller Interrupt Input** Active-Low interrupt input from external I^{2}C I/O Expanders. Used only by Serial Hot Plug-capable Transparent downstream Ports. The I/O Expander asserts its INT# output whenever any of its inputs change state, and de-asserts its INT# output when the corresponding Input Port Data register (that changed state) is read. When the SHPC_INT# Interrupt input (connected to the INT# output of all I/O Expanders) is asserted, the I^{2}C Master interface begins reading the Input Port registers of all I/O Expanders, and copies the values to the appropriate bits in the corresponding Port's **Slot Status** register (Downstream Ports, offset 80h). The I^{2}C Master interface halts the reading of I/O Expander registers when the SHPC_INT# input de-asserts. **If used, SHPC_INT# requires an external pull-up resistor.** ***Notes:*** *By default, SHPC_INT# is internally de-bounced, but must remain stable for at least 10 ms. Internal de-bouncing can be disabled, by Setting the Port's Serial Hot Plug INTx De-Bounce Disable bit (offset F70h[18]).* *Although this is an I/O signal, its logical operation is input.*

3.4.3 Serial EEPROM Signals

The PEX 8649 includes four signals for interfacing to a serial EEPROM, defined in Table 3-6. For information regarding serial EEPROM use, refer to Chapter 6, "Serial EEPROM Controller."

Table 3-6. Serial EEPROM Signals – 4 Balls

Signal Name	Type	Location	Description
EE_CS#	I/O PU	E26	**Active-Low Serial EEPROM Chip Select Output** ***Note:*** *Although this is an I/O signal, its logical operation is output.*
EE_DI	O	G23	**PEX 8649 Output to Serial EEPROM Data Input**
EE_DO	I/O PU	F26	**PEX 8649 Input from Serial EEPROM Data Output** Should be pulled High to VDD25. ***Note:*** *Although this is an I/O signal, its logical operation is input.*
EE_SK	I/O PU	E25	**Serial EEPROM Clock Frequency Output** Programmable, by way of the **Serial EEPROM Clock Frequency** register *EepFreq[2:0]* field (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 268h[2:0]), to the following: • 1 MHz (default) • 1.98 MHz • 5 MHz • 9.62 MHz • 12.5 MHz • 15.6 MHz • 17.86 MHz ***Note:*** *Although this is an I/O signal, its logical operation is output.*

3.4.4 Strapping Signals

The PEX 8649 Strapping signals, defined in Table 3-7, Set the configuration of upstream Port and NT Port assignment, Link width, and various setup and test modes.

Internal pull-up and pull-down resistors are used to Set the default configuration; if the PEX 8649 configuration must be changed from the default, external pull-up and/or pull-down resistors can be connected. External resistors are not required unless the Strapping signals:

- Must be inverted from the default logic state, –or–
- Are connected to circuit traces (the internal resistors are relatively weak, and may not be strong enough to hold circuit traces to the default input states)

After a Fundamental Reset, the **Link Capability**, **VS0 Upstream**, and **Port Configuration** registers capture ball status. Strapping ball Configuration data can be changed by writing new data to these registers from the Management Port and/or serial EEPROM. I^2C can also change Strapping ball Configuration data; however, the STRAP_I2C_CFG_EN# input should be Low, to prevent linkup and Host enumeration. Then, when I^2C programming is complete, I^2C should lastly Set the **Configuration Release** register *Initiate Configuration* bit (Port 0, offset 3ACh[0]), to enable linkup and allow subsequent Host enumeration.

Table 3-7. Strapping Signals – 33 Balls

Signal Name	Type	Location	Description
STRAP_DEBUG_SEL[1:0]	I PD	W6, AF3	***Factory Test Only* (2 Balls)** Pull or tie Low to VSS (GND). Optionally, this input can remain unconnected, because the internal pull-down resistor holds the input Low.
STRAP_FAST_BRINGUP#	I PU	Y22	***Factory Test Only*** Must be pulled or tied High to VDD25. This input can remain unconnected, because the internal pull-up resistor holds the input High.
STRAP_G1_COMPATIBLE#	I PU	W1	**Compatibility Enable for Non-Compliant Gen 1 Endpoints** When STRAP_G1_COMPATIBLE# is pulled or tied High to VDD25, the Data Rate Identifier symbol in the TS Ordered-Sets always advertises support for both the Gen 2 data rate and Autonomous Change. When STRAP_G1_COMPATIBLE# is pulled or tied Low to VSS (GND), and the Link training sequence fails during the Configuration state, the next time the Link Training and Status State Machine (LTSSM) exits the *Detect* state, TS Ordered-Sets advertise only the Gen 1 data rate, and no Autonomous Change support. The LTSSM then continues to toggle between Gen 1 and Gen 2 advertisement every time it exits the *Detect* state. ***Notes:* *This feature should be enabled only if a non-compliant device will not linkup if these Data Rate Identifier bits are Set.*** *Normally, this input should be pulled or tied High to VDD25. Optionally, this input can remain unconnected, because the internal pull-up resistor holds the input High.*

Table 3-7. Strapping Signals – 33 Balls *(Cont.)*

Signal Name	Type	Location	Description
STRAP_I2C_CFG_EN#	I PU	Y1	**I^2C Bus Configuration Enable** Enables or disables the I^2C Bus for initial device configuration prior to Link training. **Base Mode** L = Enables I^2C Bus for initial device configuration. The serial EEPROM is loaded after the PEX 8649 comes out of reset. After I^2C writes a 1 to the **Configuration Release** register *Initiate Configuration* bit (Port 0, offset 3ACh[0]), all Ports come up at the same time. ***Note:*** *I^2C protocol (bitstream) must be used for this initialization and delayed linkup feature (not SMBus protocol).* H = Disables I^2C Bus for initial device configuration. The **Configuration Release** register *Initiate Configuration* bit is Set by hardware immediately after the PEX 8649 comes out of reset. After the serial EEPROM load finishes, all Ports come up at the same time. **Virtual Switch Mode** STRAP_I2C_CFG_EN# is used in tandem with STRAP_NT_ENABLE# and STRAP_NT_UPSTRM_PORTSEL0 in Virtual Switch mode. For details, refer to Table 3-8, which illustrates the relationship between the three signals.
STRAP_NT_ENABLE#	I/O PU	A3	**Base Mode** **Enable NT Mode** Active-Low input that enables and disables NT mode. The STRAP_VS_MODE[1:0] inputs must be Low for NT mode. STRAP_NT_ENABLE# can be overridden by serial EEPROM and/or I^2C programming of the **VS0 Upstream** register *NT Enable* bit (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 360h[13]). **If the register is programmed by serial EEPROM and/or I^2C, that must be the first serial EEPROM entry, or the first register written by I^2C, with one exception. (Refer to the first Note.)** Software can enable or disable NT mode, by writing to the **VS0 Upstream** register, if the **Debug Control** register *Hardware/ Software Configuration Mode Control* bit (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 350h[9]) is already Set. The mode will change, following subsequent Hot Reset (or DL_Down condition) at the PEX 8649's upstream Port. L = Enables NT mode H = Disables NT mode (default, if input is not connected) ***Notes:*** *If STRAP_NT_ENABLE# is pulled or tied High to VDD25, and software enables NT mode by Setting the* ***VS0 Upstream*** *register NT Enable bit, this register Write must be preceded by a Write that programs the NT Port Virtual Interface* ***PCI Class Code*** *register (offset 08h) to the default value for NT mode, 068000h (Other Bridge Device).* *Although this is an I/O signal, its logical operation is input.*

Table 3-7. Strapping Signals – 33 Balls *(Cont.)*

Signal Name	Type	Location	Description
STRAP_NT_ENABLE#	I/O PU	A3	**Virtual Switch Mode** **Enable Management Port** Active-Low input that enables and disables the Management Port. The Management Port is an upstream Port in one of the virtual switches, and is designated by the STRAP_UPSTRM_PORTSEL[3:0] input Setting, and the **Management Port Control** register *Active Management Port* field (Port 0, accessible through the Management Port and Redundant Management Port, offset 354h[4, 2:0]) value. STRAP_NT_ENABLE# can be overridden by the serial EEPROM value for the register's *Active Management Port Enable* bit (offset 354h[5]). I^{2}C or SMBus can enable or disable the Active Management Port, by writing to the **Management Port Control** register. If I^{2}C programs the **Management Port Control** register, the STRAP_I2C_CFG_EN# input can be pulled or tied Low to VSS (GND), to delay linkup and Host enumeration until I^{2}C initialization is complete. After I^{2}C initialization is complete, I^{2}C (and not SMBus) must then Set the **Configuration Release** register *Initiate Configuration* bit (Port 0, offset 3ACh[0]). Software can enable or disable the Management Port, by writing through the Management Port, to the **Management Port Control** register. Table 3-8 helps to further illustrate the Virtual Switch mode relationship between STRAP_NT_ENABLE#, STRAP_NT_UPSTRM_PORTSEL0, and STRAP_I2C_CFG_EN#. L = Enables the Management Port H = Disables the Management Port ***Note:*** *Although this is an I/O signal, its logical operation is input.*

Table 3-7. Strapping Signals – 33 Balls *(Cont.)*

Signal Name	Type	Location	Description
STRAP_NT_P2P_EN#	I PU	AA1	**Base Mode Only** **NT PCI-to-PCI Bridge Enable** ***Note:*** *If NT mode is enabled (STRAP_NT_ENABLE#=L, or the **VS0 Upstream** register NT Enable bit (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 360h[13]) is Set), this input should be pulled or tied Low to VSS (GND), unless the NT PCI-to-PCI bridge between the internal Virtual PCI Bus and the NT Port Virtual Interface must be disabled for software compatibility to earlier NT mode switches.* *If NT mode is not enabled, optionally, this input can remain unconnected, because the internal pull-up resistor holds the input High.* Allows the NT function to be logically placed on the internal Virtual PCI Bus, or behind the PCI-to-PCI bridge for that Port. This input maps to the **Debug Control** register *NT P2P Enable* bit (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 350h[14]). This signal and its corresponding register bit must ***not*** be toggled at runtime. L = Enables NT PCI-to-PCI bridge mode, if NT mode is enabled (pulled down to Ground (VSS)) H = Disables NT PCI-to-PCI bridge mode, if NT mode is enabled (default; the PEX 8649 is in Legacy NT mode, if NT mode is enabled) (pulled up to VDD25)

Table 3-7. Strapping Signals – 33 Balls *(Cont.)*

Signal Name	Type	Location	Description

STRAP_NT_UPSTRM_PORTSEL [4, 2:0]	[4, 2:1]:
	I
	PD
	
	[0]:
	I/O
	PD
		AB24, AA3, G6, A2	**Base Mode**
			Select Upstream Non-Transparent Port (4 Balls)
			Select any Port to be the upstream NT Port.
			STRAP_NT_UPSTRM_PORTSEL[4, 2:0] can be overridden by the serial EEPROM value for the **VS0 Upstream** register *NT Port* field (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 360h[12, 10:8], respectively). If the **VS0 Upstream** register is programmed by serial EEPROM, that must be the first serial EEPROM entry.
			I^{2}C can select a Port to be the upstream NT Port, by writing to the **VS0 Upstream** register. If I^{2}C programs the **VS0 Upstream** register (to change the strapped configuration for the upstream Port, NT Port, and/or NT mode), I^{2}C must program this register first. The STRAP_I2C_CFG_EN# input can be pulled or tied Low to VSS (GND), to delay linkup and Host enumeration until I^{2}C initialization is complete. After I^{2}C initialization is complete, I^{2}C (and not SMBus) must then Set the **Configuration Release** register *Initiate Configuration* bit (Port 0, offset 3ACh[0]).
			Software can change which Port is configured to be the NT Port, by writing to the **VS0 Upstream** register, if the **Debug Control** register *Hardware/Software Configuration Mode Control* bit (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 350h[9]) is already Set.
			Refer to Section 14.9, "Port Programmability," for further details.
			LLLL = Port 0
			LLLH = Port 1
			LLHL = Port 2
			LLHH = Port 3
			HLLL = Port 16
			HLLH = Port 17
			HLHL = Port 18
			HLHH = Port 19
			HHLL = Port 20
			HHLH = Port 21
			HHHL = Port 22
			HHHH = Port 23
			All other encodings are ***reserved.***
			Note: *If NT mode is not used (STRAP_NT_ENABLE#=H) and/or the serial EEPROM and/or I^{2}C programs NT mode (**VS0 Upstream** register NT Enable bit (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 360h[13], is Set), thereby overriding STRAP_NT_ENABLE#), these inputs should be pulled or tied Low to VSS (GND), but can remain unconnected (N/C), in which case the **VS0 Upstream** register NT Port field value defaults to the logic level Set by the internal pull-down resistors, 0h.*

Table 3-7. Strapping Signals – 33 Balls *(Cont.)*

Signal Name	Type	Location	Description
STRAP_NT_UPSTRM_PORTSEL [4, 2:0]	[4, 2:1]: I PD [0]: I/O PD	AB24, AA3, G6, A2	**Virtual Switch Mode** **Management Port Initialization (4 Balls)** In Virtual Switch mode, the STRAP_NT_UPSTRM_PORTSEL[4, 2:1] balls are Don't Care, and can be pulled or tied Low to VSS (GND), or optionally, can remain unconnected. If the Management Port is not enabled (STRAP_NT_ENABLE#=H), STRAP_NT_UPSTRM_PORTSEL0 is also Don't Care, and can be pulled or tied Low to VSS (GND), or optionally, can remain unconnected. If the Management Port is enabled (STRAP_NT_ENABLE#=L), STRAP_NT_UPSTRM_PORTSEL0 is used to control Bring-Up Options 1 and 2: • **Option 1** – STRAP_NT_UPSTRM_PORTSEL0=L. After the serial EEPROM (if present) is loaded, the Management Port comes up first, to configure the PEX 8649. When the Management Port has completed its configuration, Management Port software and/or the serial EEPROM (not I^{2}C nor SMBus) must Set the **Configuration Release** register *Initiate Configuration* bit (Port 0, accessible through the Management Port, offset 3ACh[0]), to release the hold that is preventing the remaining Links from coming up. • **Option 2** – STRAP_NT_UPSTRM_PORTSEL0=H. After the serial EEPROM (if present) is loaded, all Ports come up concurrently (provided that the serial EEPROM does not Clear the *Initiate Configuration* bit). STRAP_NT_UPSTRM_PORTSEL[4, 2:0] can be overridden by the serial EEPROM value for the **Management Port Control** register *Active Management Port Enable* bit (Port 0, accessible through the Management Port and Redundant Management Port, offset 354h[5]). Table 3-8 helps to further illustrate the Virtual Switch mode relationship between STRAP_NT_UPSTRM_PORTSEL0 and STRAP_I2C_CFG_EN#, as well as STRAP_NT_ENABLE#. ***Note:*** *If in Virtual Switch mode, the Management Port is not enabled and/or the serial EEPROM disables the Management Port (Active Management Port Enable bit is Cleared, thereby overriding STRAP_NT_ENABLE#), these inputs should be pulled or tied Low to VSS (GND), but optionally can remain unconnected (N/C), in which case the* ***Management Port Control*** *register Active Management Port field value defaults to the logic level Set by the internal pull-down resistors, 0h.*

Table 3-7. Strapping Signals – 33 Balls *(Cont.)*

Signal Name	Type	Location	Description
STRAP_PLL_BYPASS#	I PU	Y26	***Factory Test Only*** Pull or tie High to VDD25, or optionally can remain unconnected.
STRAP_PROBE_MODE#	I PU	Y21	***Factory Test Only*** Pull or tie High to VDD25, or optionally can remain unconnected.
STRAP_RESERVED16	I	AE24	***Factory Test Only*** Must be tied directly to Ground (VSS).
STRAP_RESERVED17#	I PU	H24	***Factory Test Only*** Pull or tie High to VDD25, or optionally can remain unconnected.
STRAP_SERDES_MODE_EN#	I PU	W26	***Factory Test Only*** Pull or tie High to VDD25, or optionally can remain unconnected.
STRAP_SMBUS_EN#	I PU	W3	**System Management Bus Enable** L = Enables SMBus Slave protocol on the I2C_SCL0 and I2C_SDA0 2-wire bus H = Enables I^2C Slave protocol on the I2C_SCL0 and I2C_SDA0 2-wire bus

STRAP_STN0_PORTCFG[1:0]	[1]:
	I/O
	PD
	[0]:
	I
	PD
		AF24,
		AD24
			Strapping Signals to Select Port Configuration for Station 0 (Number of Enabled Ports (1, 2, 3, or 4), and Maximum Number of Lanes for Each Specific Port) (2 Balls)
			Defines the enabled Port Numbers and their Link widths, for Station 0. Programs the **Port Configuration** register *Port Configuration for Station 0* field (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 300h[1:0]) default value.
			LL = x4, x4, x4, x4
			LH = x16
			HL = x8, x8
			HH = x8, x4, x4

STRAP_STN4_PORTCFG[1:0]	I
	PD
		G1, C4	**Strapping Signals to Select Port Configuration for Station 4 (Number of Enabled Ports (1, 2, 3, or 4), and Maximum Number of Lanes for Each Specific Port) (2 Balls)**
			Defines the enabled Port Numbers and their Link widths, for Station 4. Programs the **Port Configuration** register *Port Configuration for Station 4* field (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 300h[9:8]) default value.
			LL = x4, x4, x4, x4
			LH = x16
			HL = x8, x8
			HH = x8, x4, x4

Table 3-7. Strapping Signals – 33 Balls *(Cont.)*

Signal Name	Type	Location	Description

STRAP_STN5_PORTCFG[1:0]	I
	PD
		B24, C23	**Strapping Signals to Select Port Configuration for Station 5 (Number of Enabled Ports (1, 2, 3, or 4), and Maximum Number of Lanes for Each Specific Port) (2 Balls)**
			Defines the enabled Port Numbers and their Link widths, for Station 5. Programs the **Port Configuration** register *Port Configuration for Station 5* field (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 300h[11:10]) default value.
			LL = x4, x4, x4, x4
			LH = x16
			HL = x8, x8
			HH = x8, x4, x4

STRAP_TESTMODE[3:0]	I PD	W2, AD4, AF2, Y6	**Test Mode Selects (4 Balls)** The STRAP_TESTMODE[3:0] value defines GPIO[31:24] and PEX_PORT_GOOD*x*# signal functionality following a Fundamental Reset. GPIO[31:24] and PEX_PORT_GOOD*x*# signal functionality can also be programmed by serial EEPROM, I^{2}C, and/or software. **HLHH (1011b or Bh)** • PEX_PORT_GOOD*x*# default to the PORT_GOOD function • GPIO[31:24] are inputs, with values reflected in the **GPIO 24_31 Input Data** register (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 620h) **HHLL (1100b or Ch)** • PEX_PORT_GOOD*x*# default to GPIO inputs, with values reflected in the **GPIO 0_11 Input Data** register (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 61Ch) • GPIO[31:24] default to the Serial Hot Plug PERST# output function **HHLH (1101b or Dh)** • PEX_PORT_GOOD*x*# default to the PORT_GOOD function • GPIO[31:24] default to the Serial Hot Plug PERST# output function **HHHH (1111b or Fh)** • PEX_PORT_GOOD*x*# default to GPIO inputs, with values reflected in the **GPIO 0_11 Input Data** register • GPIO[31:24] are inputs, with values reflected in the **GPIO 24_31 Input Data** register All other encodings are ***Factory Test Only***.

Table 3-7. Strapping Signals – 33 Balls *(Cont.)*

Signal Name	Type	Location	Description

STRAP_UPSTRM_PORTSEL[3:0]	I
	PD
		A24, G26,
		G24, G25
			Base Mode
			Strapping Signals to Select Upstream Port (4 Balls)
			Select any Port as the upstream Port. These inputs map to the **VS0 Upstream** register *Upstream Port* field (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 360h[4, 2:0], respectively).
			In Base mode, the **VS0 Upstream** register also controls the enabling or disabling of NT mode, and designation of the NT Port (if NT mode is enabled). If the **VS0 Upstream** register is programmed by serial EEPROM and/or I^{2}C, this register must be programmed first.
			If I^{2}C is used to configure the PEX 8649, the STRAP_I2C_CFG_EN# input can be pulled or tied Low to VSS (GND), to delay linkup until I^{2}C initialization is complete. After I^{2}C initialization is complete, I^{2}C (and not SMBus) must then Set the **Configuration Release** register *Initiate Configuration* bit (Port 0, offset 3ACh[0]).
			Software can change which Port is configured to be the upstream Port, by writing to the **VS0 Upstream** register, if the **Debug Control** register *Hardware/Software Configuration Mode Control* bit (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 350h[9]) is already Set.
			Refer to Section 14.9, "Port Programmability," for further details.
			LLLL = Port 0
			LLLH = Port 1
			LLHL = Port 2
			LLHH = Port 3
			LHLL = Port 16
			LHLH = Port 17
			LHHL = Port 18
			LHHH = Port 19
			HLLL = Port 20
			HLLH = Port 21
			HLHL = Port 22
			HLHH = Port 23
			All other encodings are ***reserved***.
			Note: *The upper two balls select the Station, and the lower two balls select the Port within that Station. While the PEX 8649 uses Stations 0, 4, and 5, the STRAP_UPSTRM_PORTSEL[3:2] inputs use values 0, 1, and 2 respectively, for ball compatibility with the PEX 8648. These four PEX 8649 inputs are mapped to the* ***VS0 Upstream*** *register Upstream Port field (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 360h[4, 2:0]), in which the STRAP_UPSTRM_PORTSEL3 value is shifted up one bit to map to offset 360h[4], and offset 360h[3] is internally tied Low. Therefore, while the STRAP_UPSTRM_PORTSEL[3:2] inputs indicate Stations 0, 1, and 2, the corresponding register value is translated to indicate Stations 0, 4, and 5, respectively. The resulting register value is the Port Number of the upstream Port.*

Table 3-7. Strapping Signals – 33 Balls *(Cont.)*

Signal Name	Type	Location	Description

STRAP_UPSTRM_PORTSEL[3:0]	I
	PD
		A24, G26, G24, G25	**Virtual Switch Mode**
			Strapping Signals to Select Management Port (4 Balls)
			Select any virtual switch upstream Port as the Management Port. These inputs map to the **Management Port Control** register *Active Management Port* field (Port 0, accessible through the Management Port and Redundant Management Port, offset 354h[4, 2:0], respectively).
			The **Management Port Control** register also controls the enabling or disabling of the Active Management Port, and designation and enabling of the Redundant Management Port (which is programmed by Management Port software, serial EEPROM, and/or I^2C). The Active Management Port, the Redundant Management Port, and/or I^2C can promote the Redundant Management Port to be the Active Management Port, by programming the register.
			If the STRAP_NT_UPSTRM_PORTSEL0 input is Low, after a Fundamental Reset and the serial EEPROM load, only the Management Port links up. When the Management Port has completed its configuration of the virtual switches, Management Port software (and/or the serial EEPROM, but not I^2C nor SMBus) must Set the **Configuration Release** register *Initiate Configuration* bit (Port 0, accessible through the Management Port, offset 3ACh[0]), to release the hold that is preventing the remaining Links from coming up. If instead the STRAP_NT_UPSTRM_PORTSEL0 input is pulled or tied High to VDD25, all Ports commence Link training after the serial EEPROM load completes, following a Fundamental Reset.
			If I^2C is used to configure the PEX 8649, the STRAP_I2C_CFG_EN# input can be pulled or tied Low to VSS (GND), to delay linkup until I^2C initialization is complete. After I^2C initialization is complete, I^2C (and/or the serial EEPROM) must then Set the *Initiate Configuration* bit, to enable all Ports to begin Link training.
			LLLL = Port 0
			LLLH = Port 1
			LLHL = Port 2
			LLHH = Port 3
			HLLL = Port 16
			HLLH = Port 17
			HLHL = Port 18
			HLHH = Port 19
			HHLL = Port 20
			HHLH = Port 21
			HHHL = Port 22
			HHHH = Port 23
			All other encodings are ***reserved.***

Table 3-7. Strapping Signals – 33 Balls *(Cont.)*

Signal Name	Type	Location	Description
STRAP_VS_MODE[1:0]	I/O PD	D2, H3	**Virtual Switch Enable (2 Balls)** Used together, to enable up to four virtual switches, depending upon the ball states. The quantity of virtual switches enabled by these inputs in Virtual Switch mode is reflected in the **Virtual Switch Enable** register *VSx Enable* bits (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 358h[3:0]). For Base mode, the STRAP_VS_MODE[1:0] inputs must be Low. For Virtual Switch mode, the STRAP_VS_MODE[1:0] inputs must be strapped to a non-zero value. If the STRAP_VS_MODE[1:0] inputs are strapped Low to enable Base mode, the serial EEPROM, I^{2}C/SMBus, and software ***cannot*** override the straps to enable Virtual Switch mode. Similarly, if the STRAP_VS_MODE[1:0] inputs are strapped to a non-zero value to enable Virtual Switch mode, the serial EEPROM, I^{2}C/SMBus, and software ***cannot*** override the straps to enable Base mode. However, in Virtual Switch mode, the serial EEPROM, I^{2}C/SMBus, and/or software can change the Virtual Switch Table, including the quantity of enabled virtual switches. (Refer to Section 5.5.3, “Virtual Switch Table.”) If a design must support both Base mode and Virtual Switch mode, without changing the STRAP_VS_MODE[1:0] input values, strap the STRAP_VS_MODE[1:0] inputs to a non-zero value. Then, if Base mode is needed, the serial EEPROM, I^{2}C/SMBus, and/or software can assign all Ports to VS0 (with no Ports assigned to other virtual switches). The STRAP_VS_MODE[1:0] inputs must be Low for NT mode. **Base Mode** Pull or tie Low to VSS (GND), or optionally, these inputs can remain unconnected (N/C), because the internal pull-down resistors Set the default value to LL. LL (00b) = Single switch (default, no virtual switches) **Virtual Switch Mode** LH (01b) = Two virtual switches – VS0 and VS1 HL (10b) = Three virtual switches – VS0, VS1, and VS2 HH (11b) = Four virtual switches – VS0, VS1, VS2, and VS3 The default Port configuration assignments for virtual switches are listed in Table 4-1. ***Note:*** *In Virtual Switch mode, serial EEPROM, I^{2}C/SMBus and software can change the virtual switch configuration, but must not change from Base mode to Virtual Switch mode, nor vice-versa.*

Table 3-8 describes the Virtual Switch mode operation for the Strapping options.

Table 3-8. Operation for Strapping Options – Virtual Switch Mode[a]

STRAP_I2C_CFG_EN#	STRAP_NT_UPSTRM_PORTSEL0	STRAP_NT_ENABLE# (Active Management Port Enable)	Actions
H	L	H	After the serial EEPROM load is complete, hardware Sets the **Configuration Release** register *Initiate Configuration* bit (Port 0, accessible through the Management Port, offset 3ACh[0]), and all Ports come up at the same time (provided that the serial EEPROM does not Clear the *Initiate Configuration* bit). (The Active Management Port is disabled here.)
H	L	L	After the serial EEPROM load is complete, only the Management Port comes up, and Management Port software (and/or the serial EEPROM, but not I^2C nor SMBus) Sets the **Configuration Release** register *Initiate Configuration* bit, and then all other Ports come up.
H	H	X	After the serial EEPROM load is complete, hardware Sets the **Configuration Release** register *Initiate Configuration* bit, and all Ports come up at the same time (provided that the serial EEPROM does not Clear the *Initiate Configuration* bit).
L	X	X	The serial EEPROM is loaded after the PEX 8649 comes out of reset. After I^2C (or the serial EEPROM) Sets the **Configuration Release** register *Initiate Configuration* bit, all Ports come up at the same time.

[a] *X is "Don't Care."*

3.4.5 JTAG Interface Signals

The PEX 8649 includes five signals for performing Joint Test Action Group (JTAG) boundary scan, defined in Table 3-9. If JTAG is not used, these signals can remain unconnected (N/C), because the internal pull-down resistors provide termination for the inputs.

The JTAG interface is described in Section 17.8, "JTAG Interface."

Table 3-9. JTAG Interface Signals – 5 Balls

Signal Name	Type	Location	Description
JTAG_TCK	I PD	B2	**JTAG Test Clock Input** JTAG Test Access Port (TAP) Controller clock source. Frequency can be from 0 to 15 MHz.
JTAG_TDI	I PD	C3	**JTAG Test Data Input** Serial input to the JTAG TAP Controller, for test instructions and data.
JTAG_TDO	O	G5	**JTAG Test Data Output** Serial output from the JTAG TAP Controller test instructions and data.
JTAG_TMS	I PD	B1	**JTAG Test Mode Select** Input decoded by the JTAG TAP Controller, to control test operations.
JTAG_TRST#	I PD	C2	**JTAG Test Reset** Active-Low input used to reset the Test Access Port. When JTAG functionality is not used, the JTAG_TRST# input should be driven Low, or pulled Low to VSS (GND) through a 1.5KΩ resistor, to place the JTAG TAP Controller into the *Test-Logic-Reset* state, which disables the test logic and enables standard logic operation. Alternatively, if JTAG_TRST# input is High, the JTAG TAP Controller can be placed into the *Test-Logic-Reset* state by initializing the JTAG TAP Controller's **Instruction** register to contain the *IDCODE* instruction, or by holding the JTAG_TMS input High for at least five rising edges of the JTAG_TCK input.

3.4.6 I^{2}C/SMBus Slave Interface Signals

Table 3-10 defines the five signals that support the I^{2}C/SMBus Slave interface. For further details, refer to Chapter 7, "I^{2}C/SMBus Slave Interface Operation."

Table 3-10. I^{2}C/SMBus Slave Interface Signals – 5 Balls

Signal Name	Type	Location	Description
I2C_ADDR[2:0]	I/O PU	F2, F3, E2	**I^{2}C/SMBus Slave Address Bits 2 through 0 Inputs (3 Balls)** Used to define the default value of the three least significant bits of the PEX 8649 I^{2}C/SMBus 7-bit Slave address, which is programmable in the **I^{2}C Configuration** register *Slave Address* field (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 294h[2:0]). If I^{2}C or SMBus is used, I2C_ADDR[2:0] should be strapped to a unique address, to avoid an address conflict with any other I^{2}C/SMBus devices (on the same I^{2}C Bus/SMBus segment) that have the upper four bits of their 7-bit I^{2}C/SMBus Slave address also defined as value 0011b. If the STRAP_SMBUS_EN# input (of which its inverse value defines the default value of the **SMBus Configuration** register *SMBus Enable* bit (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 2C8h[0])) is Low, to enable SMBus protocol as default, the I2C_ADDR2 input defines the same default value for two register bits – bit 2 of the Slave address (offset 294h[2]), and the **SMBus Configuration** register *ARP Disable* bit (offset 2C8h[8]). Specifically, if the STRAP_SMBUS_EN# input is Low (to enable SMBus protocol as default): • If the I2C_ADDR2 input is Low, to enable Address Resolution Protocol (ARP) as default, the *ARP Disable* bit default value is 0, and bit 2 of the **I^{2}C Configuration** register *Slave Address* field defaults to a value of 0. In this configuration, the upper five bits of the 7-bit Slave address default to value 00110b. • If the I2C_ADDR2 input is High, to disable ARP as default, the *ARP Disable* bit default value is 1, and bit 2 of the**I^{2}C Configuration** register *Slave Address* field defaults to a value of 1. In this configuration, the upper five bits of the 7-bit Slave address default to value 00111b. The internal pull-up resistors cause the I2C_ADDR[2:0] inputs to default to HHH (111b). If the I^{2}C/SMBus Slave address must be changed to a different value, add pull-down resistors, to force the appropriate I2C_ADDR[2:0] inputs to a logic Low state, and the Address bits that are to be logic High can be pulled High, or optionally, can remain unconnected. However, if the I2C_ADDR[2:0] inputs that are logic High are connected to circuit traces, external pull-up resistors are recommended, because the internal pull-up resistors might not be strong enough to hold the input(s) High. ***Note:*** *Although this is an I/O signal, its logical operation is input.*

Table 3-10. I^2C/SMBus Slave Interface Signals – 5 Balls

Signal Name	Type	Location	Description
I2C_SCL0	OD	G4	**I^2C/SMBus Serial Clock Line** I^2C/SMBus bidirectional Clock line. Data on the I^2C Bus can be transferred at rates of up to 100 kbit/s (Standard mode). **I2C_SCL0 requires an external pull-up resistor.** ***Note:*** *The PEX 8649 I^2C/SMBus Slave Interface can stretch the Low period of the I^2C/SMBus clock while a simultaneous in-band Request that also targets PEX 8649 registers is being processed.*
I2C_SDA0	OD	E3	**I^2C/SMBus Serial Data I/O** Transmits and receives I^2C/SMBus data during I^2C/SMBus accesses to PEX 8649 registers. **I2C_SDA0 requires an external pull-up resistor.**

3.4.7 Device-Specific Signals

Table 3-11 defines the Device-Specific signals – signals that are unique to the PEX 8649.

Table 3-11. Device-Specific Signals – 33 Balls

Signal Name	Type	Location	Description
FATAL_ERR#	O	C24	**Fatal Error Output (4 Balls)** FATAL_ERR# is used in Base mode, and in Virtual Switch mode for VS0. VS*x*_FATAL_ERR# are used only in Virtual Switch mode (one per each additional virtual switch – Virtual Switches 3 through 1, respectively). FATAL_ERR# and/or VS*x*_FATAL_ERR# are asserted Low when a Fatal error is detected in the PEX 8649 and the following conditions exist (all the same conditions that are required to send a Fatal Error Message to the Host): • Specific error is defined as *Fatal* in the **Uncorrectable Error Severity** register (offset FC0h), and • Reporting of the specific error condition is enabled, not masked by the corresponding bit of the **Uncorrectable Error Mask** register (offset FBCh), and • **Device Control** register *Fatal Error Reporting Enable* bit (offset 70h[2]) –or– **PCI Command** register *SERR# Enable* bit (offset 04h[8]) is Set The **Device Status** register *Fatal Error Detected* bit (offset 70h[18]) is Set, and the specific error is flagged in the **Uncorrectable Error Status** register (offset FB8h).
VS3_FATAL_ERR# VS2_FATAL_ERR# VS1_FATAL_ERR#	O	AB25, W22, AD26	

Table 3-11. Device-Specific Signals – 33 Balls *(Cont.)*

Signal Name	Type	Location	Description
GPIO[31:24]	I/O PU	AD3, AE2, Y5, AE3, W23, AA26, E24, C26	**General-Purpose I/O (8 Balls)** Default functionality is determined at Fundamental Reset; however, functionality can be switched by programming the **GPIO** registers using serial EEPROM, I^{2}C, and/or software. GPIO[31:24] provide GPIO input functionality, by default, when the STRAP_TESTMODE[3:0] signal values sampled at Fundamental Reset (PEX_PERST# and/or VS*x*_PERST# input de-assertion) are either value 1011b or 1111b (Bh or Fh, respectively). Alternatively, when the STRAP_TESTMODE[3:0] signals sampled at Fundamental Reset are either value 1100b or 1101b (Ch or Dh, respectively), GPIO[31:24] function as Serial Hot Plug PERST# Reset outputs (similar to HP_PERST_*x*# outputs), by default, for corresponding Ports that include an external I^{2}C I/O Expander. If an external I^{2}C I/O Expander is not present for a Port, the corresponding GPIO[31:24] output remains Low (the Serial Hot Plug PERST# output for that Port is not de-asserted). If Serial Hot Plug is implemented (using external I^{2}C I/O Expanders), it is recommended that the GPIO[31:24] signals be strapped as Serial Hot Plug PERST# Reset outputs and routed to the slots, rather than using the PERST# outputs from the I^{2}C I/O Expanders. **Serial Hot Plug Function – Virtual Switch Mode Only** In Virtual Switch mode, GPIO[31:24] are associated to virtual switch Ports or the Management Port, by one of two mechanisms: **1.** If GPIO[31:24] are configured by STRAP_TESTMODE[3:0] signal values to function as HP_PERST_*x*# Reset outputs, then two of the GPIO[31:24] signals will be assigned to each virtual switch, as default. **2.** If GPIO[31:24] are configured by STRAP_TESTMODE[3:0] signal values to not function as Serial Hot Plug PERST# Reset outputs, the GPIO[31:24] signals are not associated to the virtual switches, until Management Port software, serial EEPROM, and/or I^{2}C/SMBus Sets the **Virtual Switch GPIO Update** register *VS GPIOs Update* bit (Port 0, accessible through the Management Port, offset 64Ch[0]), to complete the assignment of individual GPIO*x* signals to specific virtual switches (after software, serial EEPROM, and/or I^{2}C/SMBus configures functionality in the **GPIO** Serial Hot Plug-related registers (Port 0, accessible through the Management Port, offsets 60Ch, 618h, 620h, and 628h), and assigns the signals to virtual switches, by programming the **VS*x* GPIO_SHP 0_7 Assignment** register(s) (Port 0, accessible through the Management Port, offsets 670h through 67Ch). Continued…

Table 3-11. Device-Specific Signals – 33 Balls *(Cont.)*

Signal Name	Type	Location	Description
GPIO[31:24]	I/O PU	AD3, AE2, Y5, AE3, W23, AA26, E24, C26	Continued… **Serial Hot Plug Function – Virtual Switch Mode Only *(Cont.)*** To assign individual GPIO[31:24] signals to specific virtual switches, Management Port software, serial EEPROM, and/or I^{2}C can program the **VS*x* GPIO_SHP 0_7 Assignment** register(s) (Port 0, accessible through the Management Port, offsets 670h through 67Ch, bits [7:0]). Individual GPIO[31:24] signal assignments must be mutually exclusive among the virtual switches. The 8 bits in each **VS*x* GPIO_SHP 0_7 Assignment** register correspond to the 8 GPIO signals, in the sequence in which they are listed. (Refer to the registers, for signal to bit mapping.) Setting a bit in one of the four registers assigns the signal to the virtual switch indicated by the register name. Because any GPIO[31:24] signal must not be assigned to more than one virtual switch, **each of the 8 bits can be Set exclusively in only one of the four registers**. A maximum of eight GPIO[31:24] signals can be assigned to any one virtual switch. After the **VS*x* GPIO_SHP 0_7 Assignment** register(s) are programmed, the actual assignments do not take effect, until Management Port software, serial EEPROM, and/or I^{2}C Sets the **Virtual Switch GPIO Update** register *VS GPIOs Update* bit (Port 0, accessible through the Management Port, offset 64Ch[0]). After the GPIO[31:24] signals are assigned to virtual switches, each Virtual Switch Host can then configure individual GPIO signal functionality, by programming the **Virtual Switch GPIO_SHP 0_7 Direction Control** register (VS Upstream Port(s), offset A58h). In this register, the GPIO[31:24] signals are virtualized, and the bit numbers do not correspond to specific signal names. Software can determine how many and which GPIO[31:24] signals are assigned to a unique virtual switch, by reading the **Virtual Switch GPIO_SHP 0_7 Availability** register *Number of GPIO_SHPs Available* field (VS Upstream Port(s), offset A5Ch[3:0]). Virtual switch software does not determine which of the actual GPIO[31:24] signals are assigned to the virtual switch. The register value indicates the quantity of signals assigned to each virtual switch.

Table 3-11. Device-Specific Signals – 33 Balls *(Cont.)*

Signal Name	Type	Location	Description
PEX_INTA#	OD	D1	**Interrupt Output (4 Balls)** PEX_INTA# is used in Base mode, and in Virtual Switch mode for VS0. VS*x*_PEX_INTA# are used only in Virtual Switch mode (one per each additional virtual switch – Virtual Switches 3 through 1, respectively). PEX_INTA# and/or VS*x*_PEX_INTA# Interrupt output is enabled if: • INT*x* Messages are enabled (**PCI Command** register *Interrupt Disable* bit, offset 04h[10], is Cleared), and MSIs are disabled (**MSI Control** register *MSI Enable* bit, offset 48h[16], is Cleared) • PEX_INTA# output is enabled (**ECC Error Check Disable** register *Enable PEX_INTA# Ball for x Interrupt* bits, offset 720h[9, 8, 7, 6, 5, and/or 4], are Set) For Device-Specific (RAM ECC) errors, PEX_INTA# (and ***not*** VS*x*_PEX_INTA#) Interrupt output is enabled if: • Reporting of the specific error condition in the **Device-Specific Error Status *x*** register bit(s), if not masked in their corresponding **Device-Specific Error Mask *x*** register bit(s) (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets 700h[19:2], 708h[19:2], 710h[17:0], and/or 718h[17:0] (Status) and offsets 704h[19:2], 70Ch[19:2], 714h[17:0], and/or 71Ch[17:0] (Mask)) ***Note:*** *Device-Specific (RAM ECC) errors can be signaled by interrupt, and/or as an Uncorrectable Internal error that is fatal (**Uncorrectable Error Status** register Uncorrectable Internal Error Status **Uncorrectable Error Severity** register Uncorrectable Internal Error Severity bits (offsets FB8h[22] and FC0h[22], respectively, are Set).* The three interrupt mechanisms, listed below, are mutually exclusive modes of operation, on a per-Port basis, for all interrupt sources: • Conventional PCI INT*x* Message generation • Native MSI transaction generation • Device-Specific PEX_INTA# and/or VS*x*_PEX_INTA# assertion PEX_INTA# and/or VS*x*_PEX_INTA# assertion (Low) indicates that one or more of the following events and/or errors (if not masked) were detected: • Link state events • PCI Express Hot Plug events • General-Purpose Input Interrupt events • Device-Specific Error conditions • Device-Specific NT-Link Port events • NT-Virtual Doorbell events • NT-Link Doorbell events • Management Port Doorbell-Generated interrupts • Management Link Status events Refer to Section 9.1.1, "Interrupt Sources or Events," for details.
VS3_PEX_INTA# VS2_PEX_INTA# VS1_PEX_INTA#	OD	W21, AA24, Y23	

Table 3-11. Device-Specific Signals – 33 Balls *(Cont.)*

Signal Name	Type	Location	Description
PEX_NT_RESET#	O	AD25	**Base Mode Only** **Active-Low Output Used to Propagate Reset in NT Mode** Pulse width is 1 µs.
PEX_PORT_GOOD[23:16, 3:0]#	I/O PU	AA25, W24, Y25, W25, E1, G3, F1, G2, Y2, Y4, C1, D3	**Active-Low PCI Express Port Linkup Status Indicator Outputs for Ports 23 through 16 and 3 through 0 –or– Programmable General-Purpose I/O (12 Balls)** PEX_PORT_GOOD*x*# function as general-purpose inputs, interrupt inputs, general-purpose outputs, or as the PORT_GOOD function, as outlined below. If the Port is ***not*** enabled, the signal defaults to GPIOx input (default value 0). **General-Purpose Inputs** For PEX_PORT_GOOD*x*# signals that are configured as general-purpose inputs (by STRAP_TESTMODE[3:0] signal strapping, sampled at Fundamental reset, with values 1111b or 1100b), or by subsequent programming (by serial EEPROM, I^{2}C, and/or software) of the appropriate **GPIO 0_9 Direction Control** and/or **GPIO 10_11 Direction Control** register *Direction Control* bit(s) (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offsets 600h and 604h, respectively) values, input states are reflected in the **GPIO 0_11 Input Data** register (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 61Ch). Inputs can be internally de-bounced, by setting the corresponding **GPIO 0_11 Input De-Bounce** register bits (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 614h). De-bouncing is disabled, by default; if de-bouncing is enabled, an input must be stable for approximately 1.3 ms to be latched. **General-Purpose Outputs** For PEX_PORT_GOOD*x*# signals that are configured as general-purpose outputs in the **GPIO 0_9 Direction Control** and/or **GPIO 10_11 Direction Control** register *Direction Control* bit(s) (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offsets 600h and 604h, respectively), output states are controlled by the corresponding bit values in the **GPIO 0_11 Output Data** register (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 624h). Continued…

Table 3-11. Device-Specific Signals – 33 Balls *(Cont.)*

Signal Name	Type	Location	Description
PEX_PORT_GOOD[23:16, 3:0]#	I/O PU	AA25, W24, Y25, W25, E1, G3, F1, G2, Y2, Y4, C1, D3	Continued… **Interrupt Inputs** For PEX_PORT_GOOD*x*# signals that are configured as Interrupt inputs in the **GPIO 0_9 Direction Control** and/or **GPIO 10_11 Direction Control** register *Direction Control* bit(s) (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offsets 600h and 604h, respectively), input states are reflected in the **GPIO 0_11 Interrupt Status** register (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 634h). Inputs can be internally de-bounced, by setting the corresponding **GPIO 0_11 Input De-Bounce** register bits (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 614h). De-bouncing is disabled, by default; if de-bouncing is enabled, an input must be stable for approximately 1.3 ms to be latched. Interrupt polarity (Active-High or Active-Low) is individually programmable in the **GPIO 0_11 Interrupt Polarity** register (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 62Ch). Interrupt generation can be selectively masked in the **GPIO 0_11 Interrupt Mask** register (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 63Ch). If a **GPIO 0_11 Interrupt Mask** register bit is Set, a read of the corresponding *Status* bit in the **GPIO 0_11 Interrupt Status** register returns a value of 0. Continued…

Table 3-11. Device-Specific Signals – 33 Balls *(Cont.)*

Signal Name	Type	Location	Description
PEX_PORT_GOOD[23:16, 3:0]#	I/O PU	AA25, W24, Y25, W25, E1, G3, F1, G2, Y2, Y4, C1, D3	Continued… **PORT_GOOD Function – All Modes** For PEX_PORT_GOOD*x*# signals that correspond to enabled Ports and are configured for PORT_GOOD functionality (by STRAP_TESTMODE[3:0] signal strapping sampled at reset with values 1011b or 1101b), or by subsequent programming (by serial EEPROM, I^{2}C, and/or software) of the appropriate **GPIO 0_9 Direction Control** and/or **GPIO 10_11 Direction Control** register(s) (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offsets 600h and 604h, respectively) values. The output states are not directly available from a single register (due to encoded, possibly blinking output); however, software can determine LANE_GOOD status (Physical Layer Link status for each Lane) from the **Station *x* Lane Status** registers (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offsets 330h and 338h). Software can also determine Maximum Link Width and Supported Link Speeds from the **Link Capability** register in each Port (offset 74h[9:4 and 3:0], respectively), as well as Negotiated Link Width and Current Link Speed from the **Link Status** register in each Port (offset 78h[25:20 and 19:16], respectively). The **Link Capability** and **Link Status** registers in the NT Port Virtual Interface follow the NT Port Link Interface configuration, and contain the same values as the corresponding NT Port Link Interface registers. If PORT_GOOD functionality is enabled, but some Ports are not enabled due to STRAP_STN*x*_PORTCFG*x* signal settings, the PEX_PORT_GOOD*x*# signals associated with non-enabled Ports function as GPIO signals. LED behavior when connected to PEX_PORT_GOOD*x*# signals: • **Off** – Link is down • **On** – Link is up, 5.0 GT/s, all Lanes are up • **Blinking, 0.5 seconds On, 0.5 seconds Off** – Link is up, 5.0 GT/s, reduced Lanes are up • **Blinking, 1.5 seconds On, 0.5 seconds Off** – Link is up, 2.5 GT/s, all Lanes are up • **Blinking, 0.5 seconds On, 1.5 seconds Off** – Link is up, 2.5 GT/s, reduced Lanes are up Continued…

Table 3-11. Device-Specific Signals – 33 Balls *(Cont.)*

Signal Name	Type	Location	Description
PEX_PORT_GOOD[23:16, 3:0]#	I/O PU	AA25, W24, Y25, W25, E1, G3, F1, G2, Y2, Y4, C1, D3	Continued… **PORT_GOOD Function – Virtual Switch Mode Only** In Virtual Switch mode, PEX_PORT_GOOD*x*# are associated to specific Ports, by one of two mechanisms: **1.** If the Management Port is enabled (STRAP_NT_ENABLE#=L and/or and STRAP_NT_UPSTRM_PORTSEL0=L, to enable the option to delay virtual switch Link training until Management Port software Sets the **Configuration Release** register *Initiate Configuration* bit (Port 0, accessible through the Management Port, offset 3ACh[0])), all PEX_PORT_GOOD*x*# signals are initially assigned to the Management Port. In this case, the PEX_PORT_GOOD*x*# signals are not associated to corresponding Ports in the virtual switches, until Management Port software, serial EEPROM, and/or I^{2}C/SMBus Sets the **Virtual Switch GPIO Update** register *VS GPIOs Update* bit (Port 0, accessible through the Management Port, offset 64Ch[0]), to complete the assignment of individual PEX_PORT_GOOD*x*# signals to specific virtual switches (after software, serial EEPROM, and/or I^{2}C/SMBus configures functionality in the **GPIO** registers (Port 0, accessible through the Management Port, offsets 600h, 604h, 614h, 61Ch, and 624h)), and assigns the signals to virtual switches, by programming the **VS*x* GPIO_PG 0_11 Assignment** register(s) (Port 0, accessible through the Management Port, offsets 650h through 65Ch). Therefore, in this mode, the PEX_PORT_GOOD*x*# signals do not reflect Link status for virtual switch Ports, until Management Port software, serial EEPROM, and/or I^{2}C/SMBus completes PEX_PORT_GOOD*x*# initialization, with one exception – the PEX_PORT_GOOD*x*# signal that corresponds to the Management Port reflects the Management Port Link status, provided that PORT_GOOD functionality is enabled (either as default, with the STRAP_TESTMODE[3:0] inputs (sampled at PEX_PERST# de-assertion) programmed to value Bh or Dh, or by Management Port software, serial EEPROM, and/or I^{2}C/SMBus programming the **GPIO 0_9 Direction Control** and/or **GPIO 10_11 Direction Control** register(s) (Port 0, accessible through the Management Port, offsets 600h and 604h, respectively)). **2.** If the Management Port is disabled, or if the Management Port is enabled and STRAP_NT_UPSTRM_PORTSEL0=H, to allow all Ports to concurrently linkup after the serial EEPROM download completes immediately following a Fundamental Reset, the PEX_PORT_GOOD*x*# signals are individually associated to corresponding Ports. Therefore, Continued…

Table 3-11. Device-Specific Signals – 33 Balls *(Cont.)*

Signal Name	Type	Location	Description
PEX_PORT_GOOD[23:16, 3:0]#	I/O PU	AA25, W24, Y25, W25, E1, G3, F1, G2, Y2, Y4, C1, D3	Continued… **PORT_GOOD Function – Virtual Switch Mode Only *(Cont.)*** the PEX_PORT_GOOD*x*# signals reflect the Link status of all enabled Ports, provided that PORT_GOOD functionality is enabled (either as default, with the STRAP_TESTMODE[3:0] inputs (sampled at PEX_PERST# de-assertion) programmed to value Bh or Dh, or by Management Port software, serial EEPROM, and/or I^{2}C/ SMBus programming the **GPIO 0_9 Direction Control** and/ or **GPIO 10_11 Direction Control** register(s) (Port 0, accessible through the Management Port, offsets 600h and 604h, respectively)). To assign individual PEX_PORT_GOOD*x*# signals to specific virtual switches, Management Port software, serial EEPROM, and/or I^{2}C can program the associated **VS*x* GPIO_PG 0_11 Assignment** register(s) (Port 0, accessible through the Management Port, offsets 650h through 65Ch). Individual PEX_PORT_GOOD*x*# signal assignments must be mutually exclusive among the virtual switches. The 12 bits in each **VS*x* GPIO_PG 0_11 Assignment** register correspond to the 12 PEX_PORT_GOOD*x*# signals. (Refer to the register, for signal-to-bit mapping.) Setting a bit in one of the four registers assigns the signal to the virtual switch indicated by the register name. Because any PEX_PORT_GOOD*x*# signal must not be assigned to more than one virtual switch, **each of the 12 bits can be Set exclusively in only one of the four registers**. A maximum of 12 PEX_PORT_GOOD*x*# signals can be assigned to any one virtual switch. After the **VS*x* GPIO_PG 0_11 Assignment** register(s) are programmed, the actual assignments do not take effect, until Management Port software, serial EEPROM, and/or I^{2}C Sets the **Virtual Switch GPIO Update** register *VS GPIOs Update* bit (Port 0, accessible through the Management Port, offset 64Ch[0]). After the PEX_PORT_GOOD*x*# signals are assigned to virtual switches, each virtual switch can then configure individual PEX_PORT_GOOD*x*# signal functionality, by programming the **Virtual Switch GPIO_PG 0_9 Direction Control** and/or **Virtual Switch GPIO_PG 10_11 Direction Control** register(s) (VS Upstream Port(s), offsets A34h and A38h, respectively). In these registers, the PEX_PORT_GOOD*x*# signals are virtualized, and the bit numbers do not correspond to specific signal names. Software can determine how many and which PEX_PORT_GOOD*x*# signals are assigned to a unique virtual switch, by reading the **Virtual Switch GPIO_PG 0_11 Availability** register *Number of GPIO_PGs Available* field (VS Upstream Port(s), offset A3Ch[3:0]). Virtual switch software does not determine which of the actual PEX_PORT_GOOD*x*# signals are assigned to the virtual switch. The bit numbering is relative within the context of each virtual switch.

Table 3-11. Device-Specific Signals – 33 Balls *(Cont.)*

Signal Name	Type	Location	Description
VS3_PERST# VS2_PERST# VS1_PERST# VS0_PERST#	I/O PU	AE26, AB26, AC26, Y24	**Virtual Switch Fundamental Reset (4 Balls)** Fundamental Reset signal for Virtual Switches 3 through 0, respectively. Used in Virtual Switch mode, to cause a Fundamental Reset (PERST#) (one per virtual switch). (Refer to Section 5.2, “Resets – Virtual Switch Mode,” for further details.) ***Notes:*** *Although these are I/O signals, their logical operation in Virtual Switch mode is input.* *The PEX_PERST# signal, defined in Table 3-3, is the Reset input used in Base mode.* *In Base mode, the VSx_PERST# inputs must be pulled or tied High.*

3.4.8 External Resistor Signals

Table 3-12. External Resistor Signals – 12 Balls

Signal Name	Type	Location	Description
REXT_A[11:8, 1:0]	A	D9, N4, D18, N23, AC18, AC9	**External Resistor Balls (6 Balls)** One pair per SerDes block (paired with the “B” signal). **Must attach a 1.43KΩ 1% resistor between each REXT_A and REXT_B pair.** **Do not connect to any other signal, power, nor ground.**
REXT_B[11:8, 1:0]	A	E9, N5, E18, N22, AB18, AB9	**External Resistor Balls (6 Balls)** One pair per SerDes block (paired with the “A” signal). **Must attach a 1.43KΩ 1% resistor between each REXT_A and REXT_B pair.** **Do not connect to any other signal, power, nor ground.**

3.4.9 No Connect Signals

Caution: ***Do not connect these balls to board electrical paths.***
These balls are internally connected to the device.

Table 3-13. No Connect Signals – 20 Balls

Signal Name	Type	Location	Description
N/C	***Reserved***	A9, A18, B9, B18, F9, F18, N1, N2, N6, N21, N25, N26, W4, AA9, AA18, AC24, AE18, AF18, AF25	**No Connect (19 Balls)** Do not connect these balls to board electrical paths.
SPARE2	I/O PU	AA2	**Spare** ***Reserved for future use*** Do not connect these balls to board electrical paths.

3.4.10 Power and Ground Signals

Table 3-14. Power and Ground Signals – 346 Balls

Signal Name	Type	Location	Description
VDD10	CPWR	L11, L13, L15, M12, M14, M16, N11, N13, N15, P12, P14, P16, R11, R13, R15, T12, T14, T16	**1.0V ±5% Power for Core and SerDes Digital Logic (18 Balls)**
VDD10A	APWR	G9, G10, G11, G12, G13, G14, G15, G16, G17, G18, J7, J11, J13, J14, J16, J20, K7, K20, L7, L9, L18, L20, M7, M9, M18, M20, N7, N20, P7, P9, P18, P20, R7, R10, R17, R20, T7, T9, T18, T20, U7, U20, V11, V13, V14, V16, Y9, Y10, Y11, Y12, Y13, Y14, Y15, Y16, Y17, Y18	**1.0V ±5% Power for SerDes Analog Circuits (56 Balls)**

Table 3-14. Power and Ground Signals – 346 Balls *(Cont.)*

Signal Name	Type	Location	Description
VDD25	I/OPWR	G7, G20, H8, H19, J9, J18, K10, K17, U10, U17, V8, V9, V18, V19, W7, W8, W19, W20, Y7, Y20	**2.5V ±10% Power for I/O Logic Functions (20 Balls)**
VDD25A	PLLPWR	K12, K15, N10, N17, U12, U15	**2.5V ±10% Power for Phase-Locked Loop (PLL) Circuits (6 Balls)**
VSS	GND	A1, A4, A23, A25, A26, B4, B23, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, D4, D23, E4, E23, F4, F5, F6, F7, F8, F10, F11, F12, F13, F14, F15, F16, F17, F19, F20, F21, F22, F23, G8, G19, H1, H2, H4, H5, H6, H7, H9, H10, H11, H12, H13, H14, H15, H16, H17, H18, H20, H21, H22, H23, H25, H26, J3, J6, J8, J10, J12, J15, J17, J19, J21, J24, K3, K6, K8, K9, K11, K13, K14, K16, K18, K19, K21, K24, L3, L6, L8, L10, L12, L14, L16, L17, L19, L21, L24, M3, M6, M8, M10, M11, M13, M15, M17, M19, M21, M24, N3, N8, N9, N12, N14, N16, N18, N19, N24, P3, P6, P8, P10, P11, P13, P15, P17, P19, P21, P24, R3, R6, R8, R9, R12, R14, R16, R18, R19, R21, R24, T3, T6, T8, T10, T11, T13, T15, T17, T19, T21, T24, U3, U6, U8, U9, U11, U13, U14, U16, U18, U19, U21, U24, V1, V2, V3, V4, V5, V6, V7, V10, V12, V15, V17, V20, V21, V22, V23, V24, V25, V26, W9, W10, W11, W12, W13, W14, W15, W16, W17, W18, Y8, Y19, AA4, AA5, AA6, AA7, AA8, AA10, AA11, AA12, AA13, AA14, AA15, AA16, AA17, AA19, AA20, AA21, AA22, AA23, AB4, AB23, AC4, AC23, AD5, AD6, AD7, AD8, AD9, AD10, AD11, AD12, AD13, AD14, AD15, AD16, AD17, AD18, AD19, AD20, AD21, AD22, AD23, AE4, AE23, AF1, AF4, AF23, AF26	**Ground Connections (246 Balls)**

3.5 Physical Layout

Figure 3-1. Physical Ball Assignment (See-Through Top View)

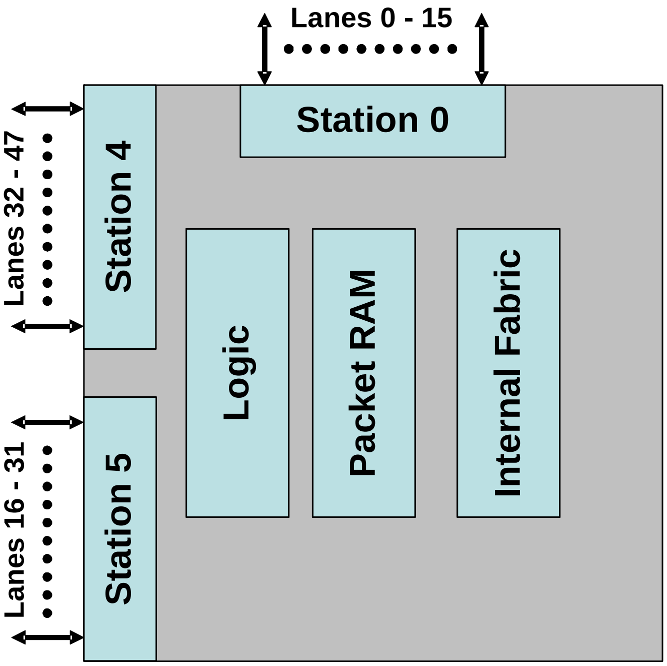
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	VSS	STRAP_NT_UPSTRM_PORTSEL0	STRAP_NT_ENABLE#	VSS	PEX_PETn24	PEX_PETn25	PEX_PETn26	PEX_PETn27	N/C	PEX_PETn28	PEX_PETn29	PEX_PETn30	PEX_PETn31	PEX_PETn47	PEX_PETn46	PEX_PETn45	PEX_PETn44	N/C	PEX_PETn43	PEX_PETn42	PEX_PETn41	PEX_PETn40	VSS	STRAP_UPSTRM_PORTSEL3	VSS	VSS	A
B	JTAG_TMS	JTAG_TCK	SHPC_INT#	VSS	PEX_PETp24	PEX_PETp25	PEX_PETp26	PEX_PETp27	N/C	PEX_PETp28	PEX_PETp29	PEX_PETp30	PEX_PETp31	PEX_PETp47	PEX_PETp46	PEX_PETp45	PEX_PETp44	N/C	PEX_PETp43	PEX_PETp42	PEX_PETp41	PEX_PETp40	VSS	STRAP_STN5_PORTCFG1	HP_ATNLED_C#	HP_PWRFLT_C#	B
C	PEX_PORT_GOOD1#	JTAG_TRST#	JTAG_TDI	STRAP_STN4_PORTCFG0	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	STRAP_STN5_PORTCFG0	FATAL_ERR#	HP_BUTTON_C#	GPIO24	C
D	PEX_INTA#	STRAP_VS_MODE1	PEX_PORT_GOOD0#	VSS	PEX_PERn24	PEX_PERn25	PEX_PERn26	PEX_PERn27	REXT_A11	PEX_PERn28	PEX_PERn29	PEX_PERn30	PEX_PERn31	PEX_PERn47	PEX_PERn46	PEX_PERn45	PEX_PERn44	REXT_A9	PEX_PERn43	PEX_PERn42	PEX_PERn41	PEX_PERn40	VSS	HP_PWREN_C	HP_PRSNT_C#	HP_PWRLED_C#	D
E	PEX_PORT_GOOD19#	I2C_ADDR0	I2C_SDA0	VSS	PEX_PERp24	PEX_PERp25	PEX_PERp26	PEX_PERp27	REXT_B11	PEX_PERp28	PEX_PERp29	PEX_PERp30	PEX_PERp31	PEX_PERp47	PEX_PERp46	PEX_PERp45	PEX_PERp44	REXT_B9	PEX_PERp43	PEX_PERp42	PEX_PERp41	PEX_PERp40	VSS	GPIO25	EE_SK	EE_CS#	E
F	PEX_PORT_GOOD17#	I2C_ADDR2	I2C_ADDR1	VSS	VSS	VSS	VSS	VSS	N/C	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	N/C	VSS	VSS	VSS	VSS	VSS	HP_CLKEN_C#	HP_PWR_GOOD_C	EE_DO	F
G	STRAP_STN4_PORTCFG1	PEX_PORT_GOOD16#	PEX_PORT_GOOD18#	I2C_SCL0	JTAG_TDO	STRAP_NT_UPSTRM_PORTSEL1	VDD25	VSS	VDD10A	VDD10A	VDD10A	VDD10A	VDD10A	VDD10A	VDD10A	VDD10A	VDD10A	VDD10A	VSS	VDD25	HP_MRL_C#	HP_PERST_C#	EE_DI	STRAP_UPSTRM_PORTSEL1	STRAP_UPSTRM_PORTSEL0	STRAP_UPSTRM_PORTSEL2	G
H	VSS	VSS	STRAP_VS_MODE0	VSS	VSS	VSS	VSS	VDD25	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD25	VSS	VSS	VSS	VSS	STRAP_RESERVED17#	VSS	VSS	H
J	PEX_PETn23	PEX_PETp23	VSS	PEX_PERn23	PEX_PERp23	VSS	VDD10A	VSS	VDD25	VSS	VDD10A	VSS	VDD10A	VDD10A	VSS	VDD10A	VSS	VDD25	VSS	VDD10A	VSS	PEX_PERp39	PEX_PERn39	VSS	PEX_PETp39	PEX_PETn39	J
K	PEX_PETn22	PEX_PETp22	VSS	PEX_PERn22	PEX_PERp22	VSS	VDD10A	VSS	VSS	VDD25	VSS	VDD25A	VSS	VSS	VDD25A	VSS	VDD25	VSS	VSS	VDD10A	VSS	PEX_PERp38	PEX_PERn38	VSS	PEX_PETp38	PEX_PETn38	K
L	PEX_PETn21	PEX_PETp21	VSS	PEX_PERn21	PEX_PERp21	VSS	VDD10A	VSS	VDD10A	VSS	VDD10	VSS	VDD10	VSS	VDD10	VSS	VSS	VDD10A	VSS	VDD10A	VSS	PEX_PERp37	PEX_PERn37	VSS	PEX_PETp37	PEX_PETn37	L
M	PEX_PETn20	PEX_PETp20	VSS	PEX_PERn20	PEX_PERp20	VSS	VDD10A	VSS	VDD10A	VSS	VSS	VDD10	VSS	VDD10	VSS	VDD10	VSS	VDD10A	VSS	VDD10A	VSS	PEX_PERp36	PEX_PERn36	VSS	PEX_PETp36	PEX_PETn36	M
N	N/C	N/C	VSS	REXT_A10	REXT_B10	N/C	VDD10A	VSS	VSS	VDD25A	VDD10	VSS	VDD10	VSS	VDD10	VSS	VDD25A	VSS	VSS	VDD10A	N/C	REXT_B8	REXT_A8	VSS	N/C	N/C	N
P	PEX_PETn19	PEX_PETp19	VSS	PEX_PERn19	PEX_PERp19	VSS	VDD10A	VSS	VDD10A	VSS	VSS	VDD10	VSS	VDD10	VSS	VDD10	VSS	VDD10A	VSS	VDD10A	VSS	PEX_PERp35	PEX_PERn35	VSS	PEX_PETp35	PEX_PETn35	P
R	PEX_PETn18	PEX_PETp18	VSS	PEX_PERn18	PEX_PERp18	VSS	VDD10A	VSS	VSS	VDD10A	VDD10	VSS	VDD10	VSS	VDD10	VSS	VDD10A	VSS	VSS	VDD10A	VSS	PEX_PERp34	PEX_PERn34	VSS	PEX_PETp34	PEX_PETn34	R
T	PEX_PETn17	PEX_PETp17	VSS	PEX_PERn17	PEX_PERp17	VSS	VDD10A	VSS	VDD10A	VSS	VSS	VDD10	VSS	VDD10	VSS	VDD10	VSS	VDD10A	VSS	VDD10A	VSS	PEX_PERp33	PEX_PERn33	VSS	PEX_PETp33	PEX_PETn33	T
U	PEX_PETn16	PEX_PETp16	VSS	PEX_PERn16	PEX_PERp16	VSS	VDD10A	VSS	VSS	VDD25	VSS	VDD25A	VSS	VSS	VDD25A	VSS	VDD25	VSS	VSS	VDD10A	VSS	PEX_PERp32	PEX_PERn32	VSS	PEX_PETp32	PEX_PETn32	U
V	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD25	VDD25	VSS	VDD10A	VSS	VDD10A	VDD10A	VSS	VDD10A	VSS	VDD25	VDD25	VSS	VSS	VSS	VSS	VSS	VSS	VSS	V
W	STRAP_G1_COMPATIBLE#	STRAP_TESTMODE3	STRAP_SMBUS_EN#	N/C	HP_PRSNT_B#	STRAP_DEBUG_SEL1	VDD25	VDD25	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD25	VDD25	VS3_PEX_INTA#	VS2_FATAL_ERR#	GPIO27	PEX_PORT_GOOD22#	PEX_PORT_GOOD20#	STRAP_SERDES_MODE_EN#	W
Y	STRAP_I2C_CFG_EN#	PEX_PORT_GOOD3#	HP_PWR_GOOD_B	PEX_PORT_GOOD2#	GPIO29	STRAP_TESTMODE0	VDD25	VSS	VDD10A	VDD10A	VDD10A	VDD10A	VDD10A	VDD10A	VDD10A	VDD10A	VDD10A	VDD10A	VSS	VDD25	STRAP_PROBE_MODE#	STRAP_FAST_BRINGUP#	VS1_PEX_INTA#	VS0_PERST#	PEX_PORT_GOOD21#	STRAP_PLL_BYPASS#	Y
AA	STRAP_NT_P2P_EN#	SPARE2	STRAP_NT_UPSTRM_PORTSEL2	VSS	VSS	VSS	VSS	VSS	N/C	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	N/C	VSS	VSS	VSS	VSS	VSS	VS2_PEX_INTA#	PEX_PORT_GOOD23#	GPIO26	AA
AB	HP_ATNLED_B#	HP_MRL_B#	HP_BUTTON_B#	VSS	PEX_PERp0	PEX_PERp1	PEX_PERp2	PEX_PERp3	REXT_B0	PEX_PERp4	PEX_PERp5	PEX_PERp6	PEX_PERp7	PEX_PERp8	PEX_PERp9	PEX_PERp10	PEX_PERp11	REXT_B1	PEX_PERp12	PEX_PERp13	PEX_PERp14	PEX_PERp15	VSS	STRAP_NT_UPSTRM_PORTSEL4	VS3_FATAL_ERR#	VS2_PERST#	AB
AC	PEX_PERST#	HP_PWREN_B	HP_PWRFLT_B#	VSS	PEX_PERn0	PEX_PERn1	PEX_PERn2	PEX_PERn3	REXT_A0	PEX_PERn4	PEX_PERn5	PEX_PERn6	PEX_PERn7	PEX_PERn8	PEX_PERn9	PEX_PERn10	PEX_PERn11	REXT_A1	PEX_PERn12	PEX_PERn13	PEX_PERn14	PEX_PERn15	VSS	N/C	I2C_SCL1	VS1_PERST#	AC
AD	HP_PERST_B#	HP_PWRLED_B#	GPIO31	STRAP_TESTMODE2	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	STRAP_STN0_PORTCFG0	PEX_NT_RESET#	VS1_FATAL_ERR#	AD
AE	HP_CLKEN_B#	GPIO30	GPIO28	VSS	PEX_PETp0	PEX_PETp1	PEX_PETp2	PEX_PETp3	PEX_REFCLKp	PEX_PETp4	PEX_PETp5	PEX_PETp6	PEX_PETp7	PEX_PETp8	PEX_PETp9	PEX_PETp10	PEX_PETp11	N/C	PEX_PETp12	PEX_PETp13	PEX_PETp14	PEX_PETp15	VSS	STRAP_RESERVED16	I2C_SDA1	VS3_PERST#	AE
AF	VSS	STRAP_TESTMODE1	STRAP_DEBUG_SEL0	VSS	PEX_PETn0	PEX_PETn1	PEX_PETn2	PEX_PETn3	PEX_REFCLKn	PEX_PETn4	PEX_PETn5	PEX_PETn6	PEX_PETn7	PEX_PETn8	PEX_PETn9	PEX_PETn10	PEX_PETn11	N/C	PEX_PETn12	PEX_PETn13	PEX_PETn14	PEX_PETn15	VSS	STRAP_STN0_PORTCFG1	N/C	VSS	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

Chapter 4 Functional Overview

4.1 Hardware Architecture

The PEX 8649 is designed with a flexible, modular architecture. The 48 PCI Express Lanes are implemented equally across three Stations (16 per Station), which are connected to one another by the internal fabric to the central RAM. Figure 4-1 provides a block diagram of the PEX 8649.

Figure 4-1. PEX 8649 Block Diagram



4.1.1 Station and Port Functions

Each Port implements the *PCI Express Base r2.0* Physical, Data Link, and Transaction Layers (PHY, DLL, and TL, respectively). Each PCI Express Station supports up to 16 integrated Serializer/ De-Serializer (SerDes) modules, which provide the 48 PCI Express hardware interface Lanes.

The Lanes can be combined, for a total of one to four PCI Express Ports per Station. Lanes from different Stations cannot be combined to form Ports.

4.1.1.1 Port Configurations

The Port configuration of each Station is independent of the other Stations' Port configurations. Ports that are not configured nor enabled are invisible to software.

The upstream and downstream Ports' Link widths are initially Set by the Strapping balls, which are pulled or tied High to VDD25 or Low to VSS (GND). The serial EEPROM option can be used to re-configure the Ports, with the options defined in Table 4-1. Serial EEPROM configuration occurs following a Fundamental Reset, and overrides the configuration Set by the Strapping balls at that time. Port configuration can also be changed through the I^2C Slave interface. The final Link width can be automatically negotiated down from the programmed width, through Link-width negotiation for linkup to a device with fewer Lanes. The narrowest Port on one end of the Link determines the maximum Link width. Additionally, if a connection is broken on one of the Lanes, the training sequence removes the broken Lane and negotiates to a narrower width. A x16 Port can negotiate down to x8, x4, x2, or x1.

If the Port cannot train to x1 (Lane 0 is broken), the Port reverses its Lanes and attempts to retrain. *For example*, a x16 Port that cannot train to x16 attempts to negotiate down to x8, x4, x2, or x1; if x1 linkup fails, the Port reverses its Lanes and re-attempts linkup negotiation. Either the lowest Lane (Lane 0) or highest Lane (if Lanes are reversed) of the programmed Link width must connect to the other device's Lane 0.

Each Port can run independently at Gen 1 (2.5 GT/s) or Gen 2 (5.0 GT/s) speed.

Table 4-1 defines the PEX 8649 Port, Station, and Lane configurations for Base mode. The Lanes are assigned to each enabled Port, in sequence, as indicated in [brackets]. The yellow highlighted cells indicate the default Parallel Hot Plug Ports. Hot Plug Port assignment is described in Section 10.8.1, "Default Parallel Hot Plug Ports – Base Mode."

Table 4-1. Port Configurations[a]

Port Configuration Strapping STRAP_STN0_PORTCFG[1:0]	Port Configuration Register Value Port 0, Offset 300h[1:0]	Station 0 [Lanes/SerDes]/Port			
		Port 0	Port 1	Port 2	Port 3
00b	00b	x4 [0-3]	x4 [4-7]	x4 [8-11]	x4 [12-15]
01b	01b	x16 [0-15]			
10b	10b	x8 [0-7]	x8 [8-15]		
11b	11b	x8 [0-7]	x4 [8-11]	x4 [12-15]	

Port Configuration Strapping STRAP_STN5_PORTCFG[1:0]	Port Configuration Register Value Port 0, Offset 300h[11:10]	Station 5 [Lanes/SerDes]/Port			
		Port 20	Port 21	Port 22	Port 23
00b	00b	x4 [16-19]	x4 [20-23]	x4 [24-27]	x4 [28-31]
01b	01b	x16 [16-31]			
10b	10b	x8 [16-23]	x8 [24-31]		
11b	11b	x8 [16-23]	x4 [24-27]	x4 [28-31]	

Port Configuration Strapping STRAP_STN4_PORTCFG[1:0]	Port Configuration Register Value Port 0, Offset 300h[9:8]	Station 4 [Lanes/SerDes]/Port			
		Port 16	Port 17	Port 18	Port 19
00b	00b	x4 [32-35]	x4 [36-39]	x4 [40-43]	x4 [44-47]
01b	01b	x16 [32-47]			
10b	10b	x8 [32-39]	x8 [40-47]		
11b	11b	x8 [32-39]	x4 [40-43]	x4 [44-47]	

[a] *Register offset 300h is located, as follows:*

Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port.

4.1.1.2 Virtual Switch Port Configurations – Virtual Switch Mode

Assignment of specific Ports to individual virtual switches can be changed by Management Port software, serial EEPROM, and/or I^{2}C/SMBus, by programming the **VS*x* Port Vector** register(s) (Port 0, accessible through the Management Port, offsets 380h through 38Ch). Each Port can be assigned to only one virtual switch.

The designation of upstream Ports for virtual switches can also be changed by Management Port software, serial EEPROM, and/or I^{2}C/SMBus, by programming the **VS*x* Upstream** register(s) (Port 0, accessible through the Management Port, offsets 360h through 36Ch). Only one Port per virtual switch can be designated as an upstream Port.

Table 4-2 lists the default Port configuration according to the number of enabled virtual switches. The default Hot Plug Ports and balls are indicated as well. The Port Numbers referenced correspond to those listed in Table 4-1.

Table 4-2. Virtual Switch Port Configurations and Default Parallel Hot Plug Ports – Virtual Switch Mode

Number of Virtual Switches	STRAP_VS_MODE[1:0] Value	Upstream Ports	Downstream Ports	Default Hot Plug Ports and Balls
2	LH	P0	P1, P2, P3, P20, P21	P20-B
		P16	P17, P18, P19, P22, P23	P22-C
3	HL	P0	P1, P2, P3	P1-B
		P16	P17, P18, P19	P17-C
		P20	P21, P22, P23	
4	HH	P0	P1, P2	P1-B
		P16	P3, P17	P3-C
		P20	P21, P18	
		P22	P23, P19	

4.1.1.3 Station, Station Register Port Number, Physical Port, Physical Lane and SerDes Module, and SerDes Quad Relationships

Table 4-3 provides an explanation of the Station, Station register Port Number, physical Port, physical Lane and SerDes module, and SerDes quad relationships, when all Ports are enabled. These relationships apply to Base mode and Virtual Switch mode.

Table 4-3. Station, Station Register Port Number, Physical Port, Physical Lane and SerDes Module, and SerDes Quad Relationships, When All Ports Are Enabled

Station	Station Register Port Number	Physical Port	Physical Lanes and SerDes Modules	SerDes Quad
0	0	0	0-3	0
		1	4-7	1
		2	8-11	2
		3	12-15	3
5	20	20	16-19	0
		21	20-23	1
		22	24-27	2
		23	28-31	3
4	16	16	32-35	0
		17	36-39	1
		18	40-43	2
		19	44-47	3

4.1.1.4 Port Numbering

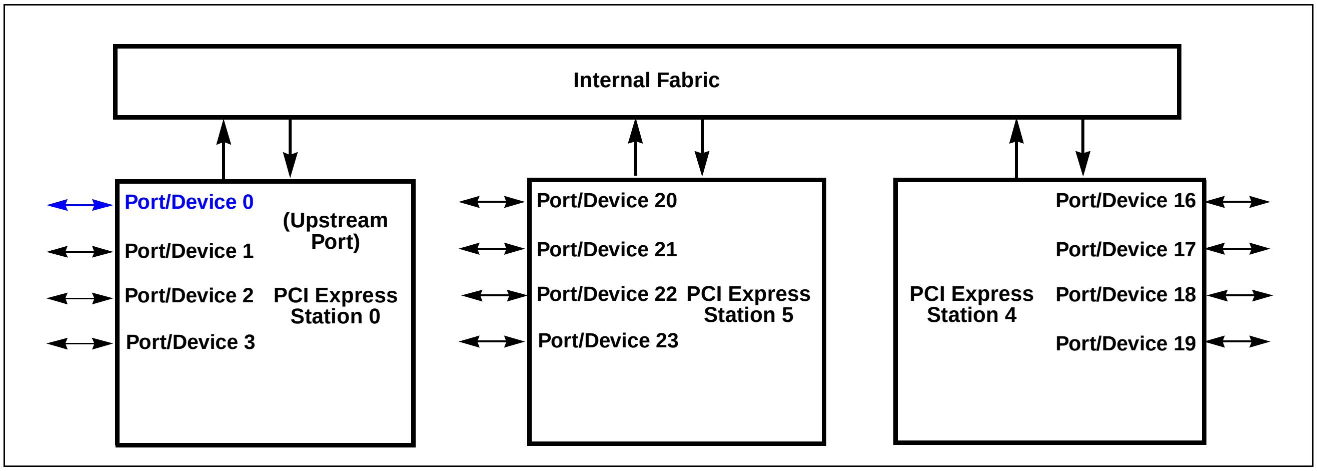
The PEX 8649 Port Numbers are as follows (refer to Table 4-1 through Table 4-3, and Figure 4-2):

- Station 0 – Ports 0, 1, 2, and 3
- Station 4 – Ports 16, 17, 18, and 19
- Station 5 – Ports 20, 21, 22, and 23

The Port Numbers have a direct relationship to the downstream Ports for the PCI Device Number assigned to the internal PCI-to-PCI bridges on the internal virtual PCI Bus. *For example*, if Port 16 is a downstream Port, the PCI-to-PCI bridge associated with that Port is Device Number 16. All downstream Device Numbers match their corresponding Port Number. *For example*, if Port 0 is the upstream Port, Ports 1 through 3 and 16 through 23 are the downstream Ports. The Device Numbers for the PCI-to-PCI bridges implemented on the downstream Ports are 1 through 3 and 16 through 23, respectively. (Refer to Figure 4-2.)

Any PEX 8649 Port can be configured as, or dynamically changed to be, the upstream Port (Port 0 is recommended in Base mode, described in the next section). The PCI-to-PCI bridge implemented on the upstream Port does not assume a Device Number – it accepts the Device Number assigned by the upstream device. Generally, the upstream device assigns Device Number 0, according to the *PCI Express Base r2.0*.

Figure 4-2. PLX Port Numbering Convention Example (Base Mode Shown, with Port 0 as Upstream Port)



4.2 PCI Express Station Functional Description

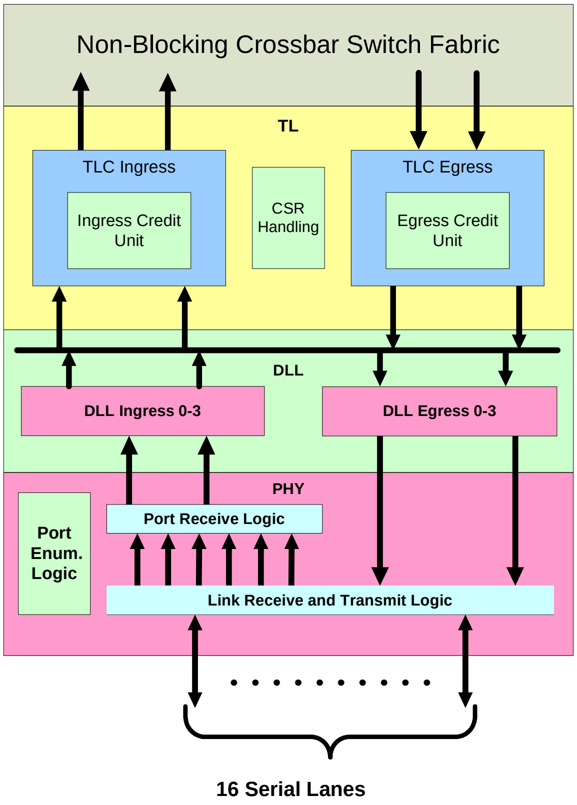
The PEX 8649 groups SerDes together into a Station, as listed in Table 4-1 and Table 4-3. The Station forwards ingress packets to the internal fabric and central RAM, and the Station pulls egress packets from the central RAM to send out of the PEX 8649.

Each Station implements the PCI Express PHY and DLL functions for each of its Ports, and aggregates traffic from these Ports onto a transaction-based, non-blocking internal crossbar fabric. The PCI Express Station also performs many TL functions, while the packet queuing and ordering aspects of this layer are handled by the Crossbar Switch Control blocks.

During system initialization, software initiates Configuration Requests that set up the PCI Express interfaces, Device Numbers, and Address maps across the various Ports. These maps are used to direct traffic between Ports during standard system operation. Traffic flow between the Ports of the same Station, or Ports on different Stations, is supported through the central internal fabric.

At the top level, each Station has a layered organization consisting of the PHY, DLL, and TL blocks, as illustrated in Figure 4-3. The PHY and DLL blocks have Port-specific data paths (one per PCI Express Port) that operate independently of one another. The Transaction Layer Control (TLC) ingress section of the TL block aggregates traffic for all ingress Ports in the Station, then sends the traffic to the internal fabric. The TLC egress section of the TL block accepts packets, by way of the internal crossbar fabric, from all ingress Ports, and schedules them to be sent out the appropriate egress Port.

Figure 4-3. PCI Express Station Block Diagram



4.3 Physical Layer

The Physical Layer (PHY) converts information received from the DLL into an appropriate serialized format and transmits it across the PCI Express Link. The PHY also receives the serialized input from the Serializer/De-Serializer (SerDes), converts it to parallel data (internal Data Bus), then writes it to the TLC Ingress buffer.

The PHY includes all circuitry for PCI Express Link interface operation, including:

- Driver and input buffers
- Parallel-to-serial and serial-to-parallel conversion
- Phase-Locked Loops (PLLs) and clock circuitry
- Impedance matching circuitry
- Interface initialization and maintenance functions

4.3.1 Physical Layer Features

- 16 SerDes, per Station
- Up to four Ports per Station, and each Port can belong to the same or different virtual hierarchies, in any combination
- Multiple upstream Port support in Virtual Switch mode – zero to four upstream Ports, per instance
- User-configurable Port division – minimum of four (4) SerDes, per Port
  - x16
  - x8, x8
  - x8, x4, x4
  - x4, x4, x4, x4
- Hardware Link training and initialization
- Hardware detection of polarity inversion
- Hardware detection of Lane reversal
- Supported Link widths – x4, x8, or x16; Link widths of x1 and x2 are also supported
- Supported Link speeds – 2.5 and 5.0 GT/s
  - Constant Core Clock frequency (250 MHz), variable-width Data path (10/9 bits at Gen 1 rate, 20/18 bits at Gen 2 rate)
- Modified Compliance Pattern support with Receiver Error Counters, per Lane
- Hardware insertion of Sequence Number, STP, SDP, END, and EDB symbols
- Hardware Autonomous Speed Control supported
- Dynamic Link speed control supported
- Dynamic Link width supported
- Data scrambling and 8b/10b encode/decode
- Receiver Error checking (Elastic buffer over/underflow, disparity and symbol encoding)
- Modified Compliance Pattern support with Receiver Error Counters, per Lane
- Link state Power Management – supported power states are as follows:
  - L0
  - L0s
  - L1
  - L2/L3 Ready (condition before L2 or L3)
  - L3 (no Vaux)
- Upstream Port(s) can operate as Link Negotiation Master (upstream cross-link)
- Downstream Port(s) can operate as Link Negotiation Slave (downstream cross-link)
- Checks and removes Data Link Layer Packet (DLLP) framing symbols
- Checks and removes DLLP Link Cyclic Redundancy Check (LCRC)

4.3.2 PHY Status and Command Registers

The PHY operating conditions are defined in:

- Section 13.15.3, “Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)”
- Section 13.15.17, “Device-Specific Registers – Physical Layer (Offsets B80h – BC8h)”

The System Host can track the Link operating status and re-configure Link parameters, by way of these registers.

4.3.3 Hardware Link Interface Configuration

The PHY can include up to 16 integrated SerDes modules on each Station. The SerDes modules are distributed among four SerDes quads (Quads 0, 1, 2, and 3) and provide the PCI Express hardware interface Lanes. (Refer to Table 4-3, which lists the relationship of the SerDes modules and quads to the Stations, Ports, and Lanes, when all Ports are enabled.) The SerDes modules also provide all physical communication controls and functions required by the *PCI Express Base r2.0*, as well as the Links (clustered into Ports) that connect the PEX 8649 to other PCI Express devices.

The number of Ports, and Link widths associated with those Ports, are configurable, on a Station-by-Station basis. Initial Port configuration is determined by Strapped signal balls, serial EEPROM, or auto Link-width negotiation. After the Ports are configured using the auto-negotiation process, the Link widths can narrow or widen (by combining multiple adjacent Lanes within the Station).

4.4 Transaction Layer

The upper layer of the architecture is the Transaction Layer (TL). The TL assembles and disassembles TLPs, which are used to communicate transactions, *such as* Read and Write, as well as certain types of events. The TL also manages credit-based Flow Control (FC) for TLPs.

The TL supports four Address spaces – it includes the three PCI Address spaces (Memory, I/O, and Configuration) and adds a Message space. (Refer to Table 4-4.) This specification uses Message space to support all prior sideband signals, *such as* interrupts, Power Management (PM) Requests, and so forth, as in-band Message transactions. PCI Express Message transactions are considered *virtual wires* that support *virtual pins*. As virtual wires, Assert and De-assert Messages are sent when a triggering event changes the state of the wire.

Table 4-4. Address Spaces Support Differing Transaction Types

Address Space	Transaction Types	Transaction Functions
Configuration	Read/Write	Device configuration or setup
Input/Output		Transfers data from/to an I/O space
Memory		Transfers data from/to a memory location
Message	Baseline/Virtual Wires	General-purpose Messages Event signaling (status, interrupts, and so forth)

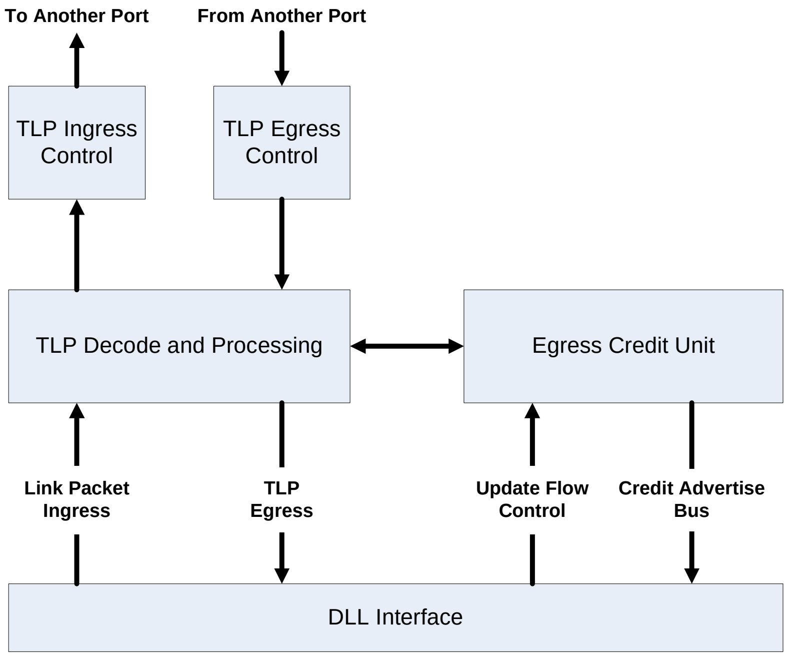
All Request packets requiring a Response packet are implemented as Split Transactions. Each packet has a unique identifier that enables Response packets to be directed to the correct originator. The packet format supports different forms of addressing, depending upon the transaction type – *Memory, I/O, Configuration, and Message*. The packets can also have attributes, *such as No Snoop* and *Relaxed Ordering*.

TL functions include:

- Decoding and checking rules for the incoming TLP
- Memory-Mapped Configuration Space register (CSR) access
- Checking incoming packets for malformed or unsupported packets
- Data Poisoning and end-to-end data integrity detection
- End-to-end Cyclic Redundancy Check (ECRC) of incoming packets
- Error logging and reporting for incoming packets
- TLP dispatching
- Write control to the packet RAM and packet Link List RAM
- Destination lookup and TC-VC mapping
- Credit-based scheduling
- Pipelined full Split Transaction protocol
- PCI/PCI-X-compatible ordering
- Interrupt handling (INT*x* or Message Signaled Interrupts (MSIs))
- Power Management (PM) support
- Hot Plug and PCI Express Hot Plug event support
- Link State event support
- QoS support
- Ordering
- Ingress and Egress credit management

The hardware functions provided by the PEX 8649 to implement *PCI Express Base r2.0* TL requirements are illustrated in Figure 4-4. The blocks provide a combination of Ingress and Egress control, as well as the data management at each stage in the flow sequence.

Figure 4-4. TL Controller



4.4.1 Locked Transactions

The PEX 8649 understands Locked transactions; however, it does not lock the resources. This is consistent with limitations for Locked transaction use, as outlined in the *PCI r3.0* (Appendix F, “Exclusive Accesses”), and prevents potential deadlock, as well as serious performance degradation, that could occur with Locked transaction use.

4.4.2 Relaxed Ordering – Base Mode Only

In Base mode, the PEX 8649 supports Relaxed Ordering for Completions. By default, if the RO attribute is Set within a Completion, then that Completion can bypass Posted transactions, if Posted TLPs are blocked at the egress Port (due to insufficient Posted credits from the connected device). This behavior can be disabled, by Setting one and/or both of the following bits:

- **Station-Based Control** register *No Special Treatment for Relaxed Ordering Traffic* bit (Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface, offset 760h[29])
- **Ingress Control** register *No Special Treatment for Relaxed Ordering Traffic* bit (All Ports, offset F60h[5])

4.4.3 TL Transmit/Egress Protocol – End-to-End Cyclic Redundancy Check

End-to-End Cyclic Redundancy Check (ECRC) is an optional 32-bit field appended to the end of the outgoing packet. ECRC is calculated over the entire packet, starting with the Header and including the Data Payload, except for the *Endpoint* (*EP*) bit and bit 0 of the *Type* field, which are always considered to be a value of 1 for ECRC calculations. The *ECRC* field is transmitted, unchanged, as it moves through the fabric to the Completer device. The PEX 8649 checks the ECRC on all incoming TLPs, if enabled (**Advanced Error Capabilities and Control** register *ECRC Check Enable* bit, offset FCCh[8], is Set, in each Port), and can optionally report detected errors. (When the ECRC is detected, the **Uncorrectable Error Status** register *ECRC Error Status* bit (offset FB8h[19]) can be used to log ECRC errors.)

Additionally, the PEX 8649 can optionally append ECRC to the end of internally generated TLPs, *such as* Interrupt and Error Messages, if enabled (**Advanced Error Capabilities and Control** register *ECRC Generation Enable* bit, offset FCCh[6], is Set, in each Port).

4.4.4 TL Receive/Ingress Protocol

The ingress side TL collects and stores inbound TLP traffic in the packet RAM. The incoming data is checked for ECRC errors, valid type field, length matching the Header *Transfer Size* field, and other TLP-specific errors defined by the *PCI Express Base r2.0*.

Header and Data Payload information is forwarded to the Source Scheduler, to be routed across the internal fabric, to the egress Port. When ECRC errors are detected, the packet is discarded.

4.4.5 Flow Control Credit Initialization

The initial number of VC0 Flow Control (FC) credits is advertised as programmed for each type of Header and Payload. After VC0 FC initialization is complete, the FC credits received are transferred to the TL egress. The TL ingress must schedule an UpdateFC DLLP for transmission, to increase the number of advertised credits.

4.4.6 Flow Control Protocol

The PEX 8649 implements FC protocol that ensures that the switch:

- Does not transmit a TLP over a Link to a remote Receiver, unless the receiving device has sufficient VC Buffer space to accommodate the packet
- Generates FC credit updates to the remote Transmitter, to replace credits used to send TLPs to the PEX 8649

This FC is automatically managed by the hardware, and is transparent to software. Software is used only to enable additional Buffer space, to supplement the initial default buffer assignment.

The initial default FC credits, which are enabled after Link training, allow TLP traffic immediately after Link training completes. The Configuration transactions are the first transactions to use the default VC credits, to set up the initial device operating modes and capabilities.

The TL Ingress Credit Unit transmits DLLPs (referred to as *FC packets*) that update the FC to the remote Transmitter device, on a periodic basis. The DLLPs contain FC credit information that updates the Transmitter regarding the amount of available Buffer space in the PEX 8649.

The TL Egress Credit Unit receives DLLPs from the remote device, indicating the amount of Buffer space available in the remote Receiver. The unit uses this credit information to schedule the sending of TLPs to the remote device.

4.5 Modes of Operation

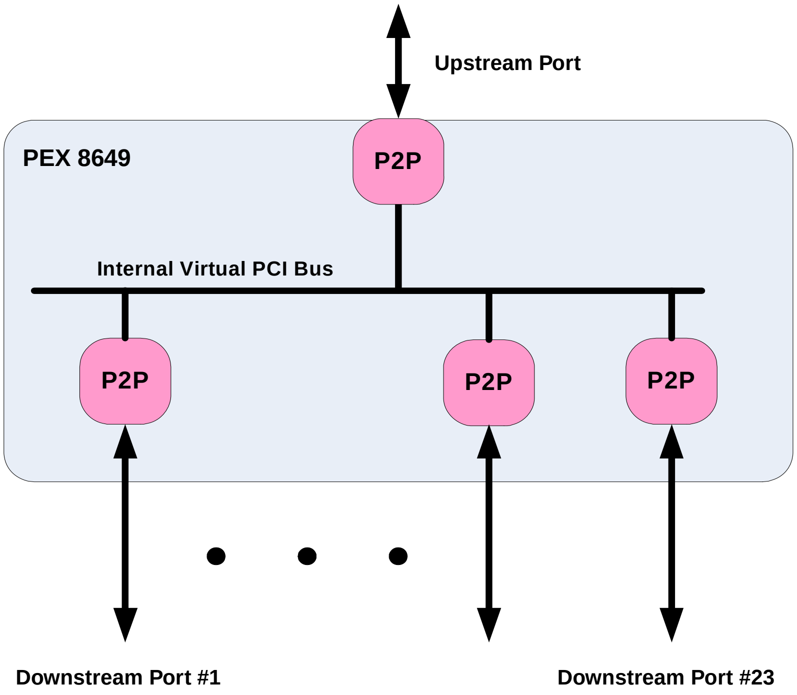
The PEX 8649 supports and implements two modes of operation – Base Mode and Virtual Switch Mode.

4.5.1 Base Mode

The PEX 8649 is a 48-Lane, 12-Port switch. Figure 4-5 illustrates the PEX 8649 in Base mode, from a software point of view. In Base mode, the PEX 8649 supports one upstream Port and up to 11 downstream Ports. The PEX 8649 implements a single NT Port, which can be optionally enabled and configured to be any Port, on any Station, within the PEX 8649. NT mode is useful in supporting high-availability systems and failover.

Note: *The P2P blocks in Figure 4-5 are a logical representation of how a Port presents itself to software.*

Figure 4-5. Base Mode



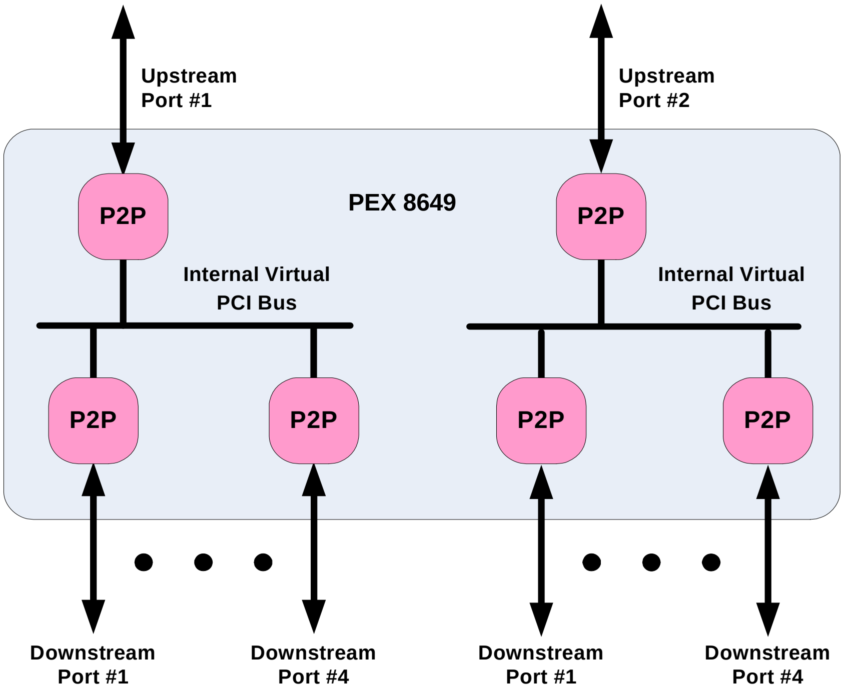
4.5.2 Virtual Switch Mode

In Virtual Switch mode, the PEX 8649 can be partitioned in up to four independent virtual switches. Each virtual switch is part of an independent PCI Express hierarchy, and do not share downstream Ports. Although the virtual switches share the same hardware infrastructure, they enforce the security between them so the traffic from one virtual switch does not leak into other virtual switches. A virtual switch can span across multiple Stations, and a Station can be shared by multiple virtual switches.

4.5.2.1 Bifurcated Switch Mode Example

The PEX 8649 can be bifurcated (partitioned) into two virtual switches of the same capacity, as illustrated in Figure 4-6. It can be used in applications *such as* two-way machines, where one Root Complex is attached to one upstream Port and a second Root Complex is attached to a second upstream Port.

Figure 4-6. Bifurcated Virtual Switch Mode Example



4.6 Failover Operations

This section describes failover operation in Base mode and Virtual Switch mode. In Base mode, the PEX 8649 supports a single Root Port and one NT Port. Users can connect two switches, using an NT Port, when there is a CPU connected to the upstream Port of each switch. This implementation allows them to support individual hierarchies, as well as a single hierarchy in case of failover. Some customers use NT to transfer bulk data from the chipset DMA engine, between the two Processors. In Virtual Switch mode, the PEX 8649 supports registers that help Management Port software to migrate/ Hot Plug/hot removal of the upstream and downstream Ports. The PEX 8649 can be used to implement failover and redundant systems, as described in the sections that follow.

4.6.1 Failover in Base Mode

In Base mode, the PEX 8649 supports one upstream Port and one NT Port. Figure 4-7 illustrates the PEX 8649 in Base mode, with the NT Port located behind the PCI-to-PCI bridge. Figure 4-8 illustrates the PEX 8649 in Base mode, with the NT Port located on the virtual Bus.

Figure 4-7. Base Mode, with NT Port behind PCI-to-PCI Bridge

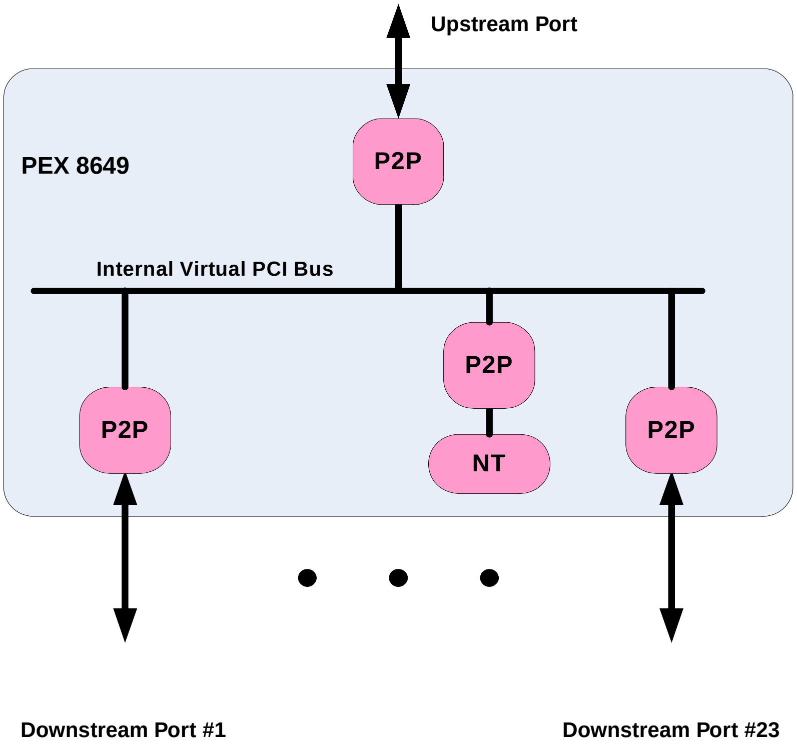
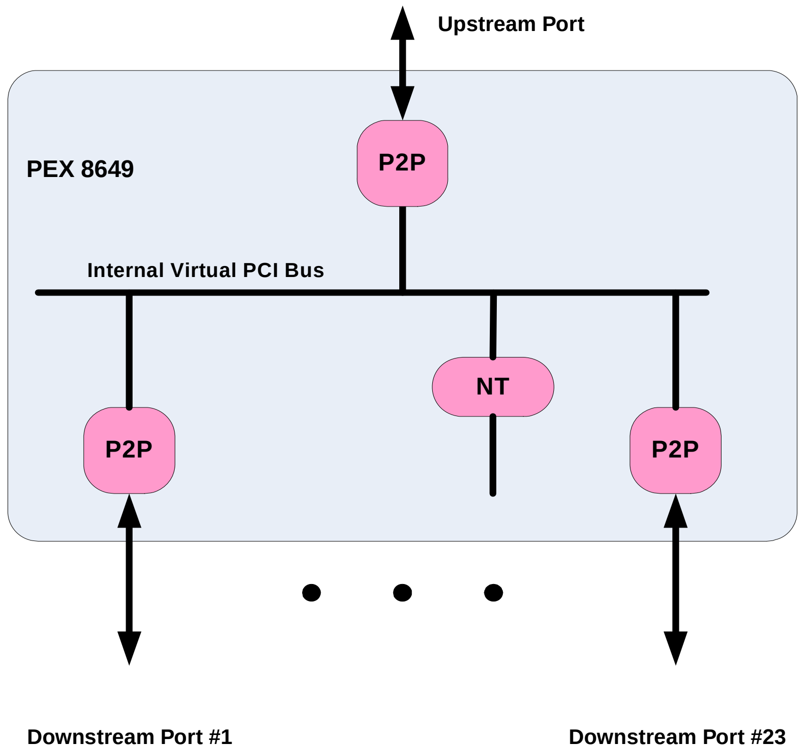


Figure 4-8. Base Mode, with NT Port on Internal Virtual PCI Bus



4.6.2 Active-Standby Redundant Systems

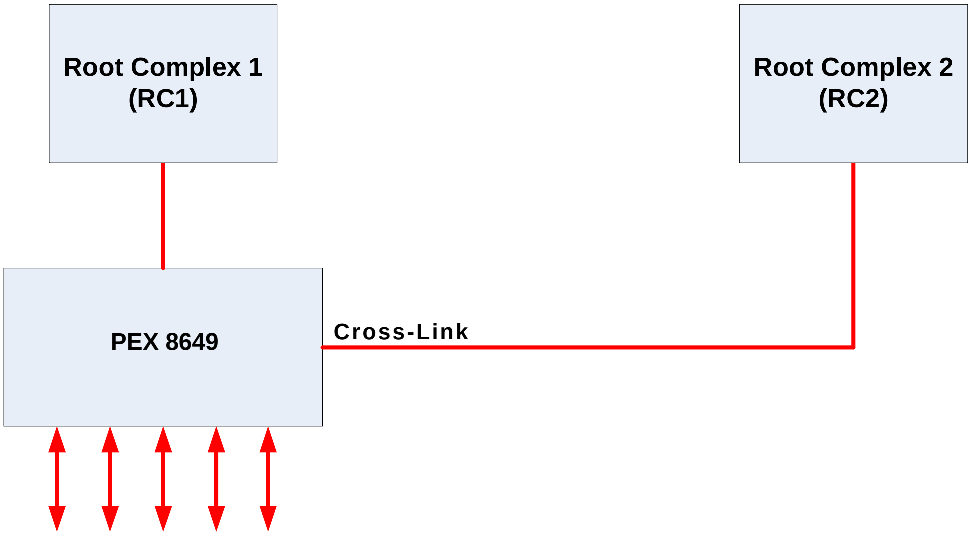
In the case of an Active-Standby Redundant system, an Active Processor owns the PCI Express hierarchy, whereas a Passive Processor is in Standby mode. This is implemented with the following options:

- Cross-Link
- Non-Transparent Port

4.6.2.1 Cross-Link

Per the *PCI Express Base r2.0*, two downstream Ports can be linked together, using a cross-link Port. Figure 4-9 illustrates a Dual-Host system in which a downstream Port of the PEX 8649 is connected to a downstream Port of Root Complex 2 (RC2). The cross-link blocks device discovery from both Root Complexes, because Configuration Space packets cannot cross the cross-link. If Root Complex 1 (RC1) fails, RC2 re-configures the Port on the far side of the cross-link as an upstream Port, using out-of-band mechanisms. RC2 can then Hot Reset the hierarchy that formerly belonged to RC1, and commence acting as the Host for the entire hierarchy.

Figure 4-9. Active Passive System with Cross-Link



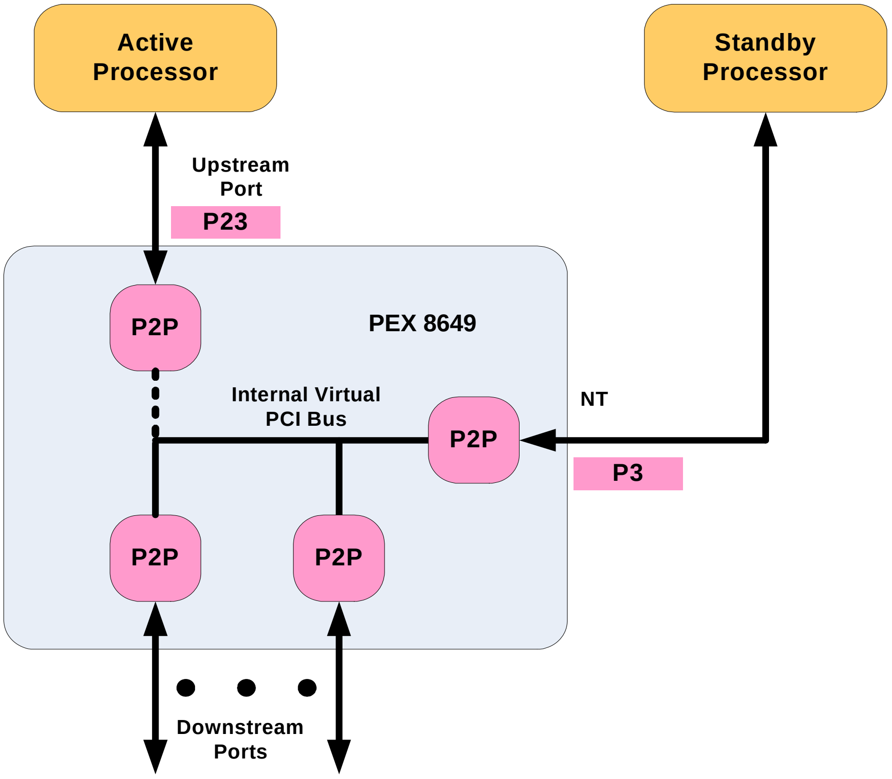
4.6.2.2 Non-Transparent Port

With this implementation, the second Processor is active and in Standby mode. The two Processors communicate with one another and rely upon heartbeat or keep alive Messages. When the Standby Processor detects failure of the Active Processor, it programs the upstream Port to be the NT Port, programs its Port to be the upstream Port, then resets the hierarchy. (Refer to Figure 4-10.)

The following actions are taken when a Processor in Standby mode detects the failure of an Active Processor:

1. Configure P23 to be a downstream Port.
2. Configure P3 from downstream/NT Port to upstream Port.
3. Configure P23 to be the NT Port.
4. Reset the hierarchy, through the upstream Port's **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]).
5. Re-enumerate the hierarchy and start operation.

Figure 4-10. Sample NT Port (Active-Standby Model)



4.6.3 Active-Active Redundant Systems

In these implementations, either a single-chip or dual-chip solution is used:

- A single-chip solution using an NT Port has a single point of failure. It is acceptable if both the processors are on the same board and redundant boards are present in the same system.
- A dual-chip solution provides true system-level redundancy, with two CPUs and two PCI Express switches.

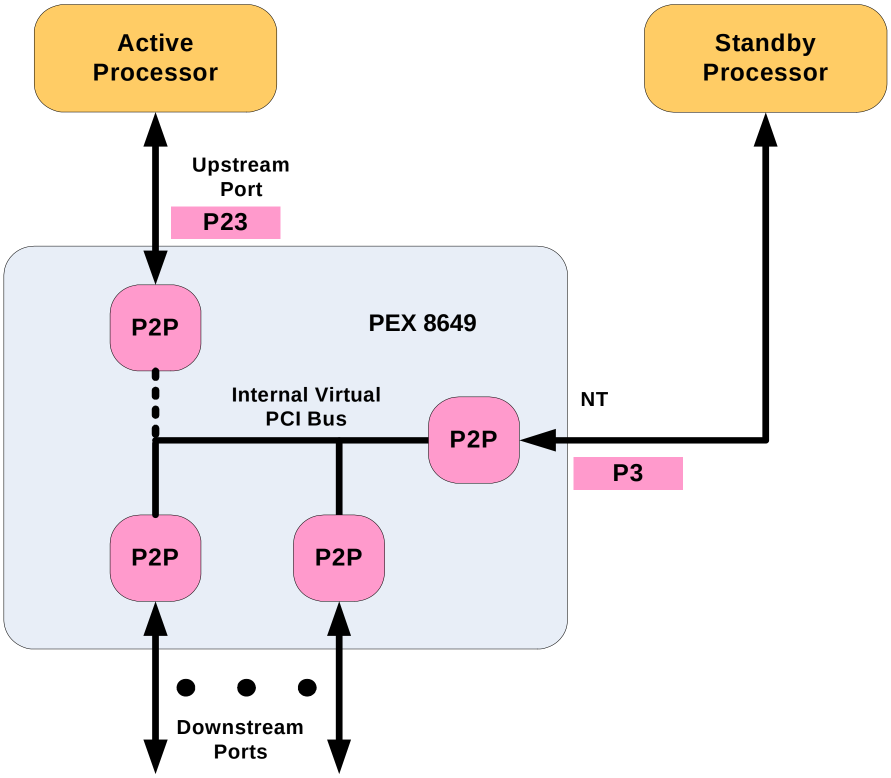
4.6.3.1 Non-Transparent Port (Active-Standby Model)

With this implementation, the second Processor is active and in Standby mode. The two Processors communicate with one another and rely upon heartbeat or keep alive Messages. When the Standby Processor detects failure of the Active Processor, it programs the upstream Port to be the NT Port, programs its Port to be the upstream Port, then resets the hierarchy. (Refer to Figure 4-11.)

The following actions are taken when a Processor in Standby mode detects the failure of an Active Processor:

1. Configure P23 to be a downstream Port.
2. Configure P3 from downstream/NT Port to upstream Port.
3. Configure P23 to be the NT Port.
4. Reset the hierarchy, through the upstream Port's **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]).
5. Re-enumerate the hierarchy and start operation.

Figure 4-11. Sample NT Port (Active-Standby Model)



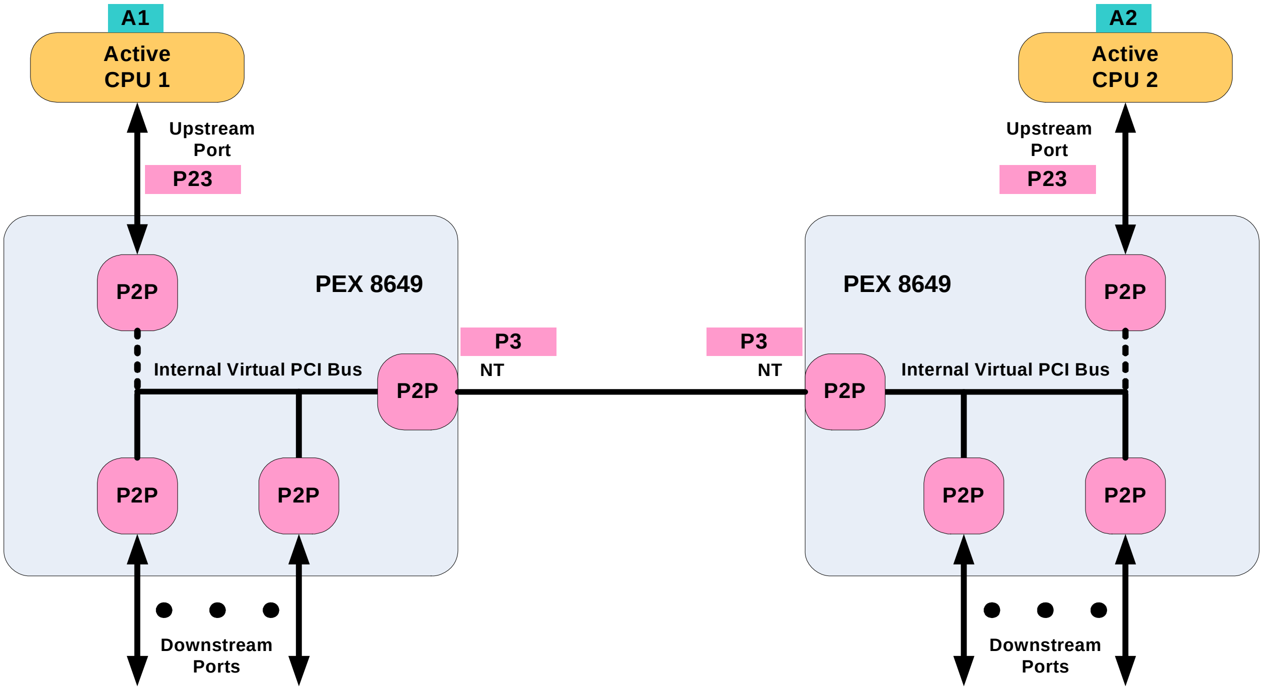
4.6.3.2 Back-to-Back NT (Active-Active Model)

In this implementation, both Processors are active and managing their respective downstream Ports. To check one another's health, the Processors communicate through their NT Ports. This provides true system-level redundancy, with two CPUs and two PCI Express switches. (Refer to Figure 4-12.)

The following actions are taken when one Active Processor detects the failure of another Active Processor (*for example*, A1 fails and A2 detects the failure):

1. A2 configures its P3 to be a downstream (Transparent) Port.
2. A2 configures A1's P3 to be an upstream Port.
3. A2 configures A1's P23 to be downstream and the NT Port.
4. A2 programs its P3 **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]) and generates a Hot Reset to the failed PCI Express switch.
5. A2 re-enumerates the hierarchy and starts operation.

Figure 4-12. Sample Back-to-Back NT (Active-Active Model)



4.6.4 Failover in Virtual Switch Mode

In Virtual Switch mode, the PEX 8649 provides multiple virtual switches in a single device. This mode can be used in various applications, such as to create an *N*-way modular system using a single CPU while supporting many I/O devices. Additional Processors can be attached, and I/O Ports can be re-assigned or added, while traffic is still going on through other I/O devices attached to the primary Processor. Users can independently scale up/down processing power and I/O bandwidth, while the system is in operation.

As illustrated in Figure 4-13, there is initially one Processor (Root Complex 1, RC1) and four I/O devices (IO1, IO2, IO3, and IO4) in the system. This configuration is used to run high I/O-centric-load applications. When more processing power is required, a second Processor (Root Complex 2, RC2) can be added, and I/O devices IO3 and IO4 are re-assigned, to RC2. RC1 traffic to IO1 and IO2 is not affected.

Other usage model is to implement an *N*-1 redundant system. In this configuration, when one of the Root Complexes fails, the failed Processor's I/O devices are assigned to another running Processor, without affecting the traffic on the running Processor.

In Virtual Switch mode, re-configuration can be initiated by software to support failover of one or more Root Ports. The non-affected Ports' (failed or the Port that is taking over) traffic should not be affected during re-configuration/re-assignment of Root hierarchies, as illustrated in Figure 4-14.

Figure 4-13. Failover in PEX 8649 – Virtual Switch Mode

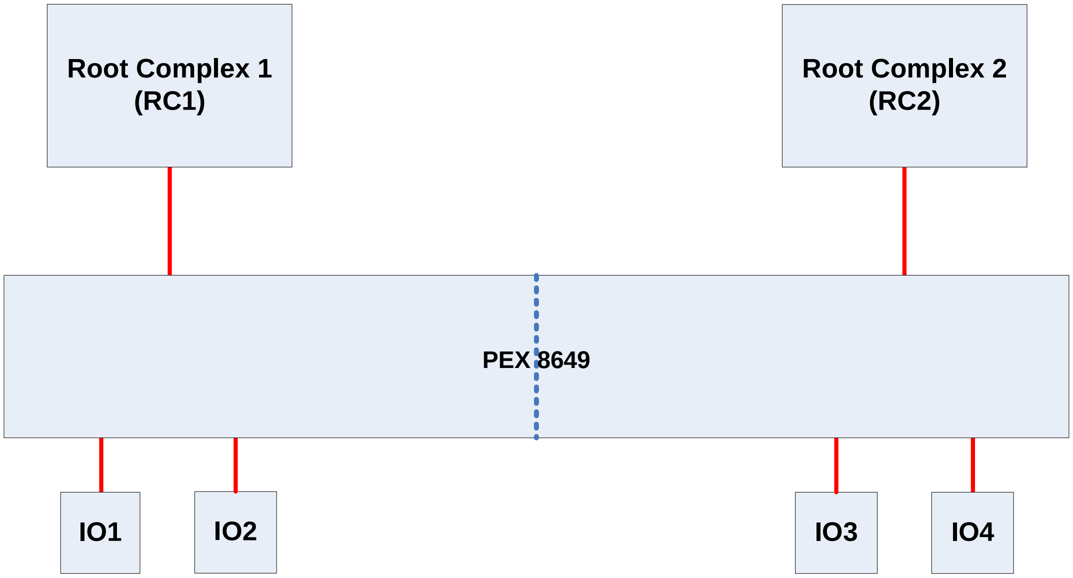
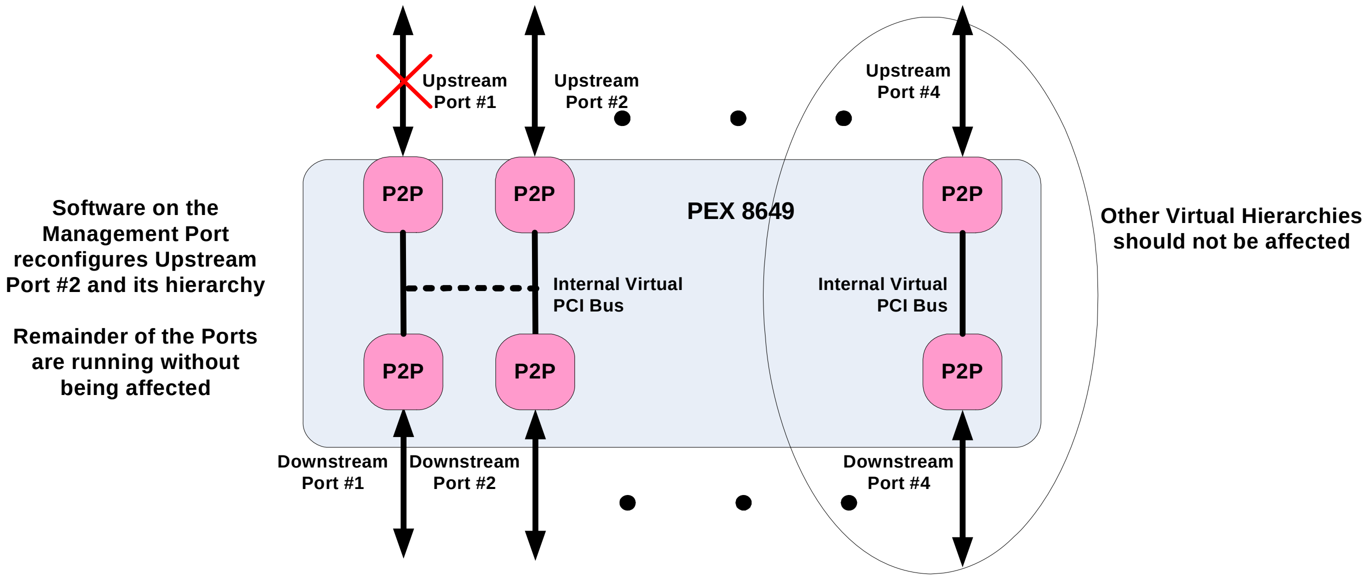


Figure 4-14. Failover in Multi-Root Switch – Virtual Switch Mode


Upstream Port #1
Upstream Port #2
Upstream Port #4
P2P
P2P
PEX 8649
P2P
Software on the Management Port reconfigures Upstream Port #2 and its hierarchy
Remainder of the Ports are running without being affected
Other Virtual Hierarchies should not be affected
Internal Virtual PCI Bus
Internal Virtual PCI Bus
P2P
P2P
P2P
Downstream Port #1
Downstream Port #2
Downstream Port #4

4.7 PCI-Compatible Software Model

The PEX 8649 can be thought of as a hierarchy of PCI-to-PCI bridges, with one upstream PCI-to-PCI bridge and one or more downstream PCI-to-PCI bridges connected by an internal Virtual PCI Bus. (Refer to Figure 4-15.) PCI-to-PCI bridges are compliant with the PCI and PCI Express system models. Figure 4-15 illustrates the concept of hierarchical PCI-to-PCI bridges, with the bus in the middle being the internal virtual PCI Bus. The Configuration Space registers (CSRs) in the upstream PCI-to-PCI bridge are accessible by Type 0 Configuration Requests that target the upstream bus interface. The upstream Port(s) capture(s) the Type 0 Configuration Write Target Bus Number and Device Number. The upstream Port(s) use(s) this Captured Bus Number and Captured Device Number, as part of the Requester ID and Completer ID for the Requests and Completions generated by the upstream Port(s).

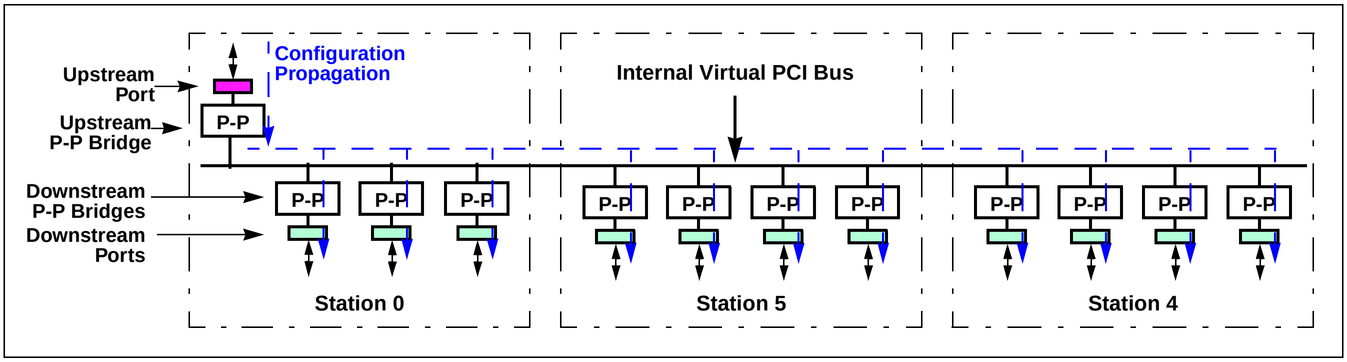
The CSRs in the downstream Port PCI-to-PCI bridges are accessible by Type 1 Configuration Requests received at the upstream Port(s) that target the internal virtual PCI Bus, by having a Bus Number value that matches the upstream bridge's Secondary Bus Number value. Each downstream bridge is associated with a unique Device Number, as explained in Section 4.1.1.4.

The CSRs of downstream devices are hit in two ways. If the Configuration Request matches the PEX 8649 downstream Port Secondary Bus Number, the PEX 8649 converts the Type 1 Configuration Request into a Type 0 Configuration Request. However, if the Bus Number does ***not*** match the Secondary Bus Number, but falls within the Subordinate Bus Number range, the Type 1 Configuration Request is forwarded out of the PEX 8649, unchanged. A Type 1 Configuration Request that targets a Bus Number that is not within range is invalid, and is terminated by the PEX 8649 upstream Port(s) as an Unsupported Request (UR).

After all PCI devices have been located and assigned Bus and Device Numbers, software can assign a Memory map and I/O map. Requests (Memory or I/O) go downstream if they fall within a bridge's Base and Limit range. In the PEX 8649, each downstream bridge has its own Base and Limit. Alternatively, Requests (Memory or I/O) go upstream if they do not target anything within the upstream bridge's Base and Limit range.

Completions are routed by the Bus Number established in the Configuration registers. If the Bus Number is in the Secondary or Subordinate range, the packet goes downstream; otherwise, the packet goes upstream.

Figure 4-15. System Configuration Propagation



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Chapter 5 Reset and Initialization

5.1 Resets – Base Mode

Reset is a mechanism that returns a device to its initial state. Reset is propagated upstream-to-downstream. Hardware and/or software mechanisms can trigger three different levels of reset – Fundamental, Hot, or Secondary Bus (each is described in the sections that follow). The re-initialized states following a reset vary, depending upon the reset type.

Table 5-1 summarizes each type of reset in Base mode.

For details on reset in NT Mode, refer to Section 14.1.4, “NT Port Reset.”

Table 5-1. Reset Summary – Base Mode

PCI Express Definition	Reset Source	Impact to Different Internal Components (upon De-Assertion)	Impact to Internal Registers
Fundamental Reset • Cold Reset • Warm Reset	PEX_PERST# input assertion	• Initializes everything • Serial EEPROM contents are loaded • HwInit types are evaluated	All registers are initialized
Hot Reset	• TS Ordered-Set *Hot Reset* bit is Set, at the upstream Port • Upstream Port enters the *DL_Down* state	• Initializes all Station Ports • Initializes internal credits and queues • Selectively reloads serial EEPROM contents	All registers, except: • Port Configuration registers • All Sticky bits not affected by Hot Reset (HwInit, ROS, RW1CS, RWS)
Secondary Bus Reset	Downstream Port’s **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]) is Set	• Downstream Port Physical Layer (PHY) generates a Hot Reset • Downstream Port Data Link Layer (DLL) is down • Downstream Port Transaction Layer (TL) is initialized, exhibits DL_Down behavior, and TLP Requests to that Port are dropped • Upstream Port and downstream Ports drain traffic, corresponding to the DL_Down condition on the downstream Port, and initialize credits corresponding to that downstream Port	Does not affect registers (other than to initialize credits)
	Upstream Port’s **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]) is Set	• All downstream Ports propagate a Hot Reset • DLL of each downstream Port is down • TL of each downstream Port is initialized, exhibits DL_Down behavior, and drops TLP Requests that target downstream Ports • Upstream Port TL exhibits DL_Up behavior	Initializes downstream Ports registers to default values

5.1.1 Fundamental Reset – Base Mode

Fundamental Reset is a hardware mechanism defined by the *PCI Express Base r2.0*, Section 6.6. Fundamental Reset input, through the PEX_PERST# signal, resets all Port states and Configuration registers to default conditions.

Additionally, software can cause a Fundamental Reset to any selected Transparent downstream Ports and NT PCI-to-PCI bridge, by Setting the Port's **Port Reset** register *Reset Port x Vector* bit(s) (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 3A0h[23:16, 3:0]). Reset remains asserted until the Port's bit is Cleared. Following this software-generated Fundamental Reset, the serial EEPROM reloads registers only if the **Debug Control** register *Port Reset EEP Load* bit (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 350h[22]) is Set. Upstream Port(s), and the NT Port Virtual and Link Interfaces, are ***not*** resettable by this software mechanism.

5.1.2 Hot Reset – Base Mode

Hot Reset is an in-band Reset that propagates from an upstream PCI Express Link to all its Transparent downstream Ports, through the Physical Layer (PHY) mechanism. The PHY mechanism communicates a reset to downstream devices through a training sequence (TS1/TS2 Ordered-Set, in which the *Hot Reset* Training Control Bit is Set). Hot Reset is also referred to as a *Soft Reset*.

A Hot Reset initializes all Ports, resets registers that are not defined as Sticky, and resets the serial EEPROM logic to reload registers (except Port Configuration registers) from serial EEPROM, if present. Hot Reset does not reset the Clock logic, and can be caused by any of the following:

- Upstream Port PHY receives two consecutive TS1 Ordered-Sets in which the *Hot Reset* Training Control bit is Set. Hot Reset is generated from an upstream device, *such as* by Setting its **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]).
- Upstream Port unexpectedly enters the *DL_Down* state.

  Exception – If the upstream Port Link is in the L2 Link Power Management (PM) state and the Link goes down, the downstream Ports do ***not*** generate Hot Reset.
- Upstream Port PHY enters either the *Loopback* or *Disabled* state, upon receiving two consecutive TS1 or TS2 Ordered-Sets in which either the *Loopback* or *Disable Link* Training Control bit is Set, respectively. An upstream device can generate the *Disable Link* sequence, by Setting its **Link Control** register *Link Disable* bit (offset 78h[4]).

5.1.3 Secondary Bus Reset – Base Mode

Any virtual upstream or downstream PCI-to-PCI bridge within the PEX 8649 can reset its downstream hierarchy, by Setting the **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]).

When the *Secondary Bus Reset* bit is Set on the upstream Port, all the downstream Ports are initialized to their default states, as defined by the *PCI Express Base r2.0*. Each of the Transparent downstream Ports generates an in-band Hot Reset onto its downstream Links (the NT Port Link Interface does not generate Hot Reset). In addition, writable registers defined by the *PCI Express Base r2.0*, in all downstream Ports, are initialized to default values (upstream Port registers are not reset, and the serial EEPROM does not reload registers).

When the *Secondary Bus Reset* bit is Set on a downstream Port, that Port is reset to its default state, as defined by the *PCI Express Base r2.0*, and generates an in-band Hot Reset onto its downstream Link. The registers of that downstream Port are not affected.

5.1.4 Register Bits that Affect Hot Reset – Base Mode

Setting the **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]) generates a Hot Reset to downstream Ports and downstream devices.

5.2 Resets – Virtual Switch Mode

Reset is a mechanism that returns a device to its initial state. Reset is propagated upstream-to-downstream. Hardware and/or software mechanisms can trigger three different levels of reset – Fundamental, Hot, or Secondary Bus (each is described in the sections that follow). The re-initialized states following a reset vary, depending upon the reset type.

The *PCI Express Base r2.0* discusses a Conventional Reset (Cold, Warm, and Hot). For Virtual Switch mode, the above cases are slightly extended (from how they function in Base mode), as discussed in the sections that follow.

5.2.1 Conventional Reset – Virtual Switch Mode

5.2.1.1 PEX_PERST# (Cold and Warm Reset)

The PEX_PERST# input is used as the Fundamental Reset for the entire PEX 8649. This reset affects the virtual switches, and impacts all on-chip components – the Stations and their Ports, the Serial EEPROM Controller, Clock logic, and so forth. All registers and states are initialized.

Use of the PEX_PERST# input is the only way to Clear Fatal errors detected in the PEX 8649.

After PEX_PERST# de-assertion, the PEX 8649 can be initialized by way of serial EEPROM, I^{2}C, and/or the Management Port.

5.2.1.2 VS*x*_PERST# (Hot Reset)

There is a virtual Fundamental Reset, per virtual switch. This input attempts to mimic the PEX_PERST# input, but on a virtual switch basis, and is controlled by the Port's **Port Reset** register *Reset Port x Vector* bit (Port 0, accessible through the Management Port, offset 3A0h[23:16, 3:0].

It resets all PCI-to-PCI bridges in the virtual switch hierarchy, from the upstream PCI-to-PCI bridge, down to the downstream PCI-to-PCI bridges and downstream Ports owned by the virtual switch that caused VS*x*_PERST# to assert.

Because some of the PEX 8649 data structures might be shared across virtual switches, VS*x*_PERST# cannot reset the entire switch to a clean state. If there are any Fatal errors in any virtual switch, a PEX 8649 PEX_PERST# is required.

VS*x*_PERST# behaves the same as an inband Hot Reset on the upstream Port. Sticky registers preserve their values, and all else is returned to an initial state. The serial EEPROM reloads registers only for the corresponding virtual switch, unless the virtual switch's **Virtual Switch Debug** register *Disable Serial EEPROM Load on Hot Reset* bit (VS Upstream Port(s), offset A30h[3]) is Set.

5.2.2 Inband Reset (TS1 Ordered-Set) or Upstream Port DL_DOWN (Hot Reset) – Virtual Switch Mode

The *PCI Express Base r2.0* defines an inband reset (with a TS1 Ordered-Set) or an upstream Port going down as a Hot Reset. These work exactly as indicated by the *PCI Express Base r2.0*. The reset is, by default, propagated downstream to all Ports in the virtual switch whose upstream Port receives the Hot Reset.

5.2.3 Secondary Bus Reset (Soft Reset) – Virtual Switch Mode

Every PCI-to-PCI bridge has a *Secondary Bus Reset* bit that resets the entire downstream hierarchy. The upstream PCI-to-PCI bridge’s Secondary Bus Reset resets all downstream PCI-to-PCI bridges owned by the virtual switch. A downstream PCI-to-PCI bridge’s Secondary Bus Reset sends a Hot Reset Training Set across the Link.

5.2.4 Reset Propagation Prevention – Virtual Switch Mode

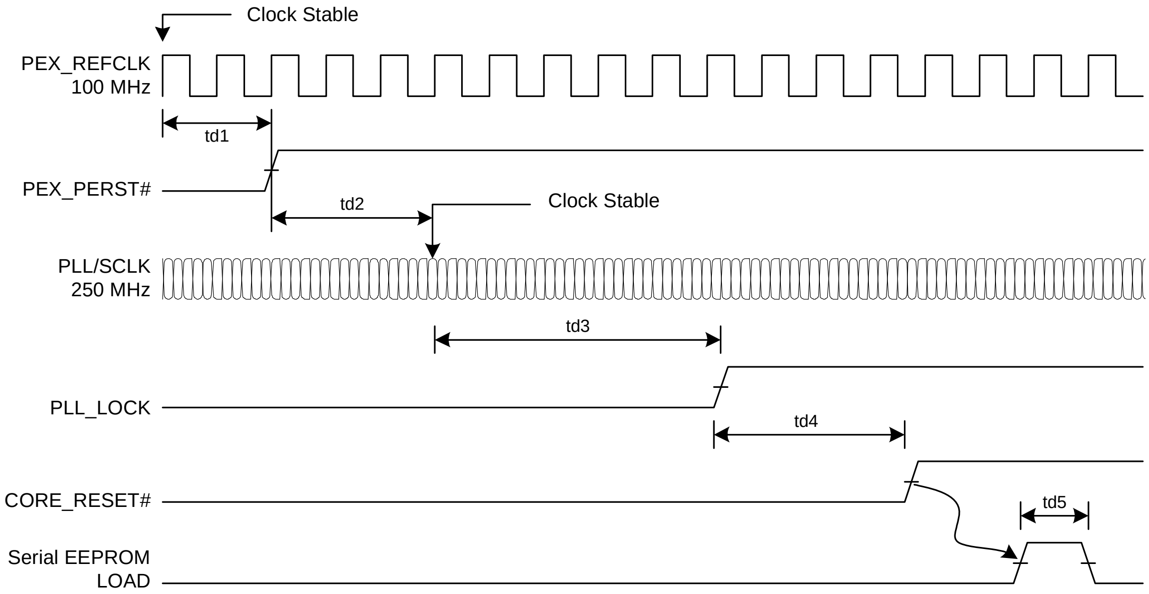
It is possible to prevent the propagation and effect of the various conventional resets (besides the Cold Reset). By Setting the virtual switch’s **Virtual Switch Debug** register *Upstream Port and NT-Link Port DL_Down Reset Propagation Disable* bit (VS Upstream Port(s), offset A30h[4]), Hot Resets are no longer propagated. By default, the bit is Cleared, and resets are propagated.

5.3 Reset and Clock Initialization Timing

Table 5-2. Reset and Clock Initialization Timing

Symbol	Description	Typical Delay
td1	REFCLK stable to PEX_Reset release time	100 µs
td2	PEX_Reset release to Reset de-bounce	1.32 ms
td3	Reset de-bounce to Phase-Locked Loop (PLL) Lock	105 µs
td4	Reset de-bounce to Core Reset release	2.63 ms
td5	Serial EEPROM load time with no serial EEPROM present	17 µs

Figure 5-1. Reset and Clock Initialization Timing



5.4 Initialization – Base Mode

The PEX 8649 initialization process starts upon exit from a Fundamental Reset. The serial EEPROM and/or I^{2}C can be used to program initial register values, prior to BIOS/OS enumeration. If the STRAP_I2C_CFG_EN# input is Low, linkup of all Ports is delayed, until I^{2}C software Sets the **Configuration Release** register *Initiate Configuration* bit (Port 0, offset 3ACh[0]).

Serial EEPROM download operates much faster than I^{2}C access (I^{2}C is relatively slow). Consequently, I^{2}C initialization might not complete prior to the first BIOS/OS Configuration access, unless the system is designed to delay BIOS/OS Configuration access until the PCI Express subsystem is ready.

5.4.1 Serial EEPROM Load Time

Serial EEPROM initialization loads only the Configuration register data that is specifically programmed into the serial EEPROM. Registers that are not included in the serial EEPROM data are initialized to default register values.

Each register entry in the serial EEPROM consists of two Address bytes and four Data bytes (refer to Section 6.4, “Serial EEPROM Data Format”); therefore, each register entry (6 bytes, or 48 bits) requires 48 serial EEPROM clocks to download. Thus, at the serial EEPROM clock default frequency of 1 MHz, after initial overhead to read the **Serial EEPROM Status** register (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 260h) (16 serial EEPROM clocks, or 16 µs), plus another 40 serial EEPROM clocks (40 µs) to begin reading the register data, each register entry in the serial EEPROM requires 48 µs to download. A serial EEPROM containing 50 register entries (typical configuration, assuming the serial EEPROM is programmed only with non-default register values) and clocked at 1 MHz takes approximately 5.2 ms to load (16 + 40 + 48) * 50 µs (5,200 µs).

To reduce the serial EEPROM initialization time, the first register entry in the serial EEPROM can increase the clock frequency by programming the **Serial EEPROM Clock Frequency** register (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 268h), to a value of 2h (5 MHz), or 3h (9.62 MHz), if the serial EEPROM supports the higher frequency at the serial EEPROM supply voltage (typically 2.5 to 3.3V). At 5 MHz clocking, the serial EEPROM load time for 50 register entries can be reduced to approximately 575 µs. Because the *PCI Express Base r2.0* allows a 20-ms budget for system hardware initialization, the default 1-MHz serial EEPROM clock is often sufficient when the quantity of Ports and registers programmed by serial EEPROM is relatively small.

If NT Port Expansion ROM (stored within the serial EEPROM) is used, the serial EEPROM clock frequency (EE_SK) must be at least 5 MHz.

5.4.2 I^{2}C Load Time

Initialization using I^{2}C is slower than serial EEPROM initialization, because the I^{2}C Slave interface operates at a lower clock frequency (100 KHz maximum) and the quantity of bits per Register access is increased (because the Device address is included in the bit stream). Writing one register using 100-KHz clocking takes approximately 830 µs (83 clock periods).

5.5 Initialization – Virtual Switch Mode

In addition to the Strapping balls, there are several ways to initialize the PEX 8649 when it is in Virtual Switch mode, by way of serial EEPROM, I^2C, and/or the Management Port. One of these three agents must initialize the Virtual Switch Table. The serial EEPROM and/or I^2C/SMBus can effectively program all registers, whereas Management Port software generally cannot modify Read-Only (RO) registers. The serial EEPROM (programmable by I^2C/SMBus and/or software) requires the least software support.

The PEX 8649 sequences these methods, in the following order:

1. Serial EEPROM
2. I^2C/SMBus
3. Management Port

Note: *It is possible to use more than one method to initialize the PEX 8649.*

*If using serial EEPROM and/or I^2C, they will program the necessary Virtual Switch registers. If using a Virtual Switch Management Port, enabled by a Strapping ball, the Management Port Sets the required Virtual Switch registers. The Virtual Switch Manager releases the remainder of the PEX 8649, by Setting the **Configuration Release** register Initiate Configuration bit (Port 0, accessible through the Management Port, offset 3ACh[0]).*

Strapping balls are used to determine whether Virtual Switch mode uses I^2C, and/or the Management Port, to initialize.

If the STRAP_I2C_CFG_EN# input is Low, then I^2C is used to configure the PEX 8649. When I^2C has finished, it must write to the **Configuration Release** register *Initiate Configuration* bit (Port 0, accessible through the Management Port, offset 3ACh[0]), to release the hold that is preventing linkup.

If the STRAP_I2C_CFG_EN# input is High, then I^2C is not used to configure the PEX 8649.

If the Management Port is enabled (STRAP_NT_ENABLE#=L), the STRAP_NT_UPSTRM_PORTSEL0 Strapping ball is used to control the two Bring-Up options:

- **Option 1** – STRAP_NT_UPSTRM_PORTSEL0=L. After the serial EEPROM (if present) is loaded, the Management Port comes up first, to configure the PEX 8649. When the Management Port has completed its configuration, it must write a 1 to the **Configuration Release** register *Initiate Configuration* bit (Port 0, accessible through the Management Port, offset 3ACh[0]), to release the hold that is preventing the remaining Links from coming up.
- **Option 2** – STRAP_NT_UPSTRM_PORTSEL0=H. After the serial EEPROM is loaded (if present), all Ports come up concurrently.

For Base mode, the STRAP_VS_MODE[1:0] inputs must be Low. For Virtual Switch mode, the STRAP_VS_MODE[1:0] inputs must be strapped to a non-zero value. If the STRAP_VS_MODE[1:0] inputs are strapped Low to enable Base mode, the serial EEPROM, I^2C/SMBus, and software ***cannot*** override the straps to enable Virtual Switch mode. Similarly, if the STRAP_VS_MODE[1:0] inputs are strapped to a non-zero value to enable Virtual Switch mode, the serial EEPROM, I^2C/SMBus, and software ***cannot*** override the straps to enable Base mode. However, in Virtual Switch mode, the serial EEPROM, I^2C/SMBus, and/or software can change the Virtual Switch Table, including the quantity of enabled virtual switches. (Refer to Section 5.5.3)

If a design must support both Base mode and Virtual Switch mode, without changing the STRAP_VS_MODE[1:0] input values, strap the STRAP_VS_MODE[1:0] inputs to a non-zero value. Then, if Base mode is needed, the serial EEPROM, I^2C/SMBus, and/or software can assign all Ports to VS0 (with no Ports assigned to other virtual switches).

Once initialized, only the Management Port has the privilege to modify the Virtual Switch Control registers.

The Active Management Port is defined by the **Management Port Control** register (Port 0, accessible through the Management Port and Redundant Management Port, offset 354h). This register also defines an optional Redundant Management Port, that can be used to back up the Active Management Port.

The RWS setting in the **Management Port Control** register indicates that the bits are Readable, Writable, and Sticky.

Note: *Sticky means that, as long as power is not removed, the bits are not changed with Hot Reset. Note however, that if a Hot Reset causes a serial EEPROM or I*^{2}*C load, these bits can be overwritten from their pre-reset value.*

The Active Management Port can read or write all the Virtual Switch Control registers. No other Ports are allowed to do so.

The quantity of enabled virtual switches is defined by the **Virtual Switch Enable** register (Port 0, accessible through the Management Port and Redundant Management Port, offset 358h). This register is initially configured by the STRAP_VS_MODE[1:0] Strapping balls.

The upstream Port for each virtual switch can also be Set by the Management Port, using the **VS*x* Upstream** register (Port 0, accessible through the Management Port, offset 360h through 36Ch).

The Management Port configures which downstream Port is owned by which upstream Port, by writing a **VS*x* Port Vector** register (Port 0, accessible through the Management Port, offset 380h through 38Ch), per virtual switch. Each downstream Port can be owned by a single upstream Port only. If software sets two or more owners for a downstream Port, behavior is not deterministic.

After ownership of all PEX 8649 Ports is defined, the **Configuration Release** register *Initiate Configuration* bit (Port 0, accessible through the Management Port, offset 3ACh[0]) is Set, allowing the Links to come up.

There can be a Redundant Management Port as well. The Redundant Management Port can promote itself to be the new Management Port, if the Management Port Host fails. The implementation of Redundant Management Port promotion to Management Port is application-specific.

After the *Initiate Configuration* bit is Set, each virtual switch Host enumerates its hierarchy, as if it had its own independent switch. Each hierarchy is independent, and there is no order in which the hierarchies must be initialized. Each Host finds only the PCI-to-PCI bridges that it owns. Each Host has its own bus numbering scheme, which applies to the upstream Port, through to the virtual internal PCI Bus and down to any downstream buses. The same is true for memory addressing – each virtual switch has a completely independent Address map, both in 32- and 64-bit Address space.

5.5.1 Management Port Policies

All Device-Specific registers can be accessed from the Active Management Port, serial EEPROM, and/or I^{2}C.

The Redundant Management Port can access only the **Management Port Control** register (Port 0, accessible through the Management Port and Redundant Management Port, offset 354h). All upstream Ports can access PCI-SIG-defined registers, within their own hierarchy.

5.5.2 Active and Redundant Management Ports

Note: *There is no Management Port when STRAP_NT_ENABLE# is de-asserted, unless serial EEPROM and/or I^{2}C initialization enables it.*

The **Management Port Control** register *Active Management Port* field (Port 0, accessible through the Management Port and Redundant Management Port, offset 354h[4, 2:0]) defines which Virtual Switch upstream Port is assigned as the Active Management Port. In Virtual Switch mode, there is no Management Port when the register's *Active Management Port Enable* bit [5] (which defaults to the inverse value of the STRAP_NT_ENABLE# Strapping ball) is Cleared.

The register's *Redundant Management Port* field [12, 10:8] defines which Virtual Switch upstream Port is assigned as the Redundant Management Port. The Redundant Management Port provides a Failover capability, should the Management Port Host fail. Software can demote the Management Port and promote the Redundant Management Port to be the new Management Port, by programming the **Management Port Control** register. (Refer to Section 5.5.6.5.)

This register can be accessed by the Management-capable (Active and Redundant) Ports, Strapping balls, and/or the I^{2}C Bus. The ***reserved*** register bits return zeros (0) during Reads. Writes to ***reserved*** register bits do not affect the register.

The register's RWS fields/bits are represented in Table 5-3. (For complete details, refer to the register offset 354h description provided in Section 13.15.8, "Device-Specific Registers – Port Configuration (Offsets 354h – 3ACh).")

Table 5-3. Management Port Control Register (Port 0, accessible through the Management Port and Redundant Management Port, Offset 354h)

Bit(s)[a]	Description
4, 2:0	**Active Management Port** Indicates the Port Number of the Active Management Port. The value of this field is latched in, upon reset de-assertion, from the STRAP_UPSTRM_PORTSEL[3:0] inputs, respectively. The upper two bits [4, 2] of this field map to STRAP_UPSTRM_PORTSEL[3:2], to select the Station, and the lower two bits [1:0] map to STRAP_UPSTRM_PORTSEL[1:0], to select the Port within that Station.
5	**Active Management Port Enable** Enables the Active Management Port. The value of this bit is latched in, upon reset de-assertion, from the STRAP_NT_ENABLE# input. 0 = STRAP_NT_ENABLE#=H 1 = STRAP_NT_ENABLE#=L
6	**Active Management Port EEPROM Load on Hot Reset for Chip and Station Registers Enable** ***Valid only for the Management Port.*** After the Management Port receives a Hot Reset or DL_Down condition, the serial EEPROM reloads registers, as described below. 0 = Serial EEPROM reloads Management Port Port-specific registers (default) 1 = Serial EEPROM reloads: • Chip-specific registers (might affect all virtual switches), • Station-specific registers for the Station that contains the Management Port (might affect other virtual switches in that Station), and, • Management Port Port-specific registers
12, 10:8	**Redundant Management Port** Indicates the Port Number of the Redundant Management Port.
13	**Redundant Management Port Enable** Enables the Redundant Management Port.

[a] *Bits not identified in Table 5-3 are **Reserved** or **Factory Test Only**.*

5.5.3 Virtual Switch Table

The PEX 8649 supports up to four virtual switches. The Virtual Switch Table defines the Port Numbers, and associated Virtual Switch Numbers and upstream Port of each virtual switch. Each table entry must be updated as a single atomic operation.

Additional information related to the table is discussed in the sections that follow.

Note: *In Virtual Switch mode, the Virtual Switch Table registers include the **VSx Port Vector** and **VSx Upstream** registers (Port 0, accessible through the Management Port, offsets 380h through 38Ch, and 360h through 36Ch). These two sets of registers define which Ports are associated to each virtual switch, and which Port is the upstream Port for each Virtual Switch, respectively. These registers must be initialized by one (or more) of the following agents:*

- *Serial EEPROM*
- *I^{2}C/SMBus, provided that the STRAP_I2C_CFG_EN# input is Low (to delay linkup until I^{2}C/SMBus Sets the **Configuration Release** register Initiate Configuration bit (Port 0, accessible through the Management Port, offset 3ACh[0]). This option might require software support, to delay Host enumeration until I^{2}C/SMBus Sets the Initiate Configuration bit after programming the PEX 8649 Configuration registers.*
- *Management Port software, provided that STRAP_NT_ENABLE# and STRAP_NT_UPSTRM_PORTSEL0 are both Low (to enable the Management Port, and delay linkup of all other Ports until software (and/or I^{2}C/SMBus) Sets the Initiate Configuration bit, respectively).*

Use of serial EEPROM for the initialization might be the best choice for most applications, because it is the simplest solution. Therefore, for Virtual Switch mode applications, the serial EEPROM is required to initialize the Virtual Switch Table registers, unless I^{2}C/SMBus and/or Management Port software can perform this task.

5.5.3.1 Virtual Switch Table Registers

The Virtual Switch Table consists of three registers, listed in Table 5-4. The first two can be accessed in any order, and the third (**Virtual Switch Enable**) must be accessed last.

Table 5-4. Virtual Switch Table Registers[a]

Offset	Register	Description
358h[3:0]	**Virtual Switch Enable**	The register's *VSx Enable* bits are used to enable or disable virtual switches within the system. There is one bit, per virtual switch (VS0 through VS3). Setting a bit enables the corresponding virtual switch. Clearing a bit disables the corresponding virtual switch. If a *VSx Enable* bit is Set, another virtual switch is being established with the new set of upstream and downstream Ports. One Write to this register can disable the previous virtual switch, and enable a new virtual switch. This ensures that Virtual Switch Enable and Disable can be implemented with a single Write to a register. The STRAP_VS_MODE[1:0] inputs map to this register.
360h – 36Ch	**VS*x* Upstream**	These registers define the upstream Port of each virtual switch. There is one register, per virtual switch (VS0 through VS3). The registers' *VSx Upstream Port* bits [4, 2:0] define which Port is the singular upstream Port, within the corresponding virtual switch. A virtual switch must include a single, unique upstream Port. The STRAP_NT_UPSTRM_PORTSEL[4, 2:0] inputs map to this register.
380h – 38Ch	**VS*x* Port Vector**	These registers define the upstream and downstream Ports associated with each virtual switch. There is one register, per virtual switch (VS0 through VS3), and each register has one bit, per Port. Bits [23:16, 3:0] correspond to Ports 23 through 16 and 3 through 0, respectively. Any Port can be assigned to a virtual switch. Setting a bit in a specific **VS*x* Port Vector** register assigns the corresponding Port to the virtual switch associated with the register. **A single Port can be assigned to only one virtual switch at any time.** Therefore, each bit (in the range listed above) must be Set in only one of the four **VS*x* Port Vector** registers, at any time. A downstream Port can be re-assigned to a different virtual switch, by Clearing the corresponding bit in one **VS*x* Port Vector** register, and Setting the same bit in another **VS*x* Port Vector** register. The STRAP_VS_MODE[1:0] inputs map to this register.

[a] *All registers listed in this table are located in Port 0, accessible through the Management Port.*

5.5.3.2 Virtual Switch Table Programming Sequence

The following describes the programming sequence for the Virtual Switch Table, by the Management Port Host.

1. Strap the STRAP_VS_MODE[1:0] balls to enable Virtual Switch mode and the quantity of virtual switches needed.

Note: *The STRAP_VS_MODE[1:0] Strapping balls are used to enable up to four virtual switches. The quantity of enabled virtual switches is reflected in the **Virtual Switch Enable** register VSx Enable bits (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 358h[3:0]). (Refer to the STRAP_VS_MODE[1:0] description, in Table 3-7, "Strapping Signals," for details.)*

2. Strap both the STRAP_NT_ENABLE# and STRAP_NT_UPSTRM_PORTSEL0 inputs Low. This allows only the Management Port to linkup, and requires a Write of 1 to the **Configuration Release** register *Initiate Configuration* bit (Port 0, accessible through the Management Port, offset 3ACh[0]), to allow the remaining Ports to linkup.
3. Strap the STRAP_UPSTRM_PORTSEL[3:0] inputs to the Active Management Port Number. The **VS0 Upstream** register *VS0 Upstream Port* field (Port 0, accessible through the Management Port, offset 360h[4, 2:0]) defaults to the Active Management Port Number, as defined by the STRAP_UPSTRM_PORTSEL[3:0] inputs.
4. When the Active Management Port is enabled and the STRAP_VS_MODE[1:0] balls are strapped to enable one active virtual switch (VS0), all Ports are assigned to VS0.
5. Adjust all **VS*x* Port Vector** and **VS*x* Upstream** registers (Port 0, accessible through the Management Port, offsets 380h through 38Ch, and offsets 360h through 36Ch, respectively) to the new table values, ensuring that the following conditions are met:
   a. The Management Port must remain in its original virtual switch.
   b. A Port can appear in only one **VS*x* Port Vector** register. The exception is when the Management Port is being migrated to a different virtual switch. If this is the case, the Management Port can appear in two **VS*x* Port Vector** registers – the original enabled virtual switch, and the newly disabled virtual switch.
   c. The virtual switch upstream Port defined in the **VS*x* Upstream** register must be included in the corresponding **VS*x* Port Vector** register. If the Management Port is migrating to a different virtual switch, the new virtual switch's **VS*x* Upstream** register must be programmed to the Management Port Number.
6. **If the Management Port is migrating to a different virtual switch** – Enable all other needed virtual switches, using **Virtual Switch Enable** register *VSx Enable* bit(s) (Port 0, accessible through the Management Port, offset 358h[3:0], as appropriate), and disable the original virtual switch that contains the Management Port, in the same Write operation. If the original virtual switch must remain disabled, skip to step 8.

   If the Management Port is not migrating to a different virtual switch – Enable all other needed virtual switches, using the *VSx Enable* bit(s), and skip to step 9.

7. Remove the Management Port from the original Management Port virtual switch (**VS*x* Port Vector** register(s)), and update the **VS*x* Upstream** register(s) to the Management Port's new Port Number.
8. Write to the **Virtual Switch Enable** register *VSx Enable* bit(s), to enable all other virtual switches that need to be enabled.
9. Set the **Configuration Release** register *Initiate Configuration* bit, to allow all Ports to begin the linkup process.

5.5.4 Port Activity Vector

The **Egress Control and Status** register *Port Activity* bit (offset F30h[31]) is implemented for each Port, and collectively, this same bit in all Ports forms the Port Activity Vector. The *Port Activity* bit is used to indicate that for this Port, there are no pending transactions inside the virtual switch. When the bit is Set, the Port's queues are empty. This bit is polled by software, to decommission and re-assign the Port to another virtual switch.

The PEX 8649 waits 20 ms after reset to the virtual switch, then indicates that the Port's queues are empty and Sets the bit. If the Port is known to be inactive, the user can write to the Virtual Switch Table (refer to Section 5.5.3), to switch over in less than 20 ms, without looking at this bit. Reset the *Port Activity* bit after writing the Virtual Switch Table entry for this Port.

5.5.5 Link-Related Registers

Link-related registers are used when a Management Port is used to manage the PEX 8649. These registers provide information, and optionally generate an interrupt to the Management Port Host when the PEX 8649's Ports change the Links' status. In standard operation, the **Link Status** register in each Port (offset 78h) provides the Link status information to the respective Virtual Switch Host, and Transparent downstream Ports can optionally generate a Data Link Layer State Changed interrupt when downstream Port linkup is lost or regained. When a side-band Management Processor is connected to manage the PEX 8649, it also must be informed of the status of all Ports.

Table 5-5. Link-Related Registers[a]

Offset	Register	Description
900h	**Switch Link Up**	When the Port's Link state transitions from down to up, the corresponding Port's bit is Set. The corresponding Port's bit is Cleared, by using software to explicitly write 1 to the bit. The register has one bit, per Port.
904h	**Switch Link Down**	When the Port's Link state transitions from up to down, the corresponding Port's bit is Set. The corresponding Port's bit is Cleared, by using software to explicitly write 1 to the bit. The register has one bit, per Port.
908h	**Switch Link Event Mask**	If the *Mask* bit is Set, the corresponding *Up* or *Down* bit (located in register offsets 900h and 904h, respectively) transition does not generate an interrupt to the Management Port. If not masked, the bit transition generates an interrupt to the Active Management Port. The register has one *Mask* bit, per Port.
90Ch	**Switch Link Status**	This Read-Only register indicates Link status. The register has one *Status* bit, per Port.
3A0h	**Port Reset**	When driven with a value of 1, this register holds the Port in reset, including the Port PCI-to-PCI bridge and the hierarchy below it. A value of 0 indicates to un-reset the PCI-to-PCI bridge and the hierarchy below it. There is one bit, per Port. Upstream Ports are not reset by this register.

[a] *All registers listed in this table are located in Port 0, accessible through the Management Port.*

5.5.6 Reconfiguration of Virtual Switches

Virtual switches and their Ports can be re-configured for a variety of reasons, including failures or insertion or removal of cards on the downstream or upstream Ports.

5.5.6.1 Graceful De-Allocation of Downstream Port

To gracefully de-allocate a downstream Port from a virtual switch, higher-level software ensures that new Requests are not initiated by the Port and its associated I/O endpoint. Higher-level software reads and checks the Port's **Egress Control and Status** register *Port Activity* bit (offset F30h[31]), to determine whether the Port's queues are empty. All pending Requests are serviced. After the Port is in an Idle state, with no pending Requests (*Port Activity* bit is Cleared), the Port can be assigned to another virtual switch, by programming the Virtual Switch Table. (Refer to Section 5.5.3.)

The operation sequence is as follows:

1. Management Port software writes in the **Bridge Control** register (offset 3Ch) or Hot Reset to the source virtual switch. (This can also be done by VS*x*_PERST# or the corresponding bit.)
2. Management Port software re-programs the Virtual Switch Table, to add this downstream Port to the new virtual switch.
3. Hot Plug Controller on the upstream Port of the new virtual switch generates a Presence Detect Changed interrupt, if not masked. The **Power Management Hot Plug User Configuration** register *Upstream Hot Plug Enable* bit (offset F70h[14]) must be Set.
4. BIOS running on a Root Complex attached to the upstream Port of the new virtual switch enumerates the devices. Whether the enumeration is partial or full, is dependent upon the software.
5. The driver is invoked on a Root Complex, and starts communicating with the endpoint connected to this downstream Port.

Definitions:

- **BIOS** – Basic Input Output Software
- **Driver software** – Software running on the Host
- **Management Port software** – Software running on the Management Processor
- **New virtual switch** – Location to which the downstream Port is being re-allocated/assigned
- **Old virtual switch** – Location from which the downstream Port is being de-allocated

5.5.6.2 Surprise Removal of Downstream Device

When an endpoint connected to a virtual switch downstream Port is removed without any indication to software, the Link goes down and an interrupt is generated to the virtual switch's Host, as well as to the Management Port Host. If a Hot Plug Controller is implemented on the downstream Port where the Surprise Down event occurs, an Uncorrectable Error Message is sent to the upstream Host.

The operation sequence is as follows:

1. Management Port is connected to a Management Processor.
2. Link Down interrupt is sent to the Management Port software running on the Management Port, and a Data Link Layer State Changed interrupt is sent to the Virtual Switch Host.
3. Host Software Clears the **Slot Status** register *Data Link Layer State Changed* bit (Downstream Ports, offset 80h[24]) interrupt, and determines that the Link is down (**Link Status** register *Data Link Layer Link Active* bit, offset 78h[29], is Cleared).
4. Host software marks the device as unreachable.
5. Interrupt Service Routine (ISR) of Management Port software reads the Device-Specific **Switch Link Up**, **Switch Link Down**, and **Switch Link Status** registers (Port 0, accessible through the Management Port, offsets 900h, 904h, and 90Ch, respectively) (Management Port's PCI-to-PCI bridge's *MSI Enable* bit is used to generate a Message Signaled Interrupt (MSI) or INT*x* interrupt to the Management Processor).
6. ISR of the Management Port software determines that the Link is down, then Clears the interrupt.
7. ISR of the Management Port software again reads the Device-Specific **Switch Link Up**, **Switch Link Down**, and **Switch Link Status** registers, and determines that the interrupt has been Cleared and the status is Link Down.
8. ISR leaves the routine, marking the downstream Port Number as "down".
9. Management Port software reports the downstream Port as "not in use" to the software's upper layer.
10. Based upon policy, this downstream Port can be assigned to the Management Port, or remain with the virtual switch to which it belongs.

    If there is no Management Port, the virtual switches set up by the serial EEPROM and upstream Port(s) manage their own virtual hierarchies.

5.5.6.3 Graceful De-Allocation of Upstream Port

When an upstream Port must be de-commissioned for scheduled maintenance, the following actions are taken:

1. Downstream Port's traffic is stopped, by disabling all endpoints it owns.
2. Software waits until the upstream Port's **Egress Control and Status** register *Port Activity* bit (offset F30h[31]) indicates a value of 1.
3. Management Port software notifies the administrator that the virtual switch upstream Port is idle.
4. Administrator can remove the upstream Port device.
5. Hot Reset is sent (as a result of item 4) to all downstream Ports that belong to this Root Port's hierarchy.
6. Based upon policy, downstream Ports can be assigned to another Root Port's hierarchy, or remain as is for future use by the same upstream Port.

5.5.6.4 Surprise Removal of Upstream Port

An upstream Port can be removed from the Root Port's hierarchy, without notifying the Management Port software. Although this is not advisable, software and hardware ensure that the removal does not bring down shared resources, and that the system gracefully recovers from this event.

The following actions are taken after the upstream Port is detected as having been removed:

1. Link goes down for this upstream Port.
2. Management Port software is interrupted.
3. ISR reads the Device-Specific **Switch Link Up**, **Switch Link Down**, and **Switch Link Status** registers (Port 0, accessible through the Management Port, offsets 900h, 904h, and 90Ch, respectively) (Management Port's PCI-to-PCI bridge's *MSI Enable* bit is used to generate an MSI or INT*x* interrupt to the Management Processor).
4. ISR determines that the Port's **Switch Link Down** register *Port x Link Down* Interrupt bit (Port 0, accessible through the Management Port, offset 904h[23:16, 3:0]) is Set.
5. DL_Down event on the virtual switch's upstream Port generates a Hot Reset within its virtual hierarchy.
6. All downstream Ports that belong to this virtual hierarchy are reset, and propagate a Hot Reset downstream.
7. Based upon policy, Management Port software programs the Virtual Switch Table (refer to Section 5.5.3), then adds the downstream Ports to its own virtual switch.

5.5.6.5 Management-Capable Port Switch Over

Typically, a system design implements a heartbeat mechanism between the Active and Redundant Management Processors. When the Redundant Management Port Host detects that the Active Management Port must be switched over, the Redundant Management Port Host writes to the **Management Port Control** register (Port 0, accessible through the Management Port and Redundant Management Port, offset 354h), removes the existing Active Management Port, and promotes itself to be the Active Management Port Host.

Chapter 6 Serial EEPROM Controller

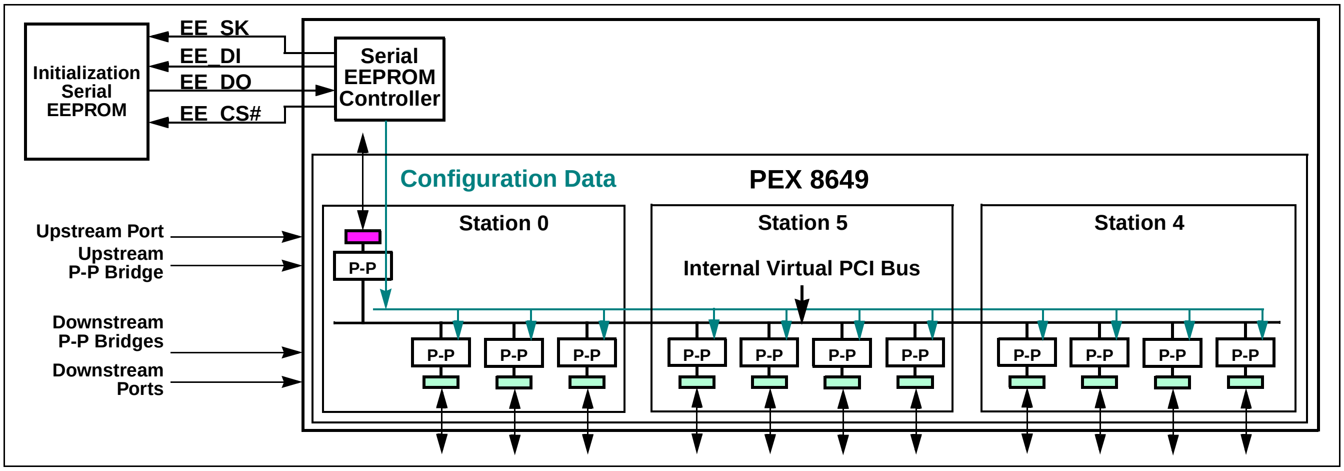
6.1 Overview

Figure 6-1The PEX 8649 provides a Serial EEPROM Controller and interface to Serial Peripheral Interface (SPI)-compatible serial EEPROMs, as illustrated in Figure 6-1. This interface consists of a Chip Select, Clock, Serial Data In, and Serial Data Out signals, and operates at a programmable frequency of up to 17.86 MHz. The PEX 8649 supports serial EEPROMs that use 1-, 2-, or 3-byte addressing; the PEX 8649 automatically determines the appropriate addressing mode.

The controller provides access to non-volatile memory. This external memory can be used for three different purposes:

- The serial EEPROM can be used to store register data, for switch configuration and initialization. When a serial EEPROM device is connected to the PEX 8649, immediately after reset, the Serial EEPROM Controller reads data from the serial EEPROM that is used to update the PEX 8649 register default values.
- System or application data can be stored into, and read from, the serial EEPROM, by software, I^{2}C and/or SMBus, initiating random-access Read or Write Requests to the serial EEPROM.
- In NT mode, the serial EEPROM can provide up to 32-KB of Expansion ROM, for the NT Port Link Interface (default) or NT Port Virtual Interface. When software reads the Expansion ROM (starting at the Expansion ROM Base Address), the PEX 8649 reads from the serial EEPROM, to return the requested ROM image.

Figure 6-1. Serial EEPROM Connections



6.2 Features

- Detection of whether a serial EEPROM is present/not present
- Supports high-speed SPI-compatible serial EEPROMs
- Non-volatile storage for register default values loaded during Power-On Reset
- 4-byte Write/Read access to the serial EEPROM, through the upstream Port(s)
- Serial EEPROM data format allows for loading registers by Station/Port/Address location
- Required serial EEPROM size is dependent upon the number of registers being changed
- Automatic support for 1-, 2-, or 3-byte-addressable serial EEPROMs
- Manual override for number of serial EEPROM Address bytes
- Programmable serial EEPROM clock frequency
- Programmable serial EEPROM clock-to-chip select timings
- No Cyclic Redundancy Check (CRC), single *Valid* byte at start of serial EEPROM memory
- Supports Expansion ROM for the NT Port (***not supported*** for 1-byte address serial EEPROMs)

6.3 Serial EEPROM Load

6.3.1 Serial EEPROM Load – Base Mode

6.3.1.1 Serial EEPROM Load Following Upstream Port Reset

The Serial EEPROM Controller performs a serial EEPROM download when the following conditions exist:

- Serial EEPROM is present[a], and
- Validation signature (first byte read from the serial EEPROM) value is 5Ah, and
- One of the following events occur:
  - PEX_PERST# is returned High, following a Fundamental Reset (*such as* a Cold or Warm Reset to the entire chip)
  - Hot Reset is received at the upstream Port (downloading upon this event can be optionally disabled, by Setting the **Virtual Switch Debug** register *Disable Serial EEPROM Load on Hot Reset* and/or *Upstream Hot Reset Control* bit (Upstream Port, offset A30h[3 and/or 2], respectively))
  - Upstream Port exits a *DL_Down* state (downloading upon this event can be optionally disabled, by Setting the **Virtual Switch Debug** register *Upstream Port and NT-Link Port DL_Down Reset Propagation Disable* and/or *Upstream Hot Reset Control* bit (Upstream Port, offset A30h[4 and/or 2], respectively))

6.3.1.2 Serial EEPROM Load Following Downstream Port Reset

Following a software-generated Fundamental Reset to a Transparent downstream Port (**Port Reset** register *Reset Port x Vector* bit (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 3A0h[23:16, 3:0]), is toggled from 1 to 0), the serial EEPROM reloads Port registers (not Chip- nor Station-specific registers) for that downstream Port, only if the **Debug Control** register *Port Reset EEP Load* bit (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 350h[22]) is Set.

[a] The serial EEPROM is considered to be present if it returns a non-zero value in response to an initial Read Status command of its Status register. This value is copied to the ***Serial EEPROM Status*** *register Status Data from Serial EEPROM fields (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 260h[31:24]). Serial EEPROM presence is reported in the register's EepPrsnt[1:0] field (field [17:16]); a value of 01b or 11b indicates that the serial EEPROM is present.*

6.3.2 Serial EEPROM Load – Virtual Switch Mode

Serial EEPROM functionality in Virtual Switch mode is identical to that in Base mode, with the following exceptions:

- Only the Management Port, I^{2}C, and SMBus can access the serial EEPROM. A PCI Express Master can access the serial EEPROM, only if that virtual switch upstream Port is designated as the Management Port (as reflected in the **Management Port Control** register *Active Management Port* field (Port 0, accessible through the Management Port and Redundant Management Port, offset 354h[4, 2:0])).
- When the serial EEPROM reloads registers following a Reset, it reloads only the Ports that are associated with that virtual switch. Determination of which Ports are associated to a particular virtual switch is dependent upon the **VS*x* Port Vector** register (Port 0, accessible through the Management Port, offsets 380h through 38Ch) value(s), initially programmed to the configuration defined by the STRAP_VS_MODE[1:0] inputs, as listed in Table 4-2, "Virtual Switch Port Configurations and Default Parallel Hot Plug Ports – Virtual Switch Mode."
- By default, Chip- and Station-specific registers are not reloaded from serial EEPROM following either a Virtual Switch Fundamental Reset (VS*x*_PERST# is de-asserted and/or a Soft Reset (Hot Reset or upstream Port *DL_Down* state)).

  A Chip- and Station-specific register reload from serial EEPROM can be enabled by the Management Port, I^{2}C, and/or SMBus Setting of the **Management Port Control** register *Active Management Port EEPROM Load on Hot Reset for Chip and Station Registers Enable* bit (Port 0, accessible through the Management Port and Redundant Management Port, offset 354h[6]).

The Serial EEPROM Controller performs a serial EEPROM download when the following conditions exist:

- Serial EEPROM is present[a], and
- Validation signature (first byte read from the serial EEPROM) value is 5Ah, and
- One of the following events occur:
  - PEX_PERST# is returned High, following a Fundamental Reset (*such as* a Cold or Warm Reset to the entire chip)
  - VS*x*_PERST# is returned High, following a Virtual Switch Fundamental Reset (*such as* a Cold or Warm Reset to a single virtual switch)
  - **VSx_PERST# Status** register *VSx_PERST# Control* bit(s) (Port 0, accessible through the Management Port, offset 3A8h[11:8]) corresponding to one or more enabled virtual switches that are Set and then Cleared, to release the virtual switch(es) from Fundamental Reset
  - Hot Reset is received at a virtual switch upstream Port (downloading upon this event can be optionally disabled, by Setting the **Virtual Switch Debug** register *Disable Serial EEPROM Load on Hot Reset* bit (VS Upstream Port(s), offset A30h[3]))
  - Virtual switch upstream Port exits a *DL_Down* state (downloading upon this event can be optionally disabled, by Setting the **Virtual Switch Debug** register *Upstream Port and NT-Link Port DL_Down Reset Propagation Disable* bit (VS Upstream Port(s), offset A30h[4]))

Serial EEPROM reload upon receiving a Soft Reset can also be disabled, by Setting the **Virtual Switch Debug** register *Upstream Hot Reset Control* bit (VS Upstream Port(s), offset A30h[2])). Setting this bit effectively converts Hot Reset severity to the lower severity of a Secondary Bus Reset.

[a] *The serial EEPROM is considered to be present if it returns a non-zero value in response to an initial Read Status command of its Status register. This value is copied to the* ***Serial EEPROM Status*** *register Status Data from Serial EEPROM fields (Port 0, accessible through the Management Port, offset 260h[31:24]). Serial EEPROM presence is reported in the register's EepPrsnt[1:0] field (field [17:16]); a value of 01b or 11b indicates that the serial EEPROM is present.*

6.4 Serial EEPROM Data Format

The data in the serial EEPROM is stored in the format defined in Table 6-1. The Validation Signature byte is located in the first address. The Serial EEPROM Controller reads this byte to determine whether a valid serial EEPROM image exists versus a blank image. REG_BYTE_COUNT[15:0] contains the number of bytes of serial EEPROM data to be loaded. It is equal to the number of registers to be loaded times 6 (6 serial EEPROM bytes per register). If the REG_BYTE_COUNT[15:0] value is not a multiple of 6, the last incomplete register entry is ignored.

For the remaining register-related locations, data is written into a 2-byte address that represents the Configuration register offset and Port Number, and the 4 bytes following are the data loaded for that Configuration register. Only Configuration register data specifically programmed into the serial EEPROM is loaded after the PEX 8649 exits reset.

Table 6-2 defines the Configuration register Address format (REGADDR[15:0] from Table 6-1):

- Bits [9:0] represent bits [11:2] of the Register address
- Bits [15:10] represent the Port Number of the register selected to be programmed by serial EEPROM

Because the PEX 8649 Serial EEPROM Controller always accesses 4 bytes of serial EEPROM data (for DWord-aligned Register addresses), register offsets are stored in the serial EEPROM as DWord address values.

To determine the 2-byte serial EEPROM value that represents the PEX 8649 Port and register offset, shift the register offset 2 bits to the right (divide by 4), then OR the resulting value with the appropriate Port Identifier value from Table 6-2.

For example, to load Port 16 register offset FA8h, shift the address to the right by 2 bits (this becomes 07Eh) and concatenate 1000_00b. The resulting DWord address in the serial EEPROM will be 1000_0000_0111_1110b (807Eh).

Table 6-1. Serial EEPROM Data

Location	Value	Description
0h	5Ah	Validation Signature
1h	00h	***Reserved***
2h	REG BYTE COUNT (LSB)	Configuration register Byte Count (LSB)
3h	REG BYTE COUNT (MSB)	Configuration register Byte Count (MSB)
4h	REGADDR (LSB)	1st Configuration Register Address (LSB)
5h	REGADDR (MSB)	1st Configuration Register Address (MSB)
6h	REGDATA (Byte 0)	1st Configuration Register Data (Byte 0)
7h	REGDATA (Byte 1)	1st Configuration Register Data (Byte 1)
8h	REGDATA (Byte 2)	1st Configuration Register Data (Byte 2)
9h	REGDATA (Byte 3)	1st Configuration Register Data (Byte 3)
Ah	REGADDR (LSB)	2nd Configuration Register Address (LSB)
Bh	REGADDR (MSB)	2nd Configuration Register Address (MSB)
Ch	REGDATA (Byte 0)	2nd Configuration Register Data (Byte 0)
Dh	REGDATA (Byte 1)	2nd Configuration Register Data (Byte 1)
Eh	REGDATA (Byte 2)	2nd Configuration Register Data (Byte 2)
Fh	REGDATA (Byte 3)	2nd Configuration Register Data (Byte 3)
…	…	…
FFFFh	REGDATA (Byte 3)	Last Configuration Register Data (Byte 3)

Note: *If the* ***VS0 Upstream*** *register (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 360h) is programmed by serial EEPROM, that must be the first register entry in the serial EEPROM (at locations 4h through 9h, as listed in Table 6-1).*

Exceptions for Legacy NT mode (STRAP_NT_P2P_EN#=H):

1. *If the STRAP_NT_ENABLE# input is logic High (disabling NT mode) and serial EEPROM/I^{2}C enables NT mode by Setting the* ***VS0 Upstream*** *register NT Enable bit (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 360h[13]), then prior to programming the* ***VS0 Upstream*** *register, serial EEPROM/I^{2}C must first load the NT Port Virtual Interface* ***PCI Class Code*** *register (offset 08h[31:8]) with the Class Code value for NT mode, 068000h (Other Bridge Device).*
2. *If serial EEPROM/I^{2}C changes the NT Port Number (by programming the* ***VS0 Upstream*** *register NT Port field (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 360h[12, 10:8])) from the value set by the STRAP_NT_UPSTRM_PORTSEL[4, 2:0] inputs, then prior to changing the NT Port Number, serial EEPROM/I^{2}C must first program:*
   - *Class Code (offset 08h[31:8]) of the Port selected by STRAP_NT_UPSTRM_PORTSEL[4, 2:0], to value 060400h (PCI-to-PCI Bridge), and,*
   - *NT Port Virtual Interface Class Code (offset 08h[31:8]) to value 068000h (Other Bridge Device).*

Table 6-2. Configuration Register Address Format

Port Number	REGADDR Bits [15:10] Value[a]	Port Identifier
Port 0	0000_00b	0000h
Port 1	0000_01b	0400h
Port 2	0000_10b	0800h
Port 3	0000_11b	0C00h
Port 16	1000_00b	8000h
Port 17	1000_01b	8400h
Port 18	1000_10b	8800h
Port 19	1000_11b	8C00h
Port 20	1010_00b	A000h
Port 21	1010_01b	A400h
Port 22	1010_10b	A800h
Port 23	1010_11b	AC00h
Legacy NT Mode		
NT Port Virtual Interface	1100_00b	C000h
NT Port Link Interface	1110_00b	E000h
NT PCI-to-PCI Bridge Mode		
NT Port Virtual Interface	1100_00b	C000h
NT Port Link Interface	1110_00b	E000h
NT PCI-to-PCI[b]	XXX0_XXb	XX00h

[a] *Encodings not listed are* ***reserved****.*

[b] *Use the values for the Station Number and Port Number for the Port that is configured as the NT Port in the* ***VS0 Upstream*** *register NT Port field (Port 0, offset 360h[12, 10:8]).*

6.5 Serial EEPROM Initialization

After the device Reset is de-asserted, the PEX 8649 determines whether a serial EEPROM is present. The serial EEPROM is considered to be present if it returns a non-zero value in response to an initial Read Status command of its **Status** register. This value is copied to the **Serial EEPROM Status** register *Status Data from Serial EEPROM* fields (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 260h[31:24]). Serial EEPROM presence is reported in the register's *EepPrsnt[1:0]* field (field [17:16]); a value of 01b or 11b indicates that the serial EEPROM is present. A pull-up resistor on the EE_DO input produces a value of FFh if a serial EEPROM is not installed.

If a serial EEPROM is detected, the first byte (validation signature) is read. If a value of 5Ah is read, it is assumed that the serial EEPROM is programmed for the PEX 8649. The serial EEPROM address width is determined while the first byte is read. If the first byte's value is not 5Ah, the serial EEPROM is blank or programmed with invalid data. In this case, no more data is read from the serial EEPROM, and the **Serial EEPROM Status** register *EepAddrWidth* field (offset 260h[23:22]) reports a value of 00b (undetermined width).

If the *EepAddrWidth* field reports a value of 00b, any subsequent accesses to the serial EEPROM (through the PEX 8649 Serial EEPROM registers) default to a serial EEPROM address width of 1 byte, unless the **Serial EEPROM Status** register *EepAddrWidth Override* bit (offset 260h[21]) is Set. The *EepAddrWidth* field is usually Read-Only; however, it is writable if the *EepAddrWidth Override* bit is Set (both can be programmed by a single Write instruction).

If the serial EEPROM contains valid data, the REG_BYTE_COUNT values in Bytes 2 and 3 determine the number of serial EEPROM locations that contain Configuration register addresses and data. Each Configuration register entry consists of 2 bytes of register Address and 4 bytes of register Write data. The REG_BYTE_COUNT must be a multiple of 6.

The EE_SK output clock frequency is determined by the **Serial EEPROM Clock Frequency** register *EepFreq[2:0]* field (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 268h[2:0]). The default clock frequency is 1 MHz. At this clock rate, it takes approximately 48 µs per DWORD during Configuration register initialization. For faster loading of large serial EEPROMs that support a faster clock, the first Configuration register load from the serial EEPROM could be to the **Serial EEPROM Clock Frequency** register.

6.6 PCI Express Configuration, Control, and Status Registers

The PCI Express Configuration, Control, and Status registers that can be initialized are detailed in:

- Chapter 13, “Transparent Port Registers”
- Chapter 15, “NT Port Virtual Interface Registers – Base Mode Only”
- Chapter 16, “NT Port Link Interface Registers – Base Mode Only”

6.7 Serial EEPROM Registers

The Serial EEPROM register (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then these registers exist in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offsets 260h through 26Ch) parameters defined in Section 13.15.4, “Device-Specific Registers – Serial EEPROM (Offsets 260h – 26Ch),” can be changed, using the serial EEPROM. It is recommended that the first serial EEPROM entry (after the **Debug Control** register (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then these registers exist in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 350h) entry, if programmed), be used to change the **Serial EEPROM Clock Frequency** register (offset 268h) value, to increase the clock frequency, and thereby reduce the time needed for the remainder of the serial EEPROM load. When the NT Port Expansion ROM feature is used, the serial EEPROM clock frequency must be 5 MHz or higher. At the last serial EEPROM entry, the **Serial EEPROM Status and Control** register (offset 260h) can be programmed to issue a Write Status Register (WRSR) command, to enable the Write Protection feature(s) within the serial EEPROM data, if needed.

6.8 Serial EEPROM Random Write/Read Access

To access the serial EEPROM, a PCI Express, I^{2}C, or SMBus Master uses the following registers (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then these registers exist in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port):

- **Serial EEPROM Status and Control** (offset 260h)
- **Serial EEPROM Buffer** (offset 264h)
- **Serial EEPROM 3rd Address Byte** (offset 26Ch)

Note: *To help streamline the text in the following subsections, the specific Port location/access of each register offset is not repeated – only the offset location is mentioned.*

The Master can only access the serial EEPROM on a DWord basis (4 bytes aligned to one DWord address).

6.8.1 Writing to Serial EEPROM

To write a DWord to the serial EEPROM:

1. If the 3rd Address byte (Address bits [23:16]) is needed (when the **Serial EEPROM Status** register *EepAddrWidth* field bits (offset 260h[23:22]) are both Set), write the value to the *Serial EEPROM 3rd Address Byte* field (offset 26Ch[7:0]).
2. Write the 32-bit data into the **Serial EEPROM Buffer** register (offset 264h).
3. Issue a Write Enable instruction to the serial EEPROM (Command = 110b, Set Write Enable Latch), by writing the value 0000_C000h into the **Serial EEPROM Status and Control** register (offset 260h).
4. Calculate and write the combined Address and Command value to write into the **Serial EEPROM Control** register, by combining the serial EEPROM 3-bit Write Data instruction (value 010b) as bits [15:13], together with the serial EEPROM address. Serial EEPROM Address bits [14:2] must be programmed into **Serial EEPROM Control** register bits [12:0], and serial EEPROM Address bit 15 must be programmed into **Serial EEPROM Status** register bit 20 (*that is*, Set bit 20 if the serial EEPROM address is in the upper 32 KB of any 64-KB address block within the serial EEPROM). The data in the **Serial EEPROM Buffer** register is written to the serial EEPROM when the **Serial EEPROM Status and Control** register is written.
5. The serial EEPROM Write operation is complete when a subsequent read of the **Serial EEPROM Status** register bit 18 returns 0. At this time, another serial EEPROM access can be started.

Because each PEX 8649 Port and Register address value (REGADDR; refer to Section 6.5), and its corresponding Data value (REGDATA), require 6 bytes of serial EEPROM memory, and the PEX 8649 serial EEPROM interface accesses 4 bytes at a time, two serial EEPROM Writes may be needed to store each set of REGADDR (one Word) and REGDATA (1 Dword) entries into the serial EEPROM. To avoid overwriting a Word of another set of 6-byte REGADDR and REGDATA values, one of the two Serial EEPROM Writes might need to be a Read-Modify-Write type of operation (preserving one Word read from the serial EEPROM and writing the value back along with a new Word value).

6.8.2 Reading from Serial EEPROM

To read a DWord from the serial EEPROM:

1. If the 3rd Address byte (Address bits [23:16]) is needed (when the **Serial EEPROM Status** register *EepAddrWidth* field bits (offset 260h[23:22]) are both Set), write the value to the **Serial EEPROM 3rd Address Byte** register *Serial EEPROM 3rd Address Byte* field (offset 26Ch[7:0]).
2. Calculate the combined Address and Command value to write into the **Serial EEPROM Control** register (offset 260h), by combining the serial EEPROM 3-bit Read Data instruction (value 011b) as bits [15:13], together with the serial EEPROM address. Serial EEPROM Address bits [14:2] must be programmed into **Serial EEPROM Control** register bits [12:0], and serial EEPROM Address bit 15 must be programmed into **Serial EEPROM Status** register bit 20 (*that is*, Set bit 20 if the serial EEPROM address is in the upper 32 KB of any 64-KB address block within the serial EEPROM).
3. Poll the **Serial EEPROM Status** register until the *EepCmdStatus* bit (offset 260h[18]) is Cleared, which signals that the transaction is complete.
4. Read the four bytes of serial EEPROM data from the **Serial EEPROM Buffer** register (offset 264h).

   For example, to read the first DWord in the serial EEPROM, write the value 0000_6000h to Port 0, register offset 260h, and then read Port 0, register offset 264h.

6.8.3 Programming a Blank Serial EEPROM

The PEX 8649 supports 1-, 2-, or 3-byte serial EEPROM addressing. 8-Kbit to 512-Kbit SPI EEPROMs use 2-byte addressing. The PEX 8649 requires that the first byte in the serial EEPROM must be the value 5Ah (ASCII Z), as a Validation Signature.

The 2nd and 3rd bytes contain the number of bytes within the serial EEPROM image, beginning with the first register entry at serial EEPROM address 04h. If this Byte Count value exceeds the actual number of register entries times 6 (*for example*, if the first DWord is programmed to the value 5A00_FFFFh), the system could hang. To simplify programming of a blank EEPROM (*such as* in a typical production build), the serial EEPROM could be pre-programmed with the first DWord, 0000_005Ah.

A 2-byte address serial EEPROM that is blank (or corrupted) can be programmed according to the following procedure (when the PEX 8649 is in 1-Byte Address mode).

To program a blank serial EEPROM:

1. Write the value 0000_005Ah into the **Serial EEPROM Buffer** register at address [upstream Port **BAR0** + 264h].
2. Issue a Write Enable instruction (Command = 110b, Set Write Enable Latch, and enable 2-byte addressing, by writing the value 00A0_C000h into the **Serial EEPROM Status and Control** register (offset 260h).
3. Copy this data value to serial EEPROM location 0, by writing the value 00A0_4000h into the **Serial EEPROM Status and Control** register. At this point, the first four bytes in the serial EEPROM now contain the value 0000_005Ah.
4. Reboot the system, to reset the PEX 8649 so that it re-detects the serial EEPROM.

6.9 Serial EEPROM Loading of NT Port Link Interface Registers – Base Mode Only

The **Virtual Switch Debug** register *Load Only EEPROM NT-Link on Hot Reset* and *Inhibit EEPROM NT-Link Load on Hot Reset* bits (Upstream Port, offset A30h[27:26], respectively) control whether the serial EEPROM is to load registers following a Soft Reset (Hot Reset or DL_Down) to the upstream Port or NT Port Link Interface, as defined in Table 6-3.

Table 6-3. Serial EEPROM Loading of NT Port Link Interface Registers (Upstream Port, Offset A30h[27:26] Values)

Bit 27 Value	Bit 26 Value	Action
0	0	Load all registers from the serial EEPROM.
0	1	Load all registers, except the NT Port Link Interface registers, from the serial EEPROM.
1	0	Load only NT Port Link Interface registers from the serial EEPROM.
1	1	Disable serial EEPROM loading of all registers.

6.10 NT Port Expansion ROM – Base Mode Only

The PEX 8649 NT Port Virtual and Link Interfaces support Expansion ROM, as defined in the *PCI r3.0*. Expansion ROM can be implemented for either Port, but not both concurrently. The Expansion ROM image is stored in the serial EEPROM, and its size can be either 16 KB (default, bit is Cleared) or 32 KB (maximum), based upon the **Serial EEPROM Clock Frequency** register *Expansion ROM Size* bit (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 268h[16]) value.

By default, the Expansion ROM is enabled on the NT Port Link Interface; however, it can be enabled instead for the NT Port Virtual Interface, by Setting the **Ingress Chip Control** register *Expansion ROM Virtual Side* bit (Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface, offset 764h[0]). The **Expansion ROM Base Address** register (BAR) must be enabled, by Setting the register’s *Expansion ROM Enable* bit, in either the NT Port Virtual Interface (offset 30h[0]) or NT Port Link Interface (offset 30h[0]).

The Expansion ROM’s location in the serial EEPROM is programmed in the **Serial EEPROM 3rd Address Byte** register *Expansion ROM Base Address* field (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 26Ch[31:16]), of which the lower six bits, [21:16], map to serial EEPROM byte Address bits [15:10] (aligned to a 256-DWord (1-KB) boundary). The Expansion ROM must not straddle a 64-KB boundary within the serial EEPROM.

The default serial EEPROM Base Address value is as follows:

- **16-KB Expansion ROM (*Expansion ROM Size* bit is Cleared)** – The value is 0020h, which corresponds to serial EEPROM Byte address 2000h (8 KB). The serial EEPROM size must be at least 32 KB.
- **32-KB Expansion ROM (*Expansion ROM Size* bit is Set)** – The value is 0040h, which corresponds to serial EEPROM byte address 4000h (16 KB). The serial EEPROM size must be at least 64 KB.

Chapter 7 I^{2}C/SMBus Slave Interface Operation

7.1 Introduction

This chapter discusses the I^{2}C Slave Interface and SMBus Slave Interface.

7.2 I^{2}C Slave Interface

7.2.1 I^{2}C Support Overview

Note: *This section applies to the I^{2}C Slave interface, which uses the I2C_ADDR[2:0], I2C_SCL0, and I2C_SDA0 signals for PEX 8649 register access by an I^{2}C Master. The I2C_SCL1 and I2C_SDA1 signals form the PEX 8649 I^{2}C Master interface, which is used only for Serial Hot Plug operation. (Refer to Section 10.9, "Serial Hot Plug Controller.")*

Inter-Integrated Circuit (I^{2}C) is a bus used to connect Integrated Circuits (ICs). Multiple ICs can be connected to an I^{2}C Bus and I^{2}C devices that have I^{2}C mastering capability can initiate a Data transfer. I^{2}C is used for Data transfers between ICs at relatively low rates (100 Kbps) and is used in a variety of applications. For further details regarding I^{2}C Buses, refer to the I2C Bus, v2.1.

The PEX 8649 is an I^{2}C Slave. Slave operations allow the PEX 8649 Configuration registers to be read from or written to by an I^{2}C Master, external from the device. I^{2}C is a sideband mechanism that allows the device Configuration registers to be programmed, read from, or written to, independent of the PCI Express upstream Link.

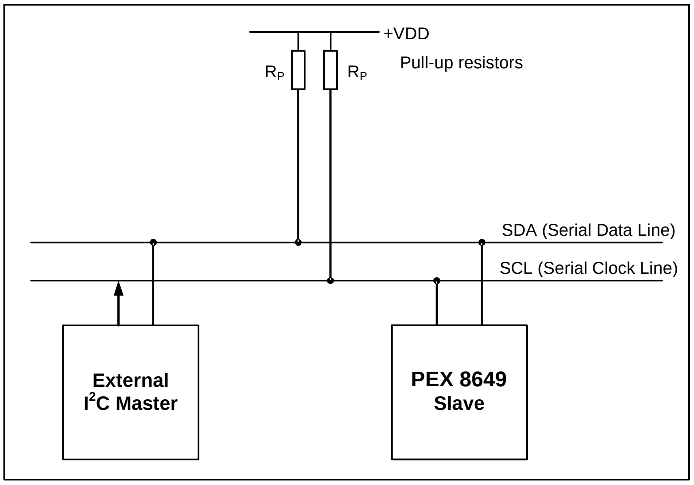
With I^{2}C, users have the option of accessing all PEX 8649 registers through the I^{2}C Slave interface. I^{2}C provides an alternative to using a serial EEPROM. I^{2}C can also be used for debugging, such as if the PEX 8649 upstream Port(s) fail(s) to linkup.

Accordingly, it is recommended that both I^{2}C/SMBus access and the serial EEPROM (or at least its footprint) be included in designs.

The I2C_SCL0 and I2C_SDA0 signals can be brought out to a 2x2 pin header on the board, to allow PLX software (*for example*, running on a laptop computer) to access the PEX 8649 registers, using an Aardvark USB-I^{2}C adapter connected to this header. (Refer to the *PEX 8649 RDK Hardware Reference Manual* for the header pin design.)

Figure 7-1 provides a block diagram that illustrates how standard devices connect to the I^{2}C Bus.

Figure 7-1. Standard Devices to I^{2}C Bus Connection Block Diagram



7.2.2 I^{2}C Addressing – Slave Mode Access

To access the PEX 8649 Configuration registers through the I^{2}C Slave interface, the PEX 8649 I^{2}C Slave address must be configured.

The PEX 8649 supports a 7-bit I^{2}C Slave address. The 7-bit I^{2}C Address bits can be configured by the serial EEPROM (recommended, if the default address must be changed), or by a Memory Write, in the **I^{2}C Configuration** register (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 294h, default value 1Fh), with the lower three bits of the address derived from the I2C_ADDR[2:0] inputs. Bits [6:0] correspond to Address Byte bits [7:1], with bit 0 of the byte indicating a Write (0) or Read (1).

The I2C_ADDR[2:0] balls can be pulled High or Low, to select a different Slave address. Up to eight PEX 8649 devices can share the same I^{2}C Bus segment without conflict, provided that each PEX 8649 has its set of I2C_ADDR[2:0] inputs strapped to a unique state. More than eight PEX 8649 devices can share the I^{2}C Bus, however, if the upper Address bits are programmed in the serial EEPROM. The default state for I2C_ADDR[2:0] inputs that are not externally connected High or Low is 111b, due to the internal pull-up resistors.

7.2.3 I^{2}C Slave Interface Register

The **I^{2}C Slave Interface** register, **I^{2}C Configuration**, is described in Section 13.15.5, "Device-Specific Registers – I^{2}C and SMBus Slave Interfaces (Offsets 290h – 2FCh)." The default I^{2}C Slave address can be changed in the **I^{2}C Configuration** register to a different value, using the serial EEPROM or a Memory Write.

The I^{2}C Slave address must not be changed by an I^{2}C Write command. (Refer to Section 7.2.2.)

Other I^{2}C Slave interface registers exist; however, they are for ***Factory Test Only***.

7.2.4 I^{2}C Command Format

An I^{2}C transfer starts as a packet with Address Phase bytes, followed by four Command Phase bytes, and one or more Data Phase bytes. The I^{2}C packet Address Phase Byte format is illustrated in Figure 7-2a. The Command Phase portion must include 4 bytes of data that contain the following:

- I^{2}C Transfer type (Read/Write)
- PCI Express Configuration Register address
- PEX 8649 Port Number being accessed
- Byte Enable(s) of the register data being accessed

When the I^{2}C Master is writing to the PEX 8649, the I^{2}C Master must transmit the Data bytes to be written to that register within the same packet that contains the Command bytes. Table 7-2 describes each I^{2}C Command byte for Write access. Figure 7-2b illustrates the Command phase portion of an I^{2}C Write packet.

When the I^{2}C Master is reading from the PEX 8649, the I^{2}C Master must separately transmit a Command Phase packet and Data Phase packet. Table 7-6 describes each I^{2}C Command byte for Read access. Figure 7-4b illustrates the Command phase portion of an I^{2}C Read packet.

Each I^{2}C packet must contain 4 bytes of data. Pad unused packet Data bytes with zeros (0) to meet this requirement.

7.2.5 I^{2}C Register Write Access

The PEX 8649 Configuration registers can be read from and written to, based upon I^{2}C register Read and Write operations, respectively. An I^{2}C Write packet consists of Address Phase bytes and Command Phase bytes, followed by one to four additional I^{2}C Data bytes. Table 7-1 defines mapping of the I^{2}C Data bytes to the Configuration register Data bytes. Figure 7-2c illustrates the I^{2}C Data byte format.

The I^{2}C packet starts with the *S* (START condition) bit. Data bytes are separated by the *A* (Acknowledge Control Packet (ACK)) or *N* (Negative Acknowledge (NAK)) bit. The packet ends with the *P* (STOP condition) bit.

If the Master generates an invalid command, the targeted PEX 8649 register is not modified.

The PEX 8649 considers the 1st Data byte of the 4-byte Data phase following the four Command bytes in the Command phase, as register Byte 3 (bits [31:24]). The next three Data bytes access register Bytes 2 through 0, respectively, respectively. Four Data Bytes are required, regardless of the Byte Enable Settings in the Command phase. The Master can then generate either a STOP condition (to finish the transfer) or a repeated START condition (to start a new transfer). If the I^{2}C Master sends more than the four Data bytes (violating PEX 8649 protocol), the PEX 8649 returns a NAK for the extra Data byte(s). (For further details regarding I^{2}C protocol, refer to the *I2C Bus, v2.1*.)

Table 7-2 describes each I^{2}C Command byte for Write access. In the packet described in Figure 7-2, Command Bytes 0 through 3 for Writes follow the format specified in Table 7-2.

Table 7-1. I^{2}C Register Write Access

I^{2}C Data Byte Order	PCI Express Configuration Register Bytes
0	Written to register Byte 3
1	Written to register Byte 2
2	Written to register Byte 1
3	Written to register Byte 0

Table 7-2. I^{2}C Command Format for Write Access

Field (Byte) On Bus	Bit(s)	Value/Description
Command Byte 1	7:3	***Reserved*** Should be Cleared.
	2:0	**Command** 011b = Write register Do not use other encodings for Writes.
Command Byte 2	7:5	***Reserved*** Should be Cleared.
	4	**NT Port Link Interface Select** 0 = Should be Cleared, for accesses to: • Transparent Ports • NT PCI-to-PCI bridge downstream Port registers, in NT PCI-to-PCI Bridge mode • NT Port Virtual Interface For NT Port Virtual Interface access: – *Station Select* value should be 110b (Byte 2, bits [3:1]), and – *Port Selector[1:0]* value should be 11b (Byte 2, bit 0 and Byte 3, bit 7) 1 = For NT Port Link Interface access: • *Station Select* value is Don’t Care (Byte 2, bits [3:1]), and • *Port Selector[1:0]* value should be 00b (Byte 2, bit 0 and Byte 3, bit 7)
	3:1	**Station Select** 000b = Station 0 100b = Station 4 101b = Station 5 110b = NT Port Virtual Interface when bit 4 value is 0 All other encodings are ***reserved***. When the bit 4 value is 0 for NT Port Virtual Interface access, the *Station Select* value must be 110b. Value is Don’t Care, when the bit 4 value is 1.
	0	**Port Selector, Bit 1**

Table 7-2. I²C Command Format for Write Access *(Cont.)*

Field (Byte) On Bus	Bit(s)	Value/Description
Command Byte 3	7	**Port Selector, Bit 0** *Port Selector[1:0]* selects the Port to access. 00b = Port 0 of the Station indicated by *Station Select* 01b = Port 1 of the Station indicated by *Station Select* 10b = Port 2 of the Station indicated by *Station Select* 11b = Port 3 of the Station indicated by *Station Select* For NT Port Link Interface access, *Port Selector[1:0]* value should be 00b. For NT Port Virtual Interface access, *Port Selector[1:0]* value should be 11b.
	6	***Reserved*** Should be Cleared.
	5:2	**Byte Enables** **Bit Description** 2 Byte Enable for Byte 0 (PEX 8649 register bits [7:0]) 3 Byte Enable for Byte 1 (PEX 8649 register bits [15:8]) 4 Byte Enable for Byte 2 (PEX 8649 register bits [23:16]) 5 Byte Enable for Byte 3 (PEX 8649 register bits [31:24]) 0 = Corresponding PEX 8649 register byte will not be modified 1 = Corresponding PEX 8649 register byte will be modified All 16 combinations are valid values.
	1:0	**PEX 8649 Register Address, Bits [11:10]**
Command Byte 4	7:0	**PEX 8649 Register Address [9:2]** ***Note:*** *All register addresses are DWord-aligned. Therefore, Address bits [1:0] are implicitly Cleared, and then internally incremented for successive I²C byte Writes.*

Figure 7-2. I^{2}C Write Packet

Figure 7-2a I^{2}C Write Packet Address Phase Bytes

1st Cycle			
START	**7 6 5 4 3 2 1**	**0**	**ACK/NAK**
S	Slave Address[7:1]	Read/Write Bit 0 = Write	A

Figure 7-2b I^{2}C Write Packet Command Phase Bytes

Command Cycle							
7 6 5 4 3 2 1 0	**ACK/NAK**	**7 6 5 4 3 2 1 0**	**ACK/NAK**	**7 6 5 4 3 2 1 0**	**ACK/NAK**	**7 6 5 4 3 2 1 0**	**ACK/NAK**
Command Byte 0	A	Command Byte 1	A	Command Byte 2	A	Command Byte 3	A

Figure 7-2c I^{2}C Write Packet Data Phase Bytes

Write Cycle								
7 6 5 4 3 2 1 0	**ACK/NAK**	**7 6 5 4 3 2 1 0**	**ACK/NAK**	**7 6 5 4 3 2 1 0**	**ACK/NAK**	**7 6 5 4 3 2 1 0**	**ACK/NAK**	**STOP**
Data Byte 0 (to selected register Byte 3)	A	Data Byte 1 (to selected register Byte 2)	A	Data Byte 2 (to selected register Byte 1)	A	Data Byte 3 (to selected register Byte 0)	A	P

7.2.5.1 I^{2}C Register Write

The following tables illustrate a sample I^{2}C packet for writing the PEX 8649 **MSI Upper Address** register (offset 50h) for Port 17 (Port 1 of Station 4), with data 1234_5678h.

Note: *The PEX 8649 has a default I^{2}C Slave address [6:0] value of 1Fh, with the I2C_ADDR[2:0] balls having a value of 111b. The byte sequence on the I^{2}C Bus, as listed in the following tables, occurs after the START and before the STOP bits are Set in the packet, by which the I^{2}C Master frames the transfer.*

Table 7-3. I^{2}C Register Write Access Example – 1st Cycle

Phase	Value	Description
Address	3Eh	**Bits [7:1] for PEX 8649 I^{2}C Slave Address (1Fh)** Last bit (bit 0) for Write = 0.

Table 7-4. I^{2}C Register Write Access Example – Command Cycle

Byte	Value	Description
0	03h	[7:3] ***Reserved*** Should be Cleared. [2:0] **Command** 011b = Write register
1	08h	[7:5] ***Reserved*** Should be Cleared. 4 **NT Port Link Interface Select** [3:1] **Station Select** 0 **Port Selector, Bit 1**
2	BCh	7 **Port Selector, Bit 0** 6 ***Reserved*** Should be Cleared. [5:2] **Byte Enables** All active. [1:0] **PEX 8649 Register Address, Bits [11:10]**
3	14h	[7:0] **PEX 8649 Register Address [9:2]**

Table 7-5. I^{2}C Register Write Access Example – Write Cycle

Byte	Value	Description
0	12h	**Data to Write for Byte 3**
1	34h	**Data to Write for Byte 2**
2	56h	**Data to Write for Byte 1**
3	78h	**Data to Write for Byte 0**

Figure 7-3. I^{2}C Write Command Packet Example

Figure 7-3a I^{2}C Write Packet Address Phase Bytes

1st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address 0011_111b	Read/Write Bit 0 0 = Write	A

Figure 7-3b I^{2}C Write Packet Command Phase Bytes

Command Cycle							
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK
Command Byte 0 0000_0011b	A	Command Byte 1 0000_1000b	A	Command Byte 2 1011_1100b	A	Command Byte 3 0001_0100b	A

Figure 7-3c I^{2}C Write Packet Data Phase Bytes

Write Cycle								
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	STOP
Data Byte 0 0001_0010b	A	Data Byte 1 0011_0100b	A	Data Byte 2 0101_0110b	A	Data Byte 3 0111_1000b	A	P

7.2.6 I^{2}C Register Read Access

When the I^{2}C Master attempts to read a PEX 8649 register, two packets are transmitted. The 1st packet consists of Address and Command Phase bytes to the Slave. The 2nd packet consists of Address and Data Phase bytes.

According to the *I2C Bus, v2.1*, a Read cycle is triggered when the Read/Write bit (bit 0) of the 1st cycle is Set. The Command phase reads the requested register content into the internal buffer. When the I^{2}C Read access occurs, the internal buffer value is transferred on to the I^{2}C Bus, starting from Byte 3 (bits [31:24]), followed by the subsequent bytes, with Byte 0 (bits [7:0]) being transferred last. If the I^{2}C Master requests more than four bytes, the PEX 8649 re-transmits the same byte sequence, starting from Byte 3 of the internal buffer.

The 1st and 2nd I^{2}C Read packets (illustrated in Figure 7-4 and Figure 7-5, respectively) perform the following functions:

- **1st packet** – Selects the register to read
- **2nd packet** – Reads the register (sample 2nd packet provided is for a 7-bit PEX 8649 I^{2}C Slave address)

Although two packets are shown for the I^{2}C Read, the I^{2}C Master can merge the two packets together into a single packet, by not generating the STOP at the end of the first packet (Master does not relinquish the bus) and generating REPEAT START.

Table 7-6 describes each I^{2}C Command byte for Read access. In the packet described in Figure 7-4, Command Bytes 0 through 3 for Reads follow the format specified in Table 7-6.

Table 7-6. I^{2}C Command Format for Read Access

Field (Byte) On Bus	Bit(s)	Value/Description
Command Byte 1	7:3	***Reserved*** Should be Cleared.
	2:0	**Command** 100b = Read register Do not use other encodings for Reads.
Command Byte 2	7:5	***Reserved*** Should be Cleared.
	4	**NT Port Link Interface Select** 0 = Should be Cleared, for accesses to: • Transparent Ports • NT PCI-to-PCI bridge downstream Port registers, in NT PCI-to-PCI Bridge mode • NT Port Virtual Interface For NT Port Virtual Interface access: – *Station Select* value should be 110b (Byte 2, bits [3:1]), and – *Port Selector[1:0]* value should be 11b (Byte 2, bit 0 and Byte 3, bit 7) 1 = For NT Port Link Interface access: • *Station Select* value is Don’t Care (Byte 2, bits [3:1]), and • *Port Selector[1:0]* value should be 00b (Byte 2, bit 0 and Byte 3, bit 7)
	3:1	**Station Select** 000b = Station 0 100b = Station 4 101b = Station 5 110b = NT Port Virtual Interface when bit 4 value is 0 All other encodings are ***reserved***. When the bit 4 value is 0 for NT Port Virtual Interface access, the *Station Select* value must be 110b. Value is Don’t Care, when the bit 4 value is 1.
	0	**Port Selector, Bit 1**

Table 7-6. I^{2}C Command Format for Read Access *(Cont.)*

Field (Byte) On Bus	Bit(s)	Value/Description
Command Byte 3	7	**Port Selector, Bit 0** *Port Selector[1:0]* selects the Port to access. 00b = Port 0 of the Station indicated by *Station Select* 01b = Port 1 of the Station indicated by *Station Select* 10b = Port 2 of the Station indicated by *Station Select* 11b = Port 3 of the Station indicated by *Station Select* For NT Port Link Interface access, *Port Selector[1:0]* value should be 00b. For NT Port Virtual Interface access, *Port Selector[1:0]* value should be 11b.
	6	***Reserved*** Should be Cleared.
	5:2	**Byte Enables** **Bit** **Description** 2 Byte Enable for Byte 0 (PEX 8649 register bits [7:0]) 3 Byte Enable for Byte 1 (PEX 8649 register bits [15:8]) 4 Byte Enable for Byte 2 (PEX 8649 register bits [23:16]) 5 Byte Enable for Byte 3 (PEX 8649 register bits [31:24]) 0 = Corresponding PEX 8649 register byte will not be modified 1 = Corresponding PEX 8649 register byte will be modified All 16 combinations are valid values.
	1:0	**PEX 8649 Register Address, Bits [11:10]**
Command Byte 4	7:0	**PEX 8649 Register Address [9:2]** ***Note:*** *All register addresses are DWord-aligned. Therefore, Address bits [1:0] are implicitly Cleared, and then internally incremented for successive I^{2}C byte Writes.*

Figure 7-4. I^{2}C Read Command Packet (1st Packet)

Figure 7-4a I^{2}C Read Command Packet Address Phase Bytes

1st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address[7:1]	Read/Write Bit 0 = Write	A

Figure 7-4b I^{2}C Read Command Packet Command Phase Bytes

Command Cycle							
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	STOP
Command Byte 0	A	Command Byte 1	A	Command Byte 2	A	Command Byte 3	P

Figure 7-5. I^{2}C Read Data Packet (2nd Packet)

Figure 7-5a I^{2}C Read Data Packet Address Phase Bytes

1st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address[7:1]	Read/Write Bit, 1 = Read	A

Figure 7-5b I^{2}C Read Data Packet Data Phase Bytes

Read Cycle								
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	STOP
Register Byte 3	A	Register Byte 2	A	Register Byte 1	A	Register Byte 0	A	P

7.2.6.1 I^{2}C Register Read Address Phase and Command Packet

The following is a sample I^{2}C packet for reading the PEX 8649 **MSI Upper Address** [63:32] register (offset 50h) in Port 17 (Port 1 of Station 4), assuming the register value is ABCD_EF01h.

Note: *The PEX 8649 has a default I^{2}C Slave address [6:0] value of 1Fh, with the I2C_ADDR[2:0] balls having a value of 111b. The byte sequence on the I^{2}C Bus, as listed in the following tables, occurs after the START and before the STOP bits are Set in the packet, by which the I^{2}C Master frames the transfer.*

Table 7-7. I^{2}C Register Read Access Example – 1st Packet

Phase	Value	Description
Address	3Eh	**Bits [7:1] for PEX 8649 I^{2}C Slave Address (1Fh)** Last bit (bit 0) for Write = 0.

Table 7-8. I^{2}C Register Read Access Example – Command Cycle

Byte	Value	Description
0	04h	[7:3] ***Reserved*** Should be Cleared. [2:0] **Command** 100b = Read register
1	08h	[7:5] ***Reserved*** Should be Cleared. 4 **NT Port Link Interface Select** [3:1] **Station Select** 0 **Port Selector, Bit 1**
2	BCh	7 **Port Selector, Bit 0** 6 ***Reserved*** Should be Cleared. [5:2] **Byte Enables** All active. [1:0] **PEX 8649 Register Address, Bits [11:10]**
3	14h	[7:0] **PEX 8649 Register Address [9:2]**

7.2.6.2 I^{2}C Register Read Data Packet

Note: *The PEX 8649 has a default I^{2}C Slave address [6:0] value of 1Fh, with the I2C_ADDR[2:0] balls having a value of 111b. The byte sequence on the I^{2}C Bus, as listed in the following following table and figures, occurs after the START and before the STOP bits are Set in the packet, by which the I^{2}C Master frames the transfer.*

Table 7-9. I^{2}C Register Read Access Example – 1st Cycle

Phase	Value	Description
Address	3Fh	**Bits [7:1] for PEX 8649 I^{2}C Slave Address (1Fh)** Last bit (bit 0) for Read = 1.
Read	ABh	**Byte 3 of Register Read**
	CDh	**Byte 2 of Register Read**
	EFh	**Byte 1 of Register Read**
	01h	**Byte 0 of Register Read**

Figure 7-6. 1st Packet – I^{2}C Command Phase

1st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address 0011_111b	Read/Write Bit 0 = Write	A

Command Cycle							
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	STOP
Command Byte 0 0000_0100b	A	Command Byte 1 0000_1000b	A	Command Byte 2 1011_1100b	A	Command Byte 3 0001_0100b	P

Figure 7-7. 2nd Packet – I^{2}C Read Phase

1st Cycle			
START	7 6 5 4 3 2 1	0	ACK/NAK
S	Slave Address[7:1] 0011_111b	Read/Write Bit 1 = Read	A

Read Cycle							
7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	ACK/NAK	7 6 5 4 3 2 1 0	STOP
Register Byte 3 1010_1011b	A	Register Byte 2 1100_1101b	A	Register Byte 1 1110_1111b	A	Register Byte 0 0000_0001b	P

7.3 SMBus Slave Interface

7.3.1 SMBus Features

- Compliant to the *SMBus v2.0*
- Supports the SMBus Slave function only
- PEX 8649 internal registers can be read and written, through the SMBus Slave interface
- Supports Address Resolution Protocol (ARP-capable)
- Strapping inputs, serial EEPROM, software, or ARP Set the Slave address
- Supports Block Read, Block Write, and Block Read - Block Write Process Call commands to access the registers
- Supports Packet Error Checking
- 10 to 100 KHz Bus operation frequency range

7.3.2 SMBus Operation

Based upon I^{2}C's principles of operation, SMBus is a two-wire bus used for communication between IC components and the remainder of the system. Electrically, I^{2}C and SMBus devices are compatible, and both protocol devices can co-exist on the same bus. Multiple devices, both Masters and Slaves, can be connected to an SMBus segment. PCI Express cards have two optional SMBus pins defined on the connector – SMCLK and SMDAT.

The PEX 8649 implements an *SMBus v2.0*-compliant Slave device, and is used to read and write PEX 8649 registers, through SMBus commands. The PEX 8649 SMBus uses the same SDA data and SCL clock balls that are used for I^{2}C, and the I2C_ADDR[1:0] inputs, to define address assignment (I2C_ADDR2 is not used as an Address bit in SMBus mode). At any time, either the I^{2}C or the SMBus feature is enabled, dependent upon the **SMBus Configuration** register *SMBus Enable* bit (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 2C8h[0]) state, which is latched (at Fundamental Reset) to the inverse value of the STRAP_SMBUS_EN# input. Software can toggle this bit to switch between I^{2}C and SMBus functionality.

The PEX 8649 SMBus Slave interface supports three command protocols for register access:

- Block Write
- Block Read
- Block Read - Block Write Process Call

The PEX 8649 SMBus logic also supports the commands that are required to support ARP. ARP is a feature specific to *SMBus v2.0*, through which an SMBus ARP Master can dynamically assign a unique address to each of the SMBus Targets residing on the same bus. Although ARP is an optional feature of the *SMBus v2.0*, PCI and PCI Express cards are required to support ARP. The ARP feature is enabled when the **SMBus Configuration** register *ARP Disable* bit (offset 2C8h[8]) is Cleared; this bit is initially latched (at Fundamental Reset) to the value of the I2C_ADDR2 input.

If ARP is disabled, by I2C_ADDR2 input being pulled High, the SMBUS Slave Address bits [6:2] default to value 001_10b. Address bits [1:0] are initially latched (at Fundamental Reset) to the value of the I2C_ADDR[1:0] inputs, which allows a maximum of four SMBus-enabled PEX 8649 to co-exist on the same SMBus segment. Software can change the SMBus Slave address, by programming the **SMBus Configuration** register *SMBus Device Address* field (offset 2C8h[7:1]).

The PEX 8649 also supports Packet Error Checking and Packet Error Code (PEC) generation, as explained in the *SMBus v2.0*. The *SMBus v2.0* optional feature, *Notify ARP Master* (which requires Master capability on the SMBus) is ***not*** supported.

7.3.3 SMBus Commands Supported

For register access, the SMBus logic supports three commands:

- Block Write (command BEh) is used to write the registers
- Block Write (command BAh), followed by Block Read (command BDh), can be used to read the registers
- Block Read - Block Write Process Call (commands BAh, CDh) can also be used to read registers

SMBus Commands that are not supported by the PEX 8649 (Quick Command, Send Byte, Receive Byte, Write Byte, Write Word, Read Byte, Read Word, and Process Call), are Negative Acknowledged (NACKed).

7.3.3.1 SMBus Block Write

The Block Write command is used to write to the PEX 8649 registers. General SMBus Block Writes are illustrated in Figure 7-8 and Figure 7-9. The sequence of Bytes include the following, in the sequence listed:

- 7-bit address,
- Command Code that indicates it is Block Write,
- *Byte Count* field with a value of 8h that indicates 4 bytes to set up the register to write (Port Number, register address, Command Byte Enable, and so forth), followed by
- 4 bytes of data to be written into the register

Figure 7-10 explains the elements used in Figure 7-8 and Figure 7-9, and Figure 7-11 indicates the Data Bytes written.

Figure 7-8. SMBus Block Write Command Format, to Write to a PEX 8649 Register without PEC

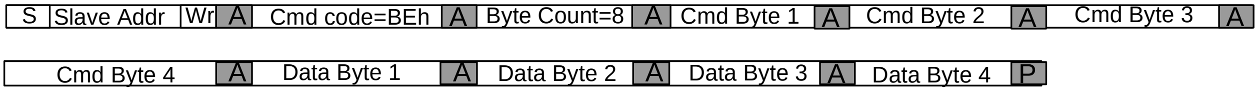


Figure 7-9. SMBus Block Write Command Format, to Write to a PEX 8649 Register with PEC

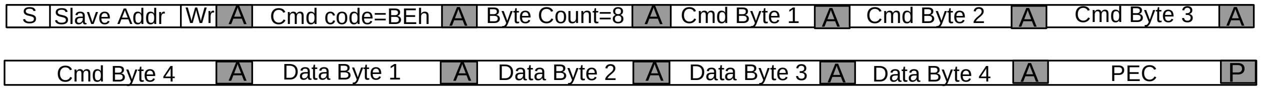


Figure 7-10. SMBus Packet Protocol Diagram Element Key

S -> START condition
P -> STOP condition

A -> Acknowledge (this bit position may be 0 for an ACK or 1 for a NACK)

□ -> Master to Slave
▨ -> Slave to Master

Figure 7-11. SMBus Block Write Bytes, as Written to Register

31:24	23:16	15:8	7:0
Data Byte 1	Data Byte 2	Data Byte 3	Data Byte 4

Note: *In each byte, the Most Significant Byte (MSB) is transmitted first.*

Table 7-10 provides a description of bytes for an SMBus Block Write.

Block Write transactions that are received with incorrect byte settings are NACKed, starting from the wrong byte setting, and including subsequent bytes in the packet. *For example*, if the Byte Count value is not 8, the PEX 8649 NACKs the byte corresponding to the Byte Count value, as well as any Data bytes following within the same packet.

The byte after Data Byte 4, if present, is taken as the PEC byte, and if present, the PEC is checked. If a packet fails Packet Error Checking, the PEX 8649 drops the packet (ignores the Write), and returns NACK for the PEC byte, to the SMBus Master. Packet Error Checking can be disabled, by Setting the **SMBus Configuration** register *PEC Check Disable* bit (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 2C8h[9]). The Byte Count value, by definition, does not include the PEC byte.

Table 7-10. Bytes for Block CSR Write on SMBus

Field (Byte) On Bus	Bit(s)	Value/Description
Command Code	7:0	BEh for **B**lock Writ**E**.
Byte Count	7:0	08h = 8 bytes to follow (4 Command and 4 Data bytes). The PEC byte is not counted.
Command Byte 1	7:3	***Reserved*** Should be Cleared.
	2:0	**Command** 011b = Write register Do not use other encodings for Writes.
Command Byte 2	7:5	***Reserved*** Should be Cleared.
	4	**NT Port Link Interface Select** 0 = Should be Cleared, for accesses to: • Transparent Ports • NT PCI-to-PCI bridge downstream Port registers, in NT PCI-to-PCI Bridge mode • NT Port Virtual Interface For NT Port Virtual Interface access: – *Station Select* value should be 110b (Byte 2, bits [3:1]), and – *Port Selector[1:0]* value should be 11b (Byte 2, bit 0 and Byte 3, bit 7) 1 = For NT Port Link Interface access: • *Station Select* value is Don’t Care (Byte 2, bits [3:1]), and • *Port Selector[1:0]* value should be 00b (Byte 2, bit 0 and Byte 3, bit 7)
	3:1	**Station Select** 000b = Station 0 100b = Station 4 101b = Station 5 110b = NT Port Virtual Interface when bit 4 value is 0 All other encodings are ***reserved***. When the bit 4 value is 0 for NT Port Virtual Interface access, the Station Select value must be 110b. Value is Don’t Care, when the bit 4 value is 1.
	0	**Port Selector, Bit 1**

Table 7-10. Bytes for Block CSR Write on SMBus *(Cont.)*

Field (Byte) On Bus	Bit(s)	Value/Description
Command Byte 3	7	**Port Selector, Bit 0** *Port Selector[1:0]* selects the Port to access. 00b = Port 0 of the Station indicated by *Station Select* 01b = Port 1 of the Station indicated by *Station Select* 10b = Port 2 of the Station indicated by *Station Select* 11b = Port 3 of the Station indicated by *Station Select* For NT Port Link Interface access, *Port Selector[1:0]* value should be 00b. For NT Port Virtual Interface access, *Port Selector[1:0]* value should be 11b.
	6	***Reserved*** Should be Cleared.
	5:2	**Byte Enables** **Bit** **Description** 2 Byte Enable for Byte 0 (PEX 8649 register bits [7:0]) 3 Byte Enable for Byte 1 (PEX 8649 register bits [15:8]) 4 Byte Enable for Byte 2 (PEX 8649 register bits [23:16]) 5 Byte Enable for Byte 3 (PEX 8649 register bits [31:24]) 0 = Corresponding PEX 8649 register byte will not be modified 1 = Corresponding PEX 8649 register byte will be modified All 16 combinations are valid values.
	1:0	**PEX 8649 Register Address, Bits [11:10]**
Command Byte 4	7:0	**PEX 8649 Register Address, Bits [9:2]** ***Note:*** *All register addresses are DWord-aligned. Therefore, Address bits [1:0] are implicitly Cleared, and then internally incremented for successive SMBus byte Writes.*

Sample Register Write Byte Sequence Using SMBus Block Write

An SMBus Block Write packet to write to the **MSI Upper Address** [63:32] register (offset 50h) in Port 17 (Port 1 of Station 4), is listed in Table 7-11. The register value is 1234_5678h, with all Bytes enabled, and without PEC. The default SMBus Device Address is 0011_011b (I2C_ADDR[2:0] are internally pulled High; therefore, ARP is disabled and the bit 2 value is 0).

Table 7-11. Sample SMBus Block Write Byte Sequence

Byte Number	Byte Type	Value	Description
1	Address	36h	Bits [7:1] for the PEX 8649 default address of 0011_011b, with bit 0 Cleared to indicate a Write.
2	Command Code	BEh	Command Code for register Write, using a Block Write.
3	Byte Count	08h	Byte Count. Four Command Bytes and Four Data Bytes.
4	Command Byte 1	03h	For Write command.
5	Command Byte 2	08h	Bits [3:1] – 100b for Station 4. Bit 0 – Port Selector MSB.
6	Command Byte 3	BCh	Bit 7 is Port Selector LSB. Bit 6 is ***reserved***. Bits [5:2] are the four Byte Enables; all are active. Bits [1:0] are register Address bits [11:10].
7	Command Byte 4	14h	PEX 8649 Register Address bits [9:2] (for offset 50h).
8	Data Byte 1	12h	Data MSB.
9	Data Byte 2	34h	Data Byte for register bits [23:16].
10	Data Byte 3	56h	Data Byte for register bits [15:8].
11	Data Byte 4	78h	Data LSB.

7.3.3.2 SMBus Block Read

A Block Read command is used to read PEX 8649 registers. Similar to register Reads using I^{2}C, an SMBus Write sequence must first be performed to select the register to read, followed by an SMBus Read of the corresponding register. There are two ways a PEX 8649 register can be read:

- Use a Block Write, followed by a Block Read. The Block Write sets up the parameters including Port Number, register address and Byte Enables, and the Block Read performs the actual Read operation.
- Use a Block Read - Block Write Process Call. This command is defined by the *SMBus v2.0*, and performs a Block Write and Block Read, using a single command. The Block Write portion of the message sets up the register to be read, and then a repeated START followed by the Block Read portion of the message returns the register data specified by the Block Write.

Note: *There is no STOP condition before the repeated START condition.*

Register Read Using SMBus Block Write, Followed by SMBus Block Read

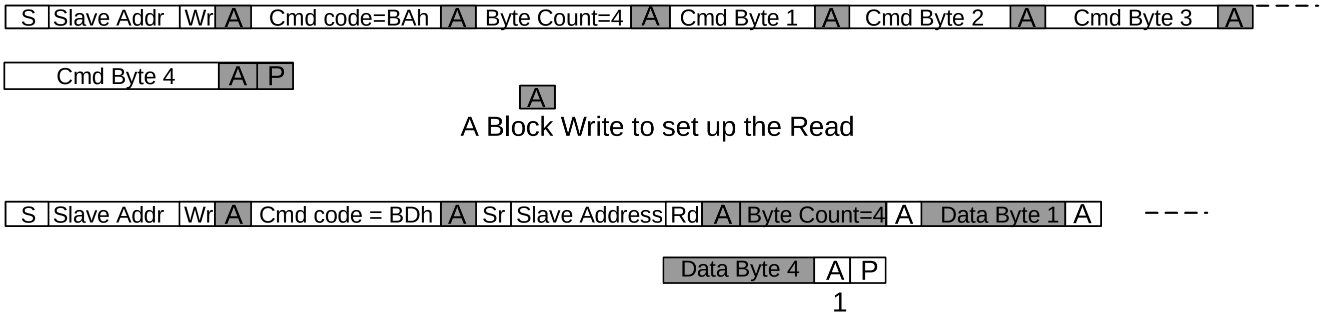
A general SMBus Block Write and Block Read sequence is illustrated in Figure 7-12.

Table 7-12 describes the Byte definitions for a Block Write bus protocol, to prepare for a subsequent Block Read of the PEX 8649 register.

The PEX 8649 always NACKs any incorrect command sequences, starting with the wrong Byte. Upon receiving the Block Read command, the PEX 8649 returns a PEC to the Master if, after the 4th byte of register data, the Master still requests one more Byte. As a Slave, the PEX 8649 recognizes the end of the Master's Read cycle, by observing the Master's NACK response for the last Data Byte transmitted by the PEX 8649.

Incorrect command sequences are always NACKed, starting with the byte that is incorrect. (Refer to Table 7-13.) On the Block Read command, a PEC is returned to the Master, if after the 4th byte of CSR data, the return Master still requests for one additional byte. As a Slave, the PEX 8649 will know the end of the Master Read cycle, by observing the NACK for the last byte read from the Master.

Figure 7-12. SMBus Block Write to Set up Read, and Resulting Read that Returns CSR Value



A Block Write to set up the Read

A Block Read, which returns the chip's CSR value

Table 7-12. SMBus Block Read Bytes

Field (Byte) On Bus	Bit(s)	Value/Description
Command Code	7:0	BAh, to set up the Read, using Block Writes.
Byte Count	7:0	04h = 4 Command bytes.
Command Byte 1	7:3	***Reserved*** Should be Cleared.
	2:0	**Command** 100b = Read register Do not use other encodings for Reads.
Command Byte 2	7:5	***Reserved*** Should be Cleared.
	4	**NT Port Link Interface Select** 0 = Should be Cleared, for accesses to: • Transparent Ports • NT PCI-to-PCI bridge downstream Port registers, in NT PCI-to-PCI Bridge mode • NT Port Virtual Interface For NT Port Virtual Interface access: – *Station Select* value should be 110b (Byte 2, bits [3:1]), and – *Port Selector[1:0]* value should be 11b (Byte 2, bit 0 and Byte 3, bit 7) 1= For NT Port Link Interface access: • *Station Select* value is Don't Care (Byte 2, bits [3:1]), and • *Port Selector[1:0]* value should be 00b (Byte 2, bit 0 and Byte 3, bit 7).
	3:1	**Station Select** 000b = Station 0 100b = Station 4 101b = Station 5 110b = NT Port Virtual Interface when bit 4 value is 0 All other encodings are ***reserved***. When the bit 4 value is 0 for NT Port Virtual Interface access, the *Station Select* value must be 110b. Value is Don't Care, when the bit 4 value is 1.
	0	**Port Selector, Bit 1**

Table 7-12. SMBus Block Read Bytes *(Cont.)*

Field (Byte) On Bus	Bit(s)	Value/Description
Command Byte 3	7	**Port Selector, Bit 0** *Port Selector[1:0]* selects the Port to access. 00b = Port 0 of the Station indicated by *Station Select* 01b = Port 1 of the Station indicated by *Station Select* 10b = Port 2 of the Station indicated by *Station Select* 11b = Port 3 of the Station indicated by *Station Select* For NT Port Link Interface access, *Port Selector[1:0]* value should be 00b. For NT Port Virtual Interface access, *Port Selector[1:0]* value should be 11b.
	6	***Reserved*** Should be Cleared.
	5:2	**Byte Enables** **Bit** **Description** 2 Byte Enable for Byte 0 (PEX 8649 register bits [7:0]) 3 Byte Enable for Byte 1 (PEX 8649 register bits [15:8]) 4 Byte Enable for Byte 2 (PEX 8649 register bits [23:16]) 5 Byte Enable for Byte 3 (PEX 8649 register bits [31:24]) 0 = Corresponding PEX 8649 register byte will not be modified 1 = Corresponding PEX 8649 register byte will be modified All 16 combinations are valid values.
	1:0	**PEX 8649 Register Address, Bits [11:10]**
Command Byte 4	7:0	**PEX 8649 Register Address, Bits [9:2]** ***Note:*** *All register addresses are DWord-aligned. Therefore, Address bits [1:0] are implicitly Cleared, and then internally incremented for successive SMBus byte Writes.*

Table 7-13. Command Format for SMBus Block Read

Field (Byte) On Bus	Bit(s)	Value/Description
Cmd Code	7:0	CDh, for Block Read (Process **C**all Rea**D**).

Sample CSR Read Byte Sequence, Using SMBus Block Write Followed by SMBus Block Read

An SMBus sequence to write and read the **MSI Upper Address** [63:32] register (offset 50h) in Port 17 (Port 1 of Station 4), is listed in Table 7-14 and Table 7-15, respectively. The register value is ABCD_EF01h, and without PEC. The Block Write sets up the Port Numbers, Register address and Byte Enables, and the Block Read performs the real Read operation. The default SMBus Device Address is 0011_011b (I2C_ADDR[2:0] are internally pulled High; therefore, ARP is disabled and the bit 2 value is 0).

Table 7-14. SMBus Block Write Portion

Byte Number	Byte Type	Value	Description
1	Address	36h	Bits [7:1] value for the PEX 8649 Slave address is 1Bh, with bit 0 Cleared to indicate a Write.
2	Block Write Command Code	BAh	Command Code for register Read setup, using a Block Write.
3	Byte Count	04h	Byte Count. Four Command Bytes.
4	Command Byte 1	04h	Write command.
5	Command Byte 2	08h	Bits [3:1] – 100b for Station 4. Bit 0 – Port Selector MSB.
6	Command Byte 3	BCh	Bit 7 is Port Selector LSB. Bit 6 is ***reserved***. Bits [5:2] are the four Byte Enables; all are active. Bits [1:0] are register Address bits [11:10].
7	Command Byte 4	14h	PEX 8649 Register Address bits [9:2] (for offset 50h).

Table 7-15. SMBus Block Read Portion

Byte Number	Byte Type	Value	Description
1	Address	36h	Bits [7:1] value for the PEX 8649 Slave address is 1Bh, with bit 0 Cleared to indicate a Write.
2	Block Read Command Code	BDh	Command code for Block Read of PEX 8649 registers.

Table 7-16. SMBus Read Command Following Repeat START from Master

Byte Number	Byte Type	Value	Description
1	Address	37h	Bits [7:1] value for the PEX 8649 Slave address is 1Bh, with bit 0 Set to indicate a Read.

Table 7-17. PEX 8649 SMBus Return Bytes

Byte Number	Byte Type	Value	Description
1	Byte Count	04h	Four Bytes in register.
2	Data Byte 1	ABh	Register data MSB.
3	Data Byte 2	CDh	Register data [23:16].
4	Data Byte 3	EFh	Register data [15:8].
5	Data Byte 4	01h	Register data LSB.

7.3.3.3 CSR Read, Using SMBus Block Read - Block Write Process Call

A general SMBus Block Read - Block Write Process Call sequence is illustrated in Figure 7-13. Alternatively, a general SMBus Block Read - Block Write Process Call with PEC sequence is illustrated in Figure 7-14.

Using this command, the register to be read can be set up and read back with one SMBus cycle (a transaction with a START and ending in STOP). There is no STOP condition before the repeated START condition. The command format for the Block Write part of this command has the same sequence as in Table 7-14, except that the Command Code changes to CDh, as illustrated below. Other Bytes remain the same as used in the sequence for SMBus Block Write followed by Block Read.

Table 7-18 lists the Command format for Block Read.

Figure 7-13. CSR Read Operation Using SMBus Block Read - Block Write Process Call

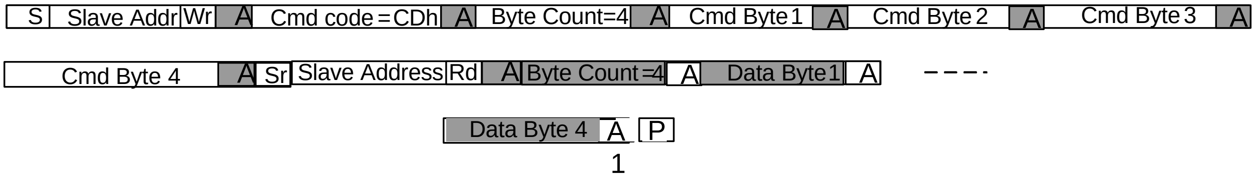


Figure 7-14. CSR Read Operation Using SMBus Block Read - Block Write Process Call with PEC

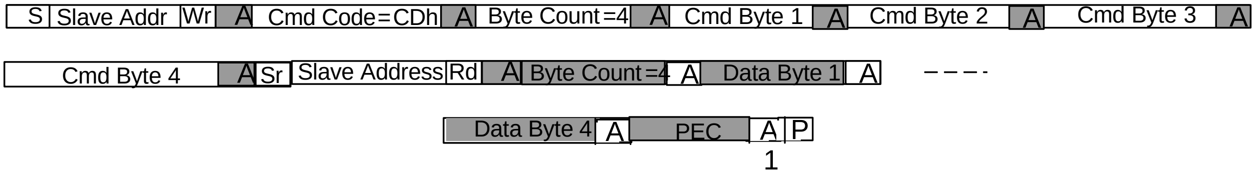


Table 7-18. Command Code for SMBus Block Read

Field (Byte) On Bus	Bit(s)	Value/Description
Cmd Code	7:0	CDh, for Block Read (Process **C**all Rea**D**).

7.3.4 SMBus Address Resolution Protocol

Address Resolution Protocol (ARP) is a protocol by which SMBus devices that implement an assignable Slave address feature are enumerated and dynamically assigned non-conflicting Slave addresses, rather than using a fixed Slave address. Although optional in the *SMBus v2.0*, it is mandatory per the *PCI r3.0* for add-in boards, to support ARP. This feature avoids conflicts with addresses used by other devices on a motherboard. ARP also allows multiple devices of the same type to co-exist on the same bus segment, without address conflicts.

To support this feature, a Slave device must implement a unique 128-bit ID, called *Unique Device Identifier (UDID)*. The fields of this ID are provided in Figure 7-15. All ARP commands use the default Device Address, 1100_001b. There are also two flags that the SMBus devices must implement to support the ARP process:

- **Address Resolved flag (AR)** – A flag bit or device internal state that indicates whether the device’s Slave address has been resolved by the ARP Master
- **Address Valid flag (AV)** – A flag bit or device internal state that indicates whether the device’s Slave address is valid

The process of assigning a Slave address starts with the ARP Master issuing a Reset Device or Prepare to ARP command, using the default Device Address. This Clears the AR flag in the Slave device (both flags are Cleared by a Reset Device command). The Master then issues a general Get UDID command. This causes all devices that support ARP to start driving their UDID onto the serial bus. A Target that loses the SMBus arbitration, backs off. Arbitration loss means that a device keeps the SMDAT line floating and it detects 0 driven by another device on the bus. Slave devices that lose arbitration issue NACK in response to further Bytes transmitted on the bus. After the ARP Master finishes the Get UDID sequence, it issues a Set Address command to the Slave device, using the Slave’s UDID. All Slave devices on the bus monitor the UDID that is transmitted by the ARP Master, but only the particular device that has the matching UDID adopts the new Slave address, and Sets its own AV and AR flags. After the Slave device sets its AR flag, that device no longer responds to a general Get UDID command, which allows other devices to participate in the ARP process. All ARP commands require PEC checking and generation.

7.3.4.1 SMBus UDID

The 128-bit UDID is comprised of the following fields, as illustrated in Figure 7-15 (not to scale). Each UDID field and its default value implemented in the PEX 8649 and meaning are explained in the tables that follow.

Figure 7-15. 128-Bit SMBus UDID

8 bits	8 bits	16 bits	16 bits	16 bits	16 bits	16 bits	32 bits
127:120	119:112	111:96	95:80	79:64	63:48	47:32	31:0
Device Capability	Version/ Revision	Vendor ID	Device ID	Interface	Subsystem Vendor ID	Subsystem Device ID	Vendor-Specific ID

Table 7-19. SMBus Device Capability [127:120]

Field	Name	Default Value	Description
0	PEC Supported	1	By default, PEC generation and checking are enabled.
5:1	***Reserved***	00_000b	
7:6	Address Type	10b	Defaults to 10b. The PEX 8649 SMBus Address Type is implemented as Dynamic and volatile. 00b = Fixed address 01b = Dynamic and persistent 10b = Dynamic and volatile 11b = Random number device

Table 7-20. SMBus Version/Revision [119:112]

Field	Name	Default Value	Description
2:0	Silicon Revision ID	001b	PEX 8649, Silicon Revision AA.
5:3	UDID Version	001b	UDID version defined for *SMBus v2.0*.
7:6	***Reserved***	00b	

Table 7-21. SMBus Vendor ID [111:96]

Field	Name	Default Value	Description
15:0	Vendor ID	10B5h	PLX Vendor ID.

Table 7-22. SMBus Device ID [95:80]

Field	Name	Default Value	Description
15:0	Device ID	8649h	PEX 8649 default Device ID value.

Table 7-23. SMBus Interface [79:64]

Field	Name	Default Value	Description
3:0	SMBus Version	0100b	*SMBus v2.0*.
15:4	***Reserved***	000h	Supported protocols.

Table 7-24. SMBus Subsystem Vendor ID [63:48]

Field	Name	Default Value	Description
15:0	Subsystem Vendor ID	10B5h	PLX Vendor ID.

Table 7-25. SMBus Subsystem Device ID [47:32]

Field	Name	Default Value	Description
15:0	Subsystem Device ID	8649h	PLX part number for the PEX 8649.

Table 7-26. SMBus Vendor-Specific ID [31:0]

Field	Name	Default Value	Description
31:0	Vendor-Specific ID	Depends upon I2C_ADDR[1:0] input settings. The four combinations provide the following ID values: 00b = 7000_0000h 01b = B000_0000h 10b = D000_0000h 11b = E000_0000h	The Vendor-Specific ID is used to provide a unique ID for functionally equivalent devices. This is for devices that would otherwise return identical UDIDs for the purpose of dynamic address assignment. The combination of two Address bits produces four unique Vendor-Specific ID values, for a maximum of four SMBus-enabled PEX 8649s to co-exist on the same SMBus segment.

7.3.4.2 SMBus Supported ARP Commands

The PEX 8649 supports all ARP Slave commands. The Notify ARP Master command, which requires Master functionality, is ***not*** supported. Table 7-27 explains the PEX 8649 response to each received ARP command.

Table 7-27. SMBus Supported ARP Commands, Format, and Actions

ARP Command	SMBus Command Format	Slave Address	Command Code	Action
Prepare to ARP (Only General)	Send Byte (Refer to Figure 7-16)	SMBus default Device Address 1100_001b	01h	Clear the *AR Flag* and prepare for the ARP process. *AV Flag* will have no change.
Reset Device (General)	Send Byte (Refer to Figure 7-16)	SMBus default Device Address 1100_001b	02h	Clear the *AR Flag* and *AV Flag*.
Reset Device (Directed)	Send Byte (Refer to Figure 7-16)	SMBus default Device Address 1100_001b	Target Device Address[7:1] + 0	If the *AV Flag* is Set, Set ACK and Clear the *AR Flag* and *AV Flag*; else, NACK/REJECT.
Get UDID (General)	Block Read (Refer to Figure 7-17)	SMBus default Device Address 1100_001b	03h	Respond only if the *AR Flag* is Cleared; else, NACK/REJECT. *AR Flag* and *AV Flag* are not changed. Address returned is all ones (1), if the *AV Flag* is Cleared.
Get UDID (Directed)	Block Read	SMBus default Device Address 1100_001b	Target Device Address[7:1] + 1	*AR Flag* and *AV Flag* are not changed. ACK if *AV Flag*=1; else, NACK/REJECT. Data Byte 17 returned will be the SMBus Slave address.
Assign Address ARP	Block Write (Refer to Figure 7-18)	SMBus default Device Address 1100_001b	04h	Always ACK and Set the *AR Flag* and *AV Flag*, if the UDID matches.

Figure 7-16. Prepare SMBus ARP Command and SMBus Reset Device Command Format

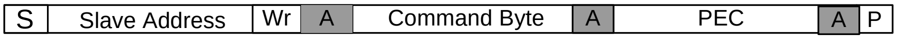
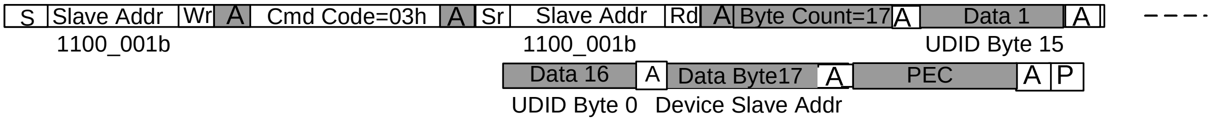
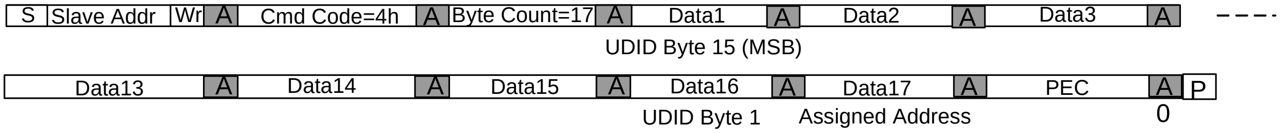


Figure 7-17. Get SMBus UDID Command Format (General Get UDID Command with PEC)



Note: *If the* ***SMBus Configuration*** *register AR Flag bit (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 2C8h[11]) is Cleared, the device returns the Slave Address field as 1111_111b; otherwise, it returns the device Slave address. Bit 0 (LSB) in the Data Byte 17 field should be 1.*

Figure 7-18. Assign SMBus Address ARP Command Format



Note: *Bit 0 (LSB) of the Data 17 field is ignored in the Assign Address command field.*

7.3.5 SMBus PEC Handling

The PEX 8649 supports the optional *SMBus v2.0* PEC generation and checking feature. This feature is required for the ARP process; however, it is optional for standard data transfer operation. The PEX 8649 supports PEC Cyclic Redundancy Check (CRC) generation and checking during ARP, as well as during Read/Write transfers to the PEX 8649 registers. The CRC polynomial used for PEC calculation is:

$$C(x) = x^8 + x^2 + x + 1$$

An 8-bit parallel CRC is implemented. The PEC calculation does not include ACK, NACK, START, STOP, nor repeated START bits. An SMBus Master can determine whether a Slave device supports PEC, from the UDID value returned by the Slave device, in response to a Get UDID command.

As a Slave device, the PEX 8649 checks the PEC, if the Master transmits the additional PEC byte and the PEX 8649 PEC checking feature is enabled (default). PEC checking can be disabled, by Setting the **SMBus Configuration** register *PEC Check Disable* bit (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 2C8h[9]).

Additionally, when PEC is enabled, packets received with an incorrect PEC value are dropped. If PEC checking is disabled and a received PEC byte value is incorrect, the PEX 8649 accepts the packet. During a register Read, if the Master requests the additional PEC byte, the PEX 8649 generates and transmits the PEC byte after the register data.

7.3.6 Addressing PEX 8649 SMBus Slave

By default, the PEX 8649 supports ARP when the I2C_ADDR2 input is tied Low, and expects the ARP Master to Set the PEX 8649 SMBus Device Address. If ARP is disabled by I2C_ADDR2 input being pulled High, the default address is 1Bh (Address bits [7:1] are 0011_011b, with Address bit [1:0] values loaded from the I2C_ADDR[1:0] inputs). The two Address bits allow a maximum of four PEX 8649 SMBus Slaves to co-exist without address conflict on the SMBus, using SMBus Address byte values of 30h, 32h, 34h, and 36h. The I2C_ADDR[2:0] inputs are loaded immediately after Fundamental Reset, and any subsequent change of input value does not affect functionality.

If the **SMBus Configuration** register *UDID Address Type* field is programmed as Fixed Address (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 2C8h[13:12], are both Cleared) without disabling ARP, the PEX 8649 still participates in ARP, but does not Set the Device Address after ARP successfully completes.

The SMBus Slave Address can be changed at any time, by software writing to the register's *SMBus Device Address* field (offset 2C8h[7:1]). ARP can also be enabled or disabled at runtime, by writing to the register's *ARP Disable* bit (offset 2C8h[8]). If ARP is disabled by software after initially being enabled, the default address (36h) is not used for subsequent transactions. In this case, software must program a Slave address into the *SMBus Device Address* field. When software writes the Device Address, it must also Set the register's *AR Flag* and *AV Flag* bits (offset 2C8h[11:10], respectively), to indicate that the address is valid and resolved.

Whenever software changes the register's *AV Flag*, *ARP Disable*, and/or *SMBus Device Address* values, software must also Set the register's *SMBus Parameter Reload* bit (offset 2C8h[15]). Writes to this register bit take effect only when the register's *SMBus Command In-Progress* bit (offset 2C8h[28]) is Cleared, which indicates that the PEX 8649 SMBus interface is in the Idle state.

7.3.7 SMBus Timeout

Unlike I^{2}C, where the Slave or Master can indefinitely hold the I2C_SCL0 line Low, SMBus has a timeout condition. No device is allowed to hold the I2C_SCL0 line Low for more than 25 ms. When the PEX 8649, as a Slave-Transmitter, detects that it has pulled I2C_SCL0 line Low for more than 25 ms, the PEX 8649 releases I2C_SCL0, and the logic returns to its default state and waits for another START condition. This can also occur when the Master pulls the I2C_SCL0 line Low for more than 25 ms during any single Clock Low interval within a transfer in progress, or during the ACK phase, if the Master pulls the I2C_SCL0 line Low to process a task. Generally, the PEX 8649 pulls I2C_SCL0 line Low if SMBus access to registers is delayed by internal arbitration for register access.

7.4 Switching between SMBus and I^{2}C Bus Protocols

The PEX 8649's I^{2}C implementation allows switching between the SMBus and I^{2}C protocols, by toggling the **SMBus Configuration** register *SMBus Enable* bit (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 2C8h[0]).

When operating in SMBus mode, Clearing this bit, using the SMBus Block Write protocol, enables I^{2}C protocol for subsequent register accesses. This SMBus Block Write can be transmitted from an SMBus and/or I^{2}C Master, provided that the Block Write Byte sequence conforms to the sequence explained in Section 7.3.3.1. In I^{2}C mode, writing 1 to the *SMBus Enable* bit turns On the SMBus protocol, immediately after the Write operation is complete.

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Chapter 8 Performance Features

8.1 Introduction

This chapter discusses guidelines for programming on-chip registers, to boost performance beyond that provided by the general-purpose default values, specifically:

- DLLP Policies
- Latency
- Queuing Options
- Read Pacing
- Multicast – All Modes Except Legacy NT

8.2 DLLP Policies

Data Link Layer Packet (DLLP) rates can vary from 0 to 2 or more DLLPs/TLP. The PEX 8649 allows programming to affect the DLLP rate. An increase in DLLPs reduces the total TLP throughput. Therefore, for designs that require high performance, it would be beneficial to minimize DLLP rates. Transmitting fewer DLLPs, however, can result in credit starvation or Replay buffer overfill, which can have a detrimental effect on TLP bandwidth. Care must be taken when changing the default PEX 8649 DLLP transmission rate.

Typically, TLPs have higher transmission priority on the wire than DLLPs. The PEX 8649, however, allows DLLPs to have higher priority under certain conditions, meaning that DLLPs can transmit before starting a new TLP. The decision to transmit a DLLP ahead of a TLP is referred to as *DLLP policy.*

The PEX 8649 can be programmed to alter its default DLLP policies, to emphasize improved TLP throughput, faster acknowledgement, more credit, or simplest behavior. The PEX 8649 default policies are designed to achieve optimal performance for most applications. Programmable choices for a DLLP policy, however, allow for further optimization.

8.2.1 ACK DLLP Policy

An *ACK DLLP* is a response indicating to the TLP Transmitter that the Receiver received a “good” copy of the TLP, meaning that it acknowledged receipt of the TLP. The simplest policy is to send 1 Acknowledge Control Packet (ACK) for every received TLP, resulting in a 1 DLLP/TLP rate for ACK alone. What an ACK means to the TLP Transmitter is that the TLP Transmitter can remove any stored copy of that TLP, because it is unnecessary to resend the TLP. ACK DLLPs can be combined, so that one ACK DLLP can serve to acknowledge multiple TLPs. This collapsing of ACKs is the basis of the ACK DLLP policy choices. Less-frequent, more-collapsed ACKs have the least impact on TLP transmit bandwidth, meaning that less-frequent ACKs result in less than 1 DLLP/TLP.

The PEX 8649 ACK policy consists of two parts – a Timer and TLP Counter. The default ACK Timer policy/value varies according to the negotiated Link width, operating Link speed, and Maximum Packet Size, as recommended in the *PCI Express Base r1.1* or *PCI Express Base r2.0*.

The ACK Transmission Latency Timer loads the appropriate value when a TLP is received and known to be good, meaning a few clocks after the END framing symbol is received. The Timer counts down each symbol time (every 4 ns (*PCI Express Base r1.1*) or 2 ns (*PCI Express Base r2.0*)). When the Timer reaches 0, an ACK DLLP takes higher priority over new TLPs (*that is*, an ACK DLLP is transmitted before a new TLP is started). The ACK DLLP transmitted acknowledges all TLPs, up to the most recently arrived good TLP.

The TLP Counter counts down on each TLP arrival until it reaches 0, then schedules a high-priority ACK DLLP. The default initialization value for the TLP Counter is 16, meaning a high-priority ACK is scheduled upon the arrival of 16 TLPs. The **Ingress Port-Based Control** register *ACK TLP Counter Timeout* field (Base mode – All Ports; Virtual Switch mode – VS Upstream Port(s), offset F48h[1:0]) value controls the ACK TLP Counter, as follows:

- 00b – Allows 16 TLPs before a high-priority ACK (default)
- 01b – Allows 8 TLPs before a high-priority ACK
- 10b – Allows 4 TLPs before a high-priority ACK
- 11b – Disables the Counter

Either the Latency Timer or TLP Counter mechanism can cause a high-priority ACK DLLP to be scheduled, and the first one to do so re-initializes both mechanisms to their starting parameters. *For example*, the time for 16 TLPs can be less than the ACK Timer above, in which case an ACK is sent earlier. The TLP Counter is useful for any system with a large programmed MPS (resulting in a large Timer value), that is capable of sending short TLPs (*such as* 12-byte Memory Reads). Rather than require the Transmitter to save possibly 100+ small TLPs, it need only save 16, plus whatever else arrives during the round-trip time.

If there is no TLP traffic being transmitted (*that is*, the Transmit Link is idle), an ACK DLLP can be transmitted immediately, before the Latency Timer expires. This is an opportunistic, low-priority ACK because it does not contend with a TLP in transmission. When an opportunistic, low-priority ACK is transmitted, both the Latency Timer and TLP Counter re-initialize, waiting for a new TLP to arrive to begin counting again.

The PEX 8649 allows a programmable override of the default Ack_Latency_Timer value, on a per-Port basis, by programming the **ACK Transmission Latency Limit** register *ACK Transmission Latency Limit* field (offset FA8h[11:0]). The value in this register is loaded when a new TLP arrives and a high-priority ACK DLLP is attempted when the Timer reaches 0. For fastest ACK response, this Timer can be programmed to 000h, resulting in one DLLP ACK transmitted immediately per each TLP received. For less impact on Transmit TLP bandwidth, a larger value can be programmed, resulting in less-frequent ACKs.

In general, a slower ACK response does not impact the Receive TLP stream, and aids the TLP Transmit stream. Every PCI Express device contains storage (Retry buffer) for storing TLPs while waiting for ACKs. The amount of Retry buffer storage a device contains is vendor-dependent. The number of TLPs the PEX 8649 can store depends upon the type and size of TLPs received. The PEX 8649 holds TLPs in the Retry buffer while waiting for an ACK. At some point, if the Retry buffer storage fills, no new TLPs can be sent until a new received ACK frees up space. In this case, the ACK can become a performance bottleneck.

8.2.2 UpdateFC DLLP Policy

An *UpdateFC DLLP* is transmitted in response to a received TLP. The UpdateFC DLLP replenishes the connected device with additional credit, to allow the Transmitter to transmit more TLPs of that type. Each TLP that arrives consumes credit, and eventually, a stream of TLPs consume all the available credit, unless an UpdateFC DLLP provides additional credit. However, if the connected device has sufficient credit to transmit more TLPs, it is not necessary to transmit UpdateFC DLLPs to it. The UpdateFC policy determines how and when to transmit an UpdateFC DLLP.

There are two parts to the UpdateFC policy – frequency of transmitting the updates and credit amount. This section discusses only the frequency.

If the PEX 8649 is not transmitting TLPs (*that is*, the Transmit Link is idle), and credit to replenish the credit used becomes available, the PEX 8649 immediately transmits an UpdateFC DLLP to the connected device. This is an opportunistic, low-priority UpdateFC DLLP.

However, if the PEX 8649 is busy transmitting TLPs to the connected device, the PEX 8649 does not transmit an UpdateFC DLLP until a programmed threshold is crossed. The PEX 8649 provides four threshold options – 100%, 75% (default), 50%, and 25%. Whenever the remaining credit drops below the programmed threshold, an UpdateFC DLLP is given high priority, meaning that the UpdateFC DLLP is transmitted before a new TLP is started. There is a separate threshold for Header and Payload credits, for each TLP type – Posted, Non-Posted, and Completion – located in the **Ingress Credit Handler (INCH) Threshold** registers (Base mode – All Ports; Virtual Switch mode – Port 0, accessible through the Management Port, offsets A00h through A08h).

8.2.3 Unidirectional DLLP Policies

For unidirectional traffic, the PEX 8649 DLLP policies allow the most-frequent DLLPs, because DLLPs do not interfere with TLPs. (DLLPs flow in the opposite direction of TLPs.)

The PEX 8649 can transmit a DLLP ACK almost immediately upon receiving and verifying a TLP. A faster ACK results in fast Transmitter de-allocation of the TLP, and can therefore allow a shallow TLP Replay buffer. The default values can be overwritten, to increase or decrease the ACK DLLP rate. For unidirectional traffic, a small number, *such as* 1, is recommended.

The number programmed into the **ACK Transmission Latency Limit** register *ACK Transmission Latency Limit* field (offset FA8h[11:0]) Sets the ACK Transmission Latency Timer, to count the number of symbol times after receiving a TLP, before transmitting an ACK.

Similar to the ACK programmability, the PEX 8649 can immediately transmit an UpdateFC after receiving only the TLP Header. By transmitting an UpdateFC earlier, the total credit advertised can be minimized. By programming fewer credits and having a fast UpdateFC policy, the system does not run out of credits and the PEX 8649 does not waste Buffer space on reservations that do not arrive. The following are the recommended settings:

- Set the UpdateFC policy for unidirectional traffic to 100%
- Set the credits to be sufficient to allow 3 to 4 TLPs

8.3 Latency

Latency is the length of time it takes to proceed from one event to another. Latency can be measured in several different ways, but perhaps the most common measurement for a switch is *Start TLP-to-Start TLP (STP-to-STP) latency*. Figure 8-1 illustrates an STP-to-STP Latency Measurement. When the Egress Start TLP symbol is transmitted out of a switch before the Ingress Port End symbol arrives, the transfer is termed *Cut-Thru*. If there is no Egress Port queue established, the PEX 8649 always cuts the packet through. The PEX 8649 has the same latency, regardless of whether the traffic is upstream or peer-to-peer.

As expected with the PEX 8649 Cut-Thru architecture, STP-to-STP latency is basically constant for all Payload sizes. A faster Link can receive the Header for decode faster, with a slightly lower latency. There will generally be a constant latency for any ingress width to the same egress width, or any ingress width to a smaller egress width, operating at the same Link speed.

For cases in which the egress Port has a higher bandwidth than the ingress Port, then a fraction of the packet, given by the following formula:

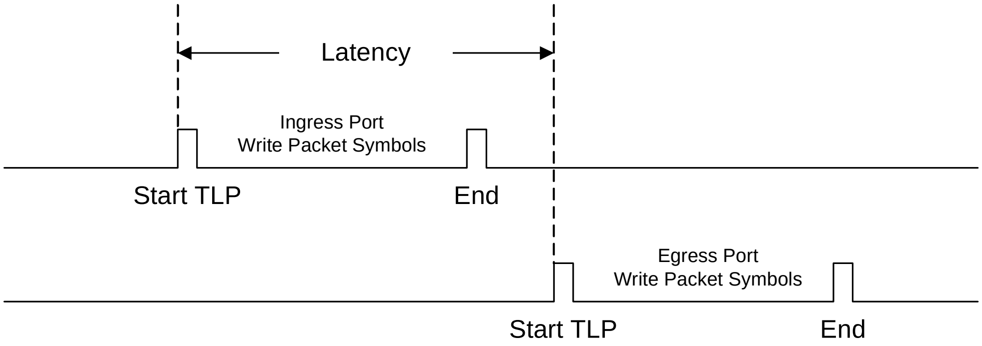
$$F = (E-I) / E$$

must be buffered (to prevent under-run in the middle of the TLP), before the TLP can be forwarded to the egress Link.

where

- *F* is the fraction sum
- *E* is egress bandwidth
- *I* is ingress bandwidth

Figure 8-1. Start TLP-to-Start TLP Latency Measurement



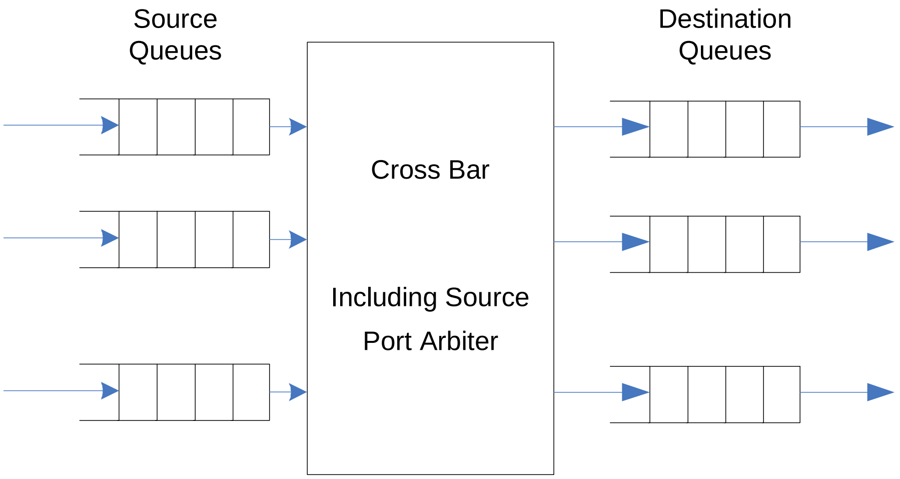
8.4 Queuing Options

On-chip queuing does not exist in balanced bandwidth scenarios, where the total ingress bandwidth is less than or equal to the egress bandwidth. In the common case, where the total ingress bandwidth is greater than the egress bandwidth, queues develop on the PEX 8649. The PEX 8649 provides two alternatives, as to where to locate such queuing (refer to Figure 8-2):

- **Destination queue** – Associated with a single Destination Port. All the TLPs in a Destination queue will egress out the same Port.
- **Source queue** – Associated with a single ingress Port. All the TLPs in a Source queue come from the same Port.

Each queue is discussed in the sections that follow.

Figure 8-2. On-Chip Queuing



8.4.1 Destination Queuing

Note: *For the queuing examples provided in this section, "Port 1" indicates "first Port," not the Port physically identified as Port 1.*

The default behavior is for all queues to develop at the Destination Port. If TLPs are arriving from four sources to a common Destination Port, the TLPs are scheduled according to First-In, First-Out (FIFO). The crossbar can forward a TLP every 4 ns, to each Destination queue; therefore, it is unlikely that a Source queue can develop or last very long.

A Destination queue develops whenever the *ingress rate* – the sum of all ingress Ports targeting a Destination Port – exceeds the egress rate. A Destination queue might also develop in a credit-starved situation, where there is no credit available to forward TLPs.

For example, if TLPs arriving from four sources all go to a common Destination Port, the TLPs are scheduled, based upon the order in which they arrive at the Destination queue FIFO[a]. If all four flows are equally active, the TLPs naturally interleave as 1,2,3,4,1,2,3,4. If three of the Ports, however, have a head start before the fourth Port turns on, the output can be 1,2,3,1,2,3,1,2,3,1,2,3,1,2,3,4,1,2,3,4. In this case, all the new Port (Port 4) TLPs must wait for the earlier Port 1,2,3 traffic to be transferred before the Port 4 TLPs can be transferred. Therefore, the latency for Port 4 traffic to travel through the PEX 8649 can widely vary, based upon the traffic passing through the switch.

[a] *Conventional PCI Strong Ordering rules can override the FIFO. Conventional PCI requires Posted TLPs to be able to pass Non-Posted and Completion TLPs, to avoid deadlock.*

8.4.2 Source Queuing

Caution: ***Source Queuing and Read Pacing should not be concurrently enabled. The two features are incompatible and doing so can result in Fatal errors.***

Note: *For the queuing examples provided in this section, "Port 1" indicates "first Port," not the Port physically identified as Port 1.*

Source queuing can be enabled for applications that require deterministic bounded latency for a few Ports, while the latency for other Ports is not as important.

Source queuing limits the Destination queue depth. When the Destination queue reaches the maximum depth, any subsequent TLPs targeting that Port are not forwarded, but are queued up in a per-Source Port-based queue. The Source Port queue does not forward TLPs until the Destination queue drops to a programmed threshold, upon which TLP forwarding is re-enabled.

Note: *A Source Port queue that cannot forward to a Destination queue blocks all subsequent TLPs arriving on that same Source Port, although the target Port is a different destination.*

The **Port Egress TLP Threshold** register (offset F38h) controls the minimum and maximum queue depths. Table 8-1 summarizes the register bit settings. The Port Lower TLP Counter is the number of TLPs to which the Destination queue must reach after becoming saturated, before re-enabling TLP forwarding. The Port Upper TLP Counter is the number of TLPs that can be queued in the Destination queue.

In the Destination queue example provided in Section 8.4.1, the early arriving Port 1,2,3 TLPs stalled Port 4's TLP for an indeterminate length of time. By programming, with source queuing enabled and a destination Port Lower TLP Counter programmed to 1 and Port Upper TLP Counter programmed to 3 (TLPs), the worst case is that Port 4 must wait for three TLPs (1,2,3) before getting its first turn. With these settings, the example TLP output would be 1,2,3,4,1,2,3,4,1,2,3,4. The *turn to be forwarded* refers to a Port Arbitration wait, described in Section 8.4.3.

For the PEX 8649, to avoid unnecessary idles on the destination Link, program a Port Lower TLP Counter of 1, and a Port Upper TLP Counter of 2.

Table 8-1. Port Egress TLP Threshold Register Port Lower and Upper TLP Counters (Offset F38h)

Bit(s)[a]	Name	Description
11:0	**Port Lower TLP Counter**	When Source Scheduling is disabled due to Threshold, it is re-enabled when the Port TLP Counter goes below this Threshold value.
27:16	**Port Upper TLP Counter**	When the Port TLP Counter is greater than or equal to this value, the Source Scheduler disables TLP scheduling to this egress Port.

[a] *Bits not identified in Table 8-1 are* ***reserved****.*

8.4.3 Port Arbitration

In the crossbar that connects the Source queues to the Destination queues, there is a Port Arbiter for each Destination Port. The Port Arbiter ensures that each Source Port receives a deterministic bandwidth connecting to a Destination Port. The Port Arbiter ensures that each Source Port receives a deterministic bandwidth connecting to a Destination Port.

In addition to the default fixed Round-Robin Port Arbiter, there is one Device-Specific Weighted Round-Robin (WRR) Port arbitration hardware resource that can enabled by system software. The Device-Specific WRR arbitration is also Round-Robin, but with programmable weighting for a particular Port or Ports.

System software discovers the Port Arbitration Capability, as reflected in the **VC0 Resource Capability** register (offset 158h[2:0]). If the system software needs to make use of an advertised WRR arbitration with 64-phase capability for a Port, it programs the Port's **VC0 Resource Control** register *Port Arbitration Select* field (offset 15Ch[19:17]) to 001b.

The WRR Source Port Arbiter has a 64-phase Port Arbitration Table, as outlined in the *PCI Express Base r2.0*, and documented in the **Port Arbitration Table Phase *x*** registers (offsets 178h through 1B4h). (Refer to the *PCI Express Base r2.0*, as well as Section 13.14.1, "WRR Port Arbitration Table Registers (Offsets 178h – 1BCh)," for further details.)

Once one or more Phase registers are written, the software writes the Port's **VC0 Resource Control** register *Load Port Arbitration Table* bit (offset 15Ch[16]). When written, the register values are transferred to the WRR arbitration logic, and immediately take effect.

Port arbitration makes decisions on a per-TLP basis. A Port with more short TLPs will appear to receive less bandwidth, compared to a Port with fewer long TLPs, if both Ports have the same weight and both target a congested Port.

8.4.4 Port Bandwidth Allocation

For applications that need to allocate a fixed bandwidth to each Port, the PEX 8649 can help enforce the relative bandwidth ratio between Ports in a congested scenario.

By combining source queuing, Port Arbitration, and initial credit, as well as some knowledge of average Payload size, many combinations of Port bandwidth allocation are possible.

8.5 Read Pacing

Caution: ***Source Queuing and Read Pacing should not be concurrently enabled. The two features are incompatible and doing so can result in Fatal errors.***

The Read Pacing feature is supported on all Ports. The Read Pacing Configuration registers, however, are implemented in only one Port per Station. (Refer to Table 13-20 in Section 13.15.1, “Device-Specific Registers – Read Pacing (Offsets 1D0h – 1D8h),” for details.)

PCI Express has a weakness concerning the number of outstanding bytes requested by Reads. It is possible that a single device can overwhelm the system with a reasonable number of large Read Requests, thereby impacting the performance of other connected devices, by filling the ingress transaction queue in the Root Complex.

The Root Complex must handle the transactions in the order in which they are posted. Transactions posted from less aggressive reading devices, which may be more sensitive to latency, suffer performance reductions due to the unfairly weighted path (head of line blocking) in the transaction queue that the large reads represent.

Read Pacing attempts to apply some rules to Memory Read Requests, so that no one Port can overwhelm a system. There are two aspects to the PEX 8649’s Read Pacing capability:

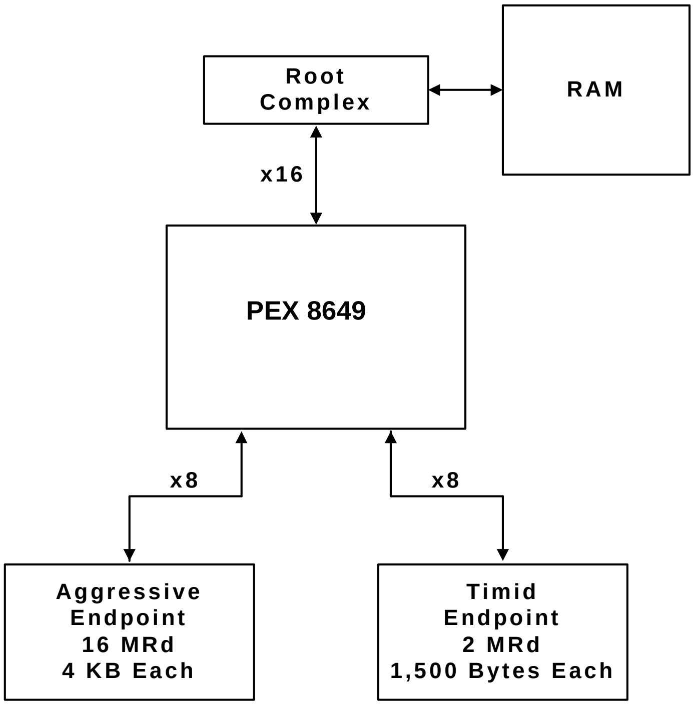
- Read spacing
- Read threshold

The following sections provide examples and further information regarding Read Pacing.

8.5.1 Read Pacing Example

Figure 8-3 illustrates an example of a system that benefits from Read Pacing.

Figure 8-3. Read Pacing Example


Root Complex
RAM
x16
PEX 8649
x8
x8
Aggressive Endpoint 16 MRd 4 KB Each
Timid Endpoint 2 MRd 1,500 Bytes Each

In a typical Host-centric application, endpoints have Direct Memory Access (DMA) engines that write to and read from Main memory. A performance bottleneck can occur during the Read to Main memory, through the Root Complex. For the example illustrated in Figure 8-3, the aggressive endpoint sends many large (16, 4-KB) Memory Read Requests, while another endpoint, or Timid Endpoint (TEP), sends only two 1,500-byte Memory Read Requests. The TEP then waits for a response before sending additional Read requests[a].

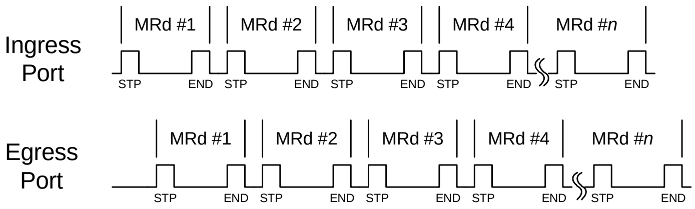
If either endpoint is running by itself, neither sees a problem. However, if both endpoints are concurrently active, the aggressive endpoint dominates the Root Complex Memory Controller. In addition, due to the bandwidth mismatch, Completions can queue up in the PEX 8649, creating too many Completions for the switch to store at one time. As a result, the PEX 8649 backpressures the Root Complex for Completions. The Root Complex can only forward Completions to the PEX 8649 at the aggressive endpoint's rate, which is significantly less than the Root Complex could otherwise handle.

The net impact is not to the aggressive endpoint, because there are a sufficient number of Completions queued up in the PEX 8649 to keep it busy. In fact, the aggressive endpoint experiences better performance with a switch, than connected directly to the Root Complex[b]. Rather, the TEP experiences lower performance results. Its Memory Read Requests wait in line behind multiple aggressive endpoint Requests, and the Root Complex can drain Requests only at the same rate of the PEX 8649, not at the upstream Link's capacity.

Figure 8-4 illustrates how a PCI Express switch, without Read Pacing, forwards Memory Read Requests (MRds).

Read Pacing solves the performance loss seen by the TEP, while improving the aggressive endpoint's performance. The following sections provide examples of the way in which the PEX 8649 functions when Read Pacing is enabled, and Read Spreading is enabled or disabled.

Figure 8-4. Read Pacing Off (Disabled)



[a] *This is based upon an actual setup in a third-party lab. Fibre Channel endpoints can easily send 16, 4-KB MRd at a time, while Gigabit Ethernet endpoints might send only one or two 1,500-byte endpoints at a time.*

[b] *Without a switch, when the Root Complex has something else to do, the aggressive endpoint loses its data stream. With a switch, the buffering of multiple Completions hides the fact that the Root Complex is multitasking.*

8.5.2 Read Spacing (Spreading) Logic

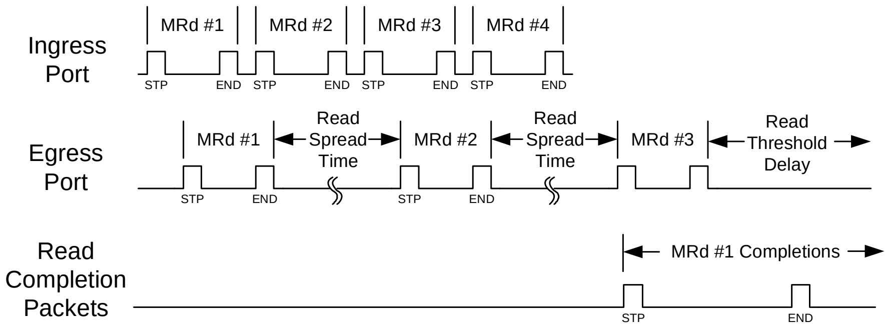
Read Spacing (also referred to as *Read Spreading*) spreads out Read requests. The PEX 8649 Read Spacing logic looks at the Read Request size and the endpoint's bandwidth, to determine how often to forward subsequent Read Requests. *For example*, Read Requests arriving on a x4 Link can only sink data at a x4 rate. If a x4 endpoint submits multiple Read Requests to a x8 Link, the Read Spacing logic does not forward the subsequent Read Requests until the endpoint has sufficient time to sink a portion of the Completion data from the previous Read Requests.

Initially, a queue of Completions must build up to hide the time that it takes for the data to return. As a result, Reads are forwarded at 2x the endpoint's bandwidth. This 2x rate is maintained until a threshold of outstanding Read data is reached, at which time Reads are forwarded at 1x the endpoint's bandwidth.

Read Pacing must be enabled for Read Spreading to be enabled. *That is*, for a Port to have Read Spreading enabled, the Port's *Port x Read Pacing Disable* and *Port x Memory Read Spread Disable* bits (offset 1D0h[3:0 and 19:16], respectively) must both be Cleared.

Figure 8-5 illustrates the way in which the PEX 8649 forwards Read requests when the **Read Pacing Control** register Read Pacing- and Read Spreading-related bits are enabled. (Refer to Section 8.5.5 for additional register/bit information.) The PEX 8649 continues to spread and forward the Read Requests, until the amount of Completion data for which it is waiting exceeds the value programmed in the **Read Pacing Threshold *x*** register for that Link width (offsets 1D4h and 1D8h).

Figure 8-5. Read Pacing On (Enabled) and Read Spreading On (Enabled)

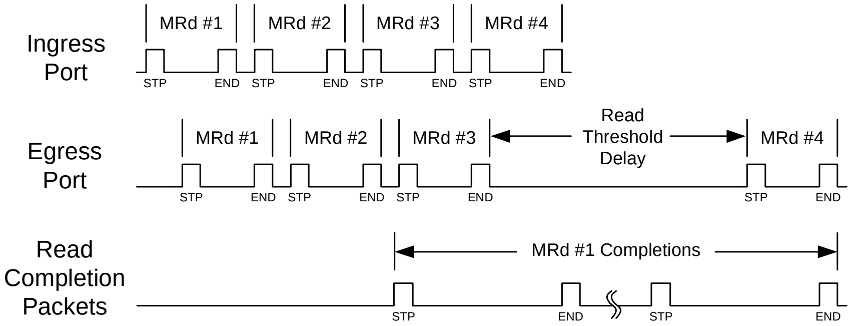


8.5.3 Read Threshold

The Read threshold is the maximum number of outstanding DWords (1 DWord = 4 bytes) that the endpoiNT Port requested to be read, but were not yet returned as Completion data. The threshold is related to the PEX 8649's buffering capacity – all outstanding Read data ought to be able to be buffered in the switch, to remain out of the way of other Completions for other endpoint's Read requests.

After a Port reaches its Read threshold, subsequent Read requests from that Port queue up in the PEX 8649, waiting for Completion data to reduce the outstanding count to below the threshold. If an overabundant number of Read requests queue in the PEX 8649, no additional Read credit is allocated, which backpressures the Read Requester. Figure 8-6 illustrates the way in which the PEX 8649 forwards Read requests when its Read Spacing logic is enabled and Read Spreading logic is disabled.

Figure 8-6. Read Pacing On (Enabled) and Read Spreading Off (Disabled)



8.5.4 Read Pacing Benefits

When Read Pacing logic is enabled, the PEX 8649 provides the follow benefits:

- Maximum Read latency that an endpoint may experience can be dramatically reduced.

  By reducing the amount of queued Read requests, and therefore pending Read Completion data at the Root Complex, new Read requests from Ports that do not have pending Read requests can be serviced with a predictable and/or reasonable amount of latency.

- Timid endpoint bandwidth is dramatically increased in busy applications.

  Because queues of pending Read requests in the Root Complex are limited, and congestion caused by a large amount of Completion data intended for a high-bandwidth, needy Port (or Ports) is avoided, the bandwidth needs of endpoints with smaller bandwidth requirements are met (*that is*, the endpoints are not starved).

- PEX 8649's Read Pacing Threshold logic allows all busy Ports to be equally serviced in congested scenarios, regardless of their individual Read requesting behavior.

  For example, all Ports might simultaneously request data, some aggressively and some timidly. While unable to quickly drain their queued Completions, the Ports' Read Pacing Threshold logic forwards the additional Read requests to the Root Complex, equally and fairly, while ensuring Completion data is available for each Port, when the Port is ready to accept it.

8.5.5 Enabling Read Pacing and Read Spreading

Read Pacing is disabled, by default. To enable Read Pacing, the Port's **Read Pacing Control** register *Port x Read Pacing Disable* bits (offset 1D0h[3:0]) must be Cleared. A bit value of 0 enables Read Pacing, whereas a value of 1 (default) disables Read Pacing.

The Port's **Read Pacing Control** register *Port x Memory Read Spread Disable* bit (offset 1D0h[19:16]) is used to enable or disable Read Spreading. A value of 1 disables Read Spreading for the corresponding Port. Read Spreading is enabled, by default (value of 0); however, it is overridden by the Port's *Port x Read Pacing Disable* bit, by default.

Both sets of Read Spreading and Pacing Control register bits are represented in Table 8-2. (For complete details, refer to the register offset 1D0h description provided in Section 13.15.1, "Device-Specific Registers – Read Pacing (Offsets 1D0h – 1D8h).") Figure 8-4 through Figure 8-6 illustrate what occurs when the bits are enabled or disabled.

The Read Pacing thresholds are Set, based upon the Source Port's programmed Link width. The **Read Pacing Threshold 1** register controls the threshold values for x16 and x8 Link widths, and the **Read Pacing Threshold 2** register controls the threshold values for x4 Link widths (offsets 1D4h and 1D8h, respectively). The thresholds are in DWords. Narrower Link widths have lower thresholds, because they must buffer smaller quantities.

Table 8-2. Read Pacing Control Register Read Pacing and Memory Read Spread Disable (Offset 1D0h)

Bit(s)[a]	Description	Default
3:0	**Port *x* Read Pacing Disable**[b] 0 = Read Pacing is enabled for this Port 1 = Read Pacing is disabled for this Port	Fh
19:16	**Port *x* Memory Read Spread Disable** 0 = Memory Read Spread is enabled for this Port 1 = Memory Read Spread is disabled for this Port	0h

a. *Bits not identified in Table 8-2 are* ***Reserved*** *or* ***Factory Test Only****.*

b. *The Read Pacing feature is supported on all Ports. The Read Pacing Configuration registers, however, are implemented in only one Port per Station. (Refer to Table 13-20 in Section 13.15.1, "Device-Specific Registers – Read Pacing (Offsets 1D0h – 1D8h)," for details.)*

8.6 Multicast – All Modes Except Legacy NT

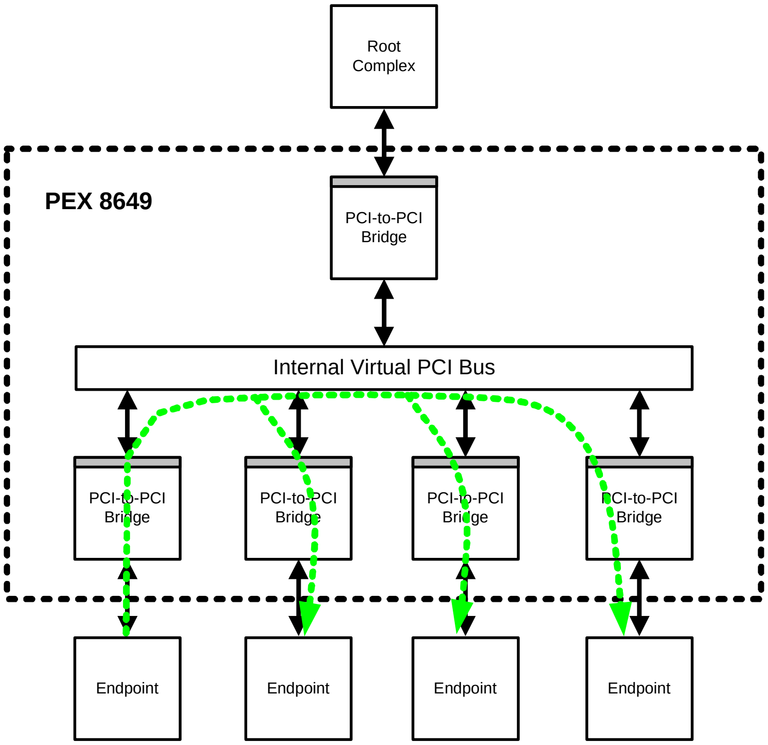
This section describes the functions and registers of the Multicast (MC) feature.

MC allows programs to concurrently write the same data to a group of multiple destinations. When Posted Memory Write TLP entering the PEX 8649 are addressed to MC Address Range (*MC BARs*), the PEX 8649 automatically generates and transmits, if enabled, a copy of the original TLP (referred to as the *MC Copy TLP*) to one or more destination Ports. The MC Address Space is divided into *MC Groups (MCG)*, defined by using *MC Base Address* and *MC Index Position*. Each Port of the PEX 8649 can elect to receive an MC Copy TLP by belonging to an *MCG*, by setting the corresponding *MC Receive* bit. An MC TLP can be blocked using the *MC Block All*, if required. *MC Overlay Bar* can be used to replace the original MC TLP's address to a Unicast address space, if the endpoint does not support MC.

The PEX 8649 supports Multicast in Transparent mode and Virtual Switch mode, and NT PCI-to-PCI Bridge mode (through the NT Port, if the NT Port appears behind a virtual downstream Port). However, Multicast is ***not supported*** through the Legacy NT Port, if the Legacy NT Port appears immediately behind the upstream Port.

Figure 8-7 illustrates an example of a Multicast operation on a peer-to-peer Write Request. An endpoint's Write Request is transmitted as copies to additional peer destination endpoints.

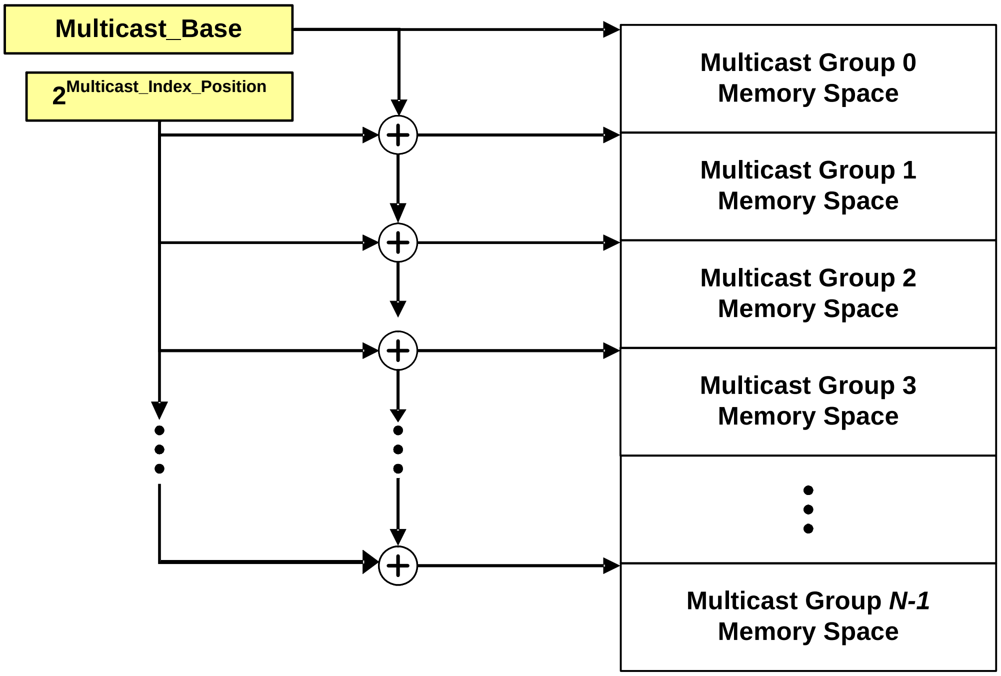
Figure 8-7. Peer-to-Peer Multicast



8.6.1 Multicast Address Range Segmentation

The **Multicast Extended Capability** structure defines an MC Address range, the segmentation of that range into a number, *N*, of equally sized MC windows, and the association of each MC window with an MCG. Each Function that supports MC within a component, implements a **Multicast Extended Capability** structure that provides routing directions and permission checking for each MCG for TLPs that pass through. The MCG is a field of up to 6 bits in width, which is embedded in the address, beginning at the MC_Index_Position.

Figure 8-8. Multicast Address Range Segmentation


Multicast_Base
2^Multicast_Index_Position
Multicast Group 0 Memory Space
Multicast Group 1 Memory Space
Multicast Group 2 Memory Space
Multicast Group 3 Memory Space
Multicast Group *N-1* Memory Space

8.6.2 Multicast TLP Processing

A TLP is processed as an MC TLP if an MC Hit occurs when all of the following conditions are true:

- MC_Enable is Set
- TLP is a Memory Write (Posted Request)
- TLP Address ≥ MC_Base_Address
- TLP Address < (MC_Base_Address + (MC_Index_Position^2) x (MC_Num_Group + 1))

While processing the TLP, each PEX 8649 ingress Port uses values of MC_Enable, MC_Base_Address, MC_Index_Position, and MC_Num_Group from its registers. the software is required to identically configure all these fields in all Ports. If this is not the case, results are indeterminate.

If an MC Hit occurs, normal address routing rules do not apply. Instead, the TLP is processed by first extracting MCG from the address in the TLP using the ingress Port's values for MC_Base_Address and MC_Index_Position. Specifically:

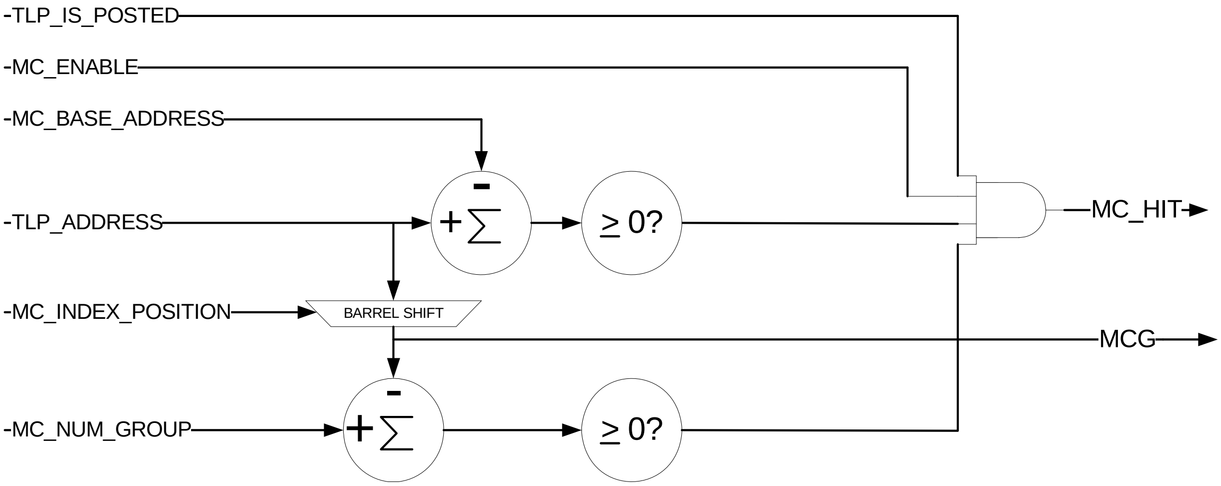
```
MCG = ((AddressTLP – MC_Base_Address) >> MC_Index_Position) & 3Fh
```

Next, the PEX 8649 checks the MC_Block_All and MC_Block_Untranslated bits corresponding to the extracted MCG using the MC_Block_All and MC_Block_Untranslated registers associated with the ingress Port. If the MC_Block_All bit corresponding to the extracted MCG is Set, the TLP is handled as an MC Blocked TLP. If the MC_Block_Untranslated bit corresponding to the extracted MCG is Set, and the TLP contains an Untranslated Address, the TLP is also handled as an MC Blocked TLP.

If the TLP is not blocked in the PEX 8649, it is forwarded through all Ports, with the exception of its ingress Port, whose MC_Receive bit corresponding to the extracted MCG is Set. If no Ports forward the TLP, the TLP is silently dropped.

Note: *To prevent loops, it is prohibited for a PEX 8649 Port to forward a TLP through its ingress Port, although specified by the MC_Receive register associated with the Port.*

Figure 8-9. Multicast TLP Processing



An MC Hit suspends normal address routing, including default Upstream routing in switches. When an MC Hit occurs, the TLP is forwarded only through those egress Ports whose MC_Receive bit associated with the MCG extracted from the address in the TLP is Set. If the address in the TLP does not decode to a downstream Port using normal address decode, the TLP is copied to the upstream Port only if specified by the upstream Port's MC_Receive register.

If the address in a Non-Posted Memory Request hits in an MC window, no MC Hit occurs, and the TLP is processed normally as a Unicast.

If an MC Hit occurs, the only ACS access control that can apply is ACS Source Validation. In particular, neither ACS redirection nor the ACS Egress Control Vector affects operations during an MC hit.

8.6.3 Multicast Ordering

No new ordering rules are defined for processing MC TLPs. All MC TLPs are Posted Requests and follow Posted Request ordering rules. MC TLPs are ordered per standard ordering rules, relative to other TLPs in a component's ingress stream, through the point of replication. Once copied into an egress stream, an MC TLP follows the same ordering as other Posted Requests in the stream.

8.6.4 Multicast Extended Capability Structure Field Updates

Certain fields of the **Multicast Extended Capability** structure can be changed at any time. Others cannot be changed with predictable results, unless the MC_Enable bit is Clear in every component function. The latter group includes MC_Base_Address and MC_Index_Position. Fields which software may change at any time include MC_Enable, MC_Num_Group, MC_Receive, MC_Block_All, and MC_Block_Untranslated. Updates to these fields must be ordered.

For example, TLPs *A* and *B* arriving in that order at the same ingress Port and in the same TC. If *A* uses *X* for one of these fields, then *B* must use the same value or a newer value.

8.6.5 MC Blocked TLP Processing

When a TLP is blocked by the MC_Block_All or the MC_Block_Untranslated mechanisms, the TLP is dropped. The ingress Port blocking the TLP serves as the Completer. It logs and signals this MC Blocked TLP. In addition, the ingress Port sets the Signaled Target Abort bit in either its Status register or Secondary Status register, as appropriate. If the error occurs with a TLP received by an ingress Port, the error is reported by that ingress Port.

8.6.6 MC_Overlay and ECRC Re-Generation

The MC Overlay mechanism is provided to allow a single BAR in an endpoint that does not contain a **Multicast Extended Capability** structure to be used for both MC and Unicast TLP reception. Software can configure the MC_Overlay mechanism to affect this, by setting the MC_Overlay_BAR in a downstream Port of the PEX 8649 so that the MC Address range, or a portion thereof, is re-mapped (overlaid) onto the Memory Space range accepted by the endpoint's BAR. At the upstream Port, the mechanism can be used to overlay a portion of the MC Address range onto a Memory Space range associated with Host memory.

When enabled, the overlay operation specifies that MC TLP Address bits, whose bit numbers are greater than or equal to the MC_Overlay_Size field, be replaced by the corresponding MC_Overlay_BAR bits. *That is*:

```
If (MC_Overlay_Size = 0)
Then:
        Egress_TLP_Addr = Ingress_TLP_Addr;
Otherwise:
        Egress_TLP_Addr =

{MC_Overlay_BAR[63:MC_Overlay_Size],Ingress_TLP_Addr[MC_Overlay_Size-1:0]};
```

If the TLP with the modified address contains the optional End-to-end Cyclic Redundancy Check (ECRC), the unmodified ECRC will almost certainly indicate an error. The action to be taken if a TLP containing an ECRC is MC copied to an egress Port that has MC_Overlay enabled, are outlined in Table 8-3. If MC_Overlay is not enabled, the TLP is forwarded unmodified. If MC_Overlay is enabled and the TLP has no ECRC, the modified TLP, with its address replaced as specified in the previous paragraph, is forwarded. If the TLP has an ECRC but ECRC re-generation is not enabled, then the modified TLP is forwarded with its ECRC dropped and the TD bit in the header Cleared, to indicate no ECRC is attached. If the TLP has an ECRC and ECRC re-generation is enabled, then an ECRC check is performed before the TLP is forwarded. If the ECRC check passes, the TLP is forwarded with re-generated ECRC. If the ECRC check fails, the TLP is forwarded with inverted re-generated ECRC.

Table 8-3. ECRC Rules for MC_Overlay[a]

MC_Overlay Enabled	TLP with ECRC	ECRC Re-Generation Supported	Action if ECRC Check Passes	Action if ECRC Check Fails
No	X	X	Forward TLP unmodified.	
Yes	No	X	Forward modified TLP.	
Yes	Yes	Yes	Forward modified TLP with re-generated ECRC.	Forward modified TLP with inverted re-generated ECRC.

[a] *"X" is "Don't Care."*

8.6.6.1 Multicast to Endpoints without Multicast Extended Capability

An endpoint function that does not contain a **Multicast Extended Capability** structure cannot distinguish MC TLPs from Unicast TLPs. It is possible to take advantage of this, to use such endpoints as MC targets. The PEX 8649 Port above the device can be configured to overlap at least part of the MC Address range, or the MC_Overlay mechanism can be used.

8.6.6.2 Congestion Avoidance

The use of MC increases the output Link use of switches to a degree proportional to both the size of the MC groups used and the fraction of MC traffic to total traffic, which can increase the risk of congestion and spreading. To mitigate this risk, design components that are intended to serve as MC targets to consume MC TLPs at wire speed. Components intended to serve as MC sources should consider adding a rate limiting mechanism.

8.6.7 Multicast Extended Capability

MC functionality is controlled by the **Multicast Extended Capability** structure. Multiple copies of this structure are required – one for each PEX 8649 Port that supports MC. To provide implementation efficiencies, certain fields within each of the MC Capability structures within a component, must be programmed the same. Results are indeterminate if this is not the case. The fields and registers that must be configured with the same values include MC_Enable, MC_Num_Group, MC_Base_Address and MC_Index_Position. These same fields in an endpoint's **Multicast Extended Capability** structure must match those configured in a **Multicast Extended Capability** structure of the PEX 8649 above the endpoint, or in which the Root Complex integrated endpoint is integrated.

8.6.8 Multicast NT – NT PCI-to-PCI Bridge Mode Only

As previously mentioned, Multicast is supported only in NT PCI-to-PCI Bridge mode; it is not supported in Legacy NT mode.

The following subsections describe Multicast behavior in NT PCI-to-PCI Bridge mode.

8.6.8.1 NT Multicast from Virtual to Link Direction

When a PEX 8649 Transparent Port receives a TLP that is a Multicast hit, the Multicast TLP that is routed to the egress Ports belongs to the extracted Multicast Group. If a virtual downstream Port is one of the Multicast Targets, the ingress Port routes the Multicast TLP through the virtual downstream Port to the NT Port Virtual Interface, if all the following conditions are true:

- Virtual downstream Port **Command** register *Memory Enable* bit is Set
- If Multicast overlay is not enabled, the Multicast TLP address hits the NT Port Virtual Interface BARs (**BAR2** through **BAR5**, offsets 18h through 24h, respectively)
- If Multicast overlay is enabled, the Multicast overlay translated address hits the NT Port Virtual Interface BARs
- NT Port Virtual Interface **PCI Command** register *Memory Access Enable* bit (offset 04h[1]) is Set
- NT Port Link Interface **PCI Command** register *Bus Master Enable* bit (offset 04h[2]) is Set
- Multicast TLP Requester ID hits the NT Port Virtual Interface **Requester ID Translation Lookup Table (LUT)** registers

If any one of these conditions is not met, the Multicast TLP to the NT Port is handled as an *Unsupported Request* (*UR*). If a Multicast TLP's Traffic Class (TC) value does not map to the **VC0 Resource Control** register VC0 *TC/VC Map* field (offset 15Ch[7:0]), the Multicast TLP is handled as a *Malformed TLP*.

The NT Port receives the Multicast TLP with either an un-translated address or Multicast overlay translated address (based upon the virtual downstream Port MC_Overlay_Enable (**Multicast BAR0** and **Multicast BAR0** registers, offsets E28h and E2Ch, respectively). The NT Port does the Address translation and Requester ID translation, as defined in the NT Port Virtual Interface Base **Address Translation** registers (offsets C3Ch through C48h) and **Requester ID Translation LUT** registers (8-Entry mode, addresses D94h through DB0h; 32-Entry mode, addresses D94h through DD0h). The translated Multicast TLP is sent out from the NT Port.

8.6.8.2 NT Multicast from Link to Virtual Direction

When the PEX 8649 NT Port Link Interface receives a Memory Write TLP, it performs the following checks, before qualifying the TLP as a Multicast hit:

- TLP hits the NT Port Link Interface BARs (**BAR2** through **BAR5**, offsets 18h through 24h, respectively).
- NT Port Link Interface **PCI Command** register *Memory Access Enable* bit (offset 04h[1]) is Set.
- NT Port Virtual Interface **PCI Command** register *Bus Master Enable* bit (offset 04h[2]) is Set.
- Virtual downstream Port **PCI Command** register *Bus Master Enable* bit is Set.
- Received TLP Requester ID hits the NT Port Link Interface **Requester ID Translation LUT** registers.
- NT Port Link Interface performs Address translation and Requester ID translation, as defined in the NT Port Link Interface Base **Address Translation** registers (offsets C3Ch through C48h) and **Requester ID Translation LUT** registers (addresses DB4h through DF0h). The translated address hits the Multicast BAR in the virtual downstream's Port **Multicast Extended Capability** structure and satisfies all other Multicast hit conditions.

When the NT Port Link Interface receives a TLP that is a Multicast hit, and the Multicast destination Port(s) **PCI Command** register *Memory Access Enable* or *Bus Master Enable* bit (based upon the traffic direction) is not Set, the Multicast TLP is handled as a UR for the corresponding destination Port(s).

When the NT Port Link Interface receives a TLP that is a Multicast hit and TLP TC value does not map to the enabled Virtual Channel, the Multicast TLP is handled as a Malformed TLP for the corresponding destination Port(s).

A Multicast TLP received at the NT Port Link Interface is forwarded with address translation and Requester ID translation to the Multicast destination Port(s). Multicast destination Port(s) transmit the TLP, either un-modified or with MC_Overlay address translation (based upon MC_Overlay_Enable).

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Chapter 9 Interrupts

9.1 Interrupt Support

The PEX 8649 supports the PCI Express interrupt model, which uses two mechanisms:

- INT*x* Interrupt Message-type emulation (compatible with the *PCI r3.0*-defined Interrupt signals)
- Message Signaled Interrupt (MSI), when enabled

For Conventional PCI compatibility, the PCI INT*x* emulation mechanism is used to signal interrupts to the System Interrupt Controller. This mechanism is compatible with existing PCI software, provides the same level of service as the corresponding PCI interrupt signaling mechanism, and is independent of System Interrupt Controller specifics. The PCI INT*x* emulation mechanism virtualizes PCI physical Interrupt signals, by using an in-band signaling mechanism, for the assertion and de-assertion of INT*x* interrupt signals.

In addition to PCI INT*x*-compatible interrupt emulation, the PEX 8649 supports the MSI mechanism. The PCI Express MSI mechanism is compatible with the MSI Capability defined in the *PCI r3.0*.

INT*x* and MSIs are mutually exclusive, on a per-Port basis; either can be enabled in a system (depending upon which interrupt type the system software supports), but never concurrently within the same domain. (Refer to the **PCI Command** register *Interrupt Disable* bit, offset 04h[10], and **MSI Capability** register, offset 48h, respectively.) The PEX 8649 does not convert received INT*x* Messages to MSI Messages.

The PEX 8649’s external Interrupt outputs, PEX_INTA# (Base mode and Virtual Switch mode) and VS*x*_PEX_INTA# (Virtual Switch mode only), indicate the assertion and/or de-assertion of the internally generated INT*x* signal:

- **Non-Hot Plug-triggered interrupts** – PEX_INTA# and VS*x*_PEX_INTA# assertion is controlled by the following **ECC Error Check Disable** register bits:
  - *Enable PEX_INTA# and/or VSx_PEX_INTA# Interrupt Output(s) for Management Link Status Event-Generated Interrupts* (offset 720h[9], Virtual Switch mode only),
  - *Enable PEX_INTA# and/or VSx_PEX_INTA# Interrupt Output(s) for Management Port Doorbell-Generated Interrupts* (offset 720h[8], Virtual Switch mode only),
  - *Enable PEX_INTA# Interrupt Output(s) for NT-Virtual Doorbell-Generated Interrupts* (offset 720h[7], NT mode only),
  - *Enable PEX_INTA# and/or VSx_PEX_INTA# Interrupt Output(s) for GPIO-Generated Interrupts* (offset 720h[6]), and/or
  - *Enable PEX_INTA# Interrupt Output(s) for Device-Specific NT-Link Port Event-Triggered Interrupt* (offset 720h[5])

  When any of these bits are Set, Device-Specific errors trigger PEX_INTA# and/or VS*x*_PEX_INTA# assertion; however, a PEX_INTA# and/or VS*x*_PEX_INTA# assertion and INT*x* Message generation are mutually exclusive, on a per-Port basis.
- **Hot Plug or Link State-triggered INT*x* events** – PEX_INTA# and VS*x*_PEX_INTA# assertion is controlled by the **ECC Error Check Disable** register *Enable PEX_INTA# and/or VSx_PEX_INTA# Interrupt Output(s) for Hot Plug or Link State Event-Triggered Interrupt* bit (offset 720h[4]). When this bit is Set, Hot Plug or Link State events trigger PEX_INTA# and/or VS*x*_PEX_INTA# assertion; however, an INT*x* Message is not generated in this case. PEX_INTA# and/or VS*x*_PEX_INTA# assertion and INT*x* Message generation for Hot Plug or Link State cases are mutually exclusive, on a per-Port basis.

The NT Port Virtual and Link Interfaces can each independently support the interrupt mechanism (INT*x* or MSI) used in their respective domains. (Refer to Section 14.6, “NT Port Interrupts,” for details.)

9.1.1 Interrupt Sources or Events

The PEX 8649 internally generated interrupt/Message sources include:

- For Hot Plug-capable Ports
  - Presence Detect Changed (logical OR of PRSNT# (HP_PRSNT_*x*# or I/O Expander PRSNT# input), and SerDes Receiver Detect[a] on Lane(s) associated with that Port)
  - Attention Button Pressed
  - Power Fault Detected
  - MRL Sensor Changed
  - Command Completed
  - Link Bandwidth Management Status
  - Link Autonomous Bandwidth Status
- For non-Hot Plug-capable downstream Ports
  - Presence Detect Changed (SerDes Receiver Detect[a] on Lane(s) associated with that Port)
  - Data Link Layer State Changed
- Device-Specific NT-Link events
  - NT-Link Port Correctable error (NT Port Link Interface, offset FC4h)
  - NT-Link Port Uncorrectable error (NT Port Link Interface, offset FB8h)
  - NT-Link Port Data Link Layer State change
  - NT-Link Port received (and consequently dropped) a Fatal or Non-Fatal Error Message
- General-Purpose Input/Output (GPIO) events
- Non-Transparent (NT) Doorbell events (refer to Section 14.6, "NT Port Interrupts")
- Virtual Switch mode
  - Link Status management
  - Doorbells

The PEX 8649 externally generated interrupt/Message sources include INT*x* Messages from downstream devices.

Table 9-1 lists the interrupt sources.

[a] *The SerDes Receiver Detect mechanism is comprised of the* ***Physical Layer Receiver Detect Status*** *register Receiver Detected on Lane x bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 200h[31:16]) or Hot Plug PRSNT# (from external I^{2}C I/O Expander) input for the Port.*

Table 9-1. Interrupt Sources

Event/Error	Description
All Modes – Base and Virtual Switch Modes	
Link state events	**Slot Status** register (Transparent Downstream Ports, offset 80h): • *Presence Detect Changed* (bit 19 = 1) • *Data Link Layer State Changed* (bit 24 = 1)
PCI Express Hot Plug events	The master control of Hot Plug interrupt is the **Slot Control** register *Hot Plug Interrupt Enable* bit (Transparent Downstream Ports, offset 80h[5]). There are six sources of Hot Plug interrupt. Each Hot Plug source has its own *Enable* bit in the **Slot Control** register: • *Attention Button Pressed* (bit 16) • *Power Fault Detected* (bit 17) • *MRL Sensor Changed* (bit 18) • *Presence Detect Changed* (bit 19) • *Command Completed* (bit 20) • *Data Link Layer State Changed* (bit 24) The interrupt status of each Hot Plug source is provided by the Port's **Slot Status** register (Downstream Ports, offset 80h). ***Note:*** *Presence (Presence Detect State, Transparent Downstream Ports, offset 80h[22]) is determined by the logical OR of:* • *SerDes Receiver Detect (**Physical Layer Receiver Detect Status** register Receiver Detected on Lane x bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 200h[31:16])), and* • *HP_PRSNT_x# –or–* • *PRSNT# (from external I^{2}C I/O Expander) input for the Port*

Table 9-1. Interrupt Sources *(Cont.)*

Event/Error	Description
General-Purpose Input Interrupt events	External interrupt from any of the GPIO[31:24] and PEX_PORT_GOOD*x*# signals that are configured as an Interrupt input in the **GPIO *x_y* Direction Control** register *Direction Control* bit(s) (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offsets 600h, 604h, and 60Ch).
Device-Specific Error conditions	• Egress Completion FIFO Overflow error indicated by the Port's **Device-Specific Error Status 1** register *Completion FIFO Overflow Status* bit (offset 700h[0]), if not masked by the Port's **Device-Specific Error Mask 1** register *Completion FIFO Overflow Mask* bit (offset 704h[0]). • Device-Specific (RAM ECC) errors indicated by the **Device-Specific Error Status *x*** register bit(s), if not masked in their corresponding **Device-Specific Error Mask *x*** register bit(s) (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets 700h[19:2], 708h[19:2], 710h[17:0], and/or 718h[17:0] (Status) and offsets 704h[19:2], 70Ch[19:2], 714h[17:0], and/or 71Ch[17:0] (Mask)). ***Note:*** *Device-Specific (RAM ECC) errors can be signaled by interrupt, and/or as an Uncorrectable Internal error that is fatal (**Uncorrectable Error Status** register Uncorrectable Internal Error Status **Uncorrectable Error Severity** register Uncorrectable Internal Error Severity bits (offsets FB8h[22] and FC0h[22], respectively, are Set).* • NT Port Link Interface Correctable errors reported by the NT Port Virtual Interface (to the Host of the upstream Port domain), collectively flagged in the **Link Error Status Virtual** register *Correctable Error Status on Link Side* bit (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE0h[0]), with specific errors indicated in the **Correctable Error Status** register (NT Port Link Interface, offset FC4h), if not masked both globally in the **Link Error Mask Virtual** register *Link Side Correctable Error Mask* bit (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE4h[0]), nor individually in the **Correctable Error Mask** register (NT Port Link Interface, offset FC8h). • NT Port Link Interface Uncorrectable errors reported by the NT Port Virtual Interface (to the Host of the upstream Port domain), collectively flagged in the **Link Error Status Virtual** register *Uncorrectable Error Status on Link Side* bit (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE0h[1]), with specific errors indicated in the **Uncorrectable Error Status** register (NT Port Link Interface, offset FB8h), if not masked both globally in the **Link Error Mask Virtual** register *Link Side Uncorrectable Error Mask* bit (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE4h[1]), nor individually in the **Uncorrectable Error Mask** register (NT Port Link Interface, offset FBCh).

Table 9-1. Interrupt Sources *(Cont.)*

Event/Error	Description
NT Mode – Base Mode Only	
Device-Specific NT-Link Port events	• NT Port Link Interface Uncorrectable errors indicated by the **Uncorrectable Error Status** register (NT Port Link Interface, offset FB8h), if not masked in the **Uncorrectable Error Mask** register (NT Port Link Interface, offset FBCh). • NT Port Link Port Correctable errors indicated by the **Correctable Error Status** register (NT Port Link Interface, offset FC4h), if not masked in the **Correctable Error Mask** register (NT Port Link Interface, offset FC8h). • NT Port Link Interface State change – Interrupt to the NT Port Virtual Interface Host, if enabled (not masked) by the **Link Error Mask Virtual** register *Link Side DL Active Change Mask* bit (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE4h[2]). • Link Side Uncorrectable Error Message Drop interrupt to the NT Port Virtual Interface Host, if enabled (not masked) by the **Link Error Mask Virtual** register *Link Side Uncorrectable Error Message Drop Mask* bit (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE4h[3]). This feature supports applications using back-to-back NT Ports, where an Uncorrectable Error Message received (and properly dropped) by the NT Port Link Interface can trigger an interrupt to the NT Port Virtual Interface Host.
NT-Virtual Doorbell events	**NT-Virtual Interface IRQ Set/Clear** register (offsets C4Ch[15:0] and/or C50h[15:0]) bit is Set while the corresponding **NT Virtual Interface IRQ Set/Clear** register (offsets C54h[15:0] and/or C58h[15:0]) bit is Cleared.
NT-Link Doorbell events	**NT-Link Interface IRQ Set/Clear** register (offsets C5Ch[15:0] and/or C60h[15:0]) bit is Set while the corresponding **NT Link Interface IRQ Set/Clear** register (offsets C64h[15:0] and/or C68h[15:0]) bit is Cleared.
Virtual Switch Mode Only	
Management Port Doorbell-Generated interrupts	• Writing a 1 to the **VS Upstream to Management Upstream Doorbell Request** register (VS Upstream Port(s) and Management Port, offset 910h[3:0]) signals an interrupt (unless it is masked by the **VS Upstream to Management Upstream Doorbell Mask** register (VS Upstream Port(s) and Management Port, offset 914h[3:0])) to the Management Port • Writing a 1 to the **Management Upstream to VS Upstream Doorbell Request** register (VS Upstream Port(s) and Management Port, offset 928h[3:0]) signals an interrupt (unless it is masked by the **Management Upstream to VS Upstream Doorbell Mask** register (VS Upstream Port(s) and Management Port, offset 92Ch[3:0])) to the Management Port ***Note:*** *If a virtual switch upstream Port is also the Management Port, that upstream Port* ***cannot*** *send Doorbell interrupts to itself.*
Management Link Status events	• A Link transition from the *DL_Inactive* state to the *DL_Active* state Sets the bit that corresponds to the Port Number (**Switch Link Up** register (Port 0, accessible through the Management Port, offset 900h[23:16, 3:0]), and generates an interrupt (unless it is masked by the **Switch Link Event Mask** register (Port 0, accessible through the Management Port, offset 908h[23:16, 3:0])) to the Management Port • A Link transition from the *DL_Active* state to the *DL_Inactive* state Sets the bit that corresponds to the Port Number (**Switch Link Down** register (Port 0, accessible through the Management Port, offset 904h[23:16, 3:0]), and generates an interrupt (unless it is masked by the **Switch Link Event Mask** register (Port 0, accessible through the Management Port, offset 908h[23:16, 3:0])) to the Management Port

9.1.2 Interrupt Handling

The PEX 8649 provides an Interrupt Generation module with each Port. The module reads the Request for interrupts from different sources and generates an MSI or PCI-compatible Assert_INT*x*/ Deassert_INT*x* Interrupt Message. MSIs support PCI Express edge-triggered interrupts, whereas Assert_INT*x* and Deassert_INT*x* Message transactions emulate PCI level-triggered interrupt signaling. The System Interrupt Controller functions include:

- Sensing Interrupt events
- Signaling the interrupt, by way of the INT*x* mechanism, and Setting the *Interrupt Status* bit
- Signaling the interrupt, by way of the MSI mechanism
- Handling INT*x*-type Interrupt Messages from downstream devices

9.1.2.1 Interrupt Handling – Base Mode

Base mode supports INT*x* or MSIs generated by the PEX 8649, as per the *PCI Express Base r2.0*.

One PEX_INTA# Interrupt output is implemented.

9.1.2.2 Interrupt Handling – Virtual Switch Mode

Virtual Switch mode supports INT*x* or MSIs generated by the PEX 8649, as per the *PCI Express Base r2.0*, within the respective hierarchy.

One INTA# Interrupt output is implemented, per virtual switch (up to four – PEX_INTA# (VS0) and VS*x*_PEX_INTA# (VS1 through VS3)).

9.2 INT*x* Emulation Support

The PEX 8649 supports PCI INT*x* emulation, to signal interrupts to the System Interrupt Controller. This mechanism is compatible with existing PCI software. PCI INT*x* emulation virtualizes PCI physical Interrupt signals, by using the in-band signaling mechanism.

PCI **Interrupt** registers (defined in the *PCI r3.0*) are supported. The *PCI r3.0* **PCI Command** register *Interrupt Disable* and **PCI Status** register *Interrupt Status* bits are also supported (offset 04h[10 and 19], respectively).

Although the *PCI Express Base r2.0* provides INTA#, INTB#, INTC#, and INTD# for INT*x* signaling, the PEX 8649 uses only INTA# and/or VS*x*_PEX_INTA# for internal Interrupt Message generation, because it is a single-function device. However, incoming Messages from downstream devices can be of INTA#, INTB#, INTC#, or INTD# type. Internally generated INTA# and/or VS*x*_PEX_INTA# Messages from the downstream Port are also re-mapped and collapsed at the upstream Port, according to the downstream Port's Device Number, with its own Device Number and Received Device Number from the downstream device.

When an interrupt is requested, the **PCI Status** register *Interrupt Status* bit is Set. If INT*x* interrupts are enabled (**PCI Command** register *Interrupt Disable* and **MSI Control** register *MSI Enable* bits, offsets 04h[10] and 48h[16], respectively, are both Cleared), an Assert_INT*x* Message is generated and transmitted upstream to indicate the Port interrupt status. For each interrupt event, there is a corresponding *Mask* bit; an Interrupt Message can be generated only when the corresponding *Mask* bit is Cleared. Software reads and Clears the event and *Interrupt Status* bit after servicing the interrupt.

A Port de-asserts INT*x* or PEX_INTA# and/or VS*x*_PEX_INTA# interrupts, in response to one or more of the following conditions:

- Port's **PCI Command** register *Interrupt Disable* bit (offset 04h[10]) is Set
- Corresponding *Interrupt Mask* bit is Set
- Upstream Port Link goes down (DL_Down condition), or receives a Hot Reset (unless Hot Reset/ DL_Down Reset is disabled, by Setting the **Virtual Switch Debug** register *Upstream Port and NT-Link Port DL_Down Reset Propagation Disable* bit (Upstream Port(s), offset A30h[4]))
- Software Clears the corresponding *Interrupt Status* bit

9.2.1 INT*x*-Type Interrupt Message Re-Mapping and Collapsing

The upstream Port(s) re-map(s) and collapse(s) the INT*x* *virtual wires* received at the downstream Port, based upon the downstream Port's Device Number and Received INT*x* Message Requester ID Device Number, and generate(s) a new Interrupt Message, according to the mapping defined in Table 9-2.

Each virtual PCI-to-PCI bridge of a downstream Port specifies the Port Number associated with the INT*x* (Interrupt) Messages received or generated, and forwards the Interrupt Messages upstream.

A downstream Port transmits an Assert_INTA/Deassert_INTA Message to the upstream Port(s), due to a Hot Plug and/or PCI Express Hot Plug, Link State, GPIO, NT Port Doorbell (Base mode only), Management Port Doorbell interrupt and/or Management Link Status (Virtual Switch mode only), and/or Device-Specific NT Port Link Interface (reported by the NT Port Virtual Interface) error/event.

Internally generated INT*x* Messages always originate as type INTA Messages, because the PEX 8649 is a single-function device. Internally generated Interrupt INTA Messages from downstream Ports are re-mapped at the upstream Port(s) to INTA, INTB, INTC, or INTD Messages, according to the mapping defined in Table 9-2.

INT*x* Messages from downstream devices and from internally generated Interrupt Messages are ORed together to generate INTA, INTB, INTC, or INTD level-sensitive signals, and edge-detection circuitry in the upstream Port generates the Assert_INT*x* and Deassert_INT*x* Messages. The upstream Port(s) then forward(s) the new Messages upstream, by way of its (their) Link.

Table 9-2. Downstream/Upstream Port INT*x* Interrupt Message Mapping

Device Number	At Downstream Port	By Upstream Port
0, 16, 20	INTA	INTA
	INTB	INTB
	INTC	INTC
	INTD	INTD
1, 17, 21	INTA	INTB
	INTB	INTC
	INTC	INTD
	INTD	INTA
2, 18, 22	INTA	INTC
	INTB	INTD
	INTC	INTA
	INTD	INTB
3, 19, 23	INTA	INTD
	INTB	INTA
	INTC	INTB
	INTD	INTC

9.2.1.1 Interrupt Re-Mapping and Collapsing in NT PCI-to-PCI Bridge Mode

In NT PCI-to-PCI Bridge mode, an NT Port Virtual Interface-generated interrupt is treated like an external event to the PCI-to-PCI bridge immediately upstream, for tracking purposes. In this mode, when the upstream Port receives an INT*x* Message from the NT Port Virtual Interface, the upstream Port re-mapping-collapsing logic performs double Swizzling, one based upon the NT Port Virtual Interface's Captured Device Number, and another based upon the virtual downstream Port (PCI-to-PCI) Device Number.

If software asserts a Secondary Bus Reset to this PCI-to-PCI bridge, the PCI-to-PCI bridge de-asserts the NT Port Virtual Interface interrupt.

9.3 MSI Support

One of the interrupt schemes supported by the PEX 8649 is the MSI mechanism, which is required for PCI Express devices. The MSI method uses Memory Write transactions to deliver interrupts. MSIs are edge-triggered interrupts.

Note: *MSIs and INTx are mutually exclusive, on a per-Port basis. These interrupt mechanisms* ***cannot*** *be simultaneously enabled.*

9.3.1 MSI Operation

At configuration time, system software traverses the function Capability list. If a Capability ID of 05h is found, the function implements MSIs. System software reads the **MSI Capability** Structure registers, to determine function capabilities.

The **MSI Control** register *Multiple Message Capable* field (offset 48h[19:17]) default value is 011b, which indicates that the PEX 8649 requests up to eight MSI Vectors (Address and Data). When the register's *Multiple Message Enable* field (offset 48h[22:20]) is Cleared (default), only one Vector is allocated, and therefore, the PEX 8649 can generate only one Vector for all errors or events. When system software writes a non-zero value to the *Multiple Message Enable* field, multiple-Vector support is enabled (the number of Vectors supported is dependent upon the value). Table 9-3 lists the six supported MSI Vector types.

Table 9-3. Supported MSI Vector Types

Vector Type	Modes		
	Base		Virtual Switch
	Transparent	NT	
Power Management, or Hot Plug or Link State events	✔	✔	✔
Device-Specific NT-Port Link events		✔	
GPIO interrupts	✔	✔	✔
NT Doorbell interrupts		✔	
Management Link Status events			✔
Management Port Doorbell interrupts			✔

System software initializes the MSI Address registers (offsets 4Ch and 50h) and **MSI Data** register (offset 54h), with a system-specified Vector. After system software enables the MSI function (by Setting the **MSI Control** register *MSI Enable* bit, offset 48h[16]), when an Interrupt event occurs, the Interrupt Generation module generates a DWord Memory Write to the address specified by the **MSI Address** (lower 32 bits of the *Message Address* field) and **MSI Upper Address** (upper 32 bits of the *Message Address* field) register contents (offsets 4Ch and 50h, respectively). The single DWord Payload includes zero (0) for the upper two bytes, and the lower two bytes are taken from the **MSI Data** register. The **MSI Control** register *Multiple Message Enable* field (offset 48h[22:20]) can be programmed to a value of 000b, 001b, 010b, or 011b. When programmed to 011b, the lower three bits of Message data are changed to indicate the general type of interrupt event that occurred. (Refer to Table 9-3.)

The number of MSI Vectors generated is dependent upon the quantity enabled, as follows:

- If **one** MSI Vector is enabled (default), all interrupt categories generate the same MSI Vector.
- If **two** MSI Vectors are enabled, Device-Specific NT-Link Port events generate their own MSI Vector, while all other categories are combined and generate the same Vector.
- If **four** MSI Vectors are enabled, Device-Specific NT-Link Port events, Hot Plug/Power Management events, and GPIO events each generate their own MSI Vector, while all other categories are combined and generate the same Vector.
- If **eight** MSI Vectors are enabled, each interrupt category generates its own MSI Vector. Up to six Vectors are used; the upper two Vectors (having the highest values of Message Data bits [2:0]) are ***not*** used.

If a non-masked Interrupt event occurs before system software Sets the *MSI Enable* bit, normally (but unlike Conventional PCI interrupts, which are level-triggered), an MSI packet is sent immediately after software Sets the *MSI Enable* bit, to notify the system of the prior event. Alternatively, MSIs for prior events can be disabled, on a per-Port basis, by Setting the **ECC Error Check Disable** register *Disable Sending MSI if MSI Is Enabled after Interrupt Status Set* bit (offset 720h[10]).

When the error or event that caused the interrupt is serviced, the PEX 8649 can generate a new MSI Memory Write as a result of new events. Because an MSI is an edge-triggered event, six bits are provided for masking the events (**MSI Mask** register *Interrupt Mask* bits, offset 58h[5:0]). A new MSI can be generated only after the *Interrupt Mask* bits are serviced. System software should mask these bits when the MSI event is being processed.

The **MSI Control** register *MSI 64-Bit Address Capable* bit (offset 48h[23]) is enabled, by default. If the serial EEPROM and/or I^{2}C/SMBus Clears the bit, the **MSI Capability** structure is reduced by 1 DWord (*that is*, register offsets 54h, 58h, and 5Ch change to 50h, 54h, and 58h, respectively).

9.3.1.1 NT PCI-to-PCI Bridge Mode MSI

In NT PCI-to-PCI Bridge mode (STRAP_NT_P2P_EN#=L), NT Port Virtual Interface MSI TLPs are not generated if the **PCI Command** register *Bus Master Enable* bit (offset 04h[2]) is Cleared in the upstream Port, NT Port Virtual Interface, and Virtual Downstream PCI-to-PCI Bridge.

9.3.2 MSI Capability Registers

For details, refer to Section 13.9, “MSI Capability Registers (Offsets 48h – 64h).”

9.4 PEX_INTA# and VS*x*_PEX_INTA# Interrupts

PEX_INTA# and/or VS*x*_PEX_INTA# Interrupt output is enabled when the following conditions exist:

- INT*x* Messages are enabled (**PCI Command** register *Interrupt Disable* bit, offset 04h[10], is Cleared) and MSIs are disabled (**MSI Control** register *MSI Enable* bit, offset 48h[16], is Cleared)
- PEX_INTA# and/or VS*x*_PEX_INTA# outputs are enabled for the following errors and events, when the **ECC Error Check Disable** register bit associated with that error or event is Set:
  - *Enable PEX_INTA# and/or VSx_PEX_INTA# Interrupt Output(s) for GPIO-Generated Interrupts* bit (offset 720h[6])
  - *Enable PEX_INTA# and/or VSx_PEX_INTA# Interrupt Output(s) for Hot Plug or Link State Event-Triggered Interrupt* bit (offset 720h[4])
  - **NT mode only (PEX_INTA# Interrupt output only)**
    - *Enable PEX_INTA# Interrupt Output(s) for NT-Virtual Doorbell-Generated Interrupts* bit (offset 720h[7])
    - *Enable PEX_INTA# Interrupt Output(s) for Device-Specific NT-Link Port Event-Triggered Interrupt* bit (offset 720h[5])
  - **Virtual Switch mode only**
    - *Enable PEX_INTA# and/or VSx_PEX_INTA# Interrupt Output(s) for Management Link Status Event-Generated Interrupts* bit (offset 720h[9])
    - *Enable PEX_INTA# and/or VSx_PEX_INTA# Interrupt Output(s) for Management Port Doorbell-Generated Interrupts* bit (offset 720h[8])

The three interrupt mechanisms, listed below, are mutually exclusive modes of operation, on a per-Port basis, for all interrupt sources:

- Conventional PCI INT*x* Message generation
- Native MSI transaction generation
- Device-Specific PEX_INTA# and/or VS*x*_PEX_INTA# assertion

PEX_INTA# and/or VS*x*_PEX_INTA# assertion (Low) indicates that the PEX 8649 detected one or more of the events and/or errors (if not masked) listed in Table 9-1.

Note: *PEX_INTA# and VSx_PEX_INTA# assertion and INTx messaging are mutually exclusive for a given interrupt event. When MSIs are enabled (offset 48h[16], is Set), both INTx and PEX_INTA# and/or VSx_PEX_INTA# are disabled for PEX 8649 internally generated interrupts. The forwarding of external INTx Messages received from a downstream Port to an upstream Port is always enabled.*

9.5 General-Purpose Input/Output

The PEX 8649 contains 20 GPIO balls, in two groups. Default functionality is programmed by the STRAP_TESTMODE[3:0] inputs, and can be selectively changed by software, serial EEPROM, and/or I^2C/SMBus.

- The first group is comprised of 12 balls – PEX_PORT_GOOD*x*# (enabled Ports only) indicators – each of which can be used as GPIOs or Interrupt inputs
- The second group is comprised of 8 balls – GPIO[31:24] – which can be used as GPIOs, Interrupt inputs, or Serial Hot Plug PERST# outputs

In Base mode, the Virtual Switch **GPIO** registers (offsets 64Ch through 67Ch and A34h through A74h) are not used. In Virtual Switch mode, the Management Port (and/or I^2C) has access to all **GPIO** registers (Chip-specific (offsets 600h through 640h), **Management Port** (offsets 64Ch through 67Ch), and **Virtual Switch** (offsets A34h through A74h) registers). Each virtual switch can access only its own **Virtual Switch** registers.

The VS GPIO_PG registers refer to the first group of 12 GPIO signals, PEX_PORT_GOOD*x*# (GPIO_PG), which are assigned to virtual switches depending upon which Bring-Up Option (1 or 2) is used during switch initialization:

- **Option 1 (STRAP_NT_UPSTRM_PORTSEL0=L)** – After the serial EEPROM (if present) is loaded, the Management Port comes up first, to configure the PEX 8649. In this option, all GPIO_PG signals are initially assigned to VS0. The Management Port can make further assignments of the GPIO_PG signals, to each of the virtual switches. The GPIO signals must be assigned in a mutually exclusive manner with respect to all virtual switches. If a particular virtual switch is disabled, it should not have any GPIO_PG signals assigned to it.
- **Option 2, during virtual switch configuration (STRAP_NT_UPSTRM_PORTSEL0=H)** – After the serial EEPROM (if present) is loaded, all Ports concurrently linkup, and the GPIO_PG signals are divided among the virtual switches, according to the Ports assigned to each virtual switch. The default settings for which GPIO_PG signals are assigned to each virtual switch are based upon the **Virtual Switch Table** registers (Port 0, accessible through the Management Port, offsets 354h through 38Ch). (Refer to Section 5.5.3, “Virtual Switch Table.”)

The **Virtual Switch GPIO_PG 0_11 Availability** register (offset A3Ch) can be read by the Virtual Switch Host, to determine how many GPIO_PG signals are available to that virtual switch. The Management Port can then adjust the number of GPIO_PG signals assigned to each virtual switch. A maximum of 12 GPIO_PG signals can be assigned to any virtual switch. A single GPIO_PG signal cannot be assigned to more than one virtual switch.

The VS GPIO_SHP registers refer to the second group of 8 GPIO signals, GPIO[31:24]. If the STRAP_TESTMODE[3:0] inputs do not configure Serial Hot Plug PERST# output functionality as default, none of the GPIO_SHP signals are assigned to the virtual switches, by default. However, if the STRAP_TESTMODE[3:0] inputs do configure Serial Hot Plug PERST# output functionality as default, two GPIO_SHP signals are assigned to each virtual switch, by default.

The **Virtual Switch GPIO_SHP 0_7 Availability** register (offset A5Ch) can be read by the Virtual Switch Host, to determine how many GPIO_SHP signals are available to that virtual switch. The Management Port can make further assignments of the GPIO_SHP signals, to each virtual switch. A maximum of eight GPIO_SHP signals can be assigned to any virtual switch. A single GPIO_SHP signal cannot be assigned to more than one virtual switch.

The logic that controls the GPIO ball function is driven from the **GPIO** Chip-specific registers (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offsets 600h through 640h). When a GPIO signal is assigned to a virtual switch, the GPIO information from the **VS GPIO** registers is multiplexed into the corresponding Chip-specific **GPIO** registers. As a result, the **VS GPIO** register(s) now control(s) the data in the Chip-specific **GPIO** register(s), for the GPIOs assigned to it, which leaves the Chip-specific **GPIO** register(s) to act as (a) Read-Only register(s) for the GPIOs that are assigned to virtual switches.

Table 9-4 lists the registers used for GPIO functionality.

Table 9-4. Registers Used for GPIO Functionality

Register Offset	Register Name
Chip Registers (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)	
600h	**GPIO 0_9 Direction Control**
604h	**GPIO 10_11 Direction Control**
60Ch	**GPIO 24_31 Direction Control**
614h	**GPIO 0_11 Input De-Bounce**
618h	**GPIO 24_31 Input De-Bounce**
61Ch	**GPIO 0_11 Input Data**
620h	**GPIO 24_31 Input Data**
624h	**GPIO 0_11 Output Data**
628h	**GPIO 24_31 Output Data**
62Ch	**GPIO 0_11 Interrupt Polarity**
630h	**GPIO 24_31 Interrupt Polarity**
634h	**GPIO 0_11 Interrupt Status**
638h	**GPIO 24_31 Interrupt Status**
63Ch	**GPIO 0_11 Interrupt Mask**
640h	**GPIO 24_31 Interrupt Mask**
Virtual Switch Management Port Registers (Virtual Switch mode – Port 0, accessible through the Management Port)	
64Ch	**Virtual Switch GPIO Update**
650h	**VS0 GPIO_PG 0_11 Assignment**
654h	**VS1 GPIO_PG 0_11 Assignment**
658h	**VS2 GPIO_PG 0_11 Assignment**
65Ch	**VS3 GPIO_PG 0_11 Assignment**
670h	**VS0 GPIO_SHP 0_7 Assignment**
674h	**VS1 GPIO_SHP 0_7 Assignment**
678h	**VS2 GPIO_SHP 0_7 Assignment**
67Ch	**VS3 GPIO_SHP 0_7 Assignment**

Table 9-4. Registers Used for GPIO Functionality *(Cont.)*

Register Offset	Register Name
Virtual Switch Registers (Virtual Switch mode – VS Upstream Port(s))	
A34h	**Virtual Switch GPIO_PG 0_9 Direction Control**
A38h	**Virtual Switch GPIO_PG 10_11 Direction Control**
A3Ch	**Virtual Switch GPIO_PG 0_11 Availability**
A40h	**Virtual Switch GPIO_PG 0_11 Input De-Bounce**
A44h	**Virtual Switch GPIO_PG 0_11 Input Data**
A48h	**Virtual Switch GPIO_PG 0_11 Output Data**
A4Ch	**Virtual Switch GPIO_PG 0_11 Interrupt Polarity**
A50h	**Virtual Switch GPIO_PG 0_11 Interrupt Status**
A54h	**Virtual Switch GPIO_PG 0_11 Interrupt Mask**
A58h	**Virtual Switch GPIO_SHP 0_7 Direction Control**
A5Ch	**Virtual Switch GPIO_SHP 0_7 Availability**
A60h	**Virtual Switch GPIO_SHP 0_7 Input De-Bounce**
A64h	**Virtual Switch GPIO_SHP 0_7 Input Data**
A68h	**Virtual Switch GPIO_SHP 0_7 Output Data**
A6Ch	**Virtual Switch GPIO_SHP 0_7 Interrupt Polarity**
A70h	**Virtual Switch GPIO_SHP 0_7 Interrupt Status**
A74h	**Virtual Switch GPIO_SHP 0_7 Interrupt Mask**

9.6 Management Port Interrupts – Virtual Switch Mode

The CPU connected to the Management Port receives interrupts for the following two events:

- Switch Ports Link Status
- Doorbell

Both are described in the sections that follow.

9.6.1 Switch Port Link Status Events – Virtual Switch Mode

The Management Port has four registers that provide Link status to the Management CPU (located in Port 0, accessible through the Management Port):

- **Switch Link Up** register (offset 900h)
- **Switch Link Down** register (offset 904h)
- **Switch Link Event Mask** register (offset 908h)
- **Switch Link Status** register (offset 90Ch)

In all four registers, each non-***reserved*** bit corresponds to one Port (for example, bit 0 corresponds to Port 0, bit 1 corresponds to Port 1, and so forth).

When a Port Link goes to an active state (DL_ACTIVE=1) from a down state, it Sets the corresponding **Switch Link Up** register *Port x Link Up* bit (offset 900h[23:16, 3:0]), regardless of the **Switch Link Event Mask** register *Port x Link Event Mask* bit (offset 908h[23:16, 3:0]) value. If the interrupt is not masked, the Management Port interrupt handler signals an Assert_INTA Message to the Management CPU if Conventional PCI interrupts (INT*x*) are enabled and MSIs are disabled. If instead MSIs are enabled, the Management Port generates an MSI Message instead of a Conventional PCI Assert_INTA Message. When the Interrupt Service Routine. (ISR) services this interrupt, it writes 1 to the corresponding **Switch Link Up** register *Port x Link Up* bit, to Clear this event. This Clear event or Interrupt Mask event generates a Deassert_INTA Message to the Management Port, if all Interrupt events in the **Switch Link Up** and **Switch Link Down** registers are Cleared, provided Conventional PCI interrupts are enabled and MSIs are disabled.

When a Port Link goes to a down state (DL_ACTIVE=0) from an active state, it Sets the corresponding **Switch Link Down** register *Port x Link Down* bit (offset 904h[23:16, 3:0]), regardless of the Port’s **Switch Link Event Mask** register *Port x Link Event Mask* bit (offset 908h[23:16, 3:0]) value. If the interrupt is not masked, the Management Port interrupt handler signals an Assert_INTA Message to the Management CPU, if Conventional PCI interrupts (INT*x*) are enabled and MSIs are disabled. If instead MSIs are enabled, the Management Port generates an MSI Message instead of a Conventional PCI Assert_INTA Message. When the ISR services this interrupt, it writes 1 to the corresponding **Switch Link Down** register *Port x Link Down* bit, to Clear this event. This Clear event or Interrupt Mask event generates a Deassert_INTA Message to the Management Port, if all Interrupt events in the **Switch Link Up** and **Switch Link Down** registers are Cleared, provided Conventional PCI interrupts are enabled and MSIs are disabled.

9.6.1.1 Special Handling for Race Conditions

If multiple DL_ACTIVE and DL_INACTIVE events occur before the ISR is able to service the Interrupt event, a race condition exists with event ordering. The Management Port implements the **Switch Link Status** register (Port 0, accessible through the Management Port, offset 90Ch) for this purpose. If the corresponding Port bits are Set in both the **Switch Link Up** and **Switch Link Down** registers (Port 0, accessible through the Management Port, offsets 900h and 904h, respectively), the ISR looks at the **Switch Link Status** register, to determine the order of these two events. If a bit in the **Switch Link Status** register is Cleared, the first event is DL_ACTIVE and the latest event is DL_INACTIVE. If a bit in the **Switch Link Status** register is Set, the first event is DL_INACTIVE and the latest event is DL_ACTIVE.

9.6.2 Doorbell Interrupts – Virtual Switch Mode

In Virtual Switch mode, each virtual switch upstream Port (other than the active Management Port) implements **Doorbell** and **Scratchpad** registers for communication (located in the VS Upstream Port(s) and Management Port):

- Virtual switch to Management CPU direction
  - **VS Upstream to Management Upstream Doorbell Request** register (offset 910h)
  - **VS Upstream to Management Upstream Doorbell Mask** register (offset 914h)
  - **VS Upstream to Management Upstream Scratchpad 1** register (offset 918h)
  - **VS Upstream to Management Upstream Scratchpad 2** register (offset 91Ch)
  - **VS Upstream to Management Upstream Scratchpad 3** register (offset 920h)
  - **VS Upstream to Management Upstream Scratchpad 4** register (offset 924h)
- Management CPU to virtual switch direction
  - **Management Upstream to VS Upstream Doorbell Request** register (offset 928h)
  - **Management Upstream to VS Upstream Doorbell Mask** register (offset 92Ch)
  - **Management Upstream to VS Upstream Scratchpad 1** register (offset 930h)
  - **Management Upstream to VS Upstream Scratchpad 2** register (offset 934h)
  - **Management Upstream to VS Upstream Scratchpad 3** register (offset 938h)
  - **Management Upstream to VS Upstream Scratchpad 4** register (offset 93Ch)

Software uses these registers to establish communication between the active Management CPU and the other CPUs. There is no in-band communication mechanism between CPUs outside the active Management Port domain.

A Fundamental Reset resets all the registers listed above.

A Hot Reset to the Management Port domain Clears the **VS Upstream to Management Upstream Doorbell Request**, **VS Upstream to Management Upstream Doorbell Mask**, and **VS Upstream to Management Upstream Scratchpad *x*** registers in the Virtual Switch to Management CPU direction.

A Hot Reset to virtual switches other than the Management Port domain Clears the **Management Upstream to VS Upstream Doorbell Request**, **Management Upstream to VS Upstream Doorbell Mask**, and **Management Upstream to VS Upstream Scratchpad *x*** registers in the Management CPU to Virtual Switch direction.

Software writing to either **Doorbell Request** register generates an interrupt if the corresponding **Doorbell Mask** register bit is not masked, and interrupt signaling is enabled.

Chapter 10 Hot Plug Support

10.1 Introduction

Note: *In this chapter, unless stated otherwise, "Hot Plug Controller" references both the Parallel and Serial Hot Plug Controllers.*

Hot Plug capability allows board insertion and removal from a running system, without adversely affecting the system. Boards are typically inserted or removed to repair faulty boards or re-configure the system without system down time. Hot Plug capability allows systems to isolate faulty boards in the event of a failure.

The PEX 8649 includes one Hot Plug Controller per Hot Plug-capable Transparent downstream Port, as well as signals for both Parallel and Serial Hot Plug support. Parallel Hot Plug is supported on any of two Transparent downstream Ports, and/or Serial Hot Plug is supported on the maximum of 11 downstream Ports.

Parallel Hot Plug can be implemented on any Transparent downstream Port, as selected by the **Parallel Hot Plug Control** register (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 3A4h[15:8 and 23:16] for Parallel Hot Plug Controllers B and C, respectively).

Serial Hot Plug can be implemented on any Transparent downstream Port. If a Transparent downstream Port is both Parallel- and Serial Hot Plug-capable, the Serial Hot Plug Controller is used, by default, unless the Port's **Power Management Hot Plug User Configuration** register *Serial Hot Plug Override Parallel Disable* bit (offset F70h[19]) is Set.

Hot Plug signals are enabled, configured and accessed through the **Slot Capability** and **Slot Status and Control** registers (Downstream Ports, offsets 7Ch and 80h, respectively). Also, each Port's **Power Management Hot Plug User Configuration** register provides additional Device-Specific configuration and control, for both Parallel and Serial Hot Plug implementations.

10.2 Hot Plug Features

The following are the PEX 8649 Hot Plug features:

- Hot Plug features are supported on all Transparent downstream Ports.
- Two sets of Hot Plug signals provided for two Parallel Hot Plug Ports.
- Any two Transparent downstream Ports can be programmed as a Parallel Hot Plug Port.
- Additional Hot Plug signals for all other Transparent downstream Ports are implemented with external I^2C I/O Expanders, which alert the PEX 8649 through the SHPC_INT# input, that inputs have toggled, and the PEX 8649 internal Hot Plug Controllers and registers automatically communicate with and control the I/O Expanders, using the PEX 8649 I^2C Master interface (I2C_SCL1 and I2C_SDA1 balls).
- Insertion and removal of PCI Express boards, without removing system power.
- Board Present and Manually operated Retention Latch (MRL) signals are implemented. Presence Detect is accomplished through either an in-band SerDes Receiver Detect mechanism (**Physical Layer Receiver Detect Status** register *Receiver Detected on Lane x* bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 200h[31:16])) – or – by using the HP_PRSNT_*x*# inputs.
- Power Indicator and Attention Indicator Output signals are controlled.
- Attention Button is monitored.
- Power Fault detection and Faulty board isolation.
- Power Controller Control bit for controlling downstream device power.
- Generates Power Management Event (PME) for Hot Plug events in sleeping systems (D3hot Device Power Management (PM) state).
- Electromechanical Interlock Control feature available on Serial Hot Plug-capable Ports.
- Hot Plug interrupts can be sent in-band using INT*x* or MSI Messages, or signaled externally using PEX_INTA# and/or VS*x*_PEX_INTA#.

10.3 Hot Plug Elements

Table 10-1 summarizes the Hot Plug elements required for PCI Express Hot Plug implementation. For specific platform requirements, refer to the PCI Express Form Factor specifications.

Table 10-1. Required Hot Plug Elements for PCI Express Implementation

Element	Purpose
Attention Button	To request Hot Plug operations. Implemented on the PEX 8649's Hot Plug-capable Transparent downstream Ports.
Attention Indicator	Implemented on the PEX 8649's Hot Plug-capable Transparent downstream Ports. LED functions: • **Off** – Standard operation. • **On** – Operational Problem at this slot. • **Blinking** – Slot is being identified at user's request. Blinking frequency is 1 Hz. 50% duty cycle.
Power Indicator	Implemented on the PEX 8649's Hot Plug-capable Transparent downstream Ports. LED functions: • **Off** – Slot is powered off. Board insertion or removal is permitted. • **On** – Board insertion or removal is not permitted. • **Blinking** – Slot is in the process of powering up or down. Blinking frequency is 2 Hz. 50% duty cycle.
MRL	Manually-operated Retention Latch, that holds add-in boards in place.
MRL Sensor	Reports the position of a slot's MRL to the Port. A logic Low indicates that the latch is closed.
Electromechanical Interlock	Prevents removal of adapter from slot.

10.4 Hot Plug Signals

10.4.1 Hot Plug Port External Signals

The on-chip signals for Parallel Hot Plug Controller support are defined in Section 3.4.2.1, "Parallel Hot Plug Signals."

The on-chip signals for Serial Hot Plug Controller support are defined in Section 3.4.2.2, "Serial Hot Plug Signals."

In addition to the set of on-chip Serial Hot Plug signals, the PEX 8649 supports Serial Hot Plug signals to and from the I^2C I/O Expander, which are used with Serial Hot Plug-capable Transparent downstream Ports. (Refer to Section 10.9.2.) Also, although the I^2C I/O Expander provides a Reset output (Serial Hot Plug PERST#), control through the serial interface is too slow for Reset functionality. As a result, the PEX 8649 provides GPIO signals that can be configured for Serial Hot Plug PERST# functionality, to replace the I/O Expander PERST# output. (Refer to the GPIO[31:24] signal description in Table 3-11, "Device-Specific Signals.")

10.4.2 Hot Plug Output States for Disabled Hot Plug Slots

When a Hot Plug slot is disabled, the Hot Plug outputs for that Port are in the logic states defined in Table 10-2.

Table 10-2. Hot Plug Outputs for Disabled Hot Plug Slot

Output Signal	Logic	Comments
HP_ATNLED_*x*#	High	Attention LED is turned Off
HP_CLKEN_*x*#	High	Reference Clock is not driven to the slot
HP_PERST_*x*#	Low	Slot remains in reset
HP_PWREN_*x*	Low	Power Controller is turned Off
HP_PWRLED_*x*#	High	Power LED is turned Off

10.5 Hot Plug Registers

All Transparent downstream Ports and Stations include identical sets of Hot Plug registers, and all Hot Plug Ports use the identical register sets, regardless of whether Hot Plug is implemented using the PEX 8649 Hot Plug signals, or Serial Hot Plug signals on the external I^2C I/O Expanders. Therefore, other than initial configuration (typically programmed by serial EEPROM), whether Hot Plug functionality for a Port is implemented using a Parallel Hot Plug Controller or Serial Hot Plug Controller (with external I^2C I/O Expander) is effectively transparent to software.

The PCI Express Hot Plug Configuration, Capability, Command, Status, and Event registers are described in Section 13.10, “PCI Express Capability Registers (Offsets 68h – A0h).”

Device-Specific Hot Plug configuration features are programmable in register offset F70h of each Station and Transparent downstream Port.

10.6 Hot Plug Interrupts

Refer to Chapter 9, “Interrupts,” for interrupt details.

10.6.1 Software Testing of Hot Plug Interrupts

Hot Plug interrupts can be generated by software (such as for testing Interrupt Handler software), without having to toggle Hot Plug signals to trigger interrupts. **Slot Status** register bits at offset 80h[24:16] (Downstream Ports) are usually Read-Only (RO; as required by the *PCI Express Base r2.0*); however, if the Port’s **Power Management Hot Plug User Configuration** register *Software-Controlled Hot Plug Enable* bit (offset F70h[12]) is Set, the RO *Status* bits that are not Set (in that Port), become writable. When this feature is enabled, if a *Status* bit is Cleared and then software Sets the bit, an interrupt is generated. When the bit is Set, writing 1 again Clears the bit (the same behavior as in standard operation).

This feature can also be used to generate Hot Plug interrupts from the upstream Port(s) (which usually does not generate Hot Plug interrupts), if needed for a particular application.

10.7 Hot Plug Controller Slot Power-Up/Down Sequence

If a Hot Plug-capable Transparent downstream Port is enabled, the Port's Hot Plug Controller can power-up or power-down the slot. This section describes how this process occurs.

10.7.1 Slot Power-Up Sequence

If a Hot Plug-capable Transparent downstream Port is connected to a slot, its associated Hot Plug Controller can power up that slot, with or without an external serial EEPROM. Hot Plug Controller sequencing is determined by the states of the following bits:

- **Slot Capability** register *Power Controller Present* bit (Downstream Ports, offset 7Ch[1])
- **Slot Capability** register *MRL Sensor Present* bit (Downstream Ports, offset 7Ch[2])
- **Slot Control** register *Power Controller Control* bit (Downstream Ports, offset 80h[10])

and the HP_MRL_*x#* input state, if the *MRL Sensor Present* bit is Set. Hot Plug-configurable features are programmable only by the serial EEPROM and/or I^{2}C.

10.7.1.1 Configuring Slot Power-Up Sequence Features with Serial EEPROM

An external serial EEPROM can be used to configure the Hot Plug Controller and Hot Plug outputs. Features can be changed by using the registers defined in Table 10-3. The Hot Plug Controller outputs remain in the default state described in Table 10-2, before the serial EEPROM image is loaded into the device.

After the serial EEPROM image is loaded, the Hot Plug Controller starts a power-up sequence on each slot that has the **Slot Capability** register *Power Controller Present* bit (Downstream Ports, offset 7Ch[1]) Set and **Slot Control** register *Power Controller Control* bit (Downstream Ports, offset 80h[10]) Cleared.

Table 10-3. Configuring Slot Power-Up Sequence Features with Serial EEPROM

Register Bit	Hot Plug Controller and Hot Plug Output Signal Configurable Features
Power Controller Present (**Slot Capability** register, Downstream Ports, offset 7Ch[1])	***Reserved*** for the upstream Port(s) and NT Port. The *Power Controller Present* bit enables or disables the Hot Plug Controller on the PEX 8649 Hot Plug-capable Transparent downstream Ports. If the *Power Controller Present* bit is Cleared, the Hot Plug Controller is disabled for that slot and a power-up sequence is not executed. The slot remains in the disabled state, as defined in Table 10-2. If the *Power Controller Present* bit is enabled (Set), the Hot Plug Controller powers up the slot when the Manually operated Retention Latch (MRL) is closed and the **Slot Control** register *Power Controller Control* bit (Downstream Ports, offset 80h[10]) is Cleared. Otherwise, if the *MRL Sensor Present* bit is disabled (Cleared), the MRL's position has no effect on powering up the slot.
MRL Sensor Present (**Slot Capability** register, Downstream Ports, offset 7Ch[2])	***Reserved*** for the upstream Port(s) and NT Port. When enabled (Set), the PEX 8649 senses whether the MRL is open or closed for a slot. If this bit is Set, the MRL should be Low for power-on for that slot. If this bit is Cleared, the MRL position is "Don't Care" for that slot.
Attention Indicator Present (**Slot Capability** register, Downstream Ports, offset 7Ch[3])	***Reserved*** for the upstream Port(s) and NT Port. When Set, this bit controls whether the HP_ATNLED_*x*# output for the slot drives out Active-Low. Otherwise, this output is not functional on the slot.
Power Indicator Present (**Slot Capability** register, Downstream Ports, offset 7Ch[4])	***Reserved*** for the upstream Port(s) and NT Port. When Set, this bit controls whether the HP_PWRLED_*x*# output for the slot drives out Active-Low. Otherwise, this output is not functional on the slot.
HPC T_{pepv} (**Power Management Hot Plug User Configuration** register, Downstream Ports, offset F70h[4:3])	Functionality associated with this field is enabled only on the downstream Ports. This field indicates the delay from when HP_PWREN_*x* is asserted High, to when power is valid at a slot. (Refer to Section 10.7.1.2.) 00b = Feature is disabled, and HP_PWR_GOOD_*x* input is used for Power Valid 01b = 128 ms 10b = 256 ms 11b = 512 ms
HP_PWR_GOOD_x Active-Low Enable (**Power Management Hot Plug User Configuration** register, offset F70h[6])	Functionality associated with this bit is enabled only on the downstream Ports. Controls the HP_PWR_GOOD_*x* input polarity. (Refer to Section 10.7.1.2.) 0 = HP_PWR_GOOD_*x* is Active-High 1 = HP_PWR_GOOD_*x* is Active-Low

10.7.1.2 Slot Power-Up Sequencing When *Power Controller Present* Bit Is Set

By default, the *Power Controller Present*, *MRL Sensor Present*, and *Power Controller Control* (when the MRL is open) bits are Set on a Hot Plug-capable downstream Port. When the serial EEPROM is not present, present but blank, or programmed with default register values, the Hot Plug Controller is initially powered up, the **PCI Express Capability** register *Slot Implemented* bit (offset 68h[24]) is Set, and the PEX 8649 is in the following state:

1. Hot Plug Controller is enabled for Hot Plug-capable Transparent downstream Port.
2. Slots associated with Hot Plug-capable Transparent downstream Ports are enabled to be powered up.
3. Attention LED (HP_ATNLED_*x*#) and Power LED (HP_PWRLED_*x*#) are High on the slot chassis.

Immediately after the PEX 8649 exits Reset (PEX_PERST# and/or VS*x*_PERST# input goes High), if the Hot Plug-capable Transparent downstream Port's *MRL Sensor Present* bit is Set (default), the HP_MRL_*x*# input for that slot is sampled. If HP_MRL_*x*# input is enabled and asserted (value of 0), the device Clears the *Power Controller Control* bit, to enable slot power-up. If the *Power Controller Control* bit is not Cleared, either by initially enabling it (default) and asserting HP_MRL_*x*#, or by programming both the *MRL Sensor Present* and *Power Controller Control* bit values to 0 in the serial EEPROM, the downstream slot is not powered up and remains in the disabled state, as defined in Table 10-2.

If a slot's *Power Controller Present* bit is Set, and the *Power Controller Control* bit is Cleared (either by initially enabling and asserting HP_MRL_*x*#, or by programming the *MRL Sensor Present* and *Power Controller Control* bits to 0 in the serial EEPROM), the slot starts power-up sequencing with HP_PWREN_*x* and HP_PWRLED_*x*# assertion, following PEX_PERST# and/or VS*x*_PERST# input de-assertion and serial EEPROM initialization. The serial EEPROM initialization delay is determined by the following:

- Serial EEPROM clock (EE_SK) frequency, programmable through the **Serial EEPROM Clock Frequency** register *EepFreq[2:0]* field (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 268h[2:0])
- Number of registers that are programmed to be initialized by the serial EEPROM

The power-up sequence is as follows:

1. The Hot Plug Controller drives HP_PWRLED_*x*# Low, to turn On the Power Indicator, and drives HP_PWREN_*x* High to turn On the external Power Controller.
2. After HP_PWR_GOOD_*x* input is sampled asserted High or T_{pepv} delay following HP_PWREN_*x* assertion, power to the slot is valid and the Hot Plug Controller drives HP_CLKEN_*x*# Low, to turn On the Reference Clock (PEX_REFCLKn/p) to the slot. The T_{pepv} time delay is specified by programming the **Power Management Hot Plug User Configuration** register *HPC* T_{pepv} field (offset F70h[4:3]) to a non-zero value. Values of 01b, 10b, or 11b program the delay to 128, 256, or 512 ms, respectively. The default value, 00b, disables the feature, and uses the HP_PWR_GOOD_*x* input instead.
3. After the 100-ms T_{pvperl} time delay following HP_CLKEN_*x*# assertion, the Hot Plug Controller de-asserts HP_PERST_*x*# to release slot reset.

   Consideration should be given to the combination of the serial EEPROM clock (EE_SK) frequency (programmable through the **Serial EEPROM Clock Frequency** register *EepFreq[2:0]* field (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 268h[2:0])), along with the number of registers to be initialized by serial EEPROM, as well as any delay for cascaded resets through multiple devices, and allow sufficient margin for devices to be ready for Host enumeration.

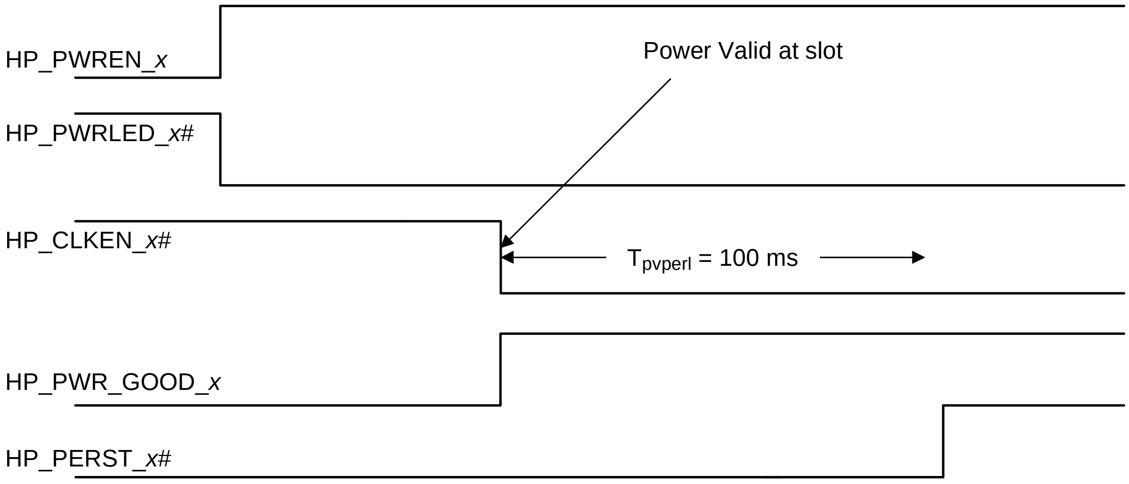
Figure 10-1 illustrates the timing sequence with the *Power Controller Present* bit (Downstream Ports, offset 7Ch[1]) Set. This timing sequence occurs at system power-up, or when a slot is being powered up by the user, using software control.

If HP_MRL_*x*# is enabled but not asserted to power-up the slot immediately after reset, HP_MRL_*x*# can be asserted at runtime to start the slot power-up sequence, provided that the *MRL Sensor Present* and *Power Controller Present* bits (Downstream Ports, offset 7Ch[2:1], respectively) are Set (either by default values when the serial EEPROM is not present or blank, or by programming the serial EEPROM to Set these bits), and the *Power Controller Control* bit (Downstream Ports, offset 80h[10]) is Cleared (either by the programmed serial EEPROM or by software).

Power-up sequencing at runtime is controlled by software Clearing the *Power Controller Control* bit in response to an interrupt caused by HP_MRL_*x*# input assertion (if an MRL Sensor is present, and the **Slot Control** register *Hot Plug Interrupt Enable* and *MRL Sensor Changed Enable* bits (Downstream Ports, offset 80h[5 and 2], respectively) are Set), and/or by the user pressing the Attention Button, if enabled (**Slot Control** register *Hot Plug Interrupt Enable* and *Attention Button Pressed Enable* bits (Downstream Ports, offset 80h[5 and 0], respectively) must be Set).

HP_MRL_*x*# and HP_BUTTON_*x*# assertion and de-assertion at runtime are not latched until the 10-ms de-bounce ensures that the state change is stable.

Figure 10-1. Slot Power-Up Timing When *Power Controller Present* Bit Is Set



Note: *HP_PWRLED_x# is not asserted if the serial EEPROM and/or I^{2}C Slave interface Clears the Power Indicator Present bit (Downstream Ports, offset 7Ch[4]).*

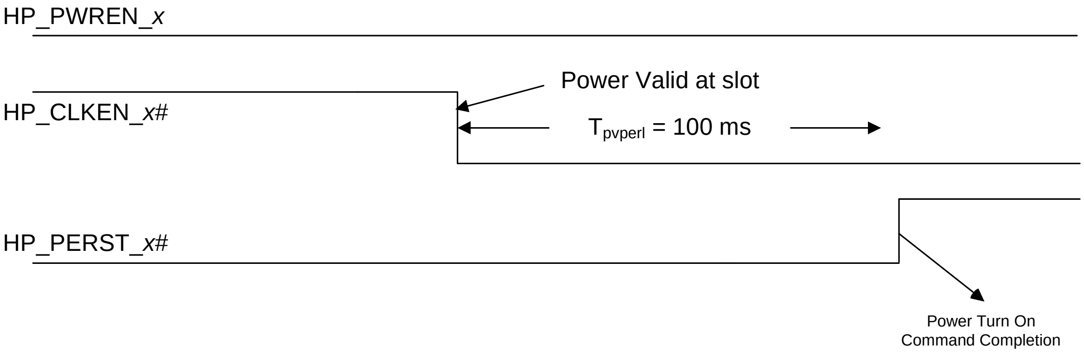
10.7.1.3 HP_PERST_*x*# (Reset) and HP_PWRLED_*x*# Output Power-Up Sequencing When *Power Controller Present* Bit Is Cleared

The HP_PERST_*x*# and HP_PWRLED_*x*# outputs can be used without enabling the Hot Plug Power Controller (HP_PWREN_*x* and HP_CLKEN_*x*# outputs and HP_PWRFLT_*x*# input). *For example*, HP_PERST_*x*# can be used to reset an on-board downstream device.

If the *Power Controller Present* and *Power Controller Control* bits (Downstream Ports, offsets 7Ch[1] and 80h[10], respectively) are Cleared by the serial EEPROM, HP_PERST_*x*# is de-asserted (High) and HP_PWRLED_*x*# is asserted (Low), after the Root Complex PERST# input is de-asserted, as illustrated in Figure 10-2. However, HP_PWRLED_*x*# is not asserted if the serial EEPROM also Cleared the *Power Indicator Present* bit (Downstream Ports, offset 7Ch[4]).

If the serial EEPROM is initially blank, causing register default values to be loaded, HP_PERST_*x*# is asserted and HP_PWRLED_*x*# is not asserted unless HP_MRL_*x*# is Low. Therefore, if the HP_PERST_*x*# and/or HP_PWRLED_*x*# outputs are used (and an MRL is ***not*** used), pull HP_MRL_*x*# Low, to allow the outputs to toggle, regardless of whether the serial EEPROM is blank.

Figure 10-2. Hot Plug Outputs When *Power Controller Present* and *Power Controller Control* Bits Are Cleared



Note: *HP_PWRLED_x# is not asserted if the serial EEPROM and/or I^{2}C Slave interface Clears the Power Indicator Present bit (Downstream Ports, offset 7Ch[4]).*

10.7.1.4 Disabling Power-Up Hot Plug Output Sequencing

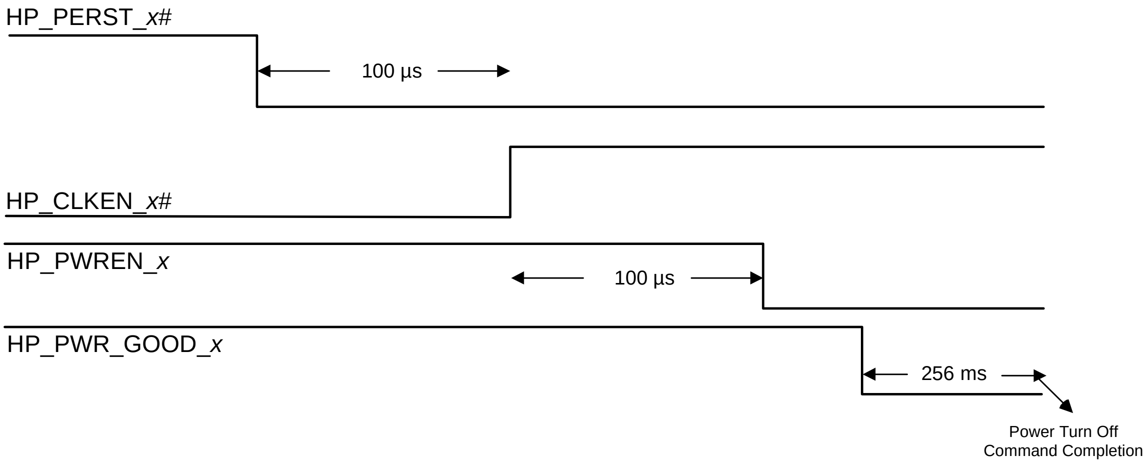
If the *Power Controller Control* bit is Set, after reset using the serial EEPROM, the HP_PWRLED_*x*#, and HP_CLKEN_*x*# outputs remain High, and the HP_PERST_*x*# and HP_PWREN_*x* outputs remain Low. The HP_PWRLED_*x*# and HP_CLKEN_*x*# outputs also remain High if HP_MRL_*x*# is not asserted in the default Hot Plug power-up sequencing described in Section 10.7.1.2.

10.7.2 Slot Power-Down Sequence

Software can power-down slots by Setting the *Power Controller Control* bit (Downstream Ports, offset 80h[10]). If the *MRL Sensor Present* bit (Downstream Ports, offset 7Ch[2]) is Set, the Hot Plug Controller automatically powers down the slot if the MRL is open. Figure 10-3 illustrates the following power-down timing sequence for either event:

1. HP_PERST_*x*# to the Port is asserted.
2. HP_CLKEN_*x*# is de-asserted to the slot 100 µs after HP_PERST_*x*# is asserted.
3. HP_PWREN_*x* is de-asserted to the slot 100 µs after HP_CLKEN_*x*# is de-asserted.

Figure 10-3. Hot Plug Automatic Power-Down Sequence



10.8 Default Parallel Hot Plug Ports

In Base mode and Virtual Switch mode, different schemes are used to assign the Parallel Hot Plug Ports. In addition, the PEX 8649 can maintain a Serial Hot Plug Controller on all Transparent downstream Ports.

10.8.1 Default Parallel Hot Plug Ports – Base Mode

The **Parallel Hot Plug Control** register (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 3A4h[15:8 and 23:16] for Parallel Hot Plug Controllers B and C, respectively) indicates the Hot Plug Port assignments, and whether the respective Parallel Hot Plug Controllers are enabled. Table 10-4 lists the default Hot Plug Ports in Base mode.

Hot Plug Ports can also be assigned by serial EEPROM, or by I^{2}C (when the STRAP_I2C_CFG_EN# input is Low, to delay linkup until I^{2}C initialization is complete) writes to the **Parallel Hot Plug Control** register.

Table 10-4. Default Hot Plug Ports – Base Mode

Hot Plug Port	
B	**C**
16	20

10.8.2 Default Parallel Hot Plug Ports – Virtual Switch Mode

The **Parallel Hot Plug Control** register (Port 0, accessible through the Management Port, offset 3A4h[15:8 and 23:16] for Parallel Hot Plug Controllers B and C, respectively) indicates the Hot Plug Port assignments and whether the respective Parallel Hot Plug Controllers are enabled.

Table 10-5 lists the PEX 8649's default Parallel Hot Plug Ports in Virtual Switch mode. The default values can be overridden by:

- Serial EEPROM
- I^{2}C, when the STRAP_I2C_CFG_EN# input is Low to delay linkup until I^{2}C Sets the **Configuration Release** register *Initiate Configuration* bit (Port 0, offset 3ACh[0])
- Management Port software, when STRAP_NT_UPSTRM_PORTSEL0 is Low, to delay linkup (of Non-Management Ports) until Management Port software Sets the *Initiate Configuration* bit

If a designated Transparent downstream Port in the Virtual Switch does not exist, the set of Hot Plug signals reserved for that Port is not re-assigned to another Port, unless the **Parallel Hot Plug Control** register is programmed accordingly, by serial EEPROM, I^{2}C, or the Management Port. The serial EEPROM, I^{2}C, and/or Management Port Hot Plug-capable Port assignments always take precedence over the hardware-selected Hot Plug-capable Port assignments. If these three agents do not write into the **Parallel Hot Plug Control** register, the hardware updates the register to select the Hot Plug-capable Ports.

Table 10-5. Virtual Switch Port Configurations and Default Parallel Hot Plug Ports – Virtual Switch Mode

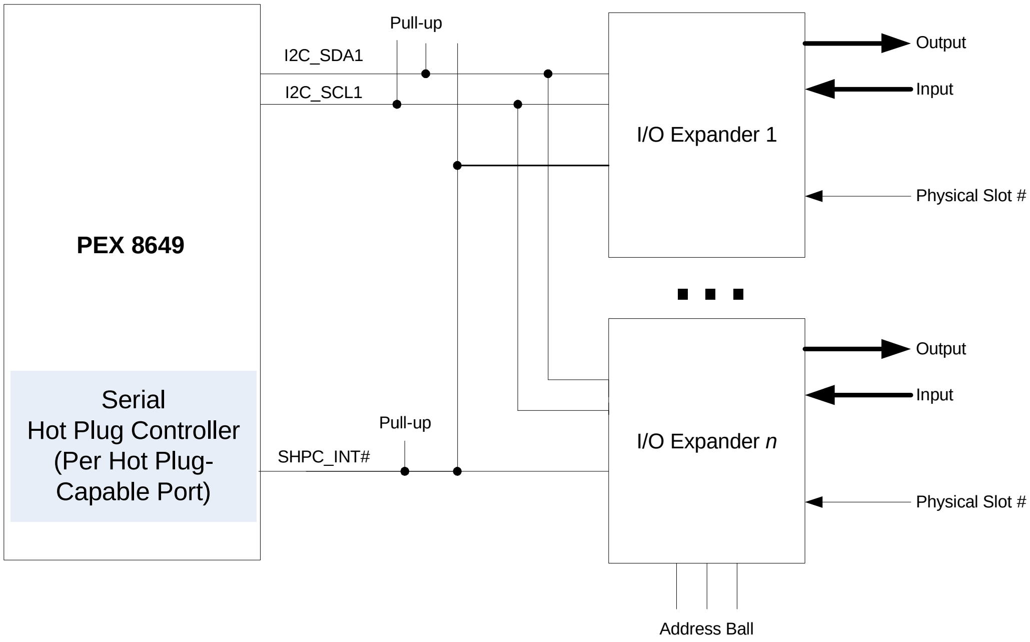
Number of Virtual Switches	STRAP_VS_MODE[1:0] Value	Upstream Ports	Downstream Ports	Default Hot Plug Ports and Balls
2	LH	P0	P1, P2, P3, P20, P21	P20-B
		P16	P17, P18, P19, P22, P23	P22-C
3	HL	P0	P1, P2, P3	P1-B
		P16	P17, P18, P19	P17-C
		P20	P21, P22, P23	
4	HH	P0	P1, P2	P1-B
		P16	P3, P17	P3-C
		P20	P21, P18	
		P22	P23, P19	

10.9 Serial Hot Plug Controller

Note: *The I^{2}C Master interface is described in this section. The Master capabilities are limited to the Serial Hot Plug Controller.*

Using I/O Expander ICs sitting on an I^{2}C Bus, the PEX 8649 has the option of Hot Plug capability on all its Transparent downstream Ports. Figure 10-4 illustrates the internal Serial Hot Plug Controller interface. The Serial Hot Plug Controller controls the output Ports on the I/O Expanders and retrieves the Port status, *such as* device connect status, Power Fault, and MRL Sensor position, from all I/O Expanders. When there is an input change to an I/O Expander, an INT*x* interrupt from an I/O Expander goes Low and the PEX 8649 reads the I/O Expander. When an I/O Expander output Port requires updating with a new value, the PEX 8649 writes to the I/O Expander through the I^{2}C Bus.

Figure 10-4. Serial Hot Plug Interface Diagram



10.9.1 Hot Plug Operations by way of External I^2C I/O Expander

When software issues a Slot Power On command, the Serial Hot Plug Controller issues an I^2C Write to the I/O Expander, to assert the PWREN output on the I/O Expander, and thereby turn On the power. After the Write is complete, either the HP_PWR_GOOD_*x* input is sampled asserted or the T_{pepv} time has elapsed, the Serial Hot Plug Controller issues another Write to the I/O Expander, to assert its RECLKEN# output, and thereby turn On the Reference Clock (REFCLK) at the slot.

Note: *The T_{pepv} value is used when the HP_PWR_GOOD_x input is not used, as indicated by the* ***Power Management Hot Plug User Configuration*** *register HPC T_{pepv} field, offset F70h[4:3], not being Cleared (Cleared is the default).*

After the RECLKEN# output is asserted, the Serial Hot Plug Controller waits 100 ms, then issues another Write, to de-assert the I/O Expander PERST# output to the slot. If there are commands, *such as* Attention or Power LED changes along with the Power Control command, the Serial Hot Plug Controller includes the LED output value change, along with these Writes, to change the LED status. The same procedure applies to other commands, *such as* Port Power Off. After the Serial Hot Plug Controller completes all Write operations, it Sets the *Command Completed* bit. When another command is issued before the current command completes, the results are undefined. With a 100-kHz I^2C clock, the time required to complete one Write operation to an I/O Expander is approximately 1 ms.

10.9.2 External I^{2}C I/O Expander Parts Selection and Pin Definition

Two types of I/O Expanders can be used for Serial Hot Plug:

- **16-bit device** – For the 16-bit device, the 7-bit I^{2}C address must be 010X_XXXb; a Maxim MAX7311, NXP PCA9555, or TI PCA9555 is recommended. I/O Expander addresses must begin with the lowest address (0100_000b), and increment sequentially (corresponding to increasing PEX 8649 Port Numbers), for each device. For MAX7311 (which supports more than the eight addresses provided by the other 16-bit devices), the 7-bit I^{2}C addresses can be in two ranges, 010X_XXXb and 1010_XXXb. All 16 I/O pins of the devices are used for one Port. A 16-bit device supports one Serial Hot Plug Port. (Refer to Figure 10-5.)

  For further details, refer to the manufacturer’s data sheets for the Maxim MAX7311, NXP PCA9555, or TI PCA9555.
- **40-bit device** – For the 40-bit device, the 7-bit I^{2}C address must be within two ranges, 0100_XXXb and 1010_XXXb; an NXP PCA9698 is recommended. I/O Expander addresses must begin with the lowest address, and increment sequentially (corresponding to increasing PEX 8649 Port Numbers), for each device. The lower 32 I/O pins are used for two Ports. A 40-bit device can support two sets of Serial Hot Plug pins. The two sets are indicated with suffix PX and PY, in Figure 10-6.

  For further details, refer to the manufacturer’s data sheet for the NXP PCA9698.

The PEX 8649 can concurrently support up to 23, 16-bit I/O Expanders or 12, 40-bit I/O Expanders, or a mix of 16- and 40-bit I/O Expanders, to provide Hot Plug services on all Transparent downstream Ports. (Refer to the **Power Management Hot Plug User Configuration** register *40-Pin I/O Expander Scan Disable* bit, offset F70h[17]). The NXP PCA9555 and Texas Instruments PCA9555 devices have only eight programmable I^{2}C addresses; therefore, the maximum number of Serial Hot Plug-capable Ports with these I/O Expanders is eight. However, the Maxim MAX7311 can have up to 64 programmable Slave addresses; therefore, if using the MAX7311 I/O Expanders, all Transparent downstream Ports can be made Hot Plug-capable.

Table 10-6 defines the external I^{2}C I/O Expander pins, in location order.

Table 10-6. External I^{2}C I/O Expander Pin Definitions, by Location

Signal Name	Direction	Description	Location	
			16-Bit Device[a]	40-Bit Device[b]
PWRLED#	O	**Hot Plug Power LED Output** Same function as HP_PWRLED_*x*#.	IO0_0 or P00	IO0_0 IO2_0
ATNLED#	O	**Hot Plug Attention LED Output** Same function as HP_ATNLED_*x*#.	IO0_1 or P01	IO0_1 IO2_1
PWREN	O	**Hot Plug Power Enable Output** Same function as HP_PWREN_*x*.	IO0_2 or P02	IO0_2 IO2_2
RECLKEN#	O	**Hot Plug Reference Clock Enable Output** Same function as HP_CLKEN_*x*#.	IO0_3 or P03	IO0_3 IO2_3
PERST#	O	**Hot Plug Reset Output** Same function as HP_PERST_*x*#.	IO0_4 or P04	IO0_4 IO2_4
INTERLOCK	O	**Electromechanical Interlock Output Control** Used to physically lock the adapter or MRL in place until software releases it. The signal default is 0. The current state of the Electromechanical Interlock is reflected in the **Slot Status** register *Electromechanical Interlock Status* bit (Downstream Ports, offset 80h[23]). This output can be toggled by writing 1 to the **Slot Control** register *Electromechanical Interlock Control* bit (Downstream Ports, offset 80h[11]). A Write of 0 has no effect. INTERLOCK is enabled when the **Slot Capability** register *Electromechanical Interlock Present* bit (Downstream Ports, offset 7Ch[17]) is Set (default for Serial Hot Plug-capable Transparent downstream Ports).	IO0_5 or P05	IO0_5 IO2_5

PORTID[4:0]	I	**Hot Plug Port ID Straps**
		Configures to which downstream Port this I^{2}C I/O Expander maps. Valid values are 0_0000b to 1_0111b.
		1_1111b is valid only for 16-bit devices, for loading the **Slot Capability** register *Physical Slot Number* field (Downstream Ports, offset 7Ch[31:19]) from the I/O Expander SLOTID inputs.
			{IO1_2:0, IO0_7:6}
			or
			{P1[2:0], P0[7:6]}
				{IO1_2:0, IO0_7:6}
				{IO3_2:0, IO2_7:6}

PRSNT#	I	**Hot Plug PRSNT2# Input** Same function as HP_PRSNT_*x*#.	IO1_3 or P13	IO1_3 IO3_3
MRL#	I	**Hot Plug Manually Operated Retention Latch Sensor Input** Same function as HP_MRL_*x*#.	IO1_4 or P14	IO1_4 IO3_4

Table 10-6. External I^{2}C I/O Expander Pin Definitions, by Location *(Cont.)*

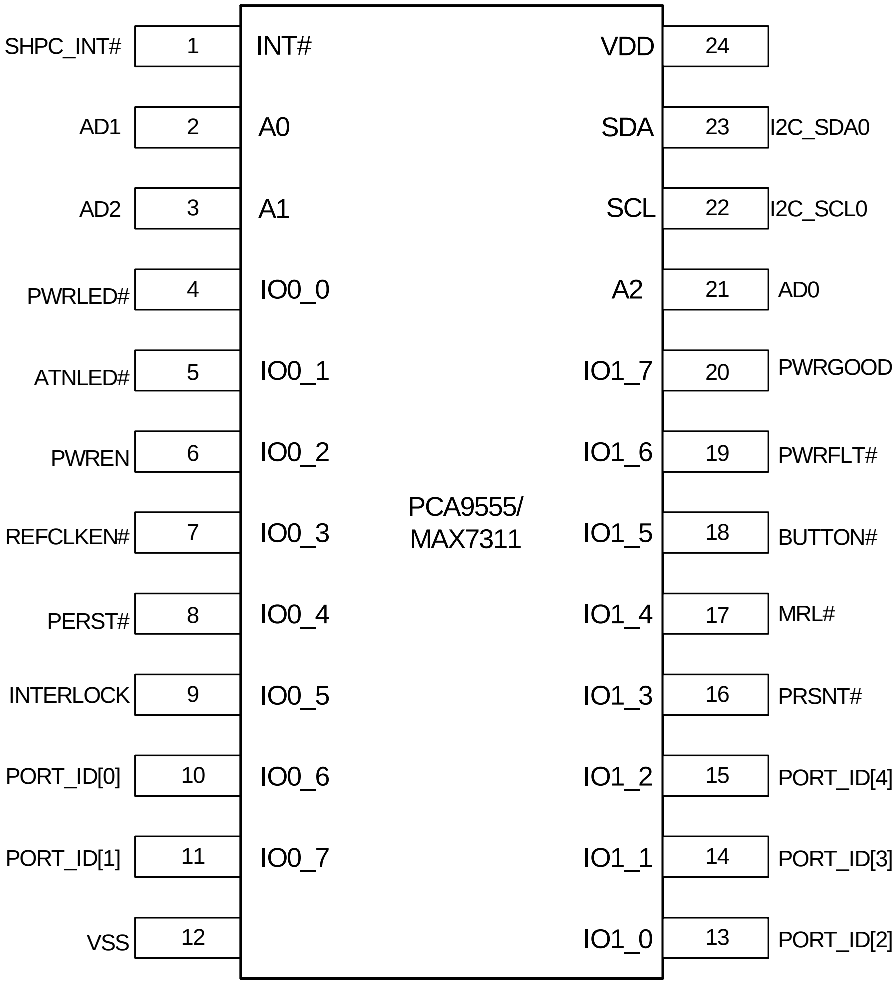
Signal Name	Direction	Description	Location	
			16-Bit Device[a]	40-Bit Device[b]
BUTTON#	I	**Hot Plug Attention Button Input** Same function as HP_BUTTON_*x*#.	IO1_5 or P15	IO1_5 IO3_5
PWRFLT#	I	**Hot Plug Power Fault Input** Same function as HP_PWRFLT_*x*#.	IO1_6 or P16	IO1_6 IO3_6
PWRGOOD	I	**Hot Plug Power Good Input** Same function as HP_PWR_GOOD_*x*.	IO1_7 or P17	IO1_7 IO3_7

SLOTID[12:5]	I	**Hot Plug Slot ID**
		Sets the value of the upper 8-bits of the **Slot Capability** register *Physical Slot Number* field (Downstream Ports, bits [31:24] of offset 7Ch[31:19]; the lower 5-bits ([23:19]) are automatically Set equal to the Port Number of the Hot Plug-capable Port).
		The 40-bit I/O Expander has provision for two sets of SLOTID inputs, for two Hot Plug-capable Ports. With 16-bit I/O Expanders, the device can be used either for Serial Hot Plug functionality or SLOTID.
			{IO0_5:0, IO1_7:6}
			or
			{P0[5:0], P1[7:6]}
				IO4_7:0

a. *Refer to Figure 10-5 for pinout.*

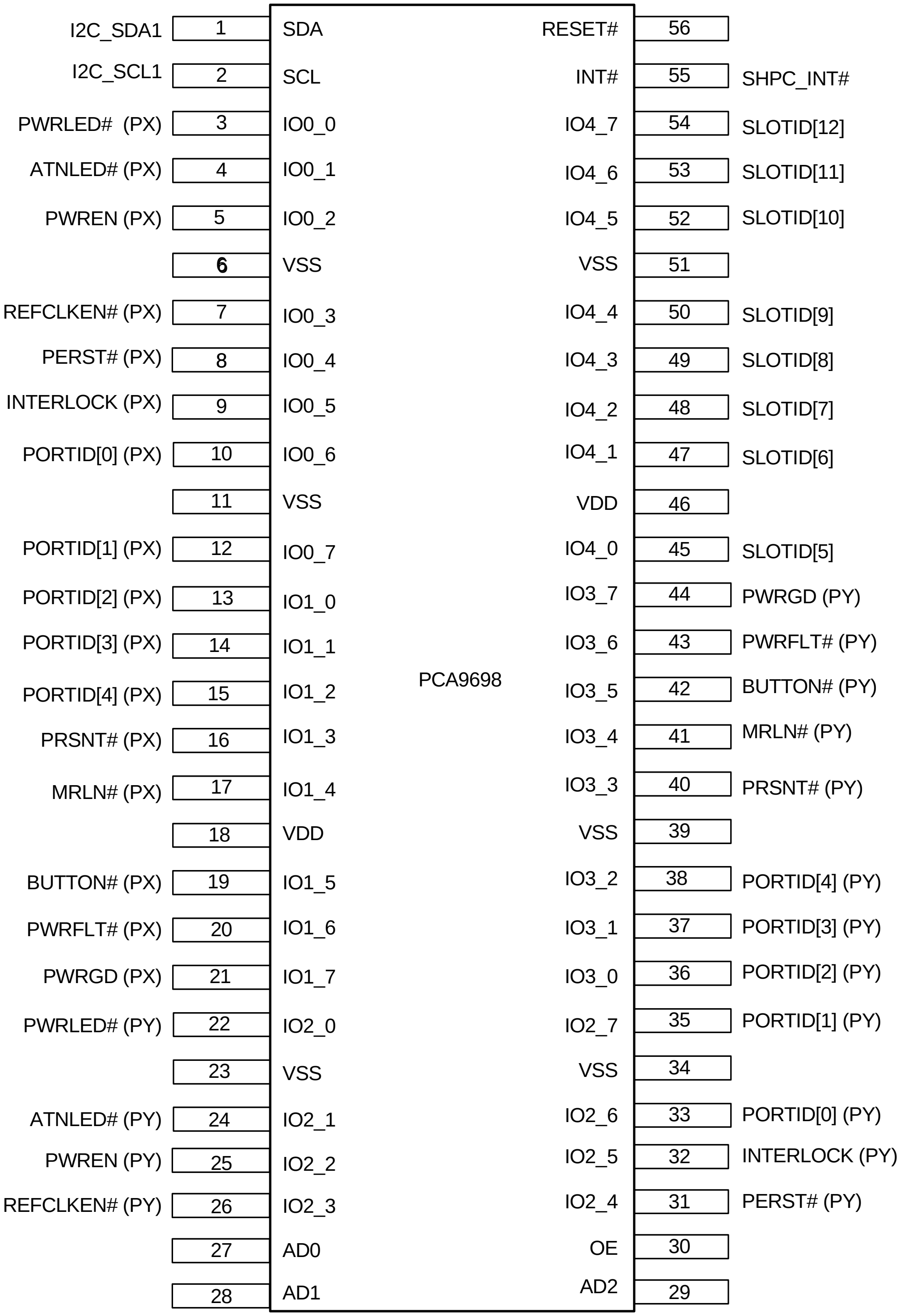
b. *Refer to Figure 10-6 for pinout.*

Figure 10-5. 16-Bit I²C I/O Expander Pinout



Note: *PWRGOOD polarity is Active-High, by default; however, it can be changed to Active-Low, by Setting the HP_PWR_GOOD_x Active-Low Enable bit (offset F70h[6]) in the corresponding Transparent downstream Port(s).*

Figure 10-6. 40-Bit I^{2}C I/O Expander Pinout



Note: *PWRGOOD polarity is Active-High, by default; however, it can be changed to Active-Low, by Setting the HP_PWR_GOOD_x Active-Low Enable bit (offset F70h[6]) in the corresponding Transparent downstream Port(s).*

10.9.3 Serial Hot Plug Port Enumeration, Assignment, and Initialization

Serial Hot Plug can be implemented using either 16- or 40-bit I^{2}C I/O Expanders, or a combination of both. The PEX 8649 Serial Hot Plug Controller has the intelligence to discover and differentiate between the 16- and 40-bit I/O Expanders, and assigns the I/O Expanders to a corresponding Transparent downstream Port. The 16-bit I/O Expanders can support one Serial Hot Plug Port, and 40-bit I/O Expanders can support one or two Ports.

After PEX_PERST# and/or VS*x*_PERST# input de-asserts and the serial EEPROM (if present) load completes, the Serial Hot Plug Controller scans the I^{2}C Bus for I/O Expanders, starting with Device address 0100_000b. If the Controller receives an Acknowledge (ACK) from the I/O Expander, it performs a Device ID code Read from that I/O Expander, to detect the presence of a 40-bit I/O Expander (40-bit device scan is enabled, by default). This scan can be disabled, by Setting the Port's **Power Management Hot Plug User Configuration** register *40-Pin I/O Expander Scan Disable* bit (offset F70h[17]) in the Transparent downstream Ports. If the Device ID code Read fails, that I/O Expander is identified as a 16-bit I/O Expander, and the PORTID[4:0] setting on the 16-bit I/O Expander determines with which PEX 8649 Port the I/O Expander is associated. If the Device ID code Read fetches the correct Device ID, that I/O Expander is identified as being 40-bit capable. The two PEX 8649 Serial Hot Plug Ports that correspond to the two sets of Hot Plug pins in a 40-bit I/O Expander are determined from two PORTID[4:0] settings. Valid PORTID[4:0] values are 0_0000b to 1_0111b.

The Serial Hot Plug Controller logic uses the I^{2}C Master interface to program the I/O Expander's I/O Configuration registers, and Sets the initial Hot Plug state for successfully scanned I/O Expanders. (Refer to Table 10-2 for the initial states of the Hot Plug outputs.) On an I/O Expander scan, if the Serial Hot Plug Controller receives a Negative Acknowledge (NAK), the Hot Plug Controller stops scanning for I^{2}C I/O Expanders. After the I^{2}C scan is complete, the Serial Hot Plug Controller starts the slot power-on sequence for Ports in which the following is true:

- MRL# input is sampled Low (**Slot Status** register *MRL Sensor State* bit (Downstream Ports, offset 80h[21], is Cleared), and
- **Slot Control** register *Power Controller Control* bit (Downstream Ports, offset 80h[10]) is not Set by the serial EEPROM load

The I^{2}C address for the I/O Expanders must be contiguous, with the first I/O Expander's I^{2}C address programmed to 0100_000b, the next programmed to 0100_001b, and so forth.

10.9.4 I^{2}C I/O Expander Interrupt Processing

The I/O Expander Interrupt outputs (INT#) must all be connected together in an Open Drain manner, to the SHPC_INT# input on the PEX 8649. When an I/O Expander Input state changes on any of the I/O Expanders, the PEX 8649 SHPC_INT# input is asserted Low. The Serial Hot Plug Controller, through the I^{2}C Bus, scans the I/O Expanders, starting with address 40h, until the SHPC_INT# input de-asserts High (as a result of the I^{2}C Read), signaling which I/O Expander asserted the interrupt (INT#). SHPC_INT# is internally de-bounced for 10 ms; therefore, if SHPC_INT# asserts Low for less than 10 ms, its assertion is ignored. The 10 ms de-bounce on the SHPC_INT# input can be disabled, by Setting the Port's **Power Management Hot Plug User Configuration** register *Serial Hot Plug INTx De-Bounce Disable* bit (offset F70h[18]). SHPC_INT# assertion due to an I/O Expander Input state change can cause a corresponding PEX 8649 **Slot Status** register bit to be Set, and cause the Port to send an INT*x* Message to the Root Complex, if the corresponding interrupt is enabled.

10.9.5 Serial Hot Plug-Capable Port Command Completion

For slot power ON or OFF commands from software to turn power ON or OFF to a specific Port, the Port's **Slot Status** register *Command Completed Interrupt Enable* bit (Downstream Ports, offset 80h[4]) is Set after the sequence of I^{2}C Master Write operations to the I/O Expander, that perform the power ON or OFF sequence, have completed.

10.9.6 Physical Slot Number Loading from I^{2}C I/O Expander

The **Slot Capability** register *Physical Slot Number* field (Downstream Ports, offset 7Ch[31:19]) is assigned a unique identifier, for each Port. The register's MSB [31:24] can be loaded from the SLOTID[12:5] input settings on the I/O Expander, and the SLOTID[12:5] inputs on all I/O Expanders should be strapped to the same non-zero value. The 40-bit I/O Expander has SLOTID[12:5] inputs implemented along with two sets of Hot Plug pins. This SLOTID[12:5] input Sets the *Physical Slot Number* field in all Transparent downstream Ports in which the **Slot Capability** register has not been programmed by serial EEPROM. The LSB [4:0] (bits [23:19]) of the Physical Slot Number are loaded with the Port Number of that PEX 8649 Port. The combination of SLOTID and Port Number forms a unique Physical Slot Number value, for each PEX 8649 Port.

For 16-bit I/O Expanders, the SLOTID[12:5] I/O pins are multiplexed with other Hot Plug functional pins. When PORTID[4:0] on a 16-bit I/O Expander is programmed to 1_1111b, the set of {IO0_5:0, IO1_7:6} or {P0[5:0], P1[7:6]} pins are sampled as SLOTID, and the *Physical Slot Number* field is Set accordingly.

Note: *16-bit I/O Expanders that have PORTID[4:0] Set as 1_1111b cannot be used for Serial Hot Plug operation, because that setting is used only for the Physical Slot Number field setting, as explained in Table 10-6. An alternative is to use the serial EEPROM to program the* ***Slot Capability*** *register.*

10.10 Hot Plug Board Insertion and Removal Process

Table 10-7 defines the board insertion procedure supported by the PEX 8649. Table 10-8 defines the board removal procedure. Both processes apply to Parallel and Serial Hot Plug-capable Transparent downstream Ports.

Table 10-7. Hot Plug Board Insertion Process

Operator / Action	Hot Plug Controller	Software
A. Places board in slot.	**1.** Sets the *Presence Detect State* bit. **2.** Sets the *Presence Detect Changed* bit. **3.** Generates Interrupt Message due to Presence Detect Changed event, if enabled.	Clears *Presence Detect Changed* bit.
	4. Transmits an Interrupt de-assertion Message, if enabled.	
B. Locks MRL.	**5.** Clears the *MRL Sensor State* bit. **6.** Sets the *MRL Sensor Changed* bit. **7.** Generates an Interrupt Message due to MRL Sensor Changed event, if enabled.	Clears the *MRL Sensor Changed* bit.
	8. Transmits an Interrupt de-assertion Message, if enabled.	
C. Presses Attention Button.	**9.** Sets the *Attention Button Pressed* bit. **10.** Generates an Interrupt Message due to Attention Button Pressed event, if enabled.	Clears the *Attention Button Pressed* bit.
	11. Transmits an Interrupt de-assertion Message, if enabled.	Programs the **Slot Control** register *Power Indicator Control* field value to 10b, to blink the Power Indicator LED, which indicates that the board is being powered up.

Continued…

Table 10-7. Hot Plug Board Insertion Process *(Cont.)*

Operator / Action	Hot Plug Controller	Software
D. Power Indicator blinks.	**12.** Blinks the Power Indicator LED. **13.** Sets the *Command Completed* bit. **14.** Generates an Interrupt Message due to Power Indicator Blink command Completion, if enabled.	Clears the *Command Completed* bit.
	15. Transmits an Interrupt de-assertion Message, if enabled.	Clears the **Slot Control** register *Power Controller Control* bit, to turn On power to the Port.
	16. Slot is powered up. **17.** After HP_PWR_GOOD_*x* input is sampled asserted High or T_{pepv} delay, Sets the *Command Completed* bit. **18.** Generates an Interrupt Message due to Power Turn On command Completion, if enabled.	Clears the *Command Completed* bit.
	19. Transmits an Interrupt de-assertion Message, if enabled.	Programs the **Slot Control** register *Power Indicator Control* field value to 01b, to turn On the Power Indicator LED, which indicates that the slot is fully powered On.
E. Power Indicator On.	**20.** Turns On the Power Indicator LED. **21.** Transmits an Interrupt assertion Message due to Power Indicator Turn On command Completion, if enabled.	Clears the *Command Completed* bit.
	22. Transmits an Interrupt de-assertion Message, if enabled. **23.** After the Data Link Layer is up, Sets the **Slot Status** register *Data Link Layer State Changed* bit (Downstream Ports, offset 80h[24]), and transmits the corresponding interrupt, if enabled.	Software can now read the **Link Status** register *Data Link Layer Link Active* bit (offset 78h[29]). A value of 1 in this bit indicates that the board is ready to be used. Clears the *Data Link Layer State Changed* bit and interrupt, if enabled.
	24. Transmits an Interrupt de-assertion Message, if enabled.	

Table 10-8. Hot Plug Board Removal Process

Operator / Action	Hot Plug Controller	Software
A. Presses Attention Button.	**1.** Sets the *Attention Button Pressed* bit. **2.** Generates an Interrupt Message due to Attention Button pressed, if enabled.	Clears the *Attention Button Pressed* bit.
	3. Transmits an Interrupt de-assertion Message, if enabled.	Programs the **Slot Control** register *Power Indicator Control* field value to 10b, to blink the Power Indicator LED, which indicates that the board is being powered down.
B. Power Indicator blinks.	**4.** Blinks the Power Indicator LED. **5.** Sets the *Command Completed* bit. **6.** Generates an Interrupt Message due to Power Indicator Blink command Completion, if enabled.	Clears the *Command Completed* bit.
	7. Transmits an Interrupt de-assertion Message, if enabled.	Sets the **Slot Control** register *Power Controller Control* bit, to turn Off power to the Port.
C. Power Indicator Off.	**8.** Slot is powered Off. **9.** Sets the *Data Link Layer State Changed* bit, and transmits an interrupt, if enabled. **10.** After a 256-ms delay from HP_PWR_GOOD_*x* sampled de-asserted (if HP_PWR_GOOD_*x* input is enabled through the *HPC* T_{pepv} field (offset F70h[4:3], are both Cleared)), Sets the *Command Completed* bit. **11.** Generates an Interrupt Message due to Power Turn Off command Completion, if enabled.	Clears the *Data Link Layer State Changed* bit and interrupt. Clears the *Command Completed* bit. Programs the *Power Indicator Control* field value to 11b, to turn Off the Power Indicator LED, which indicates that the slot is fully powered Off and the board can be removed.
D. Power Indicator Off, board ready to be removed.	**12.** Turns Off the Power Indicator LED. **13.** Sets the *Command Completed* bit, due to Power Indicator Off command Completion.	Clears the *Command Completed* bit.
	14. Transmits an Interrupt de-assertion Message, if enabled.	
E. Unlocks MRL.	**15.** Sets the *MRL Sensor State* bit. **16.** Sets the *MRL Sensor Changed* bit. **17.** Generates an Interrupt Message due to MRL Sensor state change, if enabled.	Clears the *MRL Sensor Changed* bit.
	18. Transmits an Interrupt de-assertion Message, if enabled.	
F. Removes board from slot.	**19.** Clears the *Presence Detect State* bit. **20.** Sets the *Presence Detect Changed* bit. **21.** Generates an Interrupt Message due to Presence Detect change, if enabled.	Clears the *Presence Detect Changed* bit.
	22. Transmits an Interrupt de-assertion Message, if enabled.	

Chapter 11 Power Management

11.1 Overview

The PEX 8649 Power Management (PM) features provide the following services:

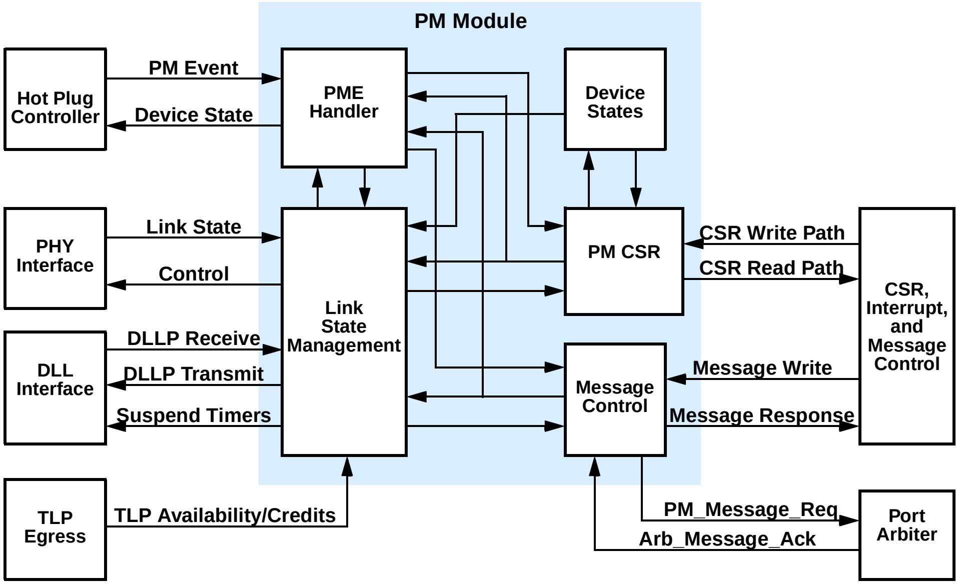
- Mechanisms to identify PM capabilities
- Ability to transition into certain PM states
- Notification of the current PM state of each Port
- Support for the option to wakeup the system upon a specific event

The PEX 8649 supports hardware-autonomous PM and software-driven D-State PM. The switch also supports the L0s and L1 Link PM states in hardware-autonomous Active State Power Management (ASPM), as well as the L1, L2/L3 Ready, and L3 Link PM states in Conventional PCI-compatible PM. D0, D3hot, and D3cold Device PM states are supported in Conventional PCI-compatible PM. Because the PEX 8649 does ***not support*** Vaux, Power Management Event (PME) generation from the D3cold Device PM state is ***not supported***.

The PM module interfaces with a Physical Layer (PHY) electrical sub-block, to transition the Link state into a low-power state, when the module receives a Power State Change Request from a downstream component, or an internal event forces the Link state entry into low-power states in hardware-autonomous ASPM mode. PCI Express Link states are not directly visible to Conventional PCI Bus driver software; however, they are derived from the PM state of the components residing on those Links.

Figure 11-1 provides a functional block diagram of the PEX 8649 PM module.

Figure 11-1. PM Module Functional Block Diagram



Note: *The Hot Plug Controller is available only on Hot Plug-capable Transparent downstream Ports.*

11.2 Power Management Features

- *PCI Express Base r2.0*-compliant
- *PCI Power Mgmt. r1.2*-compliant
- Link Power Management States (*L-States*; also referred to as *Link PM states*)
  - PCI Bus Power Management – L1, L2/L3 Ready, and L3 (Vaux is ***not supported***)
  - Active State Power Management (ASPM) – L0s and L1
- Device Power Management State (*D-States*; also referred to as *Device PM states*)
  - D0 (D0uninitialized and D0active) and D3 (D3hot and D3cold) support
- Power Management Event (PME) support from D3hot
- PME due to Hot Plug and/or PCI Express Hot Plug events
- Forwards PME_Turn_Off broadcast messages
- Supports Clock Power Management using CLK_REQ#
- Implements Gen 2-specific Control and Status registers, and associated interrupts
- Supports ASPM L0s, ASPM L1, PCI PM L1, and L2/L3 Ready Link PM states in NT mode, as well as Virtual Switch mode

11.3 Power Management Capability

11.3.1 Device Power Management States

The PEX 8649 supports the PCI Express PCI-PM D0 and D3hot Device PM states. The D1 and D2 Device PM states, which are optional in the *PCI Express Base r2.0*, are ***not supported*** by the PEX 8649.

The D3hot Device PM state can be entered from the D0 Device PM state, when system software programs the Port’s **PCI Power Management Status and Control** register *Power State* field (offset 44h[1:0]) to 11b. The D0uninitialized Device PM state can be entered from the D3hot Device PM state when system software Clears the Port’s *Power State* field.

11.3.1.1 D0 Device Power Management State

The D0 Device PM state is divided into two distinct sub-states – *uninitialized* and *active*. When power is initially applied to a PCI Express component, it defaults to the D0uninitialized Device PM state. The component remains in the D0uninitialized Device PM state until the serial EEPROM load and initial Link training completes.

A device enters the D0active Device PM state when system software Sets any combination of the **PCI Command** register *Bus Master Enable*, *Memory Access Enable*, and/or *I/O Access Enable* bits (offset 04h[2, 1, and/or 0], respectively).

11.3.1.2 D3hot Device Power Management State

Once in the D3hot Device PM state, the PEX 8649 can later be transitioned into the D3cold Device PM state, by removing power from its Host component. Functions that are in the D3hot Device PM state can be transitioned, by software, to the D0uninitialized Device PM state. When in the D3hot Device PM state, Hot Plug or Link State operations cause a PME in the PEX 8649.

Only Type 0 Configuration accesses are allowed in the D3hot Device PM state. Memory and I/O transactions result in an Unsupported Request (UR). Completions flowing in either direction are not affected.

Type 1 transactions flowing toward a PEX 8649 Port in the D3hot Device PM state are terminated as URs. Type 0 Configuration transactions complete successfully. When an PEX 8649 upstream Port is programmed to the D3hot Device PM state, the Port initiates Conventional PCI-PM L1 Link PM state entry.

11.3.2 Link Power Management States

PEX 8649 components hold their upstream and downstream Links in the L0 Link PM state when they are in the standard operational state (Conventional PCI-PM state is in the D0active Device PM state). ASPM defines a mechanism for components in the D0 Device PM state, to reduce Link power by placing their Links into a low-power state and instructing the other end of the Link to do likewise. This allows hardware-autonomous, dynamic Link power reduction beyond what is achievable by software-only-controlled PM. Table 11-1 defines the relationships between the Power state of a component and its upstream Link. Table 11-2 defines the relationships between Link PM states and power-saving actions.

Conventional PCI PM, and the L1 and L2/L3 Ready Link PM states are controlled by system software programming the PEX 8649 into the D3hot Device PM state, and subsequently causing the Root Complex to broadcast the PME_Turn_Off Message to the downstream hierarchy.

Table 11-1. Relationships between Component Power State and Upstream Link

Downstream Component Device PM State	Permissible Upstream Component Device PM State	Permissible Interconnect Link PM State
D0	D0	L0, and optionally L0s and L1 if ASPM is enabled
D3hot	D0 to D3hot	L1, L2/L3 Ready.
D3cold (no Vaux)	D0 to D3cold	L3 (off). Zero power.

Table 11-2. Relationships between Link PM States and Power-Saving Actions

Link PM State	Power-Saving Actions
Tx L0s	PHY Tx Lanes are in a high-impedance state.
Rx L0s	PHY Rx Lanes in a low-power state.
L1	PHY Tx and Rx Lanes are in a low-power state. Flow Control (FC) timers are suspended.
L2/L3 Ready	PHY Tx and Rx Lanes are in a low-power state. FC timers are suspended.
L3 (D3cold)	Component is fully powered Off.

11.3.3 PCI Express Power Management Support

The PEX 8649 supports PM features required in the *PCI Express Base r2.0*. Table 11-3 lists supported and non-supported features and the register bits/fields used for configuration or activation.

Table 11-3. Supported PCI Express PM Capabilities

Register		Description	Supported	
Offset	Bit(s)		Yes	No
40h		**PCI Power Management Capability (All Ports)**		
	7:0	**Capability ID** Program to 01h, to indicate that the Capability structure is the PCI Power Management Capability structure.	✔	
	15:8	**Next Capability Pointer** Default 48h points to the **MSI Capability** structure.	✔	
	18:16	**Version** Default 011b indicates compliance with the *PCI Power Mgmt. r1.2*.	✔	
	19	**PME Clock** Power Management Event (PME) clock. Does not apply to PCI Express. Returns 0.		✔
	21	**Device-Specific Initialization** Default 0 indicates that Device-Specific Initialization is ***not*** required.	✔	
	24:22	**AUX Current** The PEX 8649 does ***not support*** PME generation from the D3cold Device PM state; therefore, the serial EEPROM value for this field should be 000b.		✔
	25	**D1 Support** Default value of 0 indicates that the PEX 8649 does ***not support*** the D1 Device PM state.		✔
	26	**D2 Support** Default value of 0 indicates that the PEX 8649 does ***not support*** the D2 Device PM state.		✔
	31:27	**PME Support** Bits [31, 30, and 27] must be Set, to indicate that the PEX 8649 will forward PME Messages, as required by the *PCI Express Base r2.0*.	✔	

Table 11-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
44h	**PCI Power Management Status and Control (All Ports)**			
	1:0	**Power State** Used to determine the Port's current Device PM state, and to program the Port into a new Device PM state. 00b = D0 01b = D1 – ***Not supported*** 10b = D2 – ***Not supported*** 11b = D3hot If software attempts to write an unsupported state to this field, the Write operation completes normally; however, the data is discarded and no state change occurs.	✔	
	3	**No Soft Reset** 1 = Devices transitioning from the D3hot to D0 Device PM state, because of Power State commands, do not perform an internal reset	✔	
	8	**PME Enable** 0 = Disables PME generation by the corresponding PEX 8649 Port[a] 1 = Enables PME generation by the corresponding PEX 8649 Port	✔	
	12:9	**Data Select** Initially writable by serial EEPROM and I^{2}C only[b]. This Configuration Space register (CSR) access privilege changes to RW after a Serial EEPROM and/or I^{2}C Write occurs to this register. Selects the **Data** and **Data Scale** registers (fields [31:24 and 14:13], respectively). 0h = D0 power consumed 3h = D3hot power consumed 4h = D0 power dissipated 7h = D3hot power dissipated	✔	
	14:13	**Data Scale** Writable by serial EEPROM and I^{2}C only[b]. Indicates the scaling factor to be used when interpreting the value of the **Data** register. The value and meaning of this field varies, depending upon which data value is selected by field [12:9] (*Data Select*). There are four internal **Data Scale** registers (one each, per *Data Select* values 0h, 3h, 4h and 7h), per Port. For other *Data Select* values, the **Data Scale** value returned is 0h.	✔	
	15	**PME Status** 0 = PME is not generated by the corresponding PEX 8649 Port[a] 1 = PME is being generated by the corresponding PEX 8649 Port	✔	

[a] *Because the PEX 8649 does not consume auxiliary power, this bit is not sticky, and is always Cleared at power-on reset.*

[b] *With no serial EEPROM nor previous I^{2}C programming, Reads return 00h for the* ***Data Scale*** *and* ***Data*** *registers (for all Data Selects).*

Table 11-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
44h	PCI Power Management Control/Status Bridge Extensions (All Ports)			
	22	**B2/B3 Support** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.		✔
	23	**Bus Power/Clock Control Enable** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.		✔
	PCI Power Management Data (All Ports)			
	31:24	**Data** Writable by serial EEPROM and I^{2}C only[b]. There are four supported *Data Select* values (0h, 3h, 4h and 7h), per Port. For other *Data Select* values, the **Data Scale** value returned is 0h. Bits [12:9], *Data Select*, select the **Data** register.	✔	
6Ch	Device Capability (All Ports)			
	8:6	**Endpoint L0s Acceptable Latency** Because the PEX 8649 is a switch and not an endpoint, the PEX 8649 does ***not support*** this feature. 000b = Disables the capability		✔
	11:9	**Endpoint L1 Acceptable Latency** Because the PEX 8649 is a switch and not an endpoint, the PEX 8649 does ***not support*** this feature. 000b = Disables the capability		✔
	25:18	**Captured Slot Power Limit Value** For the PEX 8649 upstream Port(s), the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [27:26] (*Captured Slot Power Limit Scale*). Do not change for downstream Ports.	✔	
	27:26	**Captured Slot Power Limit Scale** For the PEX 8649 upstream Port(s), the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [25:18] (*Captured Slot Power Limit Value*). 00b = 1.0 01b = 0.1 10b = 0.01 11b = 0.001 Do not change for downstream Ports.	✔	

[a] *Because the PEX 8649 does not consume auxiliary power, this bit is not sticky, and is always Cleared at power-on reset.*

[b] *With no serial EEPROM nor previous I^{2}C programming, Reads return 00h for the **Data Scale** and **Data** registers (for all Data Selects).*

Table 11-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
70h		**Device Control (All Ports)**		
	10	**AUX Power PM Enable**		✔
		Device Status (All Ports)		
	20	**AUX Power Detected**		✔
74h		**Link Capability (All Ports)**		
	11:10	**Active State Power Management (ASPM) Support** Active State Link PM support. Indicates the level of ASPM supported by the Port. 01b = L0s Link PM state entry is supported 11b = L0s and L1 Link PM states are supported All other encodings are ***reserved***.	✔	
	14:12	**L0s Exit Latency** Indicates the L0s Link PM state exit latency for the given PCI Express Link. Value depends upon the Port’s **Synchronous Advertised N_FTS** or **Asynchronous Advertised N_FTS** register (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset B84h or B88h, respectively) *Port x Advertised N_FTS* field value, Link speed, and state of the Port’s **Link Control** register *Common Clock Configuration* bit (offset 78h[6]). When the *Common Clock Configuration* bit is Set, the Synchronous Advertised N_FTS register value is used; otherwise, the Asynchronous Advertised N_FTS register value is used. Exit latency is calculated, as follows: • **2.5 GHz** – Multiply *Port x Advertised N_FTS* x 4 (4 symbol times in 1 N_FTS) x 4 ns (1 symbol time at 2.5 GT/s) • **5.0 GHz** – Multiply *Port x Advertised N_FTS* x 4 (4 symbol times in 1 N_FTS) x 2 ns (1 symbol time at 5.0 GT/s) 100b = Corresponding PEX 8649 Port L0s Link PM state Exit Latency is 512 ns to less than 1 µs at 5.0 GT/s 101b = Corresponding PEX 8649 Port L0s Link PM state Exit Latency is 1 µs to less than 2 µs at 2.5 GT/s All other encodings are ***reserved***.	✔	
	17:15	**L1 Exit Latency** Indicates the L1 Link PM state exit latency for the given PCI Express Link. Value depends upon the Link speed. 001b = Corresponding PEX 8649 Port L1 Link PM state Exit Latency is 1 µs to less than 2 µs at 5.0 GT/s 010b = Corresponding PEX 8649 Port L1 Link PM state Exit Latency is 2 µs to less than 4 µs at 2.5 GT/s All other encodings are ***reserved***.	✔	
	18	**Clock Power Management Capable**	✔	

Table 11-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
78h		**Link Control (All Ports)**		
	1:0	**Active State Power Management (ASPM)** 00b = Disable[c] 01b = Enables only L0s Link PM state Entry 10b = Enables only L1 Link PM state Entry 11b = Enables both L0s and L1 Link PM state Entries	✔	
	8	**Clock Power Management Enable** The PEX 8649 does ***not support*** removal of the Reference Clock in the L1 and L2/L3 Ready Link PM states.		✔
7Ch		**Slot Capability (Downstream Ports; Upstream Port(s) Always Read(s) 0)**		
	0	**Attention Button Present** ***Reserved*** for the upstream Port(s). Set if the Port is Parallel and/or Serial Hot Plug-capable. 0 = Attention Button is not implemented 1 = Attention Button is implemented on the slot chassis of the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port	✔	
	1	**Power Controller Present** ***Reserved*** for the upstream Port(s). Enables or disables the Hot Plug Controller on the PEX 8649 Hot Plug-capable Transparent downstream Ports. Set if the Port is Parallel and/or Serial Hot Plug-capable. 0 = Power Controller is not implemented. The Hot Plug Controller is disabled for that slot and a power-up sequence is not executed. The slot remains in the disabled state. 1 = Power Controller is implemented for the slot of the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port. Hot Plug Controller powers up the slot when the Manually operated Retention Latch (MRL) is closed and the **Slot Control** register *Power Controller Control* bit (Downstream Ports, offset 80h[10]) is Cleared. Otherwise, if bit 2 (*MRL Sensor Present*) is disabled (Cleared), the MRL's position has no effect on powering up the slot.	✔	
	2	**MRL Sensor Present** ***Reserved*** for the upstream Port(s). Set if the Port is Parallel and/or Serial Hot Plug-capable. 0 = MRL Sensor is not implemented. MRL position is "Don't Care" for that slot. 1 = MRL Sensor is implemented on the slot chassis of the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port. The PEX 8649 senses whether the MRL is open or closed for a slot. MRL should be Low for power-on for that slot.	✔	
	3	**Attention Indicator Present** ***Reserved*** for the upstream Port(s). Set if the Port is Parallel and/or Serial Hot Plug-capable. 0 = Attention Indicator is not implemented. HP_ATNLED_*x#* output is not functional on the slot. 1 = Attention Indicator is implemented on the slot chassis of the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port. Controls whether the HP_ATNLED_*x#* output for the slot drives out Active-Low.	✔	

[c] *The Port Receiver must be capable of entering the L0s Link PM state, regardless of whether the state is disabled.*

Table 11-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
		Slot Capability (Downstream Ports; Upstream Port(s) Always Read(s) 0) *(Cont.)*		
7Ch	4	**Power Indicator Present** ***Reserved*** for the upstream Port(s). Set if the Port is Parallel and/or Serial Hot Plug-capable. 0 = Power Indicator is not implemented. HP_PWRLED_*x*# output is not functional on the slot. 1 = Power Indicator is implemented on the slot chassis of the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port. Controls whether the HP_PWRLED_*x*# output for the slot drives out Active-Low.	✔	
	5	**Hot Plug Surprise** ***Reserved*** for the upstream Port(s). 0 = No device in the corresponding PEX 8649 downstream Port slot is removed from the system without prior notification 1 = Device in the corresponding PEX 8649 downstream Port slot can be removed from the system without prior notification	✔	
	6	**Hot Plug Capable** ***Reserved*** for the upstream Port(s). Set if the Port is Parallel and/or Serial Hot Plug-capable. 0 = Corresponding PEX 8649 downstream Port slot is not capable of supporting Hot Plug operations 1 = Corresponding PEX 8649 downstream Port slot is capable of supporting Hot Plug operations	✔	
	14:7	**Slot Power Limit Value** ***Reserved*** for the upstream Port(s). The maximum power supplied by the corresponding PEX 8649 downstream slot is determined by multiplying the value in this field (expressed in decimal; 25d = 19h) by the field [16:15] (*Slot Power Limit Scale*) value. This field must be implemented if the **PCI Express Capability** register *Slot Implemented* bit (offset 68h[24]) is Set (default). Serial EEPROM and/or I^{2}C Writes to this register or a Data Link Layer (DLL) Up event causes the downstream Port to send the Set_Slot_Power_Limit Message to the device connected to it, so as to convey the Limit value to the downstream device's upstream Port **Device Capability** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields.	✔	
	16:15	**Slot Power Limit Scale** ***Reserved*** for the upstream Port(s). The maximum power supplied by the corresponding PEX 8649 downstream slot is determined by multiplying the value in this field by the field [14:7] (*Slot Power Limit Value*) value. This field must be implemented if the **PCI Express Capability** register *Slot Implemented* bit (offset 68h[24]) is Set (default). Serial EEPROM and/or I^{2}C Writes to this register or a DLL Up event causes the downstream Port to send the Set_Slot_Power_Limit Message to the device connected to it, so as to convey the Limit value to the downstream device's upstream Port **Device Capability** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	✔	

Table 11-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
80h		**Slot Control (Downstream Ports; Upstream Port(s) Always Read(s) 0)**		
	1	**Power Fault Detector Enable** ***Reserved*** for the upstream Port(s). 0 = Function is disabled 1 = Enables software notification with an interrupt if the Port is in the D0 Device PM state (**PCI Power Management Status and Control** register *Power State* field, offset 44h[1:0], are both Cleared), or with a PME Message if the Port is in the D3hot Device PM state (offset 44h[1:0], are both programmed to 11b), for a Power Fault Detected event on the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port.	✔	
	9:8	**Power Indicator Control** ***Reserved*** for the upstream Port(s). Controls the Power Indicator on the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port slot. Reads return the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port Power Indicator's current state. Writing a non-zero value triggers a Command Completed event (even if the value written is the same as the existing value). Writing 00b preserves the current value and does not trigger a Command Completed event. 00b = ***Reserved*** – Writes are ignored 01b = Turns On indicator to constant On state 10b = Causes indicator to blink 11b = Turns Off indicator	✔	
	10	**Power Controller Control** ***Reserved*** for the upstream Port(s). Controls the Power Controller on the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port slot. 0 = Turns On the Power Controller; requires some delay to be effective 1 = Turns Off the Power Controller	✔	
		Slot Status (Only Downstream Ports; Upstream Port(s) Always Read(s) 0)		
	17	**Power Fault Detected** ***Reserved*** for the upstream Port(s). 1 = Power Controller of the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port slot detected a Power Fault at the slot	✔	

Table 11-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
138h		Power Budget Extended Capability Header (Upstream Port(s))		
	15:0	**PCI Express Extended Capability ID** ***Reserved*** for the downstream Port(s). Program to 0004h, as required by the *PCI Express Base r2.0*.	✔	
	19:16	**Capability Version** ***Reserved*** for the downstream Port(s). Program to 1h, as required by the *PCI Express Base r2.0*.	✔	
	31:20	**Next Capability Offset** ***Reserved*** for the downstream Port(s). Program to 148h, which addresses the **Virtual Channel Extended Capability** structure.	✔	
13Ch		Data Select (Upstream Port(s))		
	7:0	**Data Select** ***Reserved*** for the downstream Port(s). Indexes the Power Budget data reported, by way of eight **Power Budget Data** registers, and selects the DWord of Power Budget data that appears in each **Power Budget Data** register. Index values start at 0, to select the first DWord of Power Budget data; subsequent DWords of Power Budget data are selected by increasing index values 1 to 7.	✔	

Table 11-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
140h	**Power Budget Data (Upstream Port(s))**			
	7:0	**Base Power** ***Reserved*** for the downstream Port(s). Eight registers, per upstream Port. Specifies (in Watts) the base power value in the operating condition. This value must be multiplied by the *Data Scale*, to produce the actual power consumption value.	✔	
	9:8	**Data Scale** ***Reserved*** for the downstream Port(s). Specifies the scale to apply to the Base Power value. The device power consumption is determined by multiplying the *Base Power* field contents with the value corresponding to the encoding returned by this field. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	✔	
	12:10	**PM Sub-State** ***Reserved*** for the downstream Port(s). 000b = Power Management sub-state of the operating condition being described	✔	
	14:13	**PM State** ***Reserved*** for the downstream Port(s). Power Management state of the operating condition being described. 00b = D0 Device PM state 11b = D3 Device PM state All other encodings are ***reserved***.	✔	
	17:15	**Type** ***Reserved*** for the downstream Port(s). Type of operating condition being described. 000b = PME Auxiliary 001b = Auxiliary 010b = Idle 011b = Sustained 111b = Maximum All other encodings are ***reserved***.	✔	
	20:18	**Power Rail** ***Reserved*** for the downstream Port(s). Power Rail of the operating condition being described. 000b = Power 12V 001b = Power 3.3V 010b = Power 1.8V 111b = Thermal All other encodings are ***reserved***.	✔	
	Note: *Eight registers, per upstream Port, can be programmed through the serial EEPROM, I^2C, and/or SMBus. Each non-zero register value describes the power usage for a different operating condition. Each configuration is selected by writing to the* ***Data Select*** *register* Data Select *field (Upstream Port(s), offset* 13Ch*[7:0]).*			

Table 11-3. Supported PCI Express PM Capabilities *(Cont.)*

Register		Description	Supported	
Offset	Bit(s)		Yes	No
144h		**Power Budget Capability (Upstream Port(s))**		
	0	**System Allocated** ***Reserved*** for the downstream Port(s). 1 = Power budget for the device is included within the system power budget	✔	
F70h		**Power Management Hot Plug User Configuration (All Ports)**		
	0	**L0s Entry Idle Counter** Traffic Idle time to meet, to enter the L0s Link PM state. 0 = Idle condition must last 1 µs 1 = Idle condition must last 4 µs	✔	
	2	**HPC PME Turn-Off Enable** Functionality associated with this bit is enabled only on the downstream Ports. 1 = PME Turn-Off Message is transmitted before the Port is turned Off on a downstream Port	✔	
	4:3	**HPC T_{pepv}** Functionality associated with this field is enabled only on the downstream Ports. Hot Plug Port time from Power Enable to Power Valid. Controls the delay from when HP_PWREN_*x* is asserted High, to when power is valid at a slot. (Refer to Section 10.7.1.2, "Slot Power-Up Sequencing When Power Controller Present Bit Is Set," for details.) 00b = Feature is disabled, and HP_PWR_GOOD_*x* input is used for Power Valid 01b = 128 ms 10b = 256 ms 11b = 512 ms	✔	
	6	**HP_PWR_GOOD_*x* Active Low Enable** Functionality associated with this bit is enabled only on the downstream Ports. When Set, HP_PWR_GOOD_*x* ball is Active-Low. (HP_PWR_GOOD_*x* default is Active-High.) 0 = HP_PWR_GOOD_*x* is Active-High 1 = HP_PWR_GOOD_*x* is Active-Low	✔	
	10	**L0s Entry Disable** 0 = Enables entry into the L0s Link PM state on a Port when the L0s idle conditions are met 1 = Disables entry into the L0s Link PM state on a Port when the L0s idle conditions are met	✔	

11.4 Power Management Tracking

Note: *NT Port Link Interface entry and exit to ASPM and Conventional PCI PM-compatible power states do not depend upon the Transparent upstream nor downstream Port power states or traffic. They are solely dependent upon the NT Port Link Interface's traffic conditions.*

Upstream Port logic tracks the Link status of each downstream and upstream Port Link, to derive the following conditions:

- Upstream Port(s) enter(s) the L0s Link PM state when all enabled downstream Receivers are in the L0s Link PM state or deeper, or in a Link Down state.
- Upstream Port(s) enter(s) the active L1 Link PM state, only when all downstream Ports are in the active L1 Link PM state or deeper, or the Link is down.
- When a downstream Port is in the active L1 Link PM state and an ASPM L1 Link PM state exit is occurring in the downstream Port, the upstream Port(s) exit(s) the L1 Link PM state.
- When the upstream Port(s) is (are) in the active L1 Link PM state and an active L1 Link PM state exit is occurring, due to Receiver Electrical Idle exit, the downstream Port exits the L1 Link PM state.
- When a PME_TO_Ack Message is received only on all active (not in Link Down) downstream Ports, a PME_TO_Ack Message is issued toward the upstream Port(s). The NT Port Virtual Interface is marked as being in the *DL_Down* state.
- When all downstream Ports are in the L2/L3 Ready Link PM or Link Down state, the upstream Port(s) transmit(s) PM_ENTER_L23 Data Link Layer Packets (DLLPs) toward the Root Complex.

11.5 Power Management Event Handler

PM_PME Messages are Posted Transaction Layer Packets (TLPs) that inform the PM software which agent within the PCI Express hierarchy has requested a PM-state change. PM_PME Messages are always routed toward the Root Complex.

PCI Express components are permitted to wake the system from any supported PM state, through the request of a PME.

When a PEX 8649 Transparent downstream Port is in the D3hot Device PM state, the following Hot Plug and/or PCI Express Hot Plug events cause the **PCI Power Management Status and Control** register *PME Status* bit (offset 44h[15]) to be Set:

- For Hot Plug-capable Ports:
  - Presence Detect Changed (logical OR of PRSNT# (HP_PRSNT_***x***# or I/O Expander PRSNT# input), and SerDes Receiver Detect[a] on Lane(s) associated with that Port)
  - Attention Button Pressed
  - Power Fault Detected
  - MRL Sensor Changed
  - Command Completed
  - Link Bandwidth Management Status
  - Link Autonomous Bandwidth Status
- For non-Hot Plug-capable downstream Ports:
  - Presence Detect Changed (SerDes Receiver Detect[a] on Lane(s) associated with that Port)
  - Data Link Layer State Changed

This causes the downstream Port to generate a PM_PME Message, if the **PCI Power Management Status and Control** register *PME Enable* bit (offset 44h[8]) is Set.

[a] *The SerDes Receiver Detect mechanism is comprised of the* ***Physical Layer Receiver Detect Status*** *register Receiver Detected on Lane x bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 200h[31:16]) or Hot Plug PRSNT# (from external I^{2}C I/O Expander) input for the Port.*

11.6 Power Management in Virtual Switch Mode

In Virtual Switch mode, the PEX 8649 can have multiple upstream Ports. Downstream Ports are assigned to different upstream Ports, depending upon the Virtual Switch Table. (Refer to Section 5.5.3, “Virtual Switch Table.”) Each virtual switch works as an independent switch for deciding entry into, or exit from, different PM states.

ASPM L0s and L1 Link PM state entry/exit works on the same rules defined in the previous sections. However, a particular virtual switch upstream Port monitors the Link status only on the downstream Ports that belong to that virtual switch, for ASPM L0s and L1 Link PM state entry. Similarly, the downstream Ports monitor the corresponding virtual switch upstream Port Link state, for deciding entry/ exit from the ASPM L0s and L1 Link PM states.

A virtual switch upstream Port that is programmed into the D3hot state (Port’s **PCI Power Management Status and Control** register *Power State* field, offset 44h[1:0], are both programmed to 11b) requests the PCI L1 Link PM state, and finally settles into the PCI Link PM L1 state after the upstream Port returns a Completion for this Configuration Write and L1 Link PM state negotiation successfully completes.

A PM_Turn_Off message received at a virtual switch upstream Port is broadcast only to the downstream Ports corresponding to that virtual switch. When a PME_TO_Ack message is subsequently received from all downstream Ports belonging to the virtual switch, a single PME_TO_Ack message is sent upstream of that virtual switch.

If a virtual switch has only an Upstream Port and no Downstream Ports associated with it (*such as* the case of a Management Port), the virtual switch behaves like an endpoint for entry/exit to the ASPM L0s, ASPM L1, and PCI L1 and L2/L3 Ready Link PM states. The entry/exit to different Power Management states depends only upon the idle/traffic conditions on that upstream Port.

When a new downstream Port is added to a virtual switch due to re-configuration, future entry/exit to into different power states on the virtual switch’s upstream Port also depends upon the newly added downstream Port’s power states. After a downstream Port is de-allocated from a virtual switch, that Port’s Link states are not taken into consideration for future entry/exit to power states.

Interrupts and PM_PME messages generated on the downstream Ports are routed to the corresponding virtual switch upstream Port.

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Chapter 12 Virtual Switch Mode

12.1 Multiple Virtual Switches

The PEX 8649 implements multiple virtual PCI Express switches, up to four total. Each virtual switch has its own upstream Port and zero or more downstream Ports. From a software point of view, each virtual switch consists of one upstream PCI-to-PCI (P2P or P-P) bridge and zero to *N* downstream PCI-to-PCI bridges. Each virtual switch has its own Reset, Interrupt, and Error signals. While the virtual switches share the same physical switch, traffic from one virtual switch cannot migrate to another virtual switch.

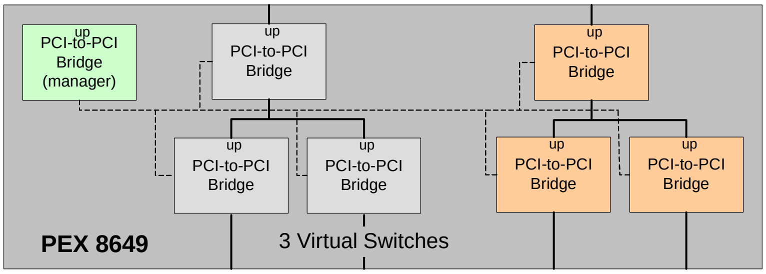
Figure 12-1 illustrates a partitioning of three virtual switches in a single physical switch – a manager hierarchy and two regular PCI Express 3-Port switches.

In Figure 12-1, the right three PCI-to-PCI bridges are owned by the right-most upstream Port, and the middle three PCI-to-PCI bridges are owned by the middle upstream Port. In this scenario, a third upstream Port is used for a Management Port, and this upstream Port has access to all other hierarchies, as indicated by the dashed line. The Management Port configures the virtual switches so that each Port – upstream or downstream – is placed in the proper configuration. Each Port can be assigned to only one virtual switch at a time. The Management Port can own downstream Ports, although this mode is not shown in Figure 12-1.

Host-to-Host messages across virtual switch boundaries can be sent by the Management Port's **Scratchpad** and **Mailbox** registers.

Changing switch configuration from Virtual Switch mode to Base mode can be performed only by strapping the STRAP_VS_MODE[1:0] inputs Low. However, Base mode can be emulated in Virtual Switch mode, by enabling two virtual switches, with all Ports assigned to one virtual switch.

Figure 12-1. Multiple Virtual Switches in a Single Physical Switch



12.2 Management Port

The PEX 8649 supports configuration and management through various options, described in the sections that follow. In Virtual Switch mode, the PEX 8649's registers are accessible by the designated Active Management Port, serial EEPROM, and/or I^{2}C Slave interface. The PEX 8649 can be configured by serial EEPROM and/or Strapping balls, without restrictions. With the PEX 8649, any two PCI Express Ports can be configured as Management Ports, with one designated as the primary Management Port, and the other as the Redundant Management Port.

The Management Port can be used to:

- Configure virtual switches
- Move Ports from one virtual switch to another
- Monitor all virtual switch Links
- Configure PEX 8649-wide registers (*such as* the Physical Layer (PHY) registers)
- Access the serial EEPROM – In Virtual Switch mode, in-band access to the serial EEPROM is restricted to the Management Port, as designated by the **Management Port Control** register *Active Management Port* field (Port 0, accessible through the Management Port and Redundant Management Port, offset 354h[4, 2:0])

The Redundant Management Port can be promoted to become the new Active Management Port, by software (through the Redundant Management Port, Management Port, and/or I^{2}C/SMBus) copying the value of the register's *Redundant Management Port* field [12, 10:8] to the *Active Management Port* field. (Refer to Section 12.5.2 for further details.)

12.2.1 Out-of-Band Interfaces

This section briefly describes the out-of-band interfaces supported by the PEX 8649.

12.2.1.1 Unused PCI Express Port – Management-Capable Port

Any Port can be designated as the Management Port and connected to a small service processor. This configuration is used in Virtual Switch mode.

12.2.1.2 Strapping Balls

The Strapping balls are used to load default configurations. Refer to Section 3.4.4, "Strapping Signals," for details.

12.2.1.3 Serial EEPROM

An on-board serial EEPROM can be used to override the Strapping balls and configure the PEX 8649. Refer to Chapter 6, "Serial EEPROM Controller," for details.

12.2.1.4 I^{2}C Bus/SMBus

The PEX 8649 supports both the I^{2}C Bus and System Management Bus (SMBus) interfaces for configuring the registers. However, if the STRAP_I2C_CFG_EN# input is enabled to delay linkup until the **Configuration Release** register *Initiate Configuration* bit (Port 0, accessible through the Management Port, offset 3ACh[0]) is Set, this register Write can only be performed by I^{2}C (not SMBus).

Refer to Chapter 7, "I^{2}C/SMBus Slave Interface Operation," for details.

12.2.2 In-Band Interface

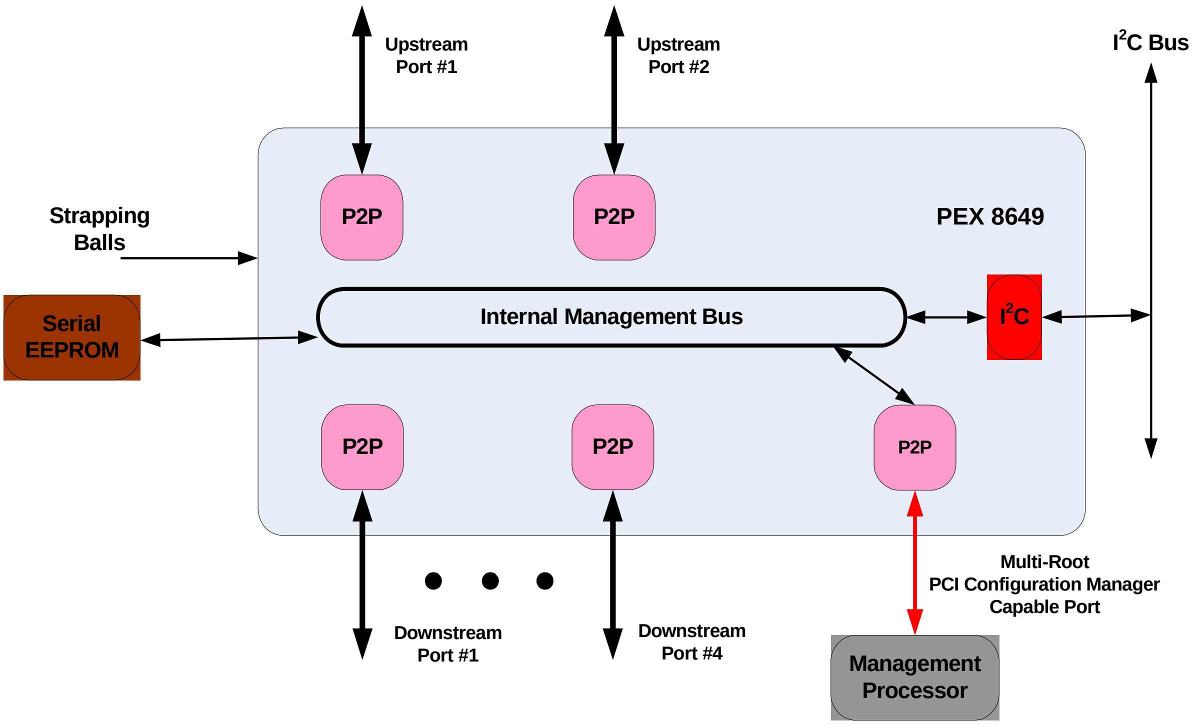
An in-band interface is typically used to manage PCI Express fabric within a single domain hierarchy, where the virtual switch's upstream Port manages the PCI Express switch. In the case of Multi-Root switches, the shared resources are being modified by a trusted resource, *such as* a designated PCI Express Port. PLX Multi-Root switches support this mode of operation, in which one of the switch's Ports can be used for in-band operations, where the CPU can send data (regular traffic), as well as control data to control the PCI Express switch fabric's behavior. Additionally, a second Port can be designated as a Redundant Management Port. If the primary Port fails, the Redundant Management Port takes over the responsibility of managing the PCI Express switch fabric.

12.2.2.1 Configuration and Management

Figure 12-2 illustrates various options for accessing the Management Bus and internal registers in Virtual Switch mode. In Virtual Switch mode, each upstream Port manages its own partition; however, another Port or interface is designated as the Management Port, with responsibility for defining and modifying partitions, as required. The PEX 8649 can also be configured by Strapping balls, serial EEPROM, and/or I^{2}C.

Note: *The PCI-to-PCI (P2P) blocks in Figure 12-2 are a logical representation of how a Port presents itself to software.*

Figure 12-2. Configuration and Management – Virtual Switch Mode



12.2.2.2 In-Band Management Port

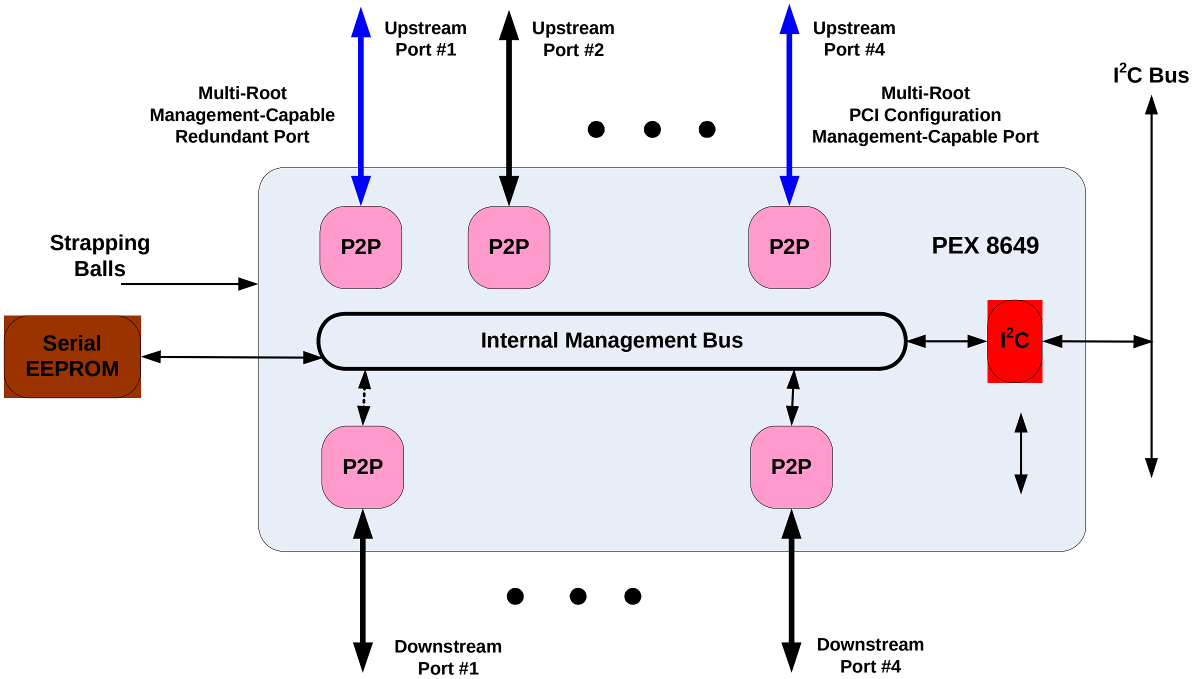
In Virtual Switch mode, an in-band PCI Express Port can be used as a Management Port and have access to all registers. (Refer to Figure 12-3.)

The Redundant Management Port can access only the **Management Port Control** register (Port 0, accessible through the Management Port and Redundant Management Port, offset 354h), to promote itself to be the Management Port if the Active Management Port Host fails, using Memory-Mapped access to offset 354h within its own **BAR0/1** register map.

Notes: *All Configuration Space registers (CSRs) requiring access by the Management Port are memory-mapped, using the Management Port's **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, respectively), located in the Type 1 CSR headers. The In-Band Management Port uses Memory-Mapped transactions, to access all registers in all virtual switches. Because Ports within a Station can be assigned to different virtual switches, Management Port Writes to Station registers can affect multiple virtual switches.*

The PCI-to-PCI (P2P) blocks in Figure 12-3 are a logical representation of how a Port presents itself to software.

Figure 12-3. Configuration and Management of In-Band Management – Virtual Switch Mode



12.2.2.3 Management Ports and Restriction

The shared registers listed in Table 12-1, and all PCI-to-PCI registers, are accessed by the Active Management Port. The Redundant Management Port can access only the **Management Port Control** register (Port 0, accessible through the Management Port and Redundant Management Port, offset 354h), to promote itself to be the Management Port if the Active Management Port Host fails.

In Virtual Switch mode, the STRAP_UPSTRM_PORTSEL[3:0] inputs define which Port is the Active Management Port, when the Management Port is enabled (STRAP_NT_ENABLE#=L). The Management Port can also be enabled and designated by serial EEPROM and/or I^2C writing an appropriate value into the register's *Active Management Port Enable* and *Active Management Port* bits (bits [5 and 4, 2:0], respectively). As mentioned previously, the Redundant Management Port can be promoted to become the new Active Management Port, by software (through the Redundant Management Port, Management Port, and/or I^2C/SMBus) copying the value of the register's *Redundant Management Port* field [12, 10:8] to the *Active Management Port* field.

Note: *In Virtual Switch mode, the* ***Virtual Switch Table*** *registers include the* ***VSx Port Vector*** *and* ***VSx Upstream*** *registers (Port 0, accessible through the Management Port, offsets 380h through 38Ch, and 360h through 36Ch). These two sets of registers define which Ports are associated to each virtual switch, and which Port is the upstream Port for each Virtual Switch, respectively. These registers must be initialized by one (or more) of the following agents:*

- *Serial EEPROM*
- *I^2C/SMBus, provided that the STRAP_I2C_CFG_EN# input is Low (to delay linkup until I^2C/SMBus Sets the* ***Configuration Release*** *register Initiate Configuration bit (Port 0, accessible through the Management Port, offset 3ACh[0]). This option might require software support, to delay Host enumeration until I^2C/SMBus Sets the Initiate Configuration bit after programming the PEX 8649 Configuration registers.*
- *Management Port software, provided that the STRAP_NT_ENABLE# and STRAP_NT_UPSTRM_PORTSEL0 inputs are both Low (to enable the Management Port, and delay linkup of all other Ports until software (and/or I^2C/SMBus) Sets the Initiate Configuration bit).*

Use of serial EEPROM for the initialization might be the best choice for most applications, because it is the simplest solution. Therefore, for Virtual Switch mode applications, the serial EEPROM is required to initialize the Virtual Switch Table registers, unless I^2C/SMBus and/or Management Port software can perform this task.

Table 12-1. Virtual Switch Management Registers (accessible from Primary Management Port)[a]

Offset	Register	Description[b]
354h	**Management Port Control**	This register contains bits that enable and indicate the Port Number of the Active and Redundant Management Ports.
358h[3:0]	**Virtual Switch Enable**	The register's *VSx Enable* bits are used to enable or disable virtual switches within the system. There is one bit, per virtual switch (VS0 through VS3).[c]
360h – 36Ch	**VS*x* Upstream**	These registers define the upstream Port of each virtual switch. There is one register, per virtual switch (VS0 through VS3).[c]
380h – 38Ch	**VS*x* Port Vector**	These registers define the upstream and downstream Ports associated with each virtual switch. There is one register, per virtual switch (VS0 through VS3). Each register has one bit, per Port.[c]
900h	**Switch Link Up**	When the Port's Link state transitions from down to up, the corresponding Port's bit is Set. The corresponding Port's bit is Cleared, by using software to explicitly write 1 to the bit. The register has one bit, per Port.
904h	**Switch Link Down**	When the Port's Link state transitions from up to down, the corresponding Port's bit is Set. The corresponding Port's bit is Cleared, by using software to explicitly write 1 to the bit. The register has one bit, per Port.
908h	**Switch Link Event Mask**	If the *Mask* bit is Set, the corresponding *Up* or *Down* bit (located in register offsets 900h and 904h, respectively) transition does not generate an interrupt to the Management Port. If not masked, the bit transition generates an interrupt to the Active Management Port. The register has one *Mask* bit, per Port.
90Ch	**Switch Link Status**	This Read-Only register indicates Link status. The register has one *Status* bit, per Port.
3A0h	**Port Reset**	When driven with a value of 1, this register holds the Port in reset, including the Port PCI-to-PCI bridge and the hierarchy below it. A value of 0 indicates to un-reset the PCI-to-PCI bridge and the hierarchy below it. There is one bit, per Port. Upstream Ports are not reset by this register.

a. All registers listed in this table are located in Port 0, accessible through the Management Port.

b. For more complete descriptions, refer to the individual registers listed.

c. Additional information is also provided in Table 5-4, "Virtual Switch Table Registers."

12.3 Virtual Switch Reset and Initialization

12.3.1 Virtual Switch Reset

For details regarding the Virtual Switch reset, refer to Section 5.2, "Resets – Virtual Switch Mode."

12.3.2 Virtual Switch Initialization

For information on Virtual Switch Initialization, refer to Section 5.5, "Initialization – Virtual Switch Mode."

12.3.3 Virtual Switch Table Programming Sequence

For details regarding the Virtual Switch Table Programming Sequence, refer to Section 5.5.3.2, "Virtual Switch Table Programming Sequence."

12.4 Moving a Port from One Virtual Switch to Another (VS*x* to VS*y*)

A downstream Port can be moved from one virtual switch (VS*x*) to another (VS*y*), by programming the two virtual switch's **VS*x* Port Vector** registers, by way of the Management Port. (The reason for the Port to be moved, and the coordination with the Management Port, are beyond the scope of this data book.)

First, the **VS*x* Port Vector** register for VS*x* (Port 0, accessible through the Management Port, offsets 380h through 38Ch) must **remove** the Port. This can be achieved by Clearing the bit(s) in the active Port Vector for the Port(s) that is (are) moving **out** of VS*x*.

Second, the **VS*x* Port Vector** register for VS*y* (Port 0, accessible through the Management Port, offsets 380h through 38Ch) must **add** the Port. This can be achieved by Setting the bit(s) in the active Port Vector for the Port(s) that just left VS*x*, that is (are) moving **to** VS*y*.

12.5 Failover in Virtual Switch Mode

This section discusses the various types of failover in Virtual Switch mode:

- Virtual Switch Host Failover
- Active Management Host Failover

Refer also to Section 4.6.4, "Failover in Virtual Switch Mode."

12.5.1 Virtual Switch Host Failover

A planned or unplanned event can cause a Host in one virtual switch to no longer be active. In either case, the first step is to make the Management Host aware that another Host is no longer available, and to quiesce the traffic in Ports owned by the no-longer-responding Host. After that, both planned or unplanned failover follow the same steps to complete the failover.

12.5.2 Active Management Host Failover

The Active Management Port has a backup (Redundant) Management Port. In the event that the Active Management Port fails, the Redundant Management Port can promote itself to be the Active Management Port while simultaneously demoting the previous Active Management Port to a backup status. The Redundant Management Port writes the **Management Port Control** register (Port 0, accessible through the Management Port and Redundant Management Port, offset 354h) with the following sequence:

1. Initially, the **Management Port Control** register status is:
   - *Active Management Port* field [4, 2:0] holds the Port Number of the Active Management Port
   - *Redundant Management Port* field [12, 10:8] holds the Port Number of the Redundant Management Port
   - *Active Management Port Enable* and *Redundant Management Port Enable* bits (bits [5 and 13], respectively) are Set
2. The Redundant Management Port determines that the Active Management Port is no longer active.
3. The Redundant Management Port writes to the **Management Port Control** register:
   - Its own Management Port Number, to the *Active Management Port* field
   - The Port Number of the previous Active Management Port, to the *Redundant Management Port* field
   - Holds the *Active Management Port Enable* and *Redundant Management Port Enable* bits Set
4. Failover is then complete. The new Active Management Port should scan the Management Interrupt Status registers (**VS Upstream to Management Upstream Doorbell Request** and **Management Upstream to VS Upstream Doorbell Request** registers (VS Upstream Port(s) and Management Port, offsets 910h and 928h, respectively), to determine whether there are any active interrupts to service, and might inform other Hosts that a new Active Manager has taken over.

12.6 Performance

The virtual switch is built upon a non-blocking, peer-to-peer switch. The virtual switch assignment merely restricts which Ports can communicate with one another. Performance for each virtual switch should be equivalent to an ideal, single-hierarchy switch.

There is one exception. The Data buffers are set up on a Station-basis (16 neighboring Lanes). If two or more Ports within a Station belong to different virtual switches, then the common pool shared by all Ports associated with those 16 Lanes can be unfairly used by one virtual switch, to the detriment of another. To prevent this from occurring, the initial credits and Port pool should be adjusted, so as to reduce the common pool to zero (0).

12.7 Host-to-Host Communication

In Base mode, the PEX 8649 is usually managed by I^2C or the Root Port. In contrast, for bladed systems, Root Complexes are not typically trusted entities, and are therefore managed by a dedicated Management Processor connected through an out-of-band mechanism (*such as* I^2C or a dedicated PCI Express Port).

A virtual switch sends Doorbell interrupts and Scratchpad register data to the Management Port, using either Configuration Requests, or Memory Requests to the offset within its own **BAR0/1** register map.

The Management Port sends Doorbell interrupts and Scratchpad register data to individual virtual switches, by Memory-Mapped access to the offset within the virtual switch upstream Port registers (rather than the offset within the Management Port, which would generate an interrupt to itself). *For example*, if Port 1 is a non-Management virtual switch upstream Port, the Management Port can generate a Doorbell interrupt to it, by writing to offset 1928h in the Management Port's **BAR0/1** register map.

Every virtual switch upstream Port has the following **Scratchpad** registers and four corresponding **Doorbell** registers (located in the VS Upstream Port(s) and Management Port):

- Virtual switch to Management CPU direction
  - **VS Upstream to Management Upstream Doorbell Request** register (offset 910h)
  - **VS Upstream to Management Upstream Doorbell Mask** register (offset 914h)
  - **VS Upstream to Management Upstream Scratchpad 1** register (offset 918h)
  - **VS Upstream to Management Upstream Scratchpad 2** register (offset 91Ch)
  - **VS Upstream to Management Upstream Scratchpad 3** register (offset 920h)
  - **VS Upstream to Management Upstream Scratchpad 4** register (offset 924h)
- Management CPU to virtual switch direction
  - **Management Upstream to VS Upstream Doorbell Request** register (offset 928h)
  - **Management Upstream to VS Upstream Doorbell Mask** register (offset 92Ch)
  - **Management Upstream to VS Upstream Scratchpad 1** register (offset 930h)
  - **Management Upstream to VS Upstream Scratchpad 2** register (offset 934h)
  - **Management Upstream to VS Upstream Scratchpad 3** register (offset 938h)
  - **Management Upstream to VS Upstream Scratchpad 4** register (offset 93Ch)

Virtual switches cannot send messages directly to another virtual switch; instead, a virtual switch upstream Port must first send the message to the Management Port, and the Management Port can then send the message to the other virtual switch.

Refer to Section 9.6.2, "Doorbell Interrupts – Virtual Switch Mode," for further details.

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Chapter 13 Transparent Port Registers

13.1 Introduction

This chapter defines the PEX 8649 Transparent Port registers. Each PEX 8649 Port has its own Configuration, Capability, Control, and Status register space. The register mapping is the same for each Port. (Refer to Table 13-1.) This chapter also presents the PEX 8649 programmable registers and the order in which they appear in the register map. Register descriptions, when applicable, include details regarding their use and meaning in the upstream Port(s) and downstream Ports. (Refer to Table 13-3.) Other registers are defined in:

- Chapter 15, “NT Port Virtual Interface Registers – Base Mode Only”
- Chapter 16, “NT Port Link Interface Registers – Base Mode Only”

Notes: *For Chip-specific registers (those that exist only in Port 0), if Port 0 is the Legacy NT Port, then those registers exist only in the NT Port Virtual Interface.*

For Station-specific registers (those that exist only in Port 0, 16, or 20), if Port 0, 16, or 20 is the Legacy NT Port, then those registers exist only in the NT Port Virtual Interface.

All PEX 8649 registers can be accessed by Configuration or Memory Requests.

For further details regarding register names and descriptions, refer to the following specifications:

- *PCI r3.0*
- *PCI Power Mgmt. r1.2*
- *PCI-to-PCI Bridge r1.2*
- *PCI Express Base r2.0*
- *I^{2}C Bus v2.1*

13.2 Type 1 Port Register Map

Table 13-1 defines the Transparent mode Type 1 Port register mapping.

Table 13-1. Type 1 Port Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16		15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI-Compatible Type 1 Configuration Header Registers (Offsets 00h – 3Ch)			Capability Pointer (40h)	00h … 34h … 3Ch
		Next Capability Pointer (48h)	Capability ID (01h)	40h
PCI Power Management Capability Registers (Offsets 40h – 44h)				44h
		Next Capability Pointer (68h)	Capability ID (05h)	48h
MSI Capability Registers (Offsets 48h – 64h)				… 64h
		Next Capability Pointer (A4h)	Capability ID (10h)	68h
PCI Express Capability Registers (Offsets 68h – A0h)				… A0h
		Next Capability Pointer (00h)	SSID/SSVID Capability ID (0Dh)	A4h
Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – FCh)				… FCh
Next Capability Offset (FB4h)	1h	PCI Express Extended Capability ID (0003h)		100h
Device Serial Number Extended Capability Registers (Offsets 100h – 134h)				… 134h
Next Capability Offset (148h)	1h	PCI Express Extended Capability ID (0004h)		138h
Power Budget Extended Capability Registers (Offsets 138h – 144h)				… 144h
Next Capability Offset (E00h or 000h)	1h	PCI Express Extended Capability ID (0002h)		148h
Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)				… 1BCh
Device-Specific Registers (Offsets 1C0h – DFCh)				1C0h …
Next Capability Offset 2 (000h)	1h	PCI Express Extended Capability ID 2 (000Bh)		B70h
Device-Specific Registers (Offsets 1C0h – DFCh)				… DFCh

Table 13-1. Type 1 Port Register Map *(Cont.)*

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16		15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (B70h or F24h)	1h	PCI Express Extended Capability ID (0012h)	E00h
Multicast Extended Capability Registers (Offsets E00h – E2Ch) – All Modes Except Legacy NT			… E2Ch
Reserved			E30h – F1Ch
Device-Specific Registers – Virtual Switch (Offset F20h), Virtual Switch Mode Only			F20h
Next Capability Offset (B70h)	1h	PCI Express Extended Capability ID (000Dh)	F24h
ACS Extended Capability Registers (Offsets F24h – F2Ch)			… F2Ch
Device-Specific Registers (Offsets F30h – FB0h)			F30h … FB0h
Next Capability Offset (138h)	1h	PCI Express Extended Capability ID (0001h)	FB4h
Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)			… FDCh
Reserved			FE0h – FFCh

13.3 Port Register Configuration and Map

The PEX 8649 Port registers are configured similarly – not all the same. Port 0 of Station 0, Port 16 of Station 4, and Port 20 of Station 5 include more Device-Specific registers than the other Ports. Port 0 also contains registers that are used to set up and control the PEX 8649, as well as a serial EEPROM interface, I^{2}C Slave interface, and SMBus Slave interface logic and control. The Port registers contain setup and control information specific to the Station and its Port(s). Table 13-2 defines the Port register configuration and map.

Notes: *For Chip-specific registers (those that exist only in Port 0), if Port 0 is the Legacy NT Port, then those registers exist only in the NT Port Virtual Interface.*

For Station-specific registers (those that exist only in Port 0, 16, or 20), if Port 0, 16, or 20 is the Legacy NT Port, then those registers exist only in the NT Port Virtual Interface.

In Virtual Switch mode, Chip- and Station-specific registers are accessible only to the Management Port, serial EEPROM, I^{2}C, and/or SMBus.

Table 13-2. Port Register Configuration and Map

Register Types	Station 0, Port 0	Station 4, Port 16 Station 5, Port 20	Station 0, Ports 1, 2, 3 Station 4, Ports 17, 18, 19 Station 5, Ports 21, 22, 23
PCI-Compatible Type 1 Configuration Header Registers (Offsets 00h – 3Ch)	00h – 3Ch	00h – 3Ch	00h – 3Ch
PCI Power Management Capability Registers (Offsets 40h – 44h)	40h – 44h	40h – 44h	40h – 44h
MSI Capability Registers (Offsets 48h – 64h)	48h – 64h	48h – 64h	48h – 64h
PCI Express Capability Registers (Offsets 68h – A0h)	68h – A0h	68h – A0h	68h – A0h
Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – FCh)	A4h – FCh	A4h – FCh	A4h – FCh
Device Serial Number Extended Capability Registers (Offsets 100h – 134h)	100h – 134h	100h – 134h	100h – 134h
Power Budget Extended Capability Registers (Offsets 138h – 144h)	Upstream Port(s) 138h – 144h		
Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)	148h – 1BCh	148h – 1BCh	148h – 1BCh
WRR Port Arbitration Table Registers (Offsets 178h – 1BCh)	Refer to Table 13-17		
Device-Specific Registers (Offsets 1C0h – DFCh)			
Device-Specific Registers – Read Pacing (Offsets 1D0h – 1D8h)	One Port per Station – Refer to Table 13-20		
Device-Specific Registers – Captured Bus and Device Numbers (Offsets 1DCh – 1FCh)	1DCh – 1FCh	1DCh, 1E0h, 1E8h – 1FCh	1DCh, 1E0h, 1E8h – 1FCh
Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)	200h – 25Ch	200h – 25Ch	
Device-Specific Registers – Serial EEPROM (Offsets 260h – 26Ch)	260h – 26Ch		
Device-Specific Registers – I^{2}C and SMBus Slave Interfaces (Offsets 290h – 2FCh)	290h – 2FCh		

Table 13-2. Port Register Configuration and Map *(Cont.)*

Register Types	Station 0, Port 0	Station 4, Port 16 Station 5, Port 20	Station 0, Ports 1, 2, 3 Station 4, Ports 17, 18, 19 Station 5, Ports 21, 22, 23
Device-Specific Registers – Port Configuration (Offsets 300h – 31Ch)	300h – 31Ch		
Device-Specific Registers – Error Checking and Debug (Offsets 320h – 350h)	320h – 350h		
Device-Specific Registers – Port Configuration (Offsets 354h – 3ACh)	354h – 3ACh		
Device-Specific Registers – General-Purpose Input/Output (Offsets 600h – 68Ch)	600h – 68Ch		
Device-Specific Registers – Error Checking and Debug (Offsets 700h – 75Ch)	700h – 75Ch	700h – 75Ch	
Device-Specific Registers – Control (Offsets 760h – 774h), Base Mode Only	760h – 774h	760h – 774h	
Device-Specific Registers – Soft Error (Offsets 778h – 8FCh)	778h – 8FCh	778h – 8FCh	
Device-Specific Registers – Virtual Switch (Offsets 900h – 9ECh), Virtual Switch Mode Only	900h – 9ECh		
Device-Specific Registers – Ingress Credit Handler (Offsets 9F0h – A2Ch)	9F0h – A2Ch	9F0h – A2Ch	9F0h – 9F8h
Device-Specific Registers – Virtual Switch Debug and GPIO Status and Control (Offsets A30h – B6Ch)	A30h – B6Ch		
Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets B70h – B7Ch)	B70h – B7Ch	B70h – B7Ch	B70h – B7Ch
Device-Specific Registers – Physical Layer (Offsets B80h – BC8h)	B80h – BC8h	B80h – BC8h	
Multicast Extended Capability Registers (Offsets E00h – E2Ch) – All Modes Except Legacy NT	E00h – E2Ch	E00h – E2Ch	E00h – E2Ch
Device-Specific Registers – Virtual Switch (Offset F20h), Virtual Switch Mode Only	F20h		
ACS Extended Capability Registers (Offsets F24h – F2Ch)	F24h – F2Ch	F24h – F2Ch	F24h – F2Ch
Device-Specific Registers (Offsets F30h – FB0h)			
Device-Specific Registers – Egress Control (Offsets F30h – F44h)	F30h – F44h	F30h – F44h	F30h – F44h
Device-Specific Registers – Ingress Control and Port Enable (Offsets F48h – F6Ch)	F48h – F6Ch	F48h – F6Ch	F48h – F6Ch
Device-Specific Registers – Error Checking and Debug (Offsets F70h – FB0h)	F70h – FB0h	F70h – FB0h	F70h – FB0h
Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)	FB4h – FDCh	FB4h – FDCh	FB4h – FDCh

13.4 Register Access

Each PEX 8649 Port implements a 4-KB Configuration Space. The lower 256 bytes (offsets 00h through FFh) are the PCI-compatible Configuration Space, and the upper 960 Dwords (offsets 100h through FFFh) are the PCI Express Extended Configuration Space. The PEX 8649 supports six mechanisms for accessing the Transparent Mode registers:

- PCI r3.0-Compatible Configuration Mechanism
- PCI Express Enhanced Configuration Access Mechanism
- Device-Specific Memory-Mapped Configuration Mechanism
- I^{2}C Slave Interface (refer to Section 7.2, "I^{2}C Slave Interface")
- SMBus Slave Interface (refer to Section 7.3, "SMBus Slave Interface")
- Serial Peripheral Interface (SPI) Bus (refer to Chapter 6, "Serial EEPROM Controller")

The sideband register access mechanisms (serial EEPROM, I^{2}C, and/or SMBus) can modify Read-Only (RO) register values.

Each Port captures the Bus Number and Device Number on every Type 0 Configuration Write, as required by the *PCI r3.0*. Therefore, following a Fundamental Reset, software must initially perform a Configuration Write to each Port (using either the PCI r3.0-Compatible Configuration Mechanism or PCI Express Enhanced Configuration Access Mechanism), to allow each Port to capture its designated Bus Number and Device Number. The initial access to each Port, *for example*, could be a Configuration Write Request to a RO register, such as the **Device ID** / **Vendor ID** register (offset 00h).

Note: *An option is provided to allow the serial EEPROM and/or I^{2}C/SMBus to initialize the* ***Captured Bus and Device Numbers*** *registers (offset 1DCh, in each Port), instead of the required initial Configuration Write to each Port; however, this option is not recommended.*

13.4.1 *PCI r3.0*-Compatible Configuration Mechanism

The *PCI r3.0*-Compatible Configuration mechanism provides standard access to the PEX 8649 Ports' first 256 bytes (the bytes at offsets 00h through FFh) of the PCI Express Configuration Space. The mechanism uses PCI Type 0 and Type 1 Configuration transactions to access the PEX 8649 Configuration registers. Each Port can convert a Type 1 Configuration Request (destined to a downstream Port or device) to a Type 0 Configuration Request (targeting the next downstream Port or device), as described below.

The PEX 8649 decodes all Type 1 Configuration accesses received on its upstream Port(s), when any of the following conditions exist:

- If the Bus Number in the Configuration access is not within the upstream Port(s') Secondary Bus Number and Subordinate Bus Number range, the PEX 8649 upstream Port(s) respond(s) with an Unsupported Request (UR).
- Specified Bus Number in the Configuration access is the PEX 8649 internal virtual PCI Bus Number, the PEX 8649 automatically converts the Type 1 Configuration access into the appropriate Type 0 Configuration access for the specified device.
  - If the specified device corresponds to the PCI-to-PCI bridge in one of the PEX 8649 downstream Ports, the PEX 8649 processes the Read or Write Request to the specified downstream Port register specified in the original Type 1 Configuration access.
  - If the specified Device Number does not correspond to any of the PEX 8649 downstream Port Device Numbers, the PEX 8649 responds with a UR.
- If the specified Bus Number in the Type 1 Configuration access is not the PEX 8649 internal virtual PCI Bus Number, but is the number of one of the PEX 8649 downstream Port secondary/ subordinate buses, the PEX 8649 passes the Configuration access on to the PCI Express Link attached to that PEX 8649 downstream Port.
- If the specified Bus Number is the downstream Port Secondary Bus Number, and the specified Device Number is 0, the PEX 8649 converts the Type 1 Configuration access to a Type 0 Configuration access before passing it on.
  - If the specified Device Number is not 0, the downstream Port drops the Transaction Layer Packet (TLP) and generates a UR.
- If the specified Bus Number is not the downstream Port Secondary Bus Number, the PEX 8649 passes along the Type 1 Configuration access, without change.

Because the mechanism is limited to the first 256 bytes of the PCI Express Configuration Space of the PEX 8649 Ports, the PCI Express Enhanced Configuration Access Mechanism or Device-Specific Memory-Mapped Configuration Mechanism must be used to access beyond Byte FFh. The PCI Express Enhanced Configuration Access mechanism can access the registers in the PCI-compatible region, as well as those in the PCI Express Extended Configuration Space.

13.4.2 PCI Express Enhanced Configuration Access Mechanism

The PCI Express Enhanced Configuration Access mechanism is implemented on all PCI Express PCs and on systems that do not implement a processor-specific firmware interface to the Configuration Space. The mechanism provides a Memory-Mapped Address space in the Root Complex, through which the Root Complex translates a Memory access into one or more Configuration Requests. Device drivers normally use an application programming interface (API) provided by the Operating System, to use this mechanism.

The PCI Express Enhanced Configuration Access mechanism can be used to access all PEX 8649 registers.

13.4.3 Device-Specific Memory-Mapped Configuration Mechanism

The Device-Specific Memory-Mapped Configuration mechanism provides a method to access the Configuration registers of all Ports in a single 256-KB Memory map, as listed in Table 13-3. The registers of each Port are contained within a 4-KB range. The PEX 8649 supports up to 12 simultaneously active Ports.

This mechanism follows the *PCI Express Base r2.0* Configuration Request Routing rules, which do not allow the propagation of Configuration Requests from downstream-to-upstream nor peer-to-peer. By default, if any PEX 8649 downstream Port receives a Memory Request from a downstream device targeting the PEX 8649 Configuration registers, the Port:

- Responds to a Memory Read Request with a UR
- By default:
  - Silently discards a Memory Write Request (in compliance with the *PCI Express Base r2.0*) –or–
  - If the Port’s **ECC Error Check Disable** register *Software Force Non-Posted Request* bit (offset 720h[3]) is Set, the Port responds with a UR

In Memory Requests that target PEX 8649 registers, the Payload Length indicated within the Memory Request Header must be 1 DWord. Lengths greater than 1 DWord result in a Completer Abort error.

To use this mechanism, program the upstream Port(s) Type 1 Configuration Space **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, Upstream Port(s), offsets 10h and 14h, respectively), which are typically enumerated at boot time by BIOS or the Operating System (OS) software. After the PEX 8649 upstream Port(s) BARs are enumerated, Port 0 registers can be accessed with Memory Reads from and Writes to the first 4 KB (0000h to 0FFFh), Port 1 registers can be accessed with Memory Reads from and Writes to the second 4 KB (1000h to 1FFFh), and so forth. (Refer to Table 13-3.) Within each of these 4-KB windows, individual registers are located at the DWord offsets indicated in Table 13-1.

In Virtual Switch mode, each virtual switch upstream Port has its own **BAR0/1** register for Memory Request access to all Port registers (excluding Chip and Station registers) within its Virtual Switch hierarchy. The Port mapping listed in Table 13-3 applies to all virtual switches; however, only the Management Port mapping can access the Chip and Station registers, as well as the registers of all virtual switches. The 4-KB Address blocks corresponding to Ports that exist in a different virtual switch ***cannot*** be accessed with the **BAR0/1** mapping of an upstream Port that is not the designated Management Port. Such attempted accesses are handled as No Operation (NOP) (Writes are ignored, Reads return 0h).

Table 13-3. Register Offsets from Upstream Port BAR0/1 Base Address

Port Number	Internal Register 4-KB Memory Space Range	Location Range
Port 0	0_0000h to 0_0FFFh	0 to 4 KB
Port 1	0_1000h to 0_1FFFh	4 to 8 KB
Port 2	0_2000h to 0_2FFFh	8 to 12 KB
Port 3	0_3000h to 0_3FFFh	12 to 16 KB
Port 16	1_0000h to 1_0FFFh	64 to 68 KB
Port 17	1_1000h to 1_1FFFh	68 to 72 KB
Port 18	1_2000h to 1_2FFFh	72 to 76 KB
Port 19	1_3000h to 1_3FFFh	76 to 80 KB
Port 20	1_4000h to 1_4FFFh	80 to 84 KB
Port 21	1_5000h to 1_5FFFh	84 to 88 KB
Port 22	1_6000h to 1_6FFFh	88 to 92 KB
Port 23	1_7000h to 1_7FFFh	92 to 96 KB

13.5 Register Descriptions

The remainder of this chapter details the PEX 8649 registers, including:

- Bit/field names
- Description of register functions for the PEX 8649 upstream Port(s), downstream Ports, and virtual switches
- Type (*such as* RW or HwInit; refer to Table 13-4 for Type descriptions)
- Whether the power-on/reset value can be modified, by way of the PEX 8649 serial EEPROM, and/or I^{2}C/SMBus Initialization feature
- Default power-on/reset value

Table 13-4. Register Types, Grouped by User Accessibility

Type	Description
HwInit	**Hardware-Initialized** Refers to the PEX 8649 Hardware-Initialization mechanism or PEX 8649 Serial EEPROM and/or I^{2}C register Initialization features. RO after initialization and can only be reset with a Fundamental Reset. HwInit register bits are not modified by a Soft Reset.
RO	**Read-Only** Read-Only and cannot be altered by software. Permitted to be initialized by the PEX 8649 Hardware-Initialization mechanism or PEX 8649 serial EEPROM and/or I^{2}C register Initialization features.
ROS	**Read-Only, Sticky** Same as RO, except that bits are neither initialized nor modified by a Soft Reset.
RsvdP	***Reserved* and Preserved** ***Reserved*** for future RW implementations. Registers are RO and must return 0 when read. Software must preserve value read for Writes to bits.
RsvdZ	***Reserved* and Zero** ***Reserved*** for future RW1C implementations. Registers are RO and must return 0 when read. Software must use 0 for Writes to bits.
RW	**Read-Write** Read/Write and permitted to be Set or Cleared by software to the needed state.
RW1C	**Write 1 to Clear Status (Transparent mode)** Indicates status when read. A status bit Set by the system (to indicate status) is Cleared by writing 1 to that bit. Writing 0 has no effect. **Read-Write, Clear Interrupt (NT mode, Doorbell interrupts, Base mode only)** Indicates that a value of 1 Clears the interrupt.
RW1CS	**Write 1 to Clear, Sticky** Same as RW1C, except that bits are neither initialized nor modified by a Soft Reset.
RW1S	**Read-Write, Set Interrupt (NT mode, Doorbell interrupts, Base mode only)** Indicates that a value of 1 Sets the interrupt.
RWS	**Read-Write, Sticky** Same as RW, except that bits are Set or Cleared by software to the needed state. Bits are neither initialized nor modified by a Soft Reset.
RZ	**Software Read Zero** Software Read always returns 0; however, software is allowed to write this register.

13.6 Port Configurations and Station/Port/Lane/SerDes Relationships

This section provides tables that list the various PEX 8649 Port configurations, in Base mode and Virtual Switch mode, in the sections that follow.

In this chapter, the term “SerDes quad” or “quad” refers to assembling SerDes modules into groups of four contiguous Lanes for testing purposes.

13.6.1 Port Configurations

Table 13-5 defines the PEX 8649 Port, Station, and Lane configurations. The Lanes are assigned to each enabled Port, in sequence, as indicated in [brackets]. The yellow highlighted cells indicate the default Parallel Hot Plug Ports. Hot Plug Port assignment is described in Section 10.8.1, “Default Parallel Hot Plug Ports – Base Mode.”

For further details, refer to Section 4.1.1.1, “Port Configurations.”

Table 13-5. Port Configurations[a]

Port Configuration Strapping STRAP_STN0_PORTCFG[1:0]	Port Configuration Register Value Port 0, Offset 300h[1:0]	Station 0 [Lanes/SerDes]/Port			
		Port 0	**Port 1**	**Port 2**	**Port 3**
00b	00b	x4 [0-3]	x4 [4-7]	x4 [8-11]	x4 [12-15]
01b	01b	x16 [0-15]			
10b	10b	x8 [0-7]	x8 [8-15]		
11b	11b	x8 [0-7]	x4 [8-11]	x4 [12-15]	
Port Configuration Strapping STRAP_STN5_PORTCFG[1:0]	**Port Configuration Register Value Port 0, Offset 300h[11:10]**	**Station 5 [Lanes/SerDes]/Port**			
		Port 20	**Port 21**	**Port 22**	**Port 23**
00b	00b	x4 [16-19]	x4 [20-23]	x4 [24-27]	x4 [28-31]
01b	01b	x16 [16-31]			
10b	10b	x8 [16-23]	x8 [24-31]		
11b	11b	x8 [16-23]	x4 [24-27]	x4 [28-31]	
Port Configuration Strapping STRAP_STN4_PORTCFG[1:0]	**Port Configuration Register Value Port 0, Offset 300h[9:8]**	**Station 4 [Lanes/SerDes]/Port**			
		Port 16	**Port 17**	**Port 18**	**Port 19**
00b	00b	x4 [32-35]	x4 [36-39]	x4 [40-43]	x4 [44-47]
01b	01b	x16 [32-47]			
10b	10b	x8 [32-39]	x8 [40-47]		
11b	11b	x8 [32-39]	x4 [40-43]	x4 [44-47]	

[a] *Register offset 300h is located, as follows:*

Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port.

13.6.2 Virtual Switch Port Configurations – Virtual Switch Mode

Strapping balls define the quantity of switches (up to four virtual switches, based upon the STRAP_VS_MODE[1:0] state), the upstream and downstream Ports, Port size, and Management Port. The Management Port and/or I^{2}C/SMBus Slave Interface can re-configure the virtual switches and dynamically re-assign downstream Ports belonging to one virtual switch, to any other virtual switch, by programming the **VS*x* Port Vector** register(s) (Port 0, accessible through the Management Port, offsets 380h through 38Ch).

Each Port can be assigned to only one virtual switch; therefore, a Port must be removed from the Virtual Switch *x* Vector to which it is assigned, prior to adding that Port to a different Virtual Switch *x* Vector. Following dynamic re-assignment of a downstream Port from one virtual switch to another virtual switch, that Port should be reset by Management Port software or the I^{2}C/SMBus Slave Interface by Setting, and then Clearing, the corresponding Port's **Port Reset** register *Reset Port x Vector* bit (Port 0, accessible through the Management Port, offset 3A0h[23:16, 3:0]).

The Management Port, serial EEPROM, and/or I^{2}C/SMBus Slave Interface can configure any single Port within a virtual switch as that virtual switch's upstream Port, by programming the **VS*x* Upstream** register(s) (Port 0, accessible through the Management Port, offsets 360h through 36Ch).

Table 13-6 lists the default Port configuration according to the number of enabled virtual switches. The default Hot Plug Ports and balls are indicated as well. The Port Numbers referenced correspond to those listed in Table 13-5.

For further details, refer to Section 4.1.1.2, "Virtual Switch Port Configurations – Virtual Switch Mode."

Table 13-6. Virtual Switch Port Configurations and Default Parallel Hot Plug Ports – Virtual Switch Mode

Number of Virtual Switches	STRAP_VS_MODE[1:0] Value	Upstream Ports	Downstream Ports	Default Hot Plug Ports and Balls
2	LH	P0	P1, P2, P3, P20, P21	P20-B
		P16	P17, P18, P19, P22, P23	P22-C
3	HL	P0	P1, P2, P3	P1-B
		P16	P17, P18, P19	P17-C
		P20	P21, P22, P23	
4	HH	P0	P1, P2	P1-B
		P16	P3, P17	P3-C
		P20	P21, P18	
		P22	P23, P19	

13.6.3 Station, Station Register Port Number, Physical Port, Physical Lane and SerDes Module, and SerDes Quad Relationships

Table 13-7 provides an explanation of the Station, Station register Port Number, physical Port, physical Lane and SerDes module, and SerDes quad relationships, when all Ports are enabled. These relationships apply to Base mode and Virtual Switch mode.

Notes: *In this section, the term "SerDes quad" or "quad" refers to assembling SerDes modules into groups of four contiguous Lanes for testing purposes.*

The Station register Port Numbers – Ports 0, 16, and 20 – are listed in addition to the individual Ports within the Station.

Table 13-7. Station, Station Register Port Number, Physical Port, Physical Lane and SerDes Module, and SerDes Quad Relationships, When All Ports Are Enabled

Station	Station Register Port Number	Physical Port	Physical Lanes and SerDes Modules	SerDes Quad
0	0	0	0-3	0
		1	4-7	1
		2	8-11	2
		3	12-15	3
5	20	20	16-19	0
		21	20-23	1
		22	24-27	2
		23	28-31	3
4	16	16	32-35	0
		17	36-39	1
		18	40-43	2
		19	44-47	3

13.7 PCI-Compatible Type 1 Configuration Header Registers (Offsets 00h – 3Ch)

This section details the PCI-Compatible Type 1 Configuration Header registers. Table 13-8 defines the register map.

Table 13-8. PCI-Compatible Type 1 Configuration Header Register Map (All Ports)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Device ID		Vendor ID		00h
PCI Status		PCI Command		04h
PCI Class Code			PCI Revision ID	08h
PCI BIST ***(Not Supported)***	PCI Header Type	Master Latency Timer ***(Not Supported)***	Cache Line Size	0Ch
Base Address 0				10h
Base Address 1				14h
Secondary Latency Timer ***(Not Supported)***	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	18h
Secondary Status	***Not Supported/Reserved***	I/O Limit	I/O Base	1Ch
Memory Limit		Memory Base		20h
Prefetchable Memory Limit		Prefetchable Memory Base		24h
Prefetchable Memory Upper Base Address				28h
Prefetchable Memory Upper Limit Address				2Ch
I/O Limit Upper 16 Bits		I/O Base Upper 16 Bits		30h
Reserved			Capability Pointer (40h)	34h
Expansion ROM Base Address ***(Reserved)***				38h
Not Supported/Reserved	Bridge Control	PCI Interrupt Pin	PCI Interrupt Line	3Ch

Register 13-1. 00h PCI Configuration ID (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
15:0	**Vendor ID** Identifies the device manufacturer. Defaults to the PCI-SIG-issued Vendor ID of PLX (10B5h), if not overwritten by serial EEPROM and/or I^{2}C.	RO	Yes	10B5h
31:16	**Device ID** Identifies the particular device. Defaults to the PLX part number for the PEX 8649, if not overwritten by serial EEPROM and/or I^{2}C.	RO	Yes	8649h

Register 13-2. 04h PCI Command/Status (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
PCI Command				
0	**I/O Access Enable** 0 = PEX 8649 ignores I/O Space accesses on the corresponding Port's primary interface 1 = PEX 8649 responds to I/O Space accesses on the corresponding Port's primary interface	RW	Yes	0
1	**Memory Access Enable** 0 = PEX 8649 ignores Memory Space accesses on the corresponding Port's primary interface 1 = PEX 8649 responds to Memory Space accesses on the corresponding Port's primary interface	RW	Yes	0
2	**Bus Master Enable** Controls PEX 8649 Memory and I/O Request forwarding upstream. Neither affect Message (including INT*x* Interrupt Messages) forwarding nor Completions traveling upstream or downstream. 0 = PEX 8649 handles Memory and I/O Requests received on the corresponding Port downstream/secondary interface as Unsupported Requests (URs); for Non-Posted Requests, the PEX 8649 returns a Completion with UR Completion status. Because MSI Messages are in-band Memory Writes, disables MSI Messages as well. 1 = PEX 8649 forwards Memory and I/O Requests upstream.	RW	Yes	0
3	**Special Cycle Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
4	**Memory Write and Invalidate Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
5	**VGA Palette Snoop** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
6	**Parity Error Response Enable** Controls bit 24 (*Master Data Parity Error Detected*).	RW	Yes	0
7	**IDSEL Stepping/Wait Cycle Control** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0

Register 13-2. 04h PCI Command/Status (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
8	**SERR# Enable** Controls bit 30 (*Signaled System Error*). 1 = Enables reporting of Fatal and Non-Fatal errors detected by the device to the Root Complex, and, enables primary interface forwarding of ERR_FATAL and ERR_NONFATAL Messages from downstream Ports and devices when the Port's **Bridge Control** register *SERR# Enable* bit (offset 3Ch[17]) is Set	RW	Yes	0
9	**Fast Back-to-Back Transactions Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0.*	RsvdP	No	0
10	**Interrupt Disable** 0 = Corresponding PEX 8649 Port is enabled to generate INT*x* Interrupt Messages and assert PEX_INTA# and/or VS*x*_PEX_INTA# output 1 = Corresponding PEX 8649 Port is prevented from generating INT*x* Interrupt Messages and asserting PEX_INTA# and/or VS*x*_PEX_INTA# output	RW	Yes	0
15:11	***Reserved***	RsvdP	No	0-0h

Register 13-2. 04h PCI Command/Status (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
PCI Status				
18:16	***Reserved***	RsvdP	No	000b
19	**Interrupt Status** 0 = No INT*x* Interrupt Message is pending 1 = INT*x* Interrupt Message is pending internally to the corresponding PEX 8649 Port –or– PEX_INTA# and/or VS*x*_PEX_INTA# (if enabled) is (are) asserted	RO	No	0
20	**Capability List** Capability function is supported. Set, as required by the *PCI Express Base r2.0*.	RO	Yes	1
21	**66 MHz Capable** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
22	***Reserved***	RsvdP	No	0
23	**Fast Back-to-Back Transactions Capable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
24	**Master Data Parity Error Detected** If bit 6 (*Parity Error Response Enable*) is Set, the corresponding PEX 8649 Port Sets this bit when the Port: • Forwards the poisoned TLP Write Request from the secondary to the primary interface, –or– • Receives a Completion marked as poisoned on the primary interface If the *Parity Error Response Enable* bit is Cleared, the PEX 8649 never Sets this bit. This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
26:25	**DEVSEL# Timing** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	00b
27	**Signaled Target Abort** The upstream Port(s) Set(s) this bit if one of the following conditions exist: • Upstream Port receives a Memory Request targeting a PEX 8649 register, and the Payload Length (indicated within the Memory Request Header) is greater than 1 DWord • Upstream Port receives a Memory Request targeting a PEX 8649 register address within a non-existent Port • Transparent downstream Port Sets this bit if it detects an Access Control Services (ACS) violation This error is reported by the **Uncorrectable Error Status** register *Completer Abort Status* bit (offset FB8h[15]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0

Register 13-2. 04h PCI Command/Status (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
28	**Received Target Abort** ***Reserved***	RsvdP	No	0
29	**Received Master Abort** ***Reserved***	RsvdP	No	0
30	**Signaled System Error** If bit 8 (*SERR# Enable*) is Set, the corresponding PEX 8649 Port Sets this bit when it transmits or forwards an ERR_FATAL or ERR_NONFATAL Message upstream. This error is natively reported by the **Device Status** register *Fatal Error Detected* and *Non-Fatal Error Detected* bits (offset 70h[18:17], respectively), which are mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
31	**Detected Parity Error** This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility. 1 = Corresponding Port received a Poisoned TLP on its primary side, regardless of the bit 6 (*Parity Error Response Enable*) state	RW1C	Yes	0

Register 13-3. 08h PCI Class Code and Revision ID (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
PCI Revision ID				
7:0	**Revision ID** Unless overwritten by the serial EEPROM, returns the Silicon Revision (AAh), the PLX-assigned Revision ID for this version of the PEX 8649. The PEX 8649 Serial EEPROM register Initialization capability is used to replace the PLX Revision ID with another Revision ID.	RO	Yes	AAh
PCI Class Code				**060400h**
15:8	**Register-Level Programming Interface** The PEX 8649 Ports support the *PCI-to-PCI Bridge r1.2* requirements, but not subtractive decoding, on their upstream interface.	RO	Yes	00h
23:16	**Sub-Class Code** PCI-to-PCI bridge.	RO	Yes	04h
31:24	**Base Class Code** Bridge device.	RO	Yes	06h

Register 13-4. 0Ch Miscellaneous Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
Cache Line Size				
7:0	**Cache Line Size** System Cache Line Size. Implemented as a RW field for Conventional PCI compatibility purposes and does not impact PEX 8649 functionality.	RW	Yes	00h
Master Latency Timer				
15:8	**Master Latency Timer** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	00h
PCI Header Type				
22:16	**Configuration Layout Type** The corresponding PEX 8649 Port Configuration Space Header adheres to the Type 1 PCI-to-PCI Bridge Configuration Space layout defined by the *PCI-to-PCI Bridge r1.2*.	RO	No	01h
23	**Multi-Function Device** 0 = Single-function device 1 = Indicates multiple (up to eight) functions (logical devices), each containing its own, individually addressable Configuration Space, 256 DWords in size	RO	No	0
PCI BIST				
31:24	**PCI BIST** ***Not supported*** Built-In Self-Test (BIST) Pass or Fail.	RsvdP	No	00h

Register 13-5. 10h Base Address 0 (Upstream Port(s))

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
0	**Memory Space Indicator** 0 = Base Address register maps the PEX 8649 Configuration registers into Memory space ***Note:*** *The upstream Ports is (are) hardwired to 0.*	Upstream	RO	No	0
	Reserved	Downstream	RsvdP	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	Upstream	RO	Yes	00b
	Reserved	Downstream	RsvdP	No	00b
3	**Prefetchable** 0 = Base Address register maps the PEX 8649 Configuration registers into Non-Prefetchable Memory space ***Note:*** *The upstream Ports is (are) hardwired to 0.*	Upstream	RO	Yes	0
	Reserved	Downstream	RsvdP	No	0
17:4	***Reserved***		RsvdP	No	0-0h
31:18	**Base Address 0** Base Address (**BAR0**) for the Device-Specific Memory-Mapped Configuration mechanism.	Upstream	RW	Yes	0-0h
	Reserved	Downstream	RsvdP	No	0-0h

Register 13-6. 14h Base Address 1 (Upstream Port(s))

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
31:0	**Base Address 1** For 64-bit addressing, Base Address 1 (**BAR1**) extends Base Address 0 (**BAR0**) to provide the upper 32 Address bits when the **Base Address 0** register *Memory Map Type* field (Upstream Port(s), offset 10h[2:1]) is programmed to 10b.	Upstream	RW	Yes	0000_0000h
	RO when the **Base Address 0** register is not enabled as a 64-bit BAR (*Memory Map Type* field (Upstream Port(s), offset 10h[2:1]) is not programmed to 10b).		RO	Yes	0000_0000h
	Reserved	Downstream	RsvdP	No	0000_0000h

Register 13-7. 18h Bus Number (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
7:0	**Primary Bus Number** Primary Bus Number of this PCI-to-PCI bridge. Records the Bus Number of the PCI Bus segment to which the primary interface of this Port is connected. Set by Configuration software.	RW	Yes	00h
15:8	**Secondary Bus Number** Secondary Bus Number of this PCI-to-PCI bridge. Records the Bus Number of the PCI Bus segment that is the secondary interface of this Port. Set by Configuration software.	RW	Yes	00h
23:16	**Subordinate Bus Number** Subordinate Bus Number of this PCI-to-PCI bridge. Records the Bus Number of the highest numbered PCI Bus segment that is subordinate to this Port. Set by Configuration software.	RW	Yes	00h
31:24	**Secondary Latency Timer** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0.*	RsvdP	No	00h

Register 13-8. 1Ch Secondary Status, I/O Limit, and I/O Base (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
	Note: *If ISA Addressing mode is enabled (**PCI Command** register I/O Access Enable bit, offset 04h[0], is Set), the PEX 8649 Port forwards I/O transactions from its primary interface to its secondary interface (downstream) if an I/O address is within the range defined by the **I/O Base** and **I/O Limit** registers when the Base is less than or equal to the Limit.* *Conversely, the PEX 8649 Port forwards I/O transactions from its secondary interface to its primary interface (upstream) if an I/O address is outside this Address range. If the PEX 8649 Port does not implement an I/O Address range, the Port forwards all I/O transactions on its secondary interface upstream, to its primary interface.*			
	I/O Base			
3:0	**I/O Base Addressing Capability** 1h = 32-bit I/O Address decoding is supported All other encodings are ***reserved***.	RO	Yes	1h
7:4	**I/O_BAR[15:12]** I/O Base Address[15:12]. The PEX 8649 Ports use their **I/O Base** and **I/O Limit** registers to determine the address range of I/O transactions to forward from one interface to the other. I/O Base Address[15:12] bits specify the corresponding PEX 8649 Port I/O Base Address[15:12]. The PEX 8649 assumes I/O Base Address[11:0]=000h. For 16-bit I/O addressing, the PEX 8649 assumes Address[31:16]=0000h. For 32-bit addressing, the PEX 8649 decodes Address[31:0], and uses the **I/O Upper Base and Limit Address** register *I/O Base Upper 16 Bits* and *I/O Limit Upper 16 Bits* fields (offset 30h[15:0 and 31:16], respectively).	RW	Yes	Fh
	I/O Limit			
11:8	**I/O Limit Addressing Capability** 1h = 32-bit I/O Address decoding is supported All other encodings are ***reserved***.	RO	Yes	1h
15:12	**I/O_Limit[15:12]** I/O Limit Address[15:12]. The PEX 8649 Ports use their **I/O Base** and **I/O Limit** registers to determine the Address range of I/O transactions to forward from one interface to the other. I/O Limit Address[15:12] bits specify the corresponding PEX 8649 Port I/O Limit Address[15:12]. The PEX 8649 assumes I/O Limit Address[11:0]=FFFh. For 16-bit I/O addressing, the PEX 8649 decodes Address bits [15:0] and assumes I/O Limit Address[31:16]=0000h. For 32-bit addressing, the PEX 8649 decodes Address bits [31:0], and uses the **I/O Upper Base and Limit Address** register *I/O Base Upper 16 Bits* and *I/O Limit Upper 16 Bits* fields (offset 30h[15:0 and 31:16], respectively). If the I/O Limit Address is less than the I/O Base Address, the PEX 8649 does not forward I/O transactions from the corresponding Port primary/upstream bus to its secondary/downstream bus. However, the PEX 8649 forwards all I/O transactions from the secondary bus of the corresponding Port to its primary bus.	RW	Yes	0h

Register 13-8. 1Ch Secondary Status, I/O Limit, and I/O Base (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
	Secondary Status			
20:16	***Reserved***	RsvdP	No	0-0h
21	**66 MHz Capable** ***Not supported*** 0 = Not enabled, because PCI Express does ***not support*** 66 MHz	RsvdP	No	0
22	***Reserved***	RsvdP	No	0
23	**Fast Back-to-Back Transactions Capable** ***Reserved*** Not enabled, because PCI Express does ***not support*** this function.	RsvdP	No	0
24	**Master Data Parity Error** If the **Bridge Control** register *Parity Error Response Enable* bit (offset 3Ch[16]) is Set, the corresponding PEX 8649 Port Sets this bit when transmitting or receiving a TLP on its downstream side, and when either of the following two conditions occur: • Port receives Completion marked poisoned • Port forwards poisoned TLP Write Request If the *Parity Error Response Enable* bit is Cleared, the PEX 8649 never Sets this bit. These errors are reported by the Port's **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), and mirrored to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
26:25	**DEVSEL# Timing** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	00b
27	**Signaled Target Abort** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
28	**Received Target Abort** Cleared, as required by the *PCI Express Base r2.0*, because the PEX 8649 never initiates a Request itself.	RsvdP	No	0
29	**Received Master Abort** Cleared, as required by the *PCI Express Base r2.0*, because the PEX 8649 never initiates a Request itself.	RsvdP	No	0
30	**Received System Error** 1 = Downstream Port received an ERR_FATAL or ERR_NONFATAL Message on its secondary interface from a downstream device	RW1C	Yes	0
31	**Detected Parity Error** 1 = Downstream Port received a poisoned TLP from a downstream device (Set regardless of the **Bridge Control** register *Parity Error Response Enable* bit (offset 3Ch[16]) state)	RW1C	Yes	0

Register 13-9. 20h Memory Base and Limit (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
Note: *The PEX 8649 Port forwards Memory transactions from its primary interface to its secondary interface (downstream) if a Memory address is within the range defined by the* ***Memory Base*** *and* ***Memory Limit*** *registers (when the Base is less than or equal to the Limit).* *Conversely, the PEX 8649 Port forwards Memory transactions from its secondary interface to its primary interface (upstream) if a Memory address is outside this Address range (provided that the address is not within the range defined by the* ***Prefetchable Memory Base*** *(offsets 28h + 24h[15:0]) and* ***Prefetchable Memory Limit*** *(offsets 2Ch + 24h[31:16]) registers).*				
Memory Base				
3:0	***Reserved***	RsvdP	No	0h
15:4	**MEM_BAR[31:20]** Memory Base Address[31:20]. Specifies the corresponding PEX 8649 Port Non-Prefetchable Memory Base Address[31:20]. The PEX 8649 assumes Memory Base Address[19:0]=0_0000h.	RW	Yes	FFFh
Memory Limit				
19:16	***Reserved***	RsvdP	No	0h
31:20	**MEM_Limit[31:20]** Memory Limit Address[31:20]. Specifies the corresponding PEX 8649 Port Non-Prefetchable Memory Limit Address[31:20]. The PEX 8649 assumes Memory Limit Address[19:0]=F_FFFFh.	RW	Yes	000h

Register 13-10. 24h Prefetchable Memory Base and Limit (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
Note: *The PEX 8649 Port forwards Memory transactions from its primary interface to its secondary interface (downstream) if a Memory address is within the range defined by the **Prefetchable Memory Base** (offsets 28h + 24h[15:0]) and **Prefetchable Memory Limit** (offsets 2Ch + 24h[31:16]) registers (when the Base is less than or equal to the Limit).* *Conversely, the PEX 8649 Port forwards Memory transactions from its secondary interface to its primary interface (upstream) if a Memory address is outside this Address range (provided that the address is not within the range defined by the **Memory Base** and **Memory Limit** registers (offset 20h)).*				
Prefetchable Memory Base				
0	**Prefetchable Memory Base Capability** 0 = Corresponding PEX 8649 Port supports 32-bit Prefetchable Memory Addressing 1 = Corresponding PEX 8649 Port defaults to 64-bit Prefetchable Memory Addressing support, as required by the *PCI Express Base r2.0* ***Note:*** *If the application needs 32-bit only Prefetchable space, the serial EEPROM and/or I^{2}C must Clear both this bit and bit 16 (Prefetchable Memory Limit Capability).*	RO	Yes	1
3:1	***Reserved***	RsvdP	No	000b
15:4	**PMEM_BAR[31:20]** Prefetchable Memory Base Address[31:20]. Specifies the corresponding PEX 8649 Port Prefetchable Memory Base Address[31:20]. The PEX 8649 assumes Prefetchable Memory Base Address[19:0]=0_0000h.	RW	Yes	FFFh
Prefetchable Memory Limit				
16	**Prefetchable Memory Limit Capability** 0 = Corresponding PEX 8649 Port supports 32-bit Prefetchable Memory Addressing 1 = Corresponding PEX 8649 Port defaults to 64-bit Prefetchable Memory Addressing support, as required by the *PCI Express Base r2.0*	RO	Yes	1
19:17	***Reserved***	RsvdP	No	000b
31:20	**PMEM_Limit[31:20]** Prefetchable Memory Limit Address[31:20]. Specifies the corresponding PEX 8649 Port Prefetchable Memory Limit Address[31:20]. The PEX 8649 assumes Prefetchable Memory Limit Address[19:0]=F_FFFFh.	RW	Yes	000h

Register 13-11. 28h Prefetchable Memory Upper Base Address (All Ports)

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
31:0	**PBUP[63:32]** Prefetchable Memory Base Address[63:32]. The PEX 8649 uses this register for Prefetchable Memory Upper Base Address[63:32]. When the **Prefetchable Memory Base** register *Prefetchable Memory Base Capability* field indicates 32-bit addressing, this register is RO and returns 0000_0000h.	Offset 24h[0]=1	RW	Yes	0000_0000h
		Offset 24h[0]=0	RO	No	0000_0000h

Register 13-12. 2Ch Prefetchable Memory Upper Limit Address (All Ports)

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
31:0	**PLIMUP[63:32]** Prefetchable Memory Limit Address[63:32]. The PEX 8649 uses this register for Prefetchable Memory Upper Limit Address[63:32]. When the **Prefetchable Memory Limit** register *Prefetchable Memory Limit Capability* field indicates 32-bit addressing, this register is RO and returns 0000_0000h. ***Note:*** *The serial EEPROM must not write a non-zero value into this register when the RO attribute is Set for this register.*	Offset 24h[16]=1	RW	Yes	0000_0000h
		Offset 24h[16]=0	RO	No	0000_0000h

Register 13-13. 30h I/O Upper Base and Limit Address (All Ports)

Bit(s)	Description		Type	Serial EEPROM and I^{2}C	Default
15:0	**I/O Base Upper 16 Bits** The PEX 8649 uses this register for I/O Base Address[31:16]. When the **I/O Base** register *I/O Base Addressing Capability* field indicates 16-bit addressing, this register is RO and returns 0000h.	Offset 1Ch[3:0]=1h	RW	Yes	0000h
		Offset 1Ch[3:0]=0h	RO	No	0000h
31:16	**I/O Limit Upper 16 Bits** The PEX 8649 uses this register for I/O Limit Address[31:16]. When the **I/O Limit** register *I/O Limit Addressing Capability* field indicates 16-bit addressing, this register is RO and returns 0000h. ***Note:*** *The serial EEPROM must not write a non-zero value into this register when the RO attribute is set for this register.*	Offset 1Ch[11:8]=1h	RW	Yes	0000h
		Offset 1Ch[11:8]=0h	RO	No	0000h

Register 13-14. 34h Capability Pointer (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
7:0	**Capability Pointer** Default 40h points to the **PCI Power Management Capability** structure.	RO	Yes	40h
31:8	***Reserved***	RsvdP	No	0000_00h

Register 13-15. 38h Expansion ROM Base Address (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
31:0	**Expansion ROM Base Address** ***Reserved***	RsvdP	No	0000_0000h

Register 13-16. 3Ch Bridge Control and PCI Interrupt Signal (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
	PCI Interrupt Signal			
7:0	**PCI Interrupt Line** Interrupt line routing value. The PEX 8649 does ***not*** use this register; however, the register is included for operating system and device driver use.	RW	Yes	00h
15:8	**PCI Interrupt Pin** Identifies the Conventional PCI Interrupt Message(s) that the device (or device function) uses. Only value 00h or 01h is allowed in the PEX 8649. 00h = Indicates that the device does not use Conventional PCI Interrupt Message(s) 01h, 02h, 03h, and 04h = Maps to Conventional PCI Interrupt Messages for INTA#, INTB#, INTC#, and INTD#, respectively	RO	Yes	01h
	Bridge Control			
16	**Parity Error Response Enable** Controls the response to Poisoned TLPs. 0 = Disables the **Secondary Status** register *Master Data Parity Error* bit (offset 1Ch[24]) 1 = Enables the **Secondary Status** register *Master Data Parity Error* bit (offset 1Ch[24])	RW	Yes	0
17	**SERR# Enable** Controls forwarding of ERR_COR, ERR_FATAL, and ERR_NONFATAL from the secondary interface to the primary interface. When Set, and the **PCI Command** register *SERR# Enable* bit (offset 04h[8]) is also Set, enables the **PCI Status** register *Signaled System Error* bit (offset 04h[30]).	RW	Yes	0
18	**ISA Enable** Modifies the PEX 8649's response to ISA I/O addresses enabled by the **I/O Base** and **I/O Limit** registers (offset 1Ch[15:8 and 7:0], respectively) and located in the first 64 KB of the PCI I/O Address space (0000_0000h to 0000_FFFFh). The default state of this bit after reset is 0. 0 = If ISA Addressing mode is enabled (**PCI Command** register *I/O Access Enable* bit, offset 04h[0], is Set), the PEX 8649 Port forwards I/O Requests within the Address range defined by the **I/O Base** and **I/O Limit** registers. 1 = PEX 8649 blocks forwarding from the primary to secondary interface, of I/O transactions addressing the last 768 bytes in each 1-KB block of the Port's I/O Address range. In the opposite direction (secondary to primary), if I/O addressing mode is enabled (**PCI Command** register *I/O Access Enable* bit, offset 04h[0], is Set), the PEX 8649 Port forwards I/O transactions that address the last 768 bytes in each 1-KB block of the Port's I/O Address range. ***Note:*** *Refer also to the* ***Ingress Control*** *register Disable VGA BIOS Memory Access Decoding bit (Base mode – All Ports; Virtual Switch mode – VS Upstream Port(s), offset F60h[28]).*	RW	Yes	0

Register 13-16. 3Ch Bridge Control and PCI Interrupt Signal (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
19	**VGA Enable** Modifies the bridge response to VGA-compatible addresses. When Set, the bridge positively decodes and forwards the following addresses on the primary interface to the secondary interface (and, conversely, blocks forwarding of these addresses from the secondary interface to the primary interface): • Memory addresses within the range 000A_0000h to 000B_FFFFh • I/O addresses in the first 64 KB of the I/O Address space (AD[31:16] is 0000h), where AD[9:0] is within the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases – AD[15:10] is not decoded) Additionally, when Set, forwarding of these addresses is independent of the: • Memory and I/O Address ranges defined by the bridge **I/O Base**, **I/O Limit**, **Memory Base**, **Memory Limit**, **Prefetchable Memory Base**, and **Prefetchable Memory Limit** registers • Bit 18 (*ISA Enable*) or **PCI Command** register *VGA Palette Snoop* bit (offset 04h[5]) Settings VGA address forwarding is qualified by the **PCI Command** register *Memory Access Enable* and *I/O Access Enable* bits (offset 04h[1:0], respectively). The default state of this bit after reset must be 0. 0 = Do not forward VGA-compatible Memory and I/O addresses from the primary to the secondary interface (addresses defined above) unless they are enabled for forwarding by the defined Memory and I/O Address ranges 1 = Forward VGA-compatible Memory and I/O addresses (addresses defined above) from the primary interface to the secondary interface (when the *I/O Access Enable* and *Memory Access Enable* bits are Set), independent of the Memory and I/O Address ranges and independent of the *ISA Enable* bit ***Notes:*** *When Set in an egress Port, the Port is configured as a non-Cut-Thru path. (Refer to Section 2.1.4.2, "Cut-Thru Mode," for further details.)* *Refer also to the **Ingress Control** register Disable VGA BIOS Memory Access Decoding bit (Base mode – All Ports; Virtual Switch mode – VS Upstream Port(s), offset F60h[28]).* ***Conventional PCI VGA support** – To avoid potential I/O address conflicts, if the VGA Enable bit is Set in an upstream Port and a downstream Port, Set the **PCI Command** register I/O Access Enable bit (offset 04h[0]) in the remaining downstream Ports, unless those downstream Ports are configured to use default 32-bit address decoding and their I/O Address range is programmed above 1_0000h.*	RW	Yes	0

Register 13-16. 3Ch Bridge Control and PCI Interrupt Signal (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
20	**VGA 16-Bit Decode Enable** Used only when bit 19 (*VGA Enable*) or the **PCI Command** register *VGA Palette Snoop* bit (offset 04h[5]) is also Set, enabling VGA I/O decoding and forwarding by the bridge. Status after reset is 0. Enables system configuration software to select between 10- and 16-bit I/O address decoding, for VGA I/O register accesses forwarded from the primary interface to the secondary interface. 0 = Execute 10-bit address decodes on VGA I/O accesses 1 = Execute 16-bit address decodes on VGA I/O accesses ***Note:*** *Refer also to the **Ingress Control** register Disable VGA BIOS Memory Access Decoding bit (Base mode – All Ports; Virtual Switch mode – VS Upstream Port(s), offset F60h[28]).*	RW	Yes	0
21	**Master Abort Mode** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
22	**Secondary Bus Reset** 1 = Causes a Hot Reset on the corresponding PEX 8649 Port downstream Link	RW	Yes	0
23	**Fast Back-to-Back Transactions Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
24	**Primary Discard Timer** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
25	**Secondary Discard Timer** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
26	**Discard Timer Status** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
27	**Discard Timer SERR# Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
31:28	***Reserved***	RsvdP	No	0h

13.8 PCI Power Management Capability Registers (Offsets 40h – 44h)

This section details the PCI Power Management Capability registers. Table 13-9 defines the register map.

Table 13-9. PCI Power Management Capability Register Map (All Ports)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Power Management Capability		Next Capability Pointer (48h)	Capability ID (01h)	40h
PCI Power Management Data	PCI Power Management Control/Status Bridge Extensions ***(Reserved)***	PCI Power Management Status and Control		44h

Register 13-17. 40h PCI Power Management Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
7:0	**Capability ID** Program to 01h, to indicate that the Capability structure is the **PCI Power Management Capability** structure.	RO	Yes	01h
15:8	**Next Capability Pointer** Default 48h points to the **MSI Capability** structure.	RO	Yes	48h
18:16	**Version** Default 011b indicates compliance with the *PCI Power Mgmt. r1.2*.	RO	Yes	011b
19	**PME Clock** Power Management Event (PME) clock. Does not apply to PCI Express. Returns 0.	RsvdP	No	0
20	***Reserved***	RsvdP	No	0
21	**Device-Specific Initialization** 0 = Device-Specific Initialization is ***not*** required	RO	Yes	0
24:22	**AUX Current** The PEX 8649 does ***not support*** PME generation from the D3cold Device Power Management (PM) state; therefore, the serial EEPROM value for this field should be 000b.	RO	Yes	000b
25	**D1 Support** ***Not supported*** 0 = PEX 8649 does ***not support*** the D1 Device PM state	RsvdP	No	0
26	**D2 Support** ***Not supported*** 0 = PEX 8649 does ***not support*** the D2 Device PM state	RsvdP	No	0
31:27	**PME Support** Bits [31, 30, and 27] must be Set, to indicate that the PEX 8649 will forward PME Messages, as required by the *PCI Express Base r2.0*.	RO	Yes	19h

Register 13-18. 44h PCI Power Management Status and Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
	PCI Power Management Status and Control			
1:0	**Power State** Used to determine the Port's current Device PM state, and to program the Port into a new Device PM state. 00b = D0 01b = D1 – ***Not supported*** 10b = D2 – ***Not supported*** 11b = D3hot If software attempts to write an unsupported state to this field, the Write operation completes normally; however, the data is discarded and no state change occurs.	RW	Yes	00b
2	***Reserved***	RsvdP	No	0
3	**No Soft Reset** 1 = Devices transitioning from the D3hot to D0 Device PM state, because of Power State commands, do not perform an internal reset	RO	Yes	1
7:4	***Reserved***	RsvdP	No	0h
8	**PME Enable** 0 = Disables PME generation by the corresponding PEX 8649 Port[a] 1 = Enables PME generation by the corresponding PEX 8649 Port	RWS	No	0
12:9	**Data Select** Initially writable by serial EEPROM and I^{2}C only[b]. This Configuration Space register (CSR) access privilege changes to RW after a Serial EEPROM and/or I^{2}C Write occurs to this register. Selects the **Data** and **Data Scale** registers (fields [31:24 and 14:13], respectively). 0h = D0 power consumed 3h = D3hot power consumed 4h = D0 power dissipated 7h = D3hot power dissipated All other encodings are ***reserved***.	RO	Yes	0h
14:13	**Data Scale** Writable by serial EEPROM and I^{2}C only[b]. Indicates the scaling factor to be used when interpreting the **Data** register value. The value and meaning of this field varies, depending upon which data value is selected by field [12:9] (*Data Select*). There are four internal **Data Scale** registers (one each, per *Data Select* values 0h, 3h, 4h and 7h), per Port. For other *Data Select* values, the **Data Scale** value returned is 0h.	RO	Yes	00b
15	**PME Status** 0 = PME is not generated by the corresponding PEX 8649 Port[a] 1 = PME is being generated by the corresponding PEX 8649 Port	RW1CS	No	0

Register 13-18. 44h PCI Power Management Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	PCI Power Management Control/Status Bridge Extensions			
21:16	***Reserved***	RsvdP	No	0-0h
22	**B2/B3 Support** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.	RsvdP	No	0
23	**Bus Power/Clock Control Enable** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.	RsvdP	No	0
	PCI Power Management Data			
31:24	**Data** Writable by serial EEPROM and I^2C only[b]. There are four supported *Data Select* values (0h, 3h, 4h and 7h), per Port. For other *Data Select* values, the **Data Scale** value returned is 0h. Selected by field [12:9] (*Data Select*).	RO	Yes	00h

[a] *Because the PEX 8649 does not consume auxiliary power, this bit is not sticky, and is always Cleared at power-on reset.*

[b] *With no serial EEPROM nor previous I^2C programming, Reads return 00h for the **Data** and **Data Scale** registers (for all Data Selects).*

13.9 MSI Capability Registers (Offsets 48h – 64h)

This section details the Message Signaled Interrupt (MSI) Capability registers. Table 13-10 defines the register map.

Table 13-10. MSI Capability Register Map (All Ports)[a]

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
MSI Control		Next Capability Pointer (68h)	Capability ID (05h)	48h
MSI Address				4Ch
MSI Upper Address				50h
Reserved		MSI Data		54h
MSI Mask				58h
MSI Status				5Ch
Reserved			60h –	64h

[a] *Offsets 54h, 58h, and 5Ch change to 50h, 54h, and 58h, respectively, when the* ***MSI Control*** *register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.*

Register 13-19. 48h MSI Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	MSI Capability Header			
7:0	**Capability ID** Program to 05h, as required by the *PCI r3.0*.	RO	Yes	05h
15:8	**Next Capability Pointer** Program to 68h, to point to the **PCI Express Capability** structure.	RO	Yes	68h
	MSI Control			
16	**MSI Enable** 0 = MSIs for the corresponding Port are disabled 1 = MSIs for the corresponding Port are enabled, and INT*x* Interrupt Messages and PEX_INTA# and/or VS*x*_PEX_INTA# output assertion are disabled	RW	Yes	0
19:17	**Multiple Message Capable** 000b = PEX 8649 Port can request only one Vector 001b = PEX 8649 Port can request two Vectors 010b = PEX 8649 Port can request four Vectors 011b = PEX 8649 Port can request eight Vectors All other encodings are ***reserved***.	RO	Yes	011b
22:20	**Multiple Message Enable** 000b = PEX 8649 Port is allocated one Vector, by default. 001b = PEX 8649 Port is allocated two Vectors. 010b = PEX 8649 Port is allocated four Vectors. 011b = PEX 8649 Port is allocated eight Vectors. Up to six Vectors are used; the upper two Vectors (having the highest values of Message Data bits [2:0]) are ***not*** used. All other encodings are ***reserved***. ***Note:*** *This field should not be programmed with a value larger than that of field [19:17] (Multiple Message Capable). If the value of this field is larger than that of field [19:17], the Multiple Message Capable value takes effect.*	RW	Yes	000b
23	**MSI 64-Bit Address Capable** 0 = PEX 8649 is capable of generating MSI 32-bit addresses (**MSI Address** register, offset 4Ch, is the Message address) 1 = PEX 8649 is capable of generating MSI 64-bit addresses (**MSI Address** register, offset 4Ch, is the lower 32 bits of the Message address, and **MSI Upper Address** register, offset 50h, is the upper 32 bits of the Message address)	RO	Yes	1
24	**Per Vector Masking Capable** 0 = PEX 8649 does not have Per Vector Masking capability 1 = PEX 8649 has Per Vector Masking capability	RO	Yes	1
31:25	***Reserved***	RsvdP	No	0-0h

Register 13-20. 4Ch MSI Address (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
1:0	***Reserved***	RsvdP	No	00b
31:2	**Message Address** ***Note:*** *Refer to register offset 50h for MSI Upper Address, if offset 48h[23] is Set (default).*	RW	Yes	0-0h

Register 13-21. 50h MSI Upper Address (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**Message Upper Address** This register is valid/used only when the **MSI Control** register *MSI 64-Bit Address Capable* bit (offset 48h[23]) is Set. MSI Write transaction upper address[63:32]. ***Note:*** *Refer to register offset 4Ch for MSI Address.*	RW	Yes	0000_0000h

Register 13-22. 54h MSI Data (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Note: *The offset for this register changes from 54h, to 50h, when the **MSI Control** register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.*				
15:0	**Message Data** MSI Write transaction TLP payload.	RW	Yes	0000h
31:16	***Reserved***	RsvdP	No	0000h

Register 13-23. 58h MSI Mask (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
The interrupt sources in a PEX 8649 Port are grouped into six categories – Power Management/Hot Plug or Link State events, Device-Specific NT-Link Port events, GPIO-generated interrupts, NT-Virtual Doorbell-generated interrupts, Virtual Switch mode Doorbell events, and Virtual Switch mode Link Status events. The number of allocated MSI Vectors is determined by the **MSI Control** register *Multiple Message Capable* and *Multiple Message Enable* fields (offset 48h[19:17 and 22:20], respectively). When the number of MSI Vectors that can be requested is: • **Eight** – Each interrupt category generates its own MSI Vector. Up to six Vectors are used; the upper two Vectors (having the highest values of Message Data bits [2:0]) are ***not*** used. • **Four** – Device-Specific NT-Link Port events, Hot Plug/Power Management events, and GPIO events each generate their own MSI Vector, while all other categories are combined and generate the same Vector. • **Two** – Device-Specific NT-Link Port events generate their own MSI Vector, while all other categories are combined and generate the same Vector. • **One** – All interrupt categories generate the same MSI Vector. NT-Virtual Doorbell interrupts are generated only on the NT Port. The Type is the same, regardless of whether it is for a Transparent or NT Port. ***Note:*** *The offset for this register changes from 58h, to 54h, when the **MSI Control** register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.* *The bits in this register can be used to mask their respective **MSI Status** register bits (offset 5Ch).*					
0	**MSI Mask for Hot Plug or Link State Events** MSI mask for Power Management event- or Hot Plug or Link State event-generated interrupts.	All Ports, Offset 48h[22:20]=010b or 011b	RW	Yes	0
	MSI Mask for Shared Interrupt Sources MSI mask for all interrupt sources when the **MSI Control** register *Multiple Message Enable* field indicates that the Host has allocated one or two Vectors.	All Ports, Offset 48h[22:20]≤001b	RW	Yes	0
1	**Base Mode** **MSI Mask for Device-Specific NT-Link Port Events** ***This bit is valid only in NT mode.*** MSI mask for Device-Specific NT-Link Port event-generated interrupts. This bit (implemented only for the NT Port Virtual Interface) enables MSIs for the following NT-Link Port events, defined in the **Link Error Status Virtual** and **Link Error Mask Virtual** registers (NT Port Virtual Interface, offsets FE0h and FE4h, respectively): • NT-Link Port Correctable error (NT Port Link Interface, offset FC4h) • NT-Link Port Uncorrectable error (NT Port Link Interface, offset FB8h) • NT-Link Port Data Link Layer State change • NT-Link Port received (and consequently dropped) a Fatal or Non-Fatal Error Message	NT Port Virtual Interface, Offset 48h[22:20]=001b, 010b or 011b	RW	Yes	0
	Reserved	Otherwise, Offset 48h[22:20]=000b	RsvdP	No	0
	Virtual Switch Mode ***Reserved***		RsvdP	No	0

Register 13-23. 58h MSI Mask (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
2	**Base Mode** **MSI Mask for GPIO-Generated Interrupts**	Port 0, Offset 48h[22:20]=010b or 011b	RW	Yes	0
	Virtual Switch Mode **MSI Mask for GPIO-Generated Interrupts**	VS Upstream Port(s), Offset 48h[22:20]=010b or 011b	RW	Yes	0
	Reserved	Otherwise, Offset 48h[22:20]≤001b	RsvdP	No	0
3	**Base Mode** **MSI Mask for NT-Virtual Doorbell-Generated Interrupts** ***This bit is valid only in NT mode.*** Refer to the NT Port registers located at offsets C4Ch through C58h.	NT Port Virtual Interface, Offset 48h[22:20]=011b	RW	Yes	0
	Reserved	Otherwise, Offset 48h[22:20]≤010b	RsvdP	No	0
	Virtual Switch Mode ***Reserved***		RsvdP	No	0
4	**Base Mode** ***Reserved***		RsvdP	No	0
	Virtual Switch Mode **MSI Mask for Management Port Doorbell-Generated Interrupts**	VS Upstream Port(s) and Management Port, Offset 48h[22:20]=011b	RW	Yes	0
	Reserved	Otherwise, when offset 48h[22:20]≤010b	RsvdP	No	0
5	**Base Mode** ***Reserved***		RsvdP	No	0
	Virtual Switch Mode **MSI Mask for Management Link Status Event**	Management Port, Offset 48h[22:20]=011b	RW	Yes	0
	Reserved	Otherwise, Offset 48h[22:20]≤010b	RsvdP	No	0
31:6	***Reserved***		RsvdP	No	0-0h

Register 13-24. 5Ch MSI Status (All Ports)

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Ports</th><th>Type</th><th>Serial EEPROM and I^{2}C</th><th>Default</th></tr>
<tr><td colspan="6">The interrupt sources in a PEX 8649 Port are grouped into six categories – Power Management/Hot Plug or Link State events, Device-Specific NT-Link Port events, GPIO-generated interrupts, NT-Virtual Doorbell-generated interrupts, Virtual Switch mode Doorbell events, and Virtual Switch mode Link Status events.
The number of allocated MSI Vectors is determined by the <b>MSI Control</b> register <i>Multiple Message Capable</i> and <i>Multiple Message Enable</i> fields (offset 48h[19:17 and 22:20], respectively). When the number of MSI Vectors that can be requested is:
• <b>Eight</b> – Each interrupt category generates its own MSI Vector. Up to six Vectors are used; the upper two Vectors (having the highest values of Message Data bits [2:0]) are <b><i>not</i></b> used.
• <b>Four</b> – Device-Specific NT-Link Port events, Hot Plug/Power Management events, and GPIO events each generate their own MSI Vector, while all other categories are combined and generate the same Vector.
• <b>Two</b> – Device-Specific NT-Link Port events generate their own MSI Vector, while all other categories are combined and generate the same Vector.
• <b>One</b> – All interrupt categories generate the same MSI Vector.
NT-Virtual Doorbell interrupts are generated only on the NT Port. The Type is the same, regardless of whether it is for a Transparent or NT Port.
<b><i>Note:</i></b> <i>The offset for this register changes from 5Ch, to 58h, when the <b>MSI Control</b> register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.</i>
<i>The bits in this register can be masked by their respective <b>MSI Mask</b> register bits (offset 58h).</i></td></tr>
<tr><td rowspan="2">0</td><td><b>MSI Pending Status for Hot Plug or Link State Events</b>
MSI pending status for Power Management event- or Hot Plug or Link State event-generated interrupts.</td><td>All Ports, Offset 48h[22:20]=010b or 011b</td><td>RO</td><td>No</td><td>0</td></tr>
<tr><td><b>MSI Pending Status for Shared Interrupt Sources</b>
MSI pending status for all interrupt sources when the <b>MSI Control</b> register <i>Multiple Message Enable</i> field indicates that the Host has allocated one or two Vectors.</td><td>All Ports, Offset 48h[22:20]≤001b</td><td>RsvdP</td><td>No</td><td>0</td></tr>
</table>

Register 13-24. 5Ch MSI Status (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
1	**Base Mode** **MSI Pending Status for Device-Specific NT-Link Port Events** ***This bit is valid only in NT mode.*** This bit (implemented only for the NT Port Virtual Interface) enables MSIs for the following NT-Link Port events, defined in the **Link Error Status Virtual** and **Link Error Mask Virtual** registers (NT Port Virtual Interface, offsets FE0h and FE4h, respectively): • NT-Link Port Correctable error (NT Port Link Interface, offset FC4h) • NT-Link Port Uncorrectable error (NT Port Link Interface, offset FB8h) • NT-Link Port Data Link Layer State change • NT-Link Port received (and consequently dropped) a Fatal or Non-Fatal Error Message	NT Port Virtual Interface, Offset 48h[22:20]=001b, 010b or 011b	RO	No	0
	Reserved	Otherwise, Offset 48h[22:20]=000b	RsvdP	No	0
	Virtual Switch Mode ***Reserved***		RsvdP	No	0
2	**Base Mode** **MSI Pending Status for GPIO-Generated Interrupts**	Port 0, Offset 48h[22:20]=010b or 011b	RO	No	0
	Virtual Switch Mode **MSI Pending Status for GPIO-Generated Interrupts**	VS Upstream Port(s), Offset 48h[22:20]=010b or 011b	RO	No	0
	Reserved	Otherwise, Offset 48h[22:20]≤001b	RsvdP	No	0
3	**Base Mode** **MSI Pending Status for NT-Virtual Doorbell-Generated Interrupts** ***This bit is valid only in NT mode.*** Refer to the NT Port registers located at offsets C4Ch through C58h.	NT Port Virtual Interface, Offset 48h[22:20]=011b	RO	No	0
	Reserved	Otherwise, Offset 48h[22:20]≤010b	RsvdP	No	0
	Virtual Switch Mode ***Reserved***		RsvdP	No	0

Register 13-24. 5Ch MSI Status (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
4	**Base Mode** ***Reserved***		RsvdP	No	0
	Virtual Switch Mode **MSI Pending Status for Management Port Doorbell-Generated Interrupts**	VS Upstream Port(s) and Management Port, Offset 48h[22:20]=011b	RO	No	0
	Reserved	Otherwise, when offset 48h[22:20]≤010b	RsvdP	No	0
5	**Base Mode** ***Reserved***		RsvdP	No	0
	Virtual Switch Mode **MSI Pending Status for Management Link Status Event**	Management Port, Offset 48h[22:20]=011b	RO	No	0
	Reserved	Otherwise, Offset 48h[22:20]≤010b	RsvdP	No	0
31:6	***Reserved***		RsvdP	No	0-0h

13.10 PCI Express Capability Registers (Offsets 68h – A0h)

This section details the PCI Express Capability registers. Hot Plug Capability, Command, Status, and Events are included in these registers. Table 13-11 defines the register map.

Table 13-11. PCI Express Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Express Capability	Next Capability Pointer (A4h)	Capability ID (10h)	68h
Device Capability			6Ch
Device Status	***Not Supported/Reserved***	Device Control	70h
Link Capability			74h
Link Status	Link Control		78h
Reserved (Upstream) Slot Capability (Downstream)			7Ch
Reserved (Upstream)			80h
Slot Status (Downstream)	Slot Control (Downstream)		
Reserved			84h – 88h
Reserved (Upstream) Device Capability 2 (Downstream)			8Ch
Reserved (Upstream)			90h
Device Status 2 (***Reserved,*** Downstream)	Device Control 2 (Downstream)		
Reserved			94h
Link Status 2	Link Control 2		98h
Reserved			9Ch – A0h

Register 13-25. 68h PCI Express Capability List and Capability (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
PCI Express Capability List					
7:0	**Capability ID** Program to 10h, as required by the *PCI Express Base r2.0.*		RO	Yes	10h
15:8	**Next Capability Pointer** Program to A4h, to point to the **Subsystem Capability** structure.		RO	Yes	A4h
PCI Express Capability					
19:16	**Capability Version** The PEX 8649 Ports program this field to 2h, as required by the *PCI Express Base r2.0.*		RO	Yes	2h
23:20	**Device/Port Type** Set at reset, as required by the *PCI Express Base r2.0.*	Upstream	RO	Yes	5h
		Downstream	RO	Yes	6h
24	**Slot Implemented** 0 = Disables or connects to an upstream Port	Upstream	RsvdP	No	0
	0 = Disables or connects to an integrated component 1 = Indicates that the downstream Port connects to a slot, as opposed to being connected to an integrated component or being disabled ***Note:*** *The PEX 8649 serial EEPROM register Initialization capability and/or I^{2}C can be used to Clear this bit, indicating that the corresponding PEX 8649 downstream Port connects to an integrated component or is disabled.*	Downstream	RO	Yes	1
29:25	**Interrupt Message Number** The serial EEPROM writes 00_000b, because the Base Message and MSI Messages are the same.		RO	Yes	00_000b
31:30	***Reserved***		RsvdP	No	00b

Register 13-26. 6Ch Device Capability (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
2:0	**Maximum Payload Size Supported** Maximum Payload Size Port limitations are as follows: • 2,048 bytes if the number of Ports is ≤ 6 • 1,024 bytes if the number of Ports is > 6 and ≤ 12 000b = PEX 8649 Port supports a 128-byte maximum payload 001b = PEX 8649 Port supports a 256-byte maximum payload 010b = PEX 8649 Port supports a 512-byte maximum payload 011b = PEX 8649 Port supports a 1,024-byte maximum payload 100b = PEX 8649 Port supports a 2,048-byte maximum payload No other encodings are supported.		HwInit	Yes	011b = > 6 and ≤ 12 Ports 100b = ≤ 6 Ports
4:3	**Phantom Functions Supported** ***Not supported***		RO	Yes	00b
5	**Extended Tag Field Supported** 0 = Maximum *Tag* field is 5 bits 1 = Maximum *Tag* field is 8 bits		RO	Yes	0
8:6	**Endpoint L0s Acceptable Latency** ***Not supported*** Because the PEX 8649 is a switch and not an endpoint, the PEX 8649 does ***not support*** this feature. 000b = Disables the capability		RO	Yes	000b
11:9	**Endpoint L1 Acceptable Latency** ***Not supported*** Because the PEX 8649 is a switch and not an endpoint, the PEX 8649 does ***not support*** this feature. 000b = Disables the capability		RO	Yes	000b
14:12	***Reserved***, as required by the *PCI Express Base r2.0*.		RsvdP	No	000b
15	**Role-Based Error Reporting**		RO	Yes	1

Register 13-26. 6Ch Device Capability (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
17:16	***Reserved***		RsvdP	No	00b
25:18	**Captured Slot Power Limit Value** For the PEX 8649 upstream Port(s), the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [27:26] (*Captured Slot Power Limit Scale*).	Upstream	RO	Yes	00h
	Not valid	Downstream	RsvdP	No	00h
27:26	**Captured Slot Power Limit Scale** For the PEX 8649 upstream Port(s), the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [25:18] (*Captured Slot Power Limit Value*). 00b = 1.0 01b = 0.1 10b = 0.01 11b = 0.001	Upstream	RO	Yes	00b
	Not valid	Downstream	RsvdP	No	00b
31:28	***Reserved***		RsvdP	No	0h

Register 13-27. 70h Device Status and Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	Device Control			
0	**Correctable Error Reporting Enable** 0 = Disables 1 = Enables the corresponding PEX 8649 Port to report Correctable errors	RW	Yes	0
1	**Non-Fatal Error Reporting Enable** 0 = Disables 1 = Enables the corresponding PEX 8649 Port to report Non-Fatal errors	RW	Yes	0
2	**Fatal Error Reporting Enable** 0 = Disables 1 = Enables the corresponding PEX 8649 Port to report Fatal errors	RW	Yes	0
3	**Unsupported Request Reporting Enable** 0 = Disables 1 = Enables the corresponding PEX 8649 Port to report UR errors	RW	Yes	0
4	**Enable Relaxed Ordering** ***Not supported***	RsvdP	No	0
7:5	**Maximum Payload Size** Software can change this field to configure the PEX 8649 Ports to support other Payload Sizes; however, software cannot change this field to a value larger than that indicated by the **Device Capability** register *Maximum Payload Size Supported* field (offset 6Ch[2:0]). 000b = PEX 8649 Port supports a 128-byte maximum payload 001b = PEX 8649 Port supports a 256-byte maximum payload 010b = PEX 8649 Port supports a 512-byte maximum payload 011b = PEX 8649 Port supports a 1,024-byte maximum payload 100b = PEX 8649 Port supports a 2,048-byte maximum payload No other encodings are supported.	RW	Yes	000b
8	**Extended Tag Field Enable** ***Not supported***	RsvdP	No	0
9	**Phantom Functions Enable** ***Not supported***	RsvdP	No	0
10	**AUX Power PM Enable** ***Not supported***	RsvdP	No	0
11	**Enable No Snoop** ***Not supported***	RsvdP	No	0
14:12	**Max Read Request Size** ***Not supported***	RsvdP	No	000b
15	***Reserved*** Hardwired to 0, as required by the *PCI Express Base r2.0*.	RsvdP	No	0

Register 13-27. 70h Device Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	Device Status			
16	**Correctable Error Detected** 0 = Corresponding PEX 8649 Port did not detect a Correctable error 1 = Corresponding PEX 8649 Port detected a Correctable error, regardless of the bit 0 (*Correctable Error Reporting Enable*) state	RW1C	Yes	0
17	**Non-Fatal Error Detected** 0 = Corresponding PEX 8649 Port did not detect a Non-Fatal error 1 = Corresponding PEX 8649 Port detected a Non-Fatal error, regardless of the bit 1 (*Non-Fatal Error Reporting Enable*) state	RW1C	Yes	0
18	**Fatal Error Detected** 0 = Corresponding PEX 8649 Port did not detect a Fatal error 1 = Corresponding PEX 8649 Port detected a Fatal error, regardless of the bit 2 (*Fatal Error Reporting Enable*) state	RW1C	Yes	0
19	**Unsupported Request Detected** 0 = Corresponding PEX 8649 Port did not detect a UR 1 = Corresponding PEX 8649 Port detected a UR, regardless of the bit 3 (*Unsupported Request Reporting Enable*) state	RW1C	Yes	0
20	**AUX Power Detected** ***Not supported***	RsvdP	No	0
21	**Transactions Pending** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
31:22	***Reserved***	RsvdP	No	0-0h

Register 13-28. 74h Link Capability (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
Note: *Table 13-5 lists the Port configuration (including Link width) for each Station.*					
3:0	**Supported Link Speeds** Indicates the Port's supported Link speed. 0001b = 2.5 GT/s Link speed is supported 0010b = 5.0 GT/s and 2.5 GT/s Link speeds are supported All other encodings are ***reserved***.		RO	Yes	0010b (STRAP_RESERVED17#=H) 0001b (STRAP_RESERVED17#=L)
9:4	**Maximum Link Width** The PEX 8649 maximum Link width is x16 = 01_0000b. Actual maximum Link width is Set by the STRAP_STN*x*_PORTCFG*x* balls. 00_0000b = ***Reserved*** 00_0001b = x1 00_0010b = x2 00_0100b = x4 00_1000b = x8 01_0000b = x16 All other encodings are ***not supported***.		ROS	No	Set by STRAP_STN*x*_PORTCFG*x* ball levels, or by serial EEPROM value for the **Port Configuration**-related registers (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offsets 300h through 308h)
11:10	**Active State Power Management (ASPM) Support** Active State Link PM support. Indicates the level of ASPM supported by the Port. 01b = L0s Link PM state entry is supported 11b = L0s and L1 Link PM states are supported All other encodings are ***reserved***.		RO	Yes	11b

Register 13-28. 74h Link Capability (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
14:12	**L0s Exit Latency** Indicates the L0s Link PM state exit latency for the given PCI Express Link. Value depends upon the Port's **Synchronous Advertised N_FTS** or **Asynchronous Advertised N_FTS** register (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset B84h or B88h, respectively) *Port x Advertised N_FTS* field value, Link speed, and state of the Port's **Link Control** register *Common Clock Configuration* bit (offset 78h[6]). When the *Common Clock Configuration* bit is Set, the Synchronous Advertised N_FTS register value is used; otherwise, the Asynchronous Advertised N_FTS register value is used. Exit latency is calculated, as follows: • **2.5 GHz** – Multiply *Port x Advertised N_FTS* x 4 (4 symbol times in 1 N_FTS) x 4 ns (1 symbol time at 2.5 GT/s) • **5.0 GHz** – Multiply *Port x Advertised N_FTS* x 4 (4 symbol times in 1 N_FTS) x 2 ns (1 symbol time at 5.0 GT/s) 100b = Corresponding PEX 8649 Port L0s Link PM state Exit Latency is 512 ns to less than 1 µs at 5.0 GT/s 101b = Corresponding PEX 8649 Port L0s Link PM state Exit Latency is 1 µs to less than 2 µs at 2.5 GT/s All other encodings are ***reserved***.		RO	No	100b (5.0 GT/s) 101b (2.5 GT/s)

Register 13-28. 74h Link Capability (All Ports) ***(Cont.)***

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
17:15	**L1 Exit Latency** Indicates the L1 Link PM state exit latency for the given PCI Express Link. Value depends upon the Link speed. 001b = Corresponding PEX 8649 Port L1 Link PM state Exit Latency is 1 µs to less than 2 µs at 5.0 GT/s 010b = Corresponding PEX 8649 Port L1 Link PM state Exit Latency is 2 µs to less than 4 µs at 2.5 GT/s All other encodings are ***reserved***.		RO	Yes	001b (5.0 GT/s) 010b (2.5 GT/s)
18	**Clock Power Management Capable**		RO	Yes	0
19	***Reserved*** Must be hardwired to 0, for the upstream Port(s) and components that do not support this optional capability.	Upstream	RsvdP	No	0
	Surprise Down Error Reporting Capable Must be Set if the component supports the optional capability of detecting and reporting a Surprise Down error condition. If this bit is Cleared, the **Uncorrectable Error Status** register *Surprise Down Error Status* bit (offset FB8h[5]) is disabled. ***Note:*** *If this bit is Set and later Cleared at runtime (such as by I^2C), it must be Cleared while the Link is up; otherwise, if the Link is down when this bit is Cleared, a subsequent Surprise Down error event is not masked.*	Downstream	RO	Yes	1

Register 13-28. 74h Link Capability (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
20	***Reserved***	Upstream	RsvdP	No	0
	Data Link Layer Link Active Reporting Capable Valid for downstream Ports only.	Downstream	RO	Yes	1
21	***Reserved*** Hardwired to 0, as required by the *PCI Express Base r2.0*.	Upstream	RsvdP	No	0
	Link Bandwidth Notification Capability 1 = Indicates support for the Link Bandwidth Notification status and interrupt mechanisms	Downstream	RO	Yes	1
23:22	***Reserved***		RsvdP	No	00b
31:24	**Port Number** The Port Number is Set by signal ball Strapping options. (Refer to Table 13-5.) Station 0, STRAP_STN0_PORTCFG[1:0] – Ports 0, 1, 2, 3 Station 4, STRAP_STN4_PORTCFG[1:0] – Ports 16, 17, 18, 19 Station 5, STRAP_STN5_PORTCFG[1:0] – Ports 20, 21, 22, 23		ROS	No	Set by STRAP_STN*x*_PORTCFG*x* ball levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station x* bits (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 300h[11:8, 1:0])

Register 13-29. 78h Link Status and Control (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
	Link Control				
1:0	**Active State Power Management (ASPM)** 00b = Disable[a] 01b = Enables only L0s Link PM state Entry 10b = Enables only L1 Link PM state Entry 11b = Enables both L0s and L1 Link PM state Entries		RW	Yes	00b
2	***Reserved***		RsvdP	No	0
3	**Read Request Return Parameter Control** Read Request Return Parameter "R" control. Read Completion Boundary (RCB). Cleared, as required by the *PCI Express Base r2.0.*		RO	Yes	0
4	***Not valid***	Upstream	RsvdP	No	0
	Link Disable 1 = Places the Link on the corresponding PEX 8649 downstream Port to the *Disabled* Link Training state	Downstream	RW	Yes	0
5	***Not valid*** Always read as 0.	Upstream	RsvdP	No	0
	Retrain Link For PEX 8649 Ports, always returns 0 when read; however, software is allowed to write this register. Writing 1 to this bit causes the corresponding PEX 8649 downstream Port to initiate retraining of its PCI Express Link.	Downstream	RZ	Yes	0
6	**Common Clock Configuration** 0 = Corresponding PEX 8649 Port and the device at the other end of the corresponding Port's PCI Express Link use an asynchronous Reference Clock source 1 = Corresponding PEX 8649 Port and the device at the other end of the corresponding Port's PCI Express Link use a common (synchronous) Reference Clock source (constant phase relationship)		RW	Yes	0
7	**Extended Sync** Setting this bit causes the corresponding PEX 8649 Port to transmit: • 4,096 FTS Ordered-Sets in the L0s Link PM state, • Followed by a single SKIP Ordered-Set prior to entering the L0 Link PM state, • Finally, transmission of 1,024 TS1 Ordered-Sets in the *Recovery* state.		RW	Yes	0

Register 13-29. 78h Link Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
8	**Clock Power Management Enable** ***Reserved*** Read and Writable only when the **Link Capability** register *Clock Power Management Capable* bit is Set. The PEX 8649 does ***not support*** removal of the Reference Clock in the L1 and L2/L3 Ready Link PM states.		RsvdP	No	0
9	**Hardware-Autonomous Width Disable** ***Reserved***		RsvdP	No	0
10	***Reserved***	Upstream	RsvdP	No	0
	Link Bandwidth Management Interrupt Enable 0 = Disables interrupt generation 1 = Enables generation of an interrupt, to indicate that the **Link Status** register *Link Bandwidth Management Status* bit (offset 78h[30]) has been Set	Downstream	RW	Yes	0
11	***Reserved***	Upstream	RsvdP	No	0
	Link Autonomous Bandwidth Interrupt Enable 0 = Disables interrupt generation 1 = Enables generation of an interrupt, to indicate that the **Link Status** register *Link Autonomous Bandwidth Status* bit (offset 78h[31]) has been Set	Downstream	RW	Yes	0
15:12	***Reserved***		RsvdP	No	0h

Register 13-29. 78h Link Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
Link Status					
19:16	**Current Link Speed** Indicates the negotiated Link speed of the Port's PCI Express Link. 0001b = 2.5 GT/s Link speed 0010b = 5.0 GT/s Link speed All other encodings are ***reserved***. The value in this field is undefined when the Link is not up.		RO	No	0001b
25:20	**Negotiated Link Width** Dependent upon the physical Port configuration. Link width is determined by the negotiated value with the attached Lane/Port. If the Link is not up, the value of this field is undefined. 00_0000b = Link is down (default) 00_0001b = x1 00_0010b = x2 00_0100b = x4 00_1000b = x8 01_0000b = x16 All other encodings are ***not supported***.		RO	No	00_0000b
26	***Reserved***		RsvdP	No	0
27	***Reserved***	Upstream	RsvdP	No	0
	Link Training 1 = Indicates that the corresponding PEX 8649 downstream Port requested Link training, and the Link training is in-progress or about to start	Downstream	RO	No	0

Register 13-29. 78h Link Status and Control (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
28	**Slot Clock Configuration** 0 = Indicates that the PEX 8649 uses an independent clock 1 = Indicates that the PEX 8649 uses the same physical Reference Clock that the platform provides on the connector		HwInit	Yes	0
29	***Reserved***	Upstream	RsvdP	No	0
	Data Link Layer Link Active When Set, and the **Link Capability** register *Data Link Layer Link Active Reporting Capable* bit (offset 74h[20]) is also Set, indicates the following: • Data Link Layer (DLL) is in the *DL_Active* state • Link is operational • Flow Control (FC) Initialization has successfully completed	Downstream	RO	Yes	0
30	***Reserved***	Upstream	RsvdP	No	0
	Link Bandwidth Management Status Set by hardware to indicate that either of the following has occurred, without the Port transitioning through DL_Down status: • Link retraining has completed following a Write of 1 to the **Link Control** register *Retrain Link* bit (offset 78h[5]) • Hardware has changed Link speed or width, to attempt to correct unreliable Link operation, either through a Link Training and Status State Machine (LTSSM) timeout or higher-level process	Downstream	RW1C	Yes	0
31	***Reserved***	Upstream	RsvdP	No	0
	Link Autonomous Bandwidth Status Set by hardware to indicate that hardware has autonomously changed Link speed or width, without the Port transitioning through DL_Down status, for reasons other than to attempt to correct unreliable Link operation.	Downstream	RW1C	Yes	0

[a] *The Port Receiver must be capable of entering the L0s Link PM state, regardless of whether the state is disabled.*

Register 13-30. 7Ch Slot Capability (Downstream Ports; Upstream Port(s) Always Read(s) 0)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
Notes: *For bits [6, 4:0], the default values are shown to be 1 for downstream Ports, which is true only if the Port is Parallel and/or Serial Hot Plug-capable; otherwise, the default value is 0. This also applies to bit 17 for Serial Hot Plug Ports.* *Serial Hot Plug-capable means that the PEX 8649 has detected that an external I^{2}C I/O Expander is present.* *Each Transparent downstream Port can support one* **Parallel** *Hot Plug Controller, which uses the set of on-chip Hot Plug I/O signals designated with suffixes B and C. The assignment of Parallel Hot Plug Controllers, to individual Ports, is programmed in the* ***Parallel Hot Plug Control*** *register (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 3A4h[15:8 and 23:16] for Parallel Hot Plug Controllers B and C, respectively). All other Transparent downstream Ports support a* **Serial** *Hot Plug Controller, which uses signals on an external I^{2}C I/O Expander, for Hot Plug signaling.* *By default, all Transparent downstream Ports use a* **Serial** *Hot Plug Controller, unless the Port's* ***Power Management Hot Plug User Configuration*** *register Serial Hot Plug Override Parallel Disable bit (offset F70h[19]) is Set. Ports that use a Serial Hot Plug Controller have the register's Port Is Serial Hot Plug Port bit (offset F70h[15]) Set.*					
0	***Reserved***	Upstream	RsvdP	No	0
	Attention Button Present Set if the Port is Parallel and/or Serial Hot Plug-capable. 0 = Attention Button is not implemented 1 = Attention Button is implemented on the slot chassis of the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port	Downstream	RO	Yes	1
1	***Reserved***	Upstream	RsvdP	No	0
	Power Controller Present Enables or disables the Hot Plug Controller on the PEX 8649 Hot Plug-capable Transparent downstream Ports. Set if the Port is Parallel and/or Serial Hot Plug-capable. 0 = Power Controller is not implemented. The Hot Plug Controller is disabled for that slot and a power-up sequence is not executed. The slot remains in the disabled state. 1 = Power Controller is implemented for the slot of the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port. The Hot Plug Controller powers up the slot when the Manually operated Retention Latch (MRL) is closed and the **Slot Control** register *Power Controller Control* bit (Downstream Ports, offset 80h[10]) is Cleared. Otherwise, if bit 2 (*MRL Sensor Present*) is disabled (Cleared), the MRL's position has no effect on powering up the slot.	Downstream	RO	Yes	1

Register 13-30. 7Ch Slot Capability (Downstream Ports; Upstream Port(s) Always Read(s) 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
2	***Reserved***	Upstream	RsvdP	No	0
	MRL Sensor Present Set if the Port is Parallel and/or Serial Hot Plug-capable. 0 = MRL Sensor is not implemented. MRL position is "Don't Care" for that slot. 1 = MRL Sensor is implemented on the slot chassis of the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port. The PEX 8649 senses whether the MRL is open or closed for a slot. MRL should be Low for power-on for that slot.	Downstream	RO	Yes	1
3	***Reserved***	Upstream	RsvdP	No	0
	Attention Indicator Present Set if the Port is Parallel and/or Serial Hot Plug-capable. 0 = Attention Indicator is not implemented. HP_ATNLED_*x*# output is not functional on the slot. 1 = Attention Indicator is implemented on the slot chassis of the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port. Controls whether the HP_ATNLED_*x*# output for the slot drives out Active-Low.	Downstream	RO	Yes	1

Register 13-30. 7Ch Slot Capability (Downstream Ports; Upstream Port(s) Always Read(s) 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
4	***Reserved***	Upstream	RsvdP	No	0
	Power Indicator Present Set if the Port is Parallel and/or Serial Hot Plug-capable. 0 = Power Indicator is not implemented. HP_PWRLED_*x*# output is not functional on the slot. 1 = Power Indicator is implemented on the slot chassis of the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port. Controls whether the HP_PWRLED_*x*# output for the slot drives out Active-Low.	Downstream	RO	Yes	1
5	***Reserved***	Upstream	RsvdP	No	0
	Hot Plug Surprise 0 = No device in the corresponding PEX 8649 downstream Port slot is removed from the system without prior notification 1 = Device in the corresponding PEX 8649 downstream Port slot can be removed from the system without prior notification	Downstream	RO	Yes	0
6	***Reserved***	Upstream	RsvdP	No	0
	Hot Plug Capable Set if the Port is Parallel and/or Serial Hot Plug-capable. 0 = Corresponding PEX 8649 downstream Port slot is not capable of supporting Hot Plug operations 1 = Corresponding PEX 8649 downstream Port slot is capable of supporting Hot Plug operations	Downstream	RO	Yes	1
14:7	***Reserved***	Upstream	RsvdP	No	00h
	Slot Power Limit Value The maximum power supplied by the corresponding PEX 8649 downstream slot is determined by multiplying the value in this field (expressed in decimal; 25d = 19h) by the field [16:15] (*Slot Power Limit Scale*) value. This field must be implemented if the **PCI Express Capability** register *Slot Implemented* bit (offset 68h[24]) is Set (default). Serial EEPROM and/or I^{2}C Writes to this register or a DLL Up event causes the downstream Port to send the Set_Slot_Power_Limit Message to the device connected to it, so as to convey the Limit value to the downstream device's upstream Port **Device Capability** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields.	Downstream	RO	Yes	19h

Register 13-30. 7Ch Slot Capability (Downstream Ports; Upstream Port(s) Always Read(s) 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
16:15	***Reserved***	Upstream	RsvdP	No	00b
	Slot Power Limit Scale The maximum power supplied by the corresponding PEX 8649 downstream slot is determined by multiplying the value in this field by the field [14:7] (*Slot Power Limit Value*) value. This field must be implemented if the **PCI Express Capability** register *Slot Implemented* bit (offset 68h[24]) is Set (default). Serial EEPROM and/or I^{2}C Writes to this register or a DLL Up event causes the downstream Port to send the Set_Slot_Power_Limit Message to the device connected to it, so as to convey the Limit value to the downstream device's upstream Port **Device Capability** register *Captured Slot Power Limit Value* and *Captured Slot Power Limit Scale* fields. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	Downstream	RO	Yes	00b
17	***Reserved***	Upstream; Downstream non-Serial Hot Plug-enabled	RsvdP	No	0
	Electromechanical Interlock Present This bit is valid for Serial Hot Plug Ports that have an I/O Expander; this bit is ***not*** valid for Parallel Hot Plug Ports. 0 = Electromechanical Interlock is not implemented on the chassis for this slot 1 = Electromechanical Interlock is implemented on the chassis for this slot	Downstream Serial Hot Plug-enabled	RO	Yes	1
18	**No Command Completed Support** ***Reserved***		RsvdP	No	0

Register 13-30. 7Ch Slot Capability (Downstream Ports; Upstream Port(s) Always Read(s) 0) *(Cont.)*

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Ports</th><th>Type</th><th>Serial EEPROM and I^{2}C</th><th>Default</th></tr>
<tr><td rowspan="2">31:19</td><td><b><i>Reserved</i></b></td><td>Upstream</td><td>RsvdP</td><td>No</td><td>0-0h</td></tr>
<tr><td><b>Physical Slot Number</b>
Indicates the physical Slot Number attached to this Port.
If the <b>PCI Express Capability</b> register <i>Slot Implemented</i> bit (offset 68h[24]) is Set (default), this field must be hardware-initialized to a value that assigns a Slot Number that is unique within the chassis, regardless of the form factor associated with the slot. Must be initialized to 0h for Ports connected to devices that are integrated on the system board. Bit usage depends upon whether the Port is Serial Hot Plug-capable.
<table>
<tr><th colspan="2">Serial Hot Plug-Capable Downstream Ports</th></tr>
<tr><th>Bit(s)</th><th>Description/Function</th></tr>
<tr><td>23:19</td><td>Port Numbers 0 through 3 and 16 through 23</td></tr>
<tr><td>31:24</td><td>Loaded from I/O Expander</td></tr>
</table>
<table>
<tr><th colspan="2">Non-Serial Hot Plug-Capable Downstream Ports</th></tr>
<tr><th>Bit(s)</th><th>Description/Function</th></tr>
<tr><td>23:19</td><td>Port Numbers 0 through 3 and 16 through 23</td></tr>
<tr><td>26:24</td><td>Set by Value of I2C_ADDR[2:0] (same as the lower three bits of the <b>I^{2}C Configuration</b> register <i>Slave Address</i> field (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 294h[2:0]))</td></tr>
<tr><td>31:27</td><td><b><i>Reserved</i></b></td></tr>
</table></td><td>Downstream</td><td>RO</td><td>Yes</td><td>0-0h</td></tr>
</table>

Register 13-31. 80h Slot Status and Control (Downstream Ports; Upstream Port(s) Always Read(s) 0)

Bit(s)	Description		Ports	Type	Serial EEPROM and I^{2}C	Default
Slot Control						
Note: *To change the values of the MRL Sensor Changed Enable (bit 2), Power Fault Detector Enable (bit 1), and/or Attention Button Pressed Enable (bit 0) bits, the corresponding bit(s) in the **Slot Capability** register (Downstream Ports, offset 7Ch[2:0], respectively) must be Set first.*						
0	***Reserved***		Upstream	RsvdP	No	0
	Attention Button Pressed Enable 0 = Function is disabled 1 = Enables software notification with an interrupt if the Port is in the D0 Device PM state (**PCI Power Management Status and Control** register *Power State* field, offset 44h[1:0], are both Cleared), or with a PME Message if the Port is in the D3hot Device PM state (offset 44h[1:0], are both programmed to 11b), for an Attention Button Pressed event on the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port	Downstream Ports, Offset 7Ch[0]=0	Downstream	RO	No	0
		Downstream Ports, Offset 7Ch[0]=1	Downstream	RW	Yes	0
1	***Reserved***		Upstream	RsvdP	No	0
	Power Fault Detector Enable 0 = Function is disabled 1 = Enables software notification with an interrupt if the Port is in the D0 Device PM state (**PCI Power Management Status and Control** register *Power State* field, offset 44h[1:0], are both Cleared), or with a PME Message if the Port is in the D3hot Device PM state (offset 44h[1:0], are both programmed to 11b), for a Power Fault Detected event on the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port	Downstream Ports, Offset 7Ch[1]=0	Downstream	RO	No	0
		Downstream Ports, Offset 7Ch[1]=1	Downstream	RW	Yes	0

Register 13-31. 80h Slot Status and Control (Downstream Ports; Upstream Port(s) Always Read(s) 0) *(Cont.)*

Bit(s)	Description		Ports	Type	Serial EEPROM and I^{2}C	Default
2	***Reserved***		Upstream	RsvdP	No	0
	MRL Sensor Changed Enable 0 = Function is disabled 1 = Enables software notification with an interrupt if the Port is in the D0 Device PM state (**PCI Power Management Status and Control** register *Power State* field, offset 44h[1:0], are both Cleared), or with a PME Message if the Port is in the D3hot Device PM state (offset 44h[1:0], are both programmed to 11b), for an MRL Sensor Changed event on the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port	Downstream Ports, Offset 7Ch[2]=0	Downstream	RO	No	0
		Downstream Ports, Offset 7Ch[2]=1	Downstream	RW	Yes	0
3	***Not valid***		Upstream	RsvdP	No	0
	Presence Detect Changed Enable A Presence Detect Changed event is triggered by either the SerDes Receiver Detect on the corresponding PEX 8649 downstream Port (**Physical Layer Receiver Detect Status** register *Receiver Detected on Lane x* bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 200h[31:16])), or by HP_PRSNT_*x*# input or external I/O Expander PRSNT# input on the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port. 0 = Function is disabled 1 = Enables software notification with an interrupt if the Port is in the D0 Device PM state (**PCI Power Management Status and Control** register *Power State* field, offset 44h[1:0], are both Cleared), or with a PME Message if the Port is in the D3hot Device PM state (offset 44h[1:0], are both programmed to 11b), for a Presence Detect Changed event on the corresponding PEX 8649 downstream Port		Downstream	RW	Yes	0

Register 13-31. 80h Slot Status and Control (Downstream Ports; Upstream Port(s) Always Read(s) 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
4	***Reserved***	Upstream	RsvdP	No	0
	Command Completed Interrupt Enable 0 = Function is disabled 1 = Enables software notification with an interrupt when a command is completed by the Hot Plug Controller on the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port	Downstream	RW	Yes	0
5	***Reserved***	Upstream	RsvdP	No	0
	Hot Plug Interrupt Enable 0 = Function is disabled 1 = Enables an interrupt on enabled Hot Plug/Link State events for the corresponding PEX 8649 downstream Port	Downstream	RW	Yes	0
7:6	***Reserved***	Upstream	RsvdP	No	00b
	Attention Indicator Control Controls the Attention Indicator on the corresponding PEX 8649 downstream Port slot. Reads return the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port Attention Indicator's current state. Writing a non-zero value triggers a Command Completed event (even if the value written is the same as the existing value). Writing 00b preserves the current value and does not trigger a Command Completed event. 00b = ***Reserved*** – Writes are ignored 01b = Turns On indicator to constant On state 10b = Causes indicator to blink 11b = Turns Off indicator	Downstream	RW	Yes	11b

Register 13-31. 80h Slot Status and Control (Downstream Ports; Upstream Port(s) Always Read(s) 0) ***(Cont.)***

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
9:8	***Reserved***	Upstream	RsvdP	No	00b
	Power Indicator Control Controls the Power Indicator on the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port slot. Reads return the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port Power Indicator's current state. Writing a non-zero value triggers a Command Completed event (even if the value written is the same as the existing value). Writing 00b preserves the current value and does not trigger a Command Completed event. 00b = ***Reserved*** – Writes are ignored 01b = Turns On indicator to constant On state 10b = Causes indicator to blink 11b = Turns Off indicator	Downstream	RW	Yes	11b (MRL open) 01b (MRL closed)
10	***Reserved***	Upstream	RsvdP	No	0
	Power Controller Control Controls the Power Controller on the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port slot. 0 = Turns On the Power Controller; requires some delay to be effective 1 = Turns Off the Power Controller	Downstream	RW	Yes	1 (MRL open) 0 (MRL closed)
11	***Reserved***	Upstream; Downstream non-Serial Hot Plug-enabled	RsvdP	No	0
	Electromechanical Interlock Control This bit is valid for Serial Hot Plug Ports that have an I/O Expander; this bit is ***not*** valid for Parallel Hot Plug Ports. If an Electromechanical Interlock is implemented, writing 1 to this bit causes the state of the interlock to toggle. A Write of 0 to this bit has no effect. A Read of this bit always returns 0.	Downstream Serial Hot Plug-enabled	RW	Yes	0
12	***Not valid***	Upstream	RsvdP	No	0
	Data Link Layer State Changed Enable Enables software notification with an interrupt if the Port is in the D0 Device PM state (**PCI Power Management Status and Control** register *Power State* field, offset 44h[1:0], are both Cleared), or with a PME Message if the Port is in the D3hot Device PM state (offset 44h[1:0], are both programmed to 11b), when the **Link Status** register *Data Link Layer Link Active* bit (offset 78h[29]) is changed.	Downstream	RW	Yes	0
15:13	***Reserved***		RsvdP	No	000b

Register 13-31. 80h Slot Status and Control (Downstream Ports; Upstream Port(s) Always Read(s) 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
	Slot Status				
16	***Reserved***	Upstream	RsvdP	No	0
	Attention Button Pressed 1 = Attention Button of the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port slot was pressed	Downstream	RW1C	Yes	0
17	***Reserved***	Upstream	RsvdP	No	0
	Power Fault Detected 1 = Power Controller of the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port slot detected a Power Fault at the slot	Downstream	RW1C	Yes	0
18	***Reserved***	Upstream	RsvdP	No	0
	MRL Sensor Changed 1 = MRL Sensor state change was detected on the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port slot	Downstream	RW1C	Yes	0
19	***Reserved***	Upstream	RsvdP	No	0
	Presence Detect Changed A Presence Detect Changed event is triggered by either the SerDes Receiver Detect on the corresponding PEX 8649 downstream Port (**Physical Layer Receiver Detect Status** register *Receiver Detected on Lane x* bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 200h[31:16])), or by HP_PRSNT_*x*# or PRSNT# input (from external I^{2}C I/O Expander) on the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port. Write 1 to Clear. 1 = Value reported in bit 22 (*Presence Detect State*) changed	Downstream	RW1C	Yes	0

Register 13-31. 80h Slot Status and Control (Downstream Ports; Upstream Port(s) Always Read(s) 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
20	***Reserved***	Upstream	RsvdP	No	0
	Command Completed 1 = Hot Plug Controller on the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port slot completed an issued command to: • *Attention Indicator Control* (field [7:6]) • *Power Indicator Control* (field [9:8]) • *Power Controller Control* (bit 10) • *Electromechanical Interlock Control* (bit 11) (Serial Hot Plug-enabled Ports only)	Downstream	RW1C	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	MRL Sensor State Reveals the corresponding PEX 8649 Hot Plug-capable Transparent downstream Port MRL Sensor's current state. 0 = MRL Sensor is closed 1 = MRL Sensor is open	Downstream	RO	No	0

Register 13-31. 80h Slot Status and Control (Downstream Ports; Upstream Port(s) Always Read(s) 0) *(Cont.)*

Bit(s)	Description		Ports	Type	Serial EEPROM and I^2C	Default
22	***Not valid***		Upstream	RsvdP	No	0
	Presence Detect State For downstream Ports that implement slots, indicates the presence of an adapter in the slot, reflected by the logical OR of the corresponding downstream Port's SerDes Receiver Detect, and, if present, the Port's HP_PRSNT_*x*# input (de-bounced) or the PRSNT# input on the external I/O Expander for the Serial Hot Plug-enabled Port. Hardwired to 1 when the **PCI Express Capability** register *Slot Implemented* bit (offset 68h[24]) value is 0. 0 = Slot is empty, or device is not present 1 = Slot is occupied, or device is present	Offset 68h[24]=1	Downstream	RO	No	0
		Offset 68h[24]=0	Downstream	RO	No	1
23	***Reserved***		Upstream; Downstream non-Serial Hot Plug-enabled	RsvdZ	No	0
	Electromechanical Interlock Status This bit is valid for Serial Hot Plug Ports that have an I/O Expander; this bit is ***not*** valid for Parallel Hot Plug Ports. When an Electromechanical Interlock is implemented, indicates the Electromechanical Interlock's current status. 0 = Electromechanical Interlock is disengaged 1 = Electromechanical Interlock is engaged		Downstream Serial Hot Plug-enabled	RW1C	Yes	0
24	***Not valid***		Upstream	RsvdP	No	0
	Data Link Layer State Changed In response to a Data Link Layer State Changed event, software must read the **Link Status** register *Data Link Layer Link Active* bit (offset 78h[29]), to determine whether the Link is active before initiating Configuration Requests to the device. 1 = Value reported in the **Link Status** register *Data Link Layer Link Active* bit changed		Downstream	RW1C	Yes	0
31:25	***Reserved***			RsvdZ	No	0-0h

Register 13-32. 8Ch Device Capability 2 (Downstream Ports; Upstream Port(s) Always Read(s) 0)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
4:0	***Reserved***		RsvdP	No	0-0h
5	***Reserved***	Upstream	RsvdP	No	0
	ARI Forwarding Supported 0 = Alternative Routing-ID Interpretation (ARI) forwarding is not supported 1 = ARI forwarding is supported	Downstream	RO	Yes	1
31:6	***Reserved***		RsvdP	No	0-0h

Register 13-33. 90h Device Status and Control 2 (Downstream Ports; Upstream Port(s) Always Read(s) 0)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
Device Control 2					
4:0	***Reserved***		RsvdP	No	0-0h
5	***Reserved***	Upstream	RsvdP	No	0
	ARI Forwarding Enable 0 = Disabled 1 = Enabled; Downstream Port disables its traditional Device Number field from being forced to 0 when turning a Type 1 Configuration Request into a Type 0 Configuration Request, permitting access to extended functions in an ARI device immediately below the Port	Downstream	RW	Yes	0
15:6	***Reserved***		RsvdP	No	0-0h
Device Status 2					
31:16	***Reserved***		RsvdP	No	0000h

Register 13-34. 98h Link Status and Control 2 (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
Link Control 2					
3:0	**Target Link Speed** 0001b = 2.5 GT/s Link speed is supported 0010b = 5.0 GT/s Link speed is supported All other encodings are ***reserved***.		RWS	Yes	0010b
4	**Enter Compliance**		RWS	Yes	0
5	**Hardware Autonomous Speed Disable** ***Reserved*** Initial transition to the highest supported common Link speed is not blocked by this bit.		RsvdP	No	0
6	***Not valid***	Upstream	RsvdP	Yes	0
	Selectable De-Emphasis Selects the standard de-emphasis level when the Link is operating at 5.0 GT/s. When the Link is operating at 2.5 GT/s, the Setting of this bit has no effect (de-emphasis at 2.5 GT/s is -3.5 dB). 0 = -6 dB (Link is operating at 5.0 GT/s) 1 = -3.5 dB (Link is operating at 2.5 GT/s)	Downstream	HwInit	Yes	0 (5.0 GT/s) 1 (2.5 GT/s)
9:7	**Transmit Margin** Intended for debug and compliance testing only.		RWS	Yes	000b
10	**Enter Modified Compliance** Intended for debug and compliance testing only.		RWS	Yes	0
11	**Compliance SOS** 1 = LTSSM must periodically send SKIP Ordered-Sets between sequences when sending the Compliance Pattern or Modified Compliance Pattern		RWS	Yes	0
12	**Compliance De-Emphasis** Sets the de-emphasis level in the *Polling.Compliance* state, if the entry occurred due to bit 4 (*Enter Compliance*) being Set.		RWS	Yes	0
15:13	***Reserved***		RsvdP	No	000b
Link Status 2					
16	**Current De-Emphasis Level** Reflects the de-emphasis level. 0 = -6 dB (Link is operating at 5.0 GT/s) 1 = -3.5 dB		RO	Yes	0 (5.0 GT/s) 1 (2.5 GT/s)
31:17	***Reserved***		RsvdP	No	0-0h

13.11 Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – FCh)

This section details the Subsystem ID and Subsystem Vendor ID Capability registers. Table 13-12 defines the register map.

Table 13-12. Subsystem ID and Subsystem Vendor ID Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved	Next Capability Pointer (00h)	SSID/SSVID Capability ID (0Dh)	A4h
Subsystem ID	Subsystem Vendor ID		A8h
Reserved			ACh – FCh

Register 13-35. A4h Subsystem Capability (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**SSID/SSVID Capability ID** SSID/SSVID registers for the PCI-to-PCI bridge. Program to 0Dh, as required by the *PCI-to-PCI Bridge r1.2*.	RO	Yes	0Dh
15:8	**Next Capability Pointer** 00h = This capability is the last capability in the PEX 8649 Port's Capabilities list The PEX 8649 Extended Capabilities list starts at offset 100h.	RO	Yes	00h
31:16	***Reserved***	RsvdP	No	0000h

Register 13-36. A8h Subsystem ID and Subsystem Vendor ID (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**Subsystem Vendor ID** The Vendor ID (offset 00h[15:0]) identifies the manufacturer of the PEX 8649, and the Subsystem Vendor ID optionally identifies the board or system vendor. As with the Vendor ID value, the Subsystem Vendor ID value must be a valid PCI-SIG-assigned Vendor ID. The value of this field is usually identical for all PEX 8649 Ports.	RO	Yes	10B5h
31:16	**Subsystem ID** The Device ID (offset 00h[31:16]) identifies the PEX 8649, and optionally the Subsystem ID in combination with the Subsystem Vendor ID, uniquely identifies the board or system. The value of this field is usually identical for all PEX 8649 Ports, and is chosen or assigned only by the "owner" of the valid Vendor ID value used for the Subsystem Vendor ID. If the board or system vendor is not a PCI-SIG member, PLX can assign, free of charge, a unique Subsystem ID value, in which case the Subsystem Vendor ID remains the PLX default value, 10B5h.	RO	Yes	8649h

13.12 Device Serial Number Extended Capability Registers (Offsets 100h – 134h)

This section details the Device Serial Number Extended Capability registers. Table 13-13 defines the register map.

Table 13-13. Device Serial Number Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (FB4h)	Capability Version (1h)	PCI Express Extended Capability ID (0003h)	100h
Serial Number (Lower DW)			104h
Serial Number (Upper DW)			108h
Reserved		10Ch –	134h

Register 13-37. 100h Device Serial Number Extended Capability Header (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
15:0	**PCI Express Extended Capability ID** Program to 0003h, as required by the *PCI Express Base r2.0*.	RO	Yes	0003h
19:16	**Capability Version** Program to 1h, as required by the *PCI Express Base r2.0*.	RO	Yes	1h
31:20	**Next Capability Offset** Program to FB4h, which addresses the **Advanced Error Reporting Extended Capability** structure.	RO	Yes	FB4h

Register 13-38. 104h Serial Number (Lower DW) (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**PCI Express Device Serial Number (1st DW)** Lower half of a 64-bit register. Value programmed by Serial EEPROM register initialization. Per the *PCI Express Base r2.0*, all switch Ports must contain the same value; therefore, one physical register is shared by all PEX 8649 Ports. The Serial Number registers contain the IEEE-defined 64-bit Extended Unique Identifier (EUI-64^{TM}). The lower 24 bits are the Company ID value assigned by the IEEE registration authority, and the upper 40 bits are the Extension ID assigned by the identified Company.	RO	Yes	B5DF_0E00h

Register 13-39. 108h Serial Number (Upper DW) (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**PCI Express Device Serial Number (2nd DW)** Upper half of a 64-bit register. Value programmed by Serial EEPROM register initialization. Per the *PCI Express Base r2.0*, all switch Ports must contain the same value; therefore, one physical register is shared by all PEX 8649 Ports. The Serial Number registers contain the IEEE-defined 64-bit Extended Unique Identifier (EUI-64™). The lower 24 bits are the Company ID value assigned by the IEEE registration authority, and the upper 40 bits are the Extension ID assigned by the identified Company.	RO	Yes	AA_8600_10h

13.13 Power Budget Extended Capability Registers (Offsets 138h – 144h)

This section details the Power Budget Extended Capability registers. These registers work differently than the others, especially with respect to serial EEPROM Reads and Writes. *For example*, when writing to Index 5 of the upstream Port(s) **Power Budget Data** register (Upstream Port(s), offset 140h), write 5 into the upstream Port(s) **Data Select** register *Data Select* field (Upstream Port(s), offset 13Ch[7:0]), then write the value into the upstream Port(s) **Power Budget Data** register itself. Table 13-14 defines the register map.

Table 13-14. Power Budget Extended Capability Register Map (Upstream Port(s))

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

31:20	19:16	15:8	7:0	
Next Capability Offset (148h)	Capability Version (1h)	PCI Express Extended Capability ID (0004h)		138h
Reserved			Data Select	13Ch
Power Budget Data				140h
Power Budget Capability				144h

Register 13-40. 138h Power Budget Extended Capability Header (Upstream Port(s))

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
15:0	**PCI Express Extended Capability ID** Program to 0004h, as required by the *PCI Express Base r2.0.*	Upstream	RO	Yes	0004h
	Reserved	Downstream	RsvdP	No	0000h
19:16	**Capability Version** Program to 1h, as required by the *PCI Express Base r2.0.*	Upstream	RO	Yes	1h
	Reserved	Downstream	RsvdP	No	0h
31:20	**Next Capability Offset** Program to 148h, which addresses the **Virtual Channel Extended Capability** structure.	Upstream	RO	Yes	148h
	Reserved	Downstream	RsvdP	No	000h

Register 13-41. 13Ch Data Select (Upstream Port(s))

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
7:0	**Data Select** Indexes the Power Budget data reported, by way of eight **Power Budget Data** registers, per Port, and selects the DWord of Power Budget data that appears in each **Power Budget Data** register. Index values start at 0, to select the first DWord of Power Budget data; subsequent DWords of Power Budget data are selected by increasing index values 1 to 7.	Upstream	RW	Yes	00h
	Reserved	Downstream	RsvdP	No	00h
31:8	***Reserved***		RsvdP	No	0000_00h

Register 13-42. 140h Power Budget Data (Upstream Port(s))

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
Note: *Eight registers, per upstream Port, can be programmed, through the serial EEPROM, I^2C, and/or SMBus. Each non-zero register value describes the power usage for a different operating condition. Each configuration is selected by writing to the* ***Data Select*** *register Data Select field (Upstream Port(s), offset 13Ch[7:0]).*					
7:0	**Base Power** Eight registers, per upstream Port. Specifies (in Watts) the base power value in the operating condition. This value must be multiplied by the field [9:8] (*Data Scale*) contents, to produce the actual power consumption value.	Upstream	RO	Yes	00h
	Reserved	Downstream	RsvdP	No	00h
9:8	**Data Scale** Specifies the scale to apply to the Base Power value. The device power consumption is determined by multiplying the field [7:0] (*Base Power*) contents with the value corresponding to the encoding returned by this field. 00b = 1.0x 01b = 0.1x 10b = 0.01x 11b = 0.001x	Upstream	RO	Yes	00b
	Reserved	Downstream	RsvdP	No	00b
12:10	**PM Sub-State** 000b = Power Management sub-state of the operating condition being described	Upstream	RO	Yes	000b
	Reserved	Downstream	RsvdP	No	000b

Register 13-42. 140h Power Budget Data (Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
14:13	**PM State** Power Management state of the operating condition being described. 00b = D0 Device PM state 11b = D3 Device PM state All other encodings are ***reserved***.	Upstream	RO	Yes	00b
	Reserved	Downstream	RsvdP	No	00b
17:15	**Type** Type of operating condition being described. 000b = PME Auxiliary 001b = Auxiliary 010b = Idle 011b = Sustained 111b = Maximum All other encodings are ***reserved***.	Upstream	RO	Yes	000b
	Reserved	Downstream	RsvdP	No	000b
20:18	**Power Rail** Power Rail of the operating condition being described. 000b = Power 12V 001b = Power 3.3V 010b = Power 1.8V 111b = Thermal All other encodings are ***reserved***.	Upstream	RO	Yes	000b
	Reserved	Downstream	RsvdP	No	000b
31:21	***Reserved***		RsvdP	No	0-0h

Register 13-43. 144h Power Budget Capability (Upstream Port(s))

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
0	**System Allocated** 1 = Power budget for the device is included within the system power budget	Upstream	HwInit	Yes	1
	Reserved	Downstream	RsvdP	No	0
31:1	***Reserved***		RsvdP	No	0-0h

13.14 Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)

This section details the Virtual Channel Extended Capability registers, which are duplicated for each Port. Table 13-15 defines the register map for one Port.

Table 13-15. Virtual Channel Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16		15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (E00h or 000h)	Capability Version (1h)	PCI Express Extended Capability ID (0002h)	148h
Port VC Capability 1			14Ch
Port VC Capability 2			150h
Port VC Status ***(Reserved)***		Port VC Control	154h
VC0 Resource Capability			158h
VC0 Resource Control			15Ch
VC0 Resource Status		***Reserved***	160h
Reserved			164h – 174h
WRR Port Arbitration Table Registers (Offsets 178h – 1BCh)			178h … 1BCh

Register 13-44. 148h Virtual Channel Extended Capability Header (All Ports)

Bit(s)	Description		Type	Serial EEPROM and I^{2}C	Default
15:0	**PCI Express Extended Capability ID** Program to 0002h, as required by the *PCI Express Base r2.0*.		RO	No	0002h
19:16	**Capability Version** Program to 1h, as required by the *PCI Express Base r2.0*.		RO	No	1h
31:20	**Next Capability Offset** Next extended capability is the **Multicast Extended Capability** structure, offset E00h.	Upstream	RO	No	E00h
	000h = This extended capability is the last capability in the PEX 8649 Extended Capabilities list	Downstream	RO	No	000h

Register 13-45. 14Ch Port VC Capability 1 (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
0	**Extended VC Counter** 0 = PEX 8649 Port supports only one Virtual Channel, VC0 1 = ***Reserved***		RO	No	0
3:1	***Reserved***		RsvdP	No	000b
4	**Low-Priority Extended VC Counter** For Strict Priority arbitration, indicates the number of extended Virtual Channels (VCs) (those in addition to VC0) that belong to the Low-Priority VC group for this PEX 8649 Port. 0 = For this PEX 8649 Port, only VC0 belongs to the Low-Priority VC group 1 = ***Reserved***, because the PEX 8649 supports only one VC		RO	No	0
7:5	***Reserved***		RsvdP	No	000b
9:8	**Reference Clock** ***Reserved***		RsvdP	No	00b
11:10	**Port Arbitration Table Entry Size** 00b = Port Arbitration Table entry size is 1 bit 11b = Port Arbitration Table entry size is 8 bits All other encodings are ***reserved***.	Upstream	RO	Yes	11b
	Reserved	Downstream	RsvdP	No	00b
31:12	***Reserved***		RsvdP	No	0000_0h

Register 13-46. 150h Port VC Capability 2 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
0	**VC Arbitration Capability** 0 = Indicates that the Round-Robin (Hardware-Fixed) Arbitration scheme is not supported 1 = ***Reserved***, because the PEX 8649 supports only one VC (**Port VC Capability 2** register *Low-Priority Extended VC Counter* bit, offset 14Ch[4], is Cleared)	RO	No	0
31:1	***Reserved***	RsvdP	No	0-0h

Register 13-47. 154h Port VC Status and Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
	Port VC Control			
0	**Load VC Arbitration Table** ***Not supported*** The PEX 8649 supports only one Virtual Channel, VC0; therefore, a VC Arbitration Table is not present (**Port VC Capability 2** register *Port Arbitration Table Offset* field (offset 150h[31:24]) is Cleared). Reads always return 0.	RsvdP	No	0
3:1	**VC Arbitration Select** Selects the VC arbitration type for the corresponding PEX 8649 Port, as per the supported arbitration type indicated by the **Port VC Capability 2** register *VC Arbitration Capability* bit (offset 150h[0]) value. 000b = Bit 0; Round-Robin (Hardware-Fixed) arbitration scheme All other encodings are ***reserved***.	RW	Yes	000b
15:4	***Reserved***	RsvdP	No	000h
	Port VC Status			
16	**VC Arbitration Table Status** ***Reserved***	RsvdP	No	0
31:17	***Reserved***	RsvdP	No	0-0h

Register 13-48. 158h VC0 Resource Capability (All Ports)

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
2:0	**Port Arbitration Capability** Bit 0 = 1 – Non-configurable Round-Robin (Hardware-Fixed) arbitration Bit 1 = 1 – Weighted Round-Robin (WRR) arbitration with 32 Phases Bit 2 = 1 – WRR arbitration with 64 Phases	Port Arbitration Table is present for this Port	RO	No	100b
		Port Arbitration Table is not present for this Port	RO	No	001b
13:3	***Reserved***		RsvdP	No	0-0h
14	**Advanced Packet Switching**		RsvdP	No	0
15	**Reject Snoop Transactions** Not a PCI Express switch feature; therefore, this bit is Cleared.		RsvdP	No	0
22:16	**Maximum Time Slots** ***Reserved***		RsvdP	No	000_0000b
23	***Reserved***		RsvdP	No	0
31:24	**Port Arbitration Table Offset** Offset of the Port Arbitration Table, as the number of DQWords from the Base address of the **Virtual Channel Extended Capability** structure. (Refer to Section 13.14.1 for further details.) 00h = Port Arbitration Table is not present 03h = Port Arbitration Table is located at register offset 178h	Port Arbitration Table is present for this Port	RO	No	03h
	Reserved	Port Arbitration Table is not present for this Port	RO	No	00h

Register 13-49. 15Ch VC0 Resource Control (All Ports)

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
0	**TC/VC Map** Defines Traffic Classes [7:0], respectively, and indicates which TCs are mapped to VC0. Traffic Class 0 (TC0) must be mapped to VC0. By default, Traffic Classes [7:1] are mapped to VC0.		RO	No	1
7:1			RW	Yes	7Fh
15:8	***Reserved***		RsvdP	No	00h
16	**Load Port Arbitration Table** Software writes this bit, to load the updated WRR Port Arbitration Table value to the internal logic. Software Read always returns 0.	Port Arbitration Table is present for this Port	RW	Yes	0
	Reserved	Port Arbitration Table is not present for this Port	RsvdP	No	0
19:17	**Port Arbitration Select** Selects the Port Arbitration type for the corresponding PEX 8649 Port. Indicates the bit number in the **VC0 Resource Capability** register *Port Arbitration Capability* field (offset 158h[2:0]) that corresponds to the arbitration type. Allowed values: • 000b if the Port Arbitration Table is not present • 000b or 010b if the Port Arbitration Table is present 000b = Fair Bandwidth (Hardware-Fixed Arbitration) 010b = Weighted Round-Robin with 64 Phases ***Note:*** *If software programs other values, hardware ignores the value.*	Port Arbitration Table is present for this Port	RW	Yes	010b
		Port Arbitration Table is not present for this Port	RW	Yes	000b
23:20	***Reserved***		RsvdP	No	0h
24	**VC ID** Defines the corresponding PEX 8649 Port's VC0 ID code. 0 = VC0 (default; VC0 is the only/default VC) 1 = ***Reserved***		RO	No	0
30:25	***Reserved***		RsvdP	No	0-0h
31	**VC Enable** 0 = Not allowed 1 = Enables the corresponding PEX 8649 Port's VC0		RO	No	1

Register 13-50. 160h VC0 Resource Status (All Ports)

<table>
<tr><th>Bit(s)</th><th colspan="2">Description</th><th>Type</th><th>Serial EEPROM and I^{2}C</th><th>Default</th></tr>
<tr><td>15:0</td><td colspan="2"><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>0000h</td></tr>
<tr><td rowspan="2">16</td><td><b>Port Arbitration Table Status</b>
0 = Hardware has finished loading values stored in the Port Arbitration Table, after software Sets the <b>VC0 Resource Control</b> register <i>Load Port Arbitration Table</i> bit (offset 15Ch[16]), or if the Port Arbitration Table is not implemented, then this bit is <b><i>reserved</i></b>
1 = Port Arbitration Table entry was written to by software</td><td>Port Arbitration Table is present for this Port</td><td>RO</td><td>No</td><td>0</td></tr>
<tr><td><b><i>Reserved</i></b></td><td>Port Arbitration Table is not present for this Port</td><td>RsvdP</td><td>No</td><td>0</td></tr>
<tr><td>17</td><td colspan="2"><b>VC0 Negotiation Pending</b>
0 = VC0 negotiation is complete
1 = VC0 initialization is not complete for the corresponding PEX 8649 Port</td><td>RO</td><td>Yes</td><td>1</td></tr>
<tr><td>31:18</td><td colspan="2"><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>0-0h</td></tr>
</table>

13.14.1 WRR Port Arbitration Table Registers (Offsets 178h – 1BCh)

This section details the WRR Port Arbitration Table registers. Port Arbitration Table phases are used to determine Port weighting during “Weighted Round-Robin (WRR) with 64 Phases” Port arbitration.

Table 13-16 defines the register map. The numbers along the top of the register map table indicate the 8-bit fields of each 32-bit register. There are 64 phases, and any active Port Number can go into each Port *x* Phase *x* box. Table 13-17 describes which Ports contain one of up to five WRR Port Arbitration Tables.

***Note:** The Port Arbitration Table is used only when Weighted Round-Robin with 64-Phase Port Arbitration is selected, by way of the VC0 Resource Control register Port Arbitration Select field (offset 15Ch[19:17]=010b).*

Table 13-16. WRR Port Arbitration Table Register Map (Ports – Refer to Table 13-17)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Port *x*, Phase 3	Port *x*, Phase 2	Port *x*, Phase 1	Port *x*, Phase 0	178h
Port *x*, Phase 7	Port *x*, Phase 6	Port *x*, Phase 5	Port *x*, Phase 4	17Ch
Port *x*, Phase 11	Port *x*, Phase 10	Port *x*, Phase 9	Port *x*, Phase 8	180h
Port *x*, Phase 15	Port *x*, Phase 14	Port *x*, Phase 13	Port *x*, Phase 12	184h
Port *x*, Phase 19	Port *x*, Phase 18	Port *x*, Phase 17	Port *x*, Phase 16	188h
Port *x*, Phase 23	Port *x*, Phase 22	Port *x*, Phase 21	Port *x*, Phase 20	18Ch
Port *x*, Phase 27	Port *x*, Phase 26	Port *x*, Phase 25	Port *x*, Phase 24	190h
Port *x*, Phase 31	Port *x*, Phase 30	Port *x*, Phase 29	Port *x*, Phase 28	194h
Port *x*, Phase 35	Port *x*, Phase 34	Port *x*, Phase 33	Port *x*, Phase 32	198h
Port *x*, Phase 39	Port *x*, Phase 38	Port *x*, Phase 37	Port *x*, Phase 36	19Ch
Port *x*, Phase 43	Port *x*, Phase 42	Port *x*, Phase 41	Port *x*, Phase 40	1A0h
Port *x*, Phase 47	Port *x*, Phase 46	Port *x*, Phase 45	Port *x*, Phase 44	1A4h
Port *x*, Phase 51	Port *x*, Phase 50	Port *x*, Phase 49	Port *x*, Phase 48	1A8h
Port *x*, Phase 55	Port *x*, Phase 54	Port *x*, Phase 53	Port *x*, Phase 52	1ACh
Port *x*, Phase 59	Port *x*, Phase 58	Port *x*, Phase 57	Port *x*, Phase 56	1B0h
Port *x*, Phase 63	Port *x*, Phase 62	Port *x*, Phase 61	Port *x*, Phase 60	1B4h
Reserved				1B8h – 1BCh

Table 13-17. WRR Port Arbitration Table Locations

Ports	Arbitration Function
Port 0, Port 1, Port 3	These Ports share the 64-phase WRR Port arbitration, based upon the upstream Port(s): • Port 3, if Port 3 is an upstream Port, else • Port 1, if Port 1 is an upstream Port, else • NT Port Virtual Interface, if Port 0 is a Legacy NT Port, else • Port 0
Port 16, Port 17, Port 19	These Ports share the 64-phase WRR Port arbitration, based upon the upstream Port(s): • Port 19, if Port 19 is an upstream Port, else • Port 17, if Port 17 is an upstream Port, else • NT Port Virtual Interface, if Port 16 is a Legacy NT Port, else • Port 16
Port 20, Port 21, Port 23	These Ports share the 64-phase WRR Port arbitration, based upon the upstream Port(s): • Port 23, if Port 23 is an upstream Port, else • Port 21, if Port 21 is an upstream Port, else • NT Port Virtual Interface, if Port 20 is a Legacy NT Port, else • Port 20
Port 2	Port 2's 64-phase WRR Port arbitration is based upon the upstream Port(s): • NT Port Virtual Interface, if Port 2 is a Legacy NT Port, else • Port 2
Port 18, Port 22	These Ports share the 64-phase WRR Port arbitration, based upon the upstream Port(s): • Port 22, if Port 22 is an upstream Port, else • NT Port Virtual Interface, if Port 18 is a Legacy NT Port, else • Port 18

Register 13-51. 178h Port Arbitration Table Phases 0 to 3 (Ports – Refer to Table 13-17)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4:0	**Port Arbitration Table Phase 0**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	***Reserved***	RsvdP	No	000b
12:8	**Port Arbitration Table Phase 1**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	***Reserved***	RsvdP	No	000b
20:16	**Port Arbitration Table Phase 2**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	***Reserved***	RsvdP	No	000b
28:24	**Port Arbitration Table Phase 3**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	***Reserved***	RsvdP	No	000b

Register 13-52. 17Ch Port Arbitration Table Phases 4 to 7 (Ports – Refer to Table 13-17)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
4:0	**Port Arbitration Table Phase 4**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	***Reserved***	RsvdP	No	000b
12:8	**Port Arbitration Table Phase 5**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	***Reserved***	RsvdP	No	000b
20:16	**Port Arbitration Table Phase 6**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	***Reserved***	RsvdP	No	000b
28:24	**Port Arbitration Table Phase 7**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	***Reserved***	RsvdP	No	000b

Register 13-53. 180h Port Arbitration Table Phases 8 to 11 (Ports – Refer to Table 13-17)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
4:0	**Port Arbitration Table Phase 8**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	***Reserved***	RsvdP	No	000b
12:8	**Port Arbitration Table Phase 9**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	***Reserved***	RsvdP	No	000b
20:16	**Port Arbitration Table Phase 10**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	***Reserved***	RsvdP	No	000b
28:24	**Port Arbitration Table Phase 11**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	***Reserved***	RsvdP	No	000b

Register 13-54. 184h Port Arbitration Table Phases 12 to 15 (Ports – Refer to Table 13-17)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4:0	**Port Arbitration Table Phase 12**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	***Reserved***	RsvdP	No	000b
12:8	**Port Arbitration Table Phase 13**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	***Reserved***	RsvdP	No	000b
20:16	**Port Arbitration Table Phase 14**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	***Reserved***	RsvdP	No	000b
28:24	**Port Arbitration Table Phase 15**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	***Reserved***	RsvdP	No	000b

Register 13-55. 188h Port Arbitration Table Phases 16 to 19 (Ports – Refer to Table 13-17)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4:0	**Port Arbitration Table Phase 16**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	***Reserved***	RsvdP	No	000b
12:8	**Port Arbitration Table Phase 17**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	***Reserved***	RsvdP	No	000b
20:16	**Port Arbitration Table Phase 18**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	***Reserved***	RsvdP	No	000b
28:24	**Port Arbitration Table Phase 19**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	***Reserved***	RsvdP	No	000b

Register 13-56. 18Ch Port Arbitration Table Phases 20 to 23 (Ports – Refer to Table 13-17)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
4:0	**Port Arbitration Table Phase 20**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	***Reserved***	RsvdP	No	000b
12:8	**Port Arbitration Table Phase 21**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	***Reserved***	RsvdP	No	000b
20:16	**Port Arbitration Table Phase 22**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	***Reserved***	RsvdP	No	000b
28:24	**Port Arbitration Table Phase 23**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	***Reserved***	RsvdP	No	000b

Register 13-57. 190h Port Arbitration Table Phases 24 to 27 (Ports – Refer to Table 13-17)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
4:0	**Port Arbitration Table Phase 24**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	***Reserved***	RsvdP	No	000b
12:8	**Port Arbitration Table Phase 25**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	***Reserved***	RsvdP	No	000b
20:16	**Port Arbitration Table Phase 26**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	***Reserved***	RsvdP	No	000b
28:24	**Port Arbitration Table Phase 27**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	***Reserved***	RsvdP	No	000b

Register 13-58. 194h Port Arbitration Table Phases 28 to 31 (Ports – Refer to Table 13-17)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
4:0	**Port Arbitration Table Phase 28**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	***Reserved***	RsvdP	No	000b
12:8	**Port Arbitration Table Phase 29**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	***Reserved***	RsvdP	No	000b
20:16	**Port Arbitration Table Phase 30**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	***Reserved***	RsvdP	No	000b
28:24	**Port Arbitration Table Phase 31**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	***Reserved***	RsvdP	No	000b

Register 13-59. 198h Port Arbitration Table Phases 32 to 35 (Ports – Refer to Table 13-17)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
4:0	**Port Arbitration Table Phase 32**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	***Reserved***	RsvdP	No	000b
12:8	**Port Arbitration Table Phase 33**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	***Reserved***	RsvdP	No	000b
20:16	**Port Arbitration Table Phase 34**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	***Reserved***	RsvdP	No	000b
28:24	**Port Arbitration Table Phase 35**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	***Reserved***	RsvdP	No	000b

Register 13-60. 19Ch Port Arbitration Table Phases 36 to 39 (Ports – Refer to Table 13-17)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
4:0	**Port Arbitration Table Phase 36**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	***Reserved***	RsvdP	No	000b
12:8	**Port Arbitration Table Phase 37**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	***Reserved***	RsvdP	No	000b
20:16	**Port Arbitration Table Phase 38**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	***Reserved***	RsvdP	No	000b
28:24	**Port Arbitration Table Phase 39**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	***Reserved***	RsvdP	No	000b

Register 13-61. 1A0h Port Arbitration Table Phases 40 to 43 (Ports – Refer to Table 13-17)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
4:0	**Port Arbitration Table Phase 40**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	***Reserved***	RsvdP	No	000b
12:8	**Port Arbitration Table Phase 41**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	***Reserved***	RsvdP	No	000b
20:16	**Port Arbitration Table Phase 42**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	***Reserved***	RsvdP	No	000b
28:24	**Port Arbitration Table Phase 43**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	***Reserved***	RsvdP	No	000b

Register 13-62. 1A4h Port Arbitration Table Phases 44 to 47 (Ports – Refer to Table 13-17)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
4:0	**Port Arbitration Table Phase 44**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	***Reserved***	RsvdP	No	000b
12:8	**Port Arbitration Table Phase 45**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	***Reserved***	RsvdP	No	000b
20:16	**Port Arbitration Table Phase 46**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	***Reserved***	RsvdP	No	000b
28:24	**Port Arbitration Table Phase 47**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	***Reserved***	RsvdP	No	000b

Register 13-63. 1A8h Port Arbitration Table Phases 48 to 51 (Ports – Refer to Table 13-17)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
4:0	**Port Arbitration Table Phase 48**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	***Reserved***	RsvdP	No	000b
12:8	**Port Arbitration Table Phase 49**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	***Reserved***	RsvdP	No	000b
20:16	**Port Arbitration Table Phase 50**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	***Reserved***	RsvdP	No	000b
28:24	**Port Arbitration Table Phase 51**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	***Reserved***	RsvdP	No	000b

Register 13-64. 1ACh Port Arbitration Table Phases 52 to 55 (Ports – Refer to Table 13-17)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
4:0	**Port Arbitration Table Phase 52**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	***Reserved***	RsvdP	No	000b
12:8	**Port Arbitration Table Phase 53**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	***Reserved***	RsvdP	No	000b
20:16	**Port Arbitration Table Phase 54**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	***Reserved***	RsvdP	No	000b
28:24	**Port Arbitration Table Phase 55**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	***Reserved***	RsvdP	No	000b

Register 13-65. 1B0h Port Arbitration Table Phases 56 to 59 (Ports – Refer to Table 13-17)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
4:0	**Port Arbitration Table Phase 56**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	***Reserved***	RsvdP	No	000b
12:8	**Port Arbitration Table Phase 57**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	***Reserved***	RsvdP	No	000b
20:16	**Port Arbitration Table Phase 58**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	***Reserved***	RsvdP	No	000b
28:24	**Port Arbitration Table Phase 59**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	***Reserved***	RsvdP	No	000b

Register 13-66. 1B4h Port Arbitration Table Phases 60 to 63 (Ports – Refer to Table 13-17)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
4:0	**Port Arbitration Table Phase 60**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
7:5	***Reserved***	RsvdP	No	000b
12:8	**Port Arbitration Table Phase 61**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
15:13	***Reserved***	RsvdP	No	000b
20:16	**Port Arbitration Table Phase 62**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
23:21	***Reserved***	RsvdP	No	000b
28:24	**Port Arbitration Table Phase 63**	RW	Yes	Value is based upon Negotiated Link Width and Current Link Speed (offset 78h[25:20 and 19:16], respectively)
31:29	***Reserved***	RsvdP	No	000b

13.15 Device-Specific Registers (Offsets 1C0h – DFCh)

This section details the Device-Specific registers located at offsets 1C0h through DFCh. Device-Specific registers are unique to the PEX 8649 and not referenced in the *PCI Express Base r2.0*. Table 13-18 defines the register map.

Other Device-Specific registers are detailed in:

- Section 13.17, "Device-Specific Registers – Virtual Switch (Offset F20h), Virtual Switch Mode Only"
- Section 13.19, "Device-Specific Registers (Offsets F30h – FB0h)"

***Note:** It is recommended that these registers not be changed from their default values.*

Table 13-18. Device-Specific Register Map (Offsets 1C0h – DFCh)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved	1C0h – 1CCh
Device-Specific Registers – Read Pacing (Offsets 1D0h – 1D8h)	1D0h … 1D8h
Device-Specific Registers – Captured Bus and Device Numbers (Offsets 1DCh – 1FCh)	1DCh … 1FCh
Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)	200h … 25Ch
Device-Specific Registers – Serial EEPROM (Offsets 260h – 26Ch)	260h … 26Ch
Reserved	270h – 28Ch
Device-Specific Registers – I^{2}C and SMBus Slave Interfaces (Offsets 290h – 2FCh)	290h … 2FCh
Device-Specific Registers – Port Configuration (Offsets 300h – 31Ch)	300h … 31Ch
Device-Specific Registers – Error Checking and Debug (Offsets 320h – 350h)	320h … 350h
Device-Specific Registers – Port Configuration (Offsets 354h – 3ACh)	354h … 3ACh

Table 13-18. Device-Specific Register Map (Offsets 1C0h – DFCh) *(Cont.)*

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16		15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved			3B0h – 4D8h
Factory Test Only			4DCh – 5FCh
Device-Specific Registers – General-Purpose Input/Output (Offsets 600h – 68Ch)			600h … 68Ch
Factory Test Only/Reserved			690h – 6FCh
Device-Specific Registers – Error Checking and Debug (Offsets 700h – 75Ch)			700h … 75Ch
Device-Specific Registers – Control (Offsets 760h – 774h), Base Mode Only ***Reserved*** (Virtual Switch Mode)			760h … 774h
Device-Specific Registers – Soft Error (Offsets 778h – 8FCh)			778h … 8FCh
Reserved (Base Mode) Device-Specific Registers – Virtual Switch (Offsets 900h – 9ECh), Virtual Switch Mode Only (Virtual Switch Mode)			900h … 9ECh
Device-Specific Registers – Ingress Credit Handler (Offsets 9F0h – A2Ch)			9F0h … A2Ch
Device-Specific Registers – Virtual Switch Debug and GPIO Status and Control (Offsets A30h – B6Ch)			A30h … B6Ch
Next Capability Offset 2 (000h)	1h	PCI Express Extended Capability ID 2 (000Bh)	B70h
Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets B70h – B7Ch)			… B7Ch
Device-Specific Registers – Physical Layer (Offsets B80h – BC8h)			B80h … BC8h
Factory Test Only			BCCh – BFCh
Reserved			C00h – DFCh

13.15.1 Device-Specific Registers – Read Pacing (Offsets 1D0h – 1D8h)

Caution: ***Source Queuing and Read Pacing should not be concurrently enabled.***
The two features are incompatible and doing so can result in Fatal errors.

This section details the Device-Specific Read Pacing registers. Table 13-19 defines the register map. The registers are located in one Port, per Station, as listed in Table 13-20.

Read Pacing is described, in detail, in Section 8.5, "Read Pacing."

Table 13-19. Device-Specific Read Pacing Register Map (Ports – Refer to Table 13-20)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Read Pacing Control	1D0h
Read Pacing Threshold 1	1D4h
Read Pacing Threshold 2	1D8h

Table 13-20. Read Pacing Port Locations (Single Port Per Station)

Station	Read Pacing Is Located in One Port, Based upon the Upstream Port
0	• Port 3, if Port 3 is an upstream Port, else • Port 1, if Port 1 is an upstream Port, else • NT Port Virtual Interface, if Port 0 is a Legacy NT Port, else • Port 0
4	• Port 19, if Port 19 is an upstream Port, else • Port 17, if Port 17 is an upstream Port, else • NT Port Virtual Interface, if Port 16 is a Legacy NT Port, else • Port 16
5	• Port 23, if Port 23 is an upstream Port, else • Port 21, if Port 21 is an upstream Port, else • NT Port Virtual Interface, if Port 20 is a Legacy NT Port, else • Port 20

Register 13-67. 1D0h Read Pacing Control (Ports – Refer to Table 13-20)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
Caution: ***Read Pacing and Source Queuing should not be concurrently enabled. The two features are incompatible and doing so can result in Fatal errors.*** ***Note:*** *Read Pacing must be enabled for Read Spreading to be enabled.*					
0	**Port *x* Read Pacing Disable** 0 = Read Pacing is enabled for this Port 1 = Read Pacing is disabled for this Port	0, 16, or 20	RWS	Yes	1
1		1, 17, or 21	RWS	Yes	1
2		2, 18, or 22	RWS	Yes	1
3		3, 19, or 23	RWS	Yes	1
15:4	***Reserved***		RsvdP	No	000h
16	**Port *x* Memory Read Spread Disable** 0 = Memory Read Spread is enabled for this Port 1 = Memory Read Spread is disabled for this Port	0, 16, or 20	RWS	Yes	0
17		1, 17, or 21	RWS	Yes	0
18		2, 18, or 22	RWS	Yes	0
19		3, 19, or 23	RWS	Yes	0
31:20	***Reserved***		RsvdP	No	000h

Register 13-68. 1D4h Read Pacing Threshold 1 (Ports – Refer to Table 13-20)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
12:0	**x16 Port Memory Read Outstanding Threshold** Specified in DWords. Default value of 800h Sets the threshold to 8 KB.	RWS	Yes	800h
15:13	***Reserved***	RsvdP	No	000b
28:16	**x8 Port Memory Read Outstanding Threshold** Specified in DWords. Default value of 600h Sets the threshold to 6 KB.	RWS	Yes	600h
31:29	***Reserved***	RsvdP	No	000b

Register 13-69. 1D8h Read Pacing Threshold 2 (Ports – Refer to Table 13-20)

Bit(s)	Descriptions	Ports	Type	Serial EEPROM and I^{2}C	Default
12:0	**x4 Port Memory Read Outstanding Threshold** Specified in DWords. Default value of 400h Sets the threshold to 4 KB.		RWS	Yes	400h
15:13	***Reserved***		RsvdP	No	000b
16	**Port *x* Memory Read Outstanding Counter Reset** Provides a mechanism for Clearing the Counter when an error condition occurs, with either the device that issued the Read Request, or the device that was to provide the Read Completions, where a System Level Reset will not be issued. If the Counter is not Cleared after an error condition such as this, the threshold will not be accurate. 0 = Read Outstanding Counter value increments, with each outstanding Read 1 = Resets Read Outstanding Counter	0, 16, or 20	RZ	Yes	0
17		1, 17, or 21	RZ	Yes	0
18		2, 18, or 22	RZ	Yes	0
19		3, 19, or 23	RZ	Yes	0
23:20	***Reserved***		RsvdP	No	0h
27:24	**Maximum Read Response Time** 0h = Disabled 1h = 5 ms 2h = 10 ms 3h = 15 ms 4h = 100 ms 5h = 200 ms 6h = 300 ms 7h = 500 ms 8h = 1.0s 9h = 2.0s All other encodings are ***reserved***.		RWS	Yes	1h
31:28	***Reserved***		RsvdP	No	0h

13.15.2 Device-Specific Registers – Captured Bus and Device Numbers (Offsets 1DCh – 1FCh)

This section details the Device-Specific Captured Bus and Device Numbers register. Table 13-21 defines the register map.

Table 13-21. Device-Specific Captured Bus and Device Numbers Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Captured Bus and Device Numbers	1DCh
Reserved	1E0h
Factory Test Only	1E4h
Reserved	1E8h – 1FCh

Register 13-70. 1DCh Captured Bus and Device Numbers (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
7:0	**Captured Bus Number** The Captured Bus Number value for this Port. The value of this field can be overwritten, if bit 31 (*Captured BusDev Number Override*) is Set prior to changing the Captured Bus Number. ***Note: Overwriting the Captured Bus Number value is not recommended.***		RWS	Yes	00h
12:8	**Captured Device Number** The Captured Device Number value for this Port. The value of this field can be overwritten, if bit 31 (*Captured BusDev Number Override*) is Set prior to changing the Captured Device Number. ***Note: Overwriting the Captured Device Number value is not recommended.***	Upstream	RWS	Yes	0-0h
		Downstream	RO	No	0-0h
30:13	***Reserved***		RsvdP	No	0-0h
31	**Captured BusDev Number Override** 1 = Enables the Captured Bus Number and Device Number to be overridden		RWS	Yes	0

13.15.3 Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)

This section details the Device-Specific Physical Layer (PHY) registers located at offsets 200h through 25Ch. Table 13-22 defines the register map.

Other Device-Specific PHY registers are detailed in Section 13.15.17, "Device-Specific Registers – Physical Layer (Offsets B80h – BC8h)."

Table 13-22. Device-Specific PHY Register Map (Offsets 200h – 25Ch) (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Physical Layer Receiver Detect Status	Physical Layer Electrical Idle for Compliance Mask	200h
Physical Layer Receiver Not Detected Mask	Physical Layer Electrical Idle Detect Mask	204h
Factory Test Only		208h – 20Ch
Physical Layer User Test Pattern, Bytes 0 through 3		210h
Physical Layer User Test Pattern, Bytes 4 through 7		214h
Physical Layer User Test Pattern, Bytes 8 through 11		218h
Physical Layer User Test Pattern, Bytes 12 through 15		21Ch
Physical Layer Command and Status		220h
Physical Layer Function Control		224h
Physical Layer Test		228h
Physical Layer Safety Bits		22Ch
Reserved	Physical Layer Port Command	230h
Port Control	SKIP Ordered-Set Interval	234h
SerDes Quad 0 Diagnostic Data		238h
SerDes Quad 1 Diagnostic Data		23Ch
SerDes Quad 2 Diagnostic Data		240h
SerDes Quad 3 Diagnostic Data		244h
Port Receiver Error Counter		248h
Target Link Width		24Ch
Factory Test Only		250h
Physical Layer Additional Status/Control		254h
PRBS Control/Status		258h
Reserved	Physical Layer Error Injection Control	25Ch

Notes: *In this section, the term "SerDes quad" or "quad" refers to assembling SerDes modules into groups of four contiguous Lanes for testing purposes.*

The Station register Port Numbers – Ports 0, 16, and 20 – are listed in addition to the individual Ports within the Station. Table 13-7 defines the Station, Station register Port Number, physical Port, physical Lane and SerDes module, and SerDes quad relationships.

Register 13-71. 200h Physical Layer Receiver Detect Status and Electrical Idle for Compliance Mask (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
This register is used for specifying the pre-determined quantity of Lanes that detected a Receiver during an LTSSM *Detect* state, but never detected an exit from Electrical Idle. Because the PEX 8649 has multiple Port configurations, a Mask register is used, rather than specifying a number. When multiple bits are Set, and they correspond to Lanes that belong to the same Port, any of those specified Lanes can cause entry into the LTSSM *Polling.Compliance* state. ***Note:*** *Refer to Table 13-7 for the relationship between the Port 0, 16, or 20 parameters and SerDes modules and Lanes.* *The Port 0 bits are for Ports 0, 1, 2, and 3. The Port 16 bits are for Ports 16, 17, 18, and 19. The Port 20 bits are for Ports 20, 21, 22, and 23.*				
Physical Layer Electrical Idle for Compliance Mask				
This register allows masking that specifies which Lanes must never exit Electrical Idle, for entry to the LTSSM *Polling.Compliance* state to occur.				
0	**Electrical Idle on SerDes 0, 32, or 16 Causes Entry to Compliance State** When all the bits are Cleared, the LTSSM *Polling.Compliance* state cannot be entered, due to the Electrical Idle condition. 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
1	**Electrical Idle on SerDes 1, 33, or 17 Causes Entry to Compliance State** When all the bits are Cleared, the LTSSM *Polling.Compliance* state cannot be entered, due to the Electrical Idle condition. 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
2	**Electrical Idle on SerDes 2, 34, or 18 Causes Entry to Compliance State** When all the bits are Cleared, the LTSSM *Polling.Compliance* state cannot be entered, due to the Electrical Idle condition. 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
3	**Electrical Idle on SerDes 3, 35, or 19 Causes Entry to Compliance State** When all the bits are Cleared, the LTSSM *Polling.Compliance* state cannot be entered, due to the Electrical Idle condition. 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1

Register 13-71. 200h Physical Layer Receiver Detect Status and Electrical Idle for Compliance Mask (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
4	**Electrical Idle on SerDes 4, 36, or 20 Causes Entry to Compliance State** When all the bits are Cleared, the LTSSM *Polling.Compliance* state cannot be entered, due to the Electrical Idle condition. 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
5	**Electrical Idle on SerDes 5, 37, or 21 Causes Entry to Compliance State** When all the bits are Cleared, the LTSSM *Polling.Compliance* state cannot be entered, due to the Electrical Idle condition. 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
6	**Electrical Idle on SerDes 6, 38, or 22 Causes Entry to Compliance State** When all the bits are Cleared, the LTSSM *Polling.Compliance* state cannot be entered, due to the Electrical Idle condition. 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
7	**Electrical Idle on SerDes 7, 39, or 23 Causes Entry to Compliance State** When all the bits are Cleared, the LTSSM *Polling.Compliance* state cannot be entered, due to the Electrical Idle condition. 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1

Register 13-71. 200h Physical Layer Receiver Detect Status and Electrical Idle for Compliance Mask (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
8	**Electrical Idle on SerDes 8, 40, or 24 Causes Entry to Compliance State** When all the bits are Cleared, the LTSSM *Polling.Compliance* state cannot be entered, due to the Electrical Idle condition. 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
9	**Electrical Idle on SerDes 9, 41, or 25 Causes Entry to Compliance State** When all the bits are Cleared, the LTSSM *Polling.Compliance* state cannot be entered, due to the Electrical Idle condition. 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
10	**Electrical Idle on SerDes 10, 42, or 26 Causes Entry to Compliance State** When all the bits are Cleared, the LTSSM *Polling.Compliance* state cannot be entered, due to the Electrical Idle condition. 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
11	**Electrical Idle on SerDes 11, 43, or 27 Causes Entry to Compliance State** When all the bits are Cleared, the LTSSM *Polling.Compliance* state cannot be entered, due to the Electrical Idle condition. 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1

Register 13-71. 200h Physical Layer Receiver Detect Status and Electrical Idle for Compliance Mask (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) ***(Cont.)***

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
12	**Electrical Idle on SerDes 12, 44, or 28 Causes Entry to Compliance State** When all the bits are Cleared, the LTSSM *Polling.Compliance* state cannot be entered, due to the Electrical Idle condition. 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
13	**Electrical Idle on SerDes 13, 45, or 29 Causes Entry to Compliance State** When all the bits are Cleared, the LTSSM *Polling.Compliance* state cannot be entered, due to the Electrical Idle condition. 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
14	**Electrical Idle on SerDes 14, 46, or 30 Causes Entry to Compliance State** When all the bits are Cleared, the LTSSM *Polling.Compliance* state cannot be entered, due to the Electrical Idle condition. 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1
15	**Electrical Idle on SerDes 15, 47, or 31 Causes Entry to Compliance State** When all the bits are Cleared, the LTSSM *Polling.Compliance* state cannot be entered, due to the Electrical Idle condition. 1 = Corresponding Lane must have detected a Receiver during an LTSSM *Detect* state, and must not see an exit from Electrical Idle during the *Polling.Active* state, to cause entry to the *Polling.Compliance* state	RWS	Yes	1

Register 13-71. 200h Physical Layer Receiver Detect Status and Electrical Idle for Compliance Mask (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
Physical Layer Receiver Detect Status				
This register returns the Receiver’s LTSSM *Detect* state status for all Lanes within the Station.				
16	**Receiver Detected on Lane 0, 32, or 16** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
17	**Receiver Detected on Lane 1, 33, or 17** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
18	**Receiver Detected on Lane 2, 34, or 18** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
19	**Receiver Detected on Lane 3, 35, or 19** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
20	**Receiver Detected on Lane 4, 36, or 20** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
21	**Receiver Detected on Lane 5, 37, or 21** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
22	**Receiver Detected on Lane 6, 38, or 22** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
23	**Receiver Detected on Lane 7, 39, or 23** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
24	**Receiver Detected on Lane 8, 40, or 24** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
25	**Receiver Detected on Lane 9, 41, or 25** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
26	**Receiver Detected on Lane 10, 42, or 26** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
27	**Receiver Detected on Lane 11, 43, or 27** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
28	**Receiver Detected on Lane 12, 44, or 28** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
29	**Receiver Detected on Lane 13, 45, or 29** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
30	**Receiver Detected on Lane 14, 46, or 30** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes
31	**Receiver Detected on Lane 15, 47, or 31** Reads back as 1 when a Receiver is detected on the Lane.	RO	No	Set by SerDes

Register 13-72. 204h Electrical Idle Detect/Receiver Detect Mask (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Masking Electrical Idle detect will not affect the inferred Electrical Idle detection. ***Notes:* Use this register with caution.** *Refer to Table 13-7 for the relationship between the Port 0, 16, or 20 parameters and SerDes modules and Lanes.* *The Port 0 bits are for Ports 0, 1, 2, and 3. The Port 16 bits are for Ports 16, 17, 18, and 19. The Port 20 bits are for Ports 20, 21, 22, and 23.*				
Physical Layer Electrical Idle Detect Mask				
Never Detect Electrical Idle mask. This register allows masking of the Electrical Idle Detect function, on a per-SerDes basis. When the bits in this register are Set, the Electrical Idle Condition flag of the corresponding Lane does not assert, regardless of the actual presence of Electrical Idle. Masking Electrical Idle detect does not affect the inferred Electrical Idle detection.				
0	**SerDes 0, 32, or 16 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station – the corresponding Lane will never detect Electrical Idle.	RWS	Yes	0
1	**SerDes 1, 33, or 17 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station – the corresponding Lane will never detect Electrical Idle.	RWS	Yes	0
2	**SerDes 2, 34, or 18 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station – the corresponding Lane will never detect Electrical Idle.	RWS	Yes	0
3	**SerDes 3, 35, or 19 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station – the corresponding Lane will never detect Electrical Idle.	RWS	Yes	0
4	**SerDes 4, 36, or 20 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station – the corresponding Lane will never detect Electrical Idle.	RWS	Yes	0
5	**SerDes 5, 37, or 21 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station – the corresponding Lane will never detect Electrical Idle.	RWS	Yes	0
6	**SerDes 6, 38, or 22 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station – the corresponding Lane will never detect Electrical Idle.	RWS	Yes	0
7	**SerDes 7, 39, or 23 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station – the corresponding Lane will never detect Electrical Idle.	RWS	Yes	0

Register 13-72. 204h Electrical Idle Detect/Receiver Detect Mask (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
8	**SerDes 8, 40, or 24 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station – the corresponding Lane will never detect Electrical Idle.	RWS	Yes	0
9	**SerDes 9, 41, or 25 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station – the corresponding Lane will never detect Electrical Idle.	RWS	Yes	0
10	**SerDes 10, 42, or 26 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station – the corresponding Lane will never detect Electrical Idle.	RWS	Yes	0
11	**SerDes 11, 43, or 27 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station – the corresponding Lane will never detect Electrical Idle.	RWS	Yes	0
12	**SerDes 12, 44, or 28 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station – the corresponding Lane will never detect Electrical Idle.	RWS	Yes	0
13	**SerDes 13, 45, or 29 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station – the corresponding Lane will never detect Electrical Idle.	RWS	Yes	0
14	**SerDes 14, 46, or 30 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station – the corresponding Lane will never detect Electrical Idle.	RWS	Yes	0
15	**SerDes 15, 47, or 31 Mask Electrical Idle Detect** 1 = Masks the Electrical Idle Detect for the SerDes, by Station – the corresponding Lane will never detect Electrical Idle.	RWS	Yes	0

Register 13-72. 204h Electrical Idle Detect/Receiver Detect Mask (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
Physical Layer Receiver Not Detected Mask				
Always Detect a Receiver mask. This register allows masking of the Receiver Detect function, on a per SerDes basis. When the bits in this register are Set, the PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.				
16	**SerDes 0, 32, or 16 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes, by Station – the corresponding Lane will always detect a Receiver. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
17	**SerDes 1, 33, or 17 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes, by Station – the corresponding Lane will always detect a Receiver. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
18	**SerDes 2, 34, or 18 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes, by Station – the corresponding Lane will always detect a Receiver. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
19	**SerDes 3, 35, or 19 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes, by Station – the corresponding Lane will always detect a Receiver. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
20	**SerDes 4, 36, or 20 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes, by Station – the corresponding Lane will always detect a Receiver. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
21	**SerDes 5, 37, or 21 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes, by Station – the corresponding Lane will always detect a Receiver. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
22	**SerDes 6, 38, or 22 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes, by Station – the corresponding Lane will always detect a Receiver. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
23	**SerDes 7, 39, or 23 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes, by Station – the corresponding Lane will always detect a Receiver. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0

Register 13-72. 204h Electrical Idle Detect/Receiver Detect Mask (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
24	**SerDes 8, 40, or 24 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes, by Station – the corresponding Lane will always detect a Receiver. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
25	**SerDes 9, 41, or 25 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes, by Station – the corresponding Lane will always detect a Receiver. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
26	**SerDes 10, 42, or 26 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes, by Station – the corresponding Lane will always detect a Receiver. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
27	**SerDes 11, 43, or 27 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes, by Station – the corresponding Lane will always detect a Receiver. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
28	**SerDes 12, 44, or 28 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes, by Station – the corresponding Lane will always detect a Receiver. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
29	**SerDes 13, 45, or 29 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes, by Station – the corresponding Lane will always detect a Receiver. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
30	**SerDes 14, 46, or 30 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes, by Station – the corresponding Lane will always detect a Receiver. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0
31	**SerDes 15, 47, or 31 Mask Receiver Not Detected** 1 = Masks the Receiver Not Detected for the SerDes, by Station – the corresponding Lane will always detect a Receiver. The PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.	RWS	Yes	0

Register 13-73. 210h Physical Layer User Test Pattern, Bytes 0 through 3 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
UTP Bytes 0 through 3. Used for Digital Far-End Loopback testing. ***Note:*** *A 16-byte test pattern can be written to register offsets 210h through 21Ch (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port). When User Test Pattern (UTP) transmission is enabled, Byte 0 of register offset 210h is transmitted first and Byte 3 (Byte 15 of the UTP) of register offset 21Ch is transmitted last. (Refer to Section 17.2.3, "Digital Loopback Master Mode," for further details.) Every byte of the UTP can be a Control or Data character. Illegal Control characters can be specified.*				
7:0	Byte 0 of the UTP. This is the first byte transferred.	RWS	Yes	00h
15:8	Byte 1 of the UTP.	RWS	Yes	00h
23:16	Byte 2 of the UTP.	RWS	Yes	00h
31:24	Byte 3 of the UTP.	RWS	Yes	00h

Register 13-74. 214h Physical Layer User Test Pattern, Bytes 4 through 7 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
UTP Bytes 4 through 7. Used for Digital Far-End Loopback testing. ***Note:*** *A 16-byte test pattern can be written to register offsets 210h through 21Ch (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port). When User Test Pattern (UTP) transmission is enabled, Byte 0 of register offset 210h is transmitted first and Byte 3 (Byte 15 of the UTP) of register offset 21Ch is transmitted last. (Refer to Section 17.2.3, "Digital Loopback Master Mode," for further details.) Every byte of the UTP can be a Control or Data character. Illegal Control characters can be specified.*				
7:0	Byte 4 of the UTP. This is the fifth byte transferred.	RWS	Yes	00h
15:8	Byte 5 of the UTP.	RWS	Yes	00h
23:16	Byte 6 of the UTP.	RWS	Yes	00h
31:24	Byte 7 of the UTP.	RWS	Yes	00h

Register 13-75. 218h Physical Layer User Test Pattern, Bytes 8 through 11 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
UTP Bytes 8 through 11. Used for Digital Far-End Loopback testing. ***Note:*** *A 16-byte test pattern can be written to register offsets 210h through 21Ch (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port). When User Test Pattern (UTP) transmission is enabled, Byte 0 of register offset 210h is transmitted first and Byte 3 (Byte 15 of the UTP) of register offset 21Ch is transmitted last. (Refer to Section 17.2.3, "Digital Loopback Master Mode," for further details.) Every byte of the UTP can be a Control or Data character. Illegal Control characters can be specified.*				
7:0	Byte 8 of the UTP. This is the ninth byte transferred.	RWS	Yes	00h
15:8	Byte 9 of the UTP.	RWS	Yes	00h
23:16	Byte 10 of the UTP.	RWS	Yes	00h
31:24	Byte 11 of the UTP.	RWS	Yes	00h

Register 13-76. 21Ch Physical Layer User Test Pattern, Bytes 12 through 15 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
UTP Bytes 12 through 15. Used for Digital Far-End Loopback testing. ***Note:*** *A 16-byte test pattern can be written to register offsets 210h through 21Ch (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port). When User Test Pattern (UTP) transmission is enabled, Byte 0 of register offset 210h is transmitted first and Byte 3 (Byte 15 of the UTP) of register offset 21Ch is transmitted last. (Refer to Section 17.2.3, "Digital Loopback Master Mode," for further details.) Every byte of the UTP can be a Control or Data character. Illegal Control characters can be specified.*				
7:0	Byte 12 of the UTP. This is the thirteenth byte transferred.	RWS	Yes	00h
15:8	Byte 13 of the UTP.	RWS	Yes	00h
23:16	Byte 14 of the UTP.	RWS	Yes	00h
31:24	Byte 15 of the UTP.	RWS	Yes	00h

Register 13-77. 220h Physical Layer Command and Status (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register provides various Command and Status bits for PHY operation.				
2:0	**Number of Ports Available in the Station** Returns the quantity of enabled Ports that this Station contains, based upon the selected Port configuration.	RO	No	Set by STRAP_STN*x*_PORTCFG*x* ball levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station x* bits (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 300h[11:8, 1:0])
3	**Upstream Cross-Link Enable** 0 = Disables upstream cross-link, upstream Port(s) cannot be connected to other upstream Port(s) 1 = Enables upstream cross-link, upstream Port(s) can be connected to other upstream Port(s)	RWS	Yes	1
4	**Downstream Cross-Link Enable** 0 = Disables downstream cross-link, downstream Ports cannot be connected to other downstream Ports 1 = Enables downstream cross-link, downstream Ports can be connected to other downstream Ports	RWS	Yes	1
5	**Lane Reversal Disable** 0 = Enables Lane reversal on all Ports 1 = Disables Lane reversal on all Ports	RWS	Yes	0
6	***Reserved***	RsvdP	No	0
7	**Elastic Buffer Low-Latency Mode Disable** 0 = Enables Elastic Buffer Low-Latency mode. 1 = Disables Elastic Buffer Low-Latency mode. Latency through the Elastic buffer is increased from 4 symbol times, to 7 symbol times, on all Lanes.	RWS	Yes	0

Register 13-77. 220h Physical Layer Command and Status (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:8	***Reserved***	RsvdP	No	00h
31:16	**User Test Pattern Control/Data** The UTP generators send out a set of 16 bytes of User Programmable data. A k-code bit can be Set for each byte. Bit 16 corresponds to Byte 0 of the User Test Pattern. … Bit 31 corresponds to Byte 15 of the User Test Pattern. 1 = Corresponding byte of the User Test Pattern is transmitted as a Control character; otherwise, the corresponding byte is transmitted as a Data character. ***Note: Use caution when Setting bits in this field, because UTP logic does not check the validity of Control characters.***	RWS	Yes	0000h

Register 13-78. 224h Physical Layer Function Control (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
This register allows for the configuration of various functions within the PHY logic. ***Note:*** *Bits [31:24] – The Port 0 bits are for Ports 0, 1, 2, and 3. The Port 16 bits are for Ports 16, 17, 18, and 19. The Port 20 bits are for Ports 20, 21, 22, and 23.*					
3:0	**Configuration Fail Counter [3:0]** Specifies the number of times that the *Configuration* state must fail before a Port toggles its Gen 2 Feature Disable flag. Writing 0000b to this field disables this Gen 1 compatibility function. The initial value of this register is determined by the STRAP_G1_COMPATIBLE# Strapping input state. If the input is Low when reset de-asserts, the initial value of this field is 0001b; otherwise, the initial value is 0000b.		RWS	Yes	0000b (STRAP_G1_COMPATIBLE#=H) 0001b (STRAP_G1_COMPATIBLE#=L)
6:4	**Electrical Idle Inference Time Select** Selects the amount of time to wait until no SKIP Ordered-Sets are detected, for Electrical Idle to be inferred. Does not affect Electrical Idle inference during the *Recovery.Speed* state. 000b = 4 µs 001b = 6 µs 010b = 8 µs 011b = 16 µs 100b = 32 µs 101b = 64 µs 110b = 128 µs (default) 111b = 256 µs		RWS	Yes	110b
7	***Reserved***		RsvdP	No	0

Register 13-78. 224h Physical Layer Function Control (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
9:8	**Recovery.Speed Electrical Idle Inference Time Divider Select** Selects the amount of time that no TS1 nor TS2 Ordered-Sets are detected during the *Recovery.Speed* state, for Electrical Idle to be inferred. (Refer to the *PCI Express Base r2.0*, Section 4.2.4.3, for the specific Unit Interval (UI) values.) 00b = *PCI Express Base r2.0* UI 01b = *PCI Express Base r2.0* UI/2 10b = *PCI Express Base r2.0* UI/4 11b = *PCI Express Base r2.0* UI/8		RWS	Yes	00b
11:10	**Detect.Quiet Wait Time Select Code [1:0]** Selects the amount of time to wait during the *Detect.Quiet* state, before starting the Receiver Detect operation, when a break from Electrical Idle is detected. If Electrical Idle is detected on all Lanes, the wait time is 12 ms. 00b = 0 ms 01b = 4 ms 10b = 8 ms 11b = 12 ms		RWS	Yes	00b
15:12	**Unconditional SerDes Quad Disable**		RWS	Yes	0h

Register 13-78. 224h Physical Layer Function Control (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
16	**Inferred Electrical Idle Inference Exit Type** Selects the method used to detect exit from Electrical Idle, after Electrical Idle has been inferred. 0 = **Fast Method** – Type 0 Exit mode is used, which uses conventional analog Electrical Idle Exit Detection circuitry 1 = **Slow Method** – Type 1 Exit mode is used, which uses the Symbol Framer Detection Time Select Code and Inferred Electrical Idle Exit Time Select Code Timers (fields [21:20 and 19:18], respectively)		RWS	Yes	0
17	***Reserved***		RsvdP	No	0
19:18	**Inferred Electrical Idle Exit Time Select Code** When Electrical Idle has been inferred and the Electrical Idle Inference Exit Type is 1, this field selects the amount of time the SerDes Receive Data path remains disabled. 00b = 2 µs 01b = 4 µs 10b = 8 µs 11b = 16 µs		RWS	Yes	00b
21:20	**Symbol Framer Detection Time Select Code** When Electrical Idle has been inferred and the Electrical Idle Inference Exit Type is 1, this field selects the amount of time that the symbol framer is allowed to obtain symbol lock. 00b = 128 ns 01b = 256 ns 10b = 512 ns 11b = 1 µs		RWS	Yes	10b
23:22	***Reserved***		RsvdP	No	00b

Register 13-78. 224h Physical Layer Function Control (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
24	**Port *x* Electrical Idle Inference Disable** 0 = Electrical Idle inference is enabled, if the **Physical Layer Electrical Idle Detect Mask** register *SerDes x Mask Electrical Idle Detect* bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 204h[15:0]) are Set, for the SerDes associated with the Port. 1 = Overall Electrical Idle inference logic is disabled on the corresponding Port. Electrical Idle inference during the *Recovery.Speed* state is not affected and will continue to operate.	0, 16, or 20	RWS	Yes	0
25		1, 17, or 21	RWS	Yes	0
26		2, 18, or 22	RWS	Yes	0
27		3, 19, or 23	RWS	Yes	0
28	**Port *x* Electrical Idle Inference on EIOS Receipt Enable** Electrical Idle Inference on Electrical Idle Ordered-Set (EIOS) Receipt enable, for the corresponding Port. 0 = Electrical Idle inference is enabled upon EIOS receipt, if the **Physical Layer Electrical Idle Detect Mask** register *SerDes x Mask Electrical Idle Detect* bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 204h[15:0]) are Set, for the SerDes associated with the Port 1 = Electrical Idle will be inferred as soon as an EIOS is received on any Lane of the corresponding Port	0, 16, or 20	RWS	Yes	0
29		1, 17, or 21	RWS	Yes	0
30		2, 18, or 22	RWS	Yes	0
31		3, 19, or 23	RWS	Yes	0

Register 13-79. 228h Physical Layer Test (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
This register provides controls to enable the various PHY Test modes. ***Note:*** *Refer to Table 13-7 for the relationship between the Port 0, 16, or 20 parameters and SerDes modules and Lanes.* *Bits [31:16, 3:0] – The Port 0 bits are for Ports 0, 1, 2, and 3. The Port 16 bits are for Ports 16, 17, 18, and 19. The Port 20 bits are for Ports 20, 21, 22, and 23.*					
0	**Port *x* Timer Test Mode Enable** 0 = Normal PHY Timer parameters are used 1 = Millisecond scale timers in the LTSSM of the corresponding Port are reduced to microsecond scale	0, 16, or 20	RWS	Yes	0
1		1, 17, or 21	RWS	Yes	0
2		2, 18, or 22	RWS	Yes	0
3		3, 19, or 23	RWS	Yes	0
4	**Skip Timer Test Mode Enable** 0 = Disables Skip Timer Test mode. 1 = Enables Skip Timer Test mode. SKIP Ordered-Sets are transmitted every 256 symbol times, on all Ports, regardless of the **SKIP Ordered-Set Interval** register *SKIP Ordered-Set Interval* field (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 234h[11:0]) value.		RW	Yes	0
5	**Ignore Compliance Receive TCB** Ignore the *Compliance Receive* Training Control Bit (TCB) field in Training Sets. 1 = Causes the PHY to ignore the *Compliance Receive* TCB when it is Set in received Training Sets		RWS	Yes	0
6	**Analog Loopback Enable** 0 = PEX 8649 enters Digital Loopback Slave mode if an external device sends at least two consecutive TS1 Ordered-Sets that have the *Loopback* bit exclusively Set in the TS1 Training Control symbol. The PEX 8649 then loops back data through the Elastic buffer, 8b/10b decoder, and 8b/10b encoder. 1 = When operating as a Loopback Slave, the Loopback point of all Ports will be before the Elastic buffer in the Recovered Receive Clock domain.		RWS	Yes	0
7	***Factory Test Only***		RW	Yes	0
15:8	***Factory Test Only***		RWS	Yes	00h

Register 13-79. 228h Physical Layer Test (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
16	**SerDes Quad 0 PRBS Enable** 0 = Disables PRBS sequence generation/checking on SerDes[0-3]/[32-35]/[16-19], by Station. 1 = Enables PRBS sequence generation/checking on SerDes[0-3]/[32-35]/[16-19], by Station. The corresponding SerDes quad will transmit the PRBS 7 data pattern. ***Notes:* Bits [19:16 and 31:28] (SerDes Quad x PRBS Enable and SerDes Quad x User Test Pattern Enable, respectively) are mutually exclusive functions and must not be enabled together for the same SerDes quad. In each Station register (Ports 0, 16, and 20), the logical result of bits [19:16] ANDed with bits [31:28] must be 0000b.** ***PRBS transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet state and the corresponding Port's Port Control register Hold Port x Quiet bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 234h[23:20]) is Set.***		RW	Yes	0
17	**SerDes Quad 1 PRBS Enable** 0 = Disables PRBS sequence generation/checking on SerDes[4-7]/[36-39]/[20-23], by Station. 1 = Enables PRBS sequence generation/checking on SerDes[4-7]/[36-39]/[20-23], by Station. The corresponding SerDes quad will transmit the PRBS 7 data pattern. ***Notes:* Bits [19:16 and 31:28] (SerDes Quad x PRBS Enable and SerDes Quad x User Test Pattern Enable, respectively) are mutually exclusive functions and must not be enabled together for the same SerDes quad. In each Station register (Ports 0, 16, and 20), the logical result of bits [19:16] ANDed with bits [31:28] must be 0000b.** ***PRBS transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet state and the corresponding Port's Port Control register Hold Port x Quiet bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 234h[23:20]) is Set.***		RW	Yes	0

Register 13-79. 228h Physical Layer Test (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
18	**SerDes Quad 2 PRBS Enable** 0 = Disables PRBS sequence generation/checking on SerDes[8-11]/[40-43]/[24-27], by Station. 1 = Enables PRBS sequence generation/checking on SerDes[8-11]/[40-43]/[24-27], by Station. The corresponding SerDes quad will transmit the PRBS 7 data pattern. ***Notes:*** ***Bits [19:16 and 31:28] (SerDes Quad x PRBS Enable and SerDes Quad x User Test Pattern Enable, respectively) are mutually exclusive functions and must not be enabled together for the same SerDes quad. In each Station register (Ports 0, 16, and 20), the logical result of bits [19:16] ANDed with bits [31:28] must be 0000b.*** ***PRBS transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet state and the corresponding Port's Port Control register Hold Port x Quiet bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 234h[23:20]) is Set.***		RW	Yes	0
19	**SerDes Quad 3 PRBS Enable** 0 = Disables PRBS sequence generation/checking on SerDes[12-15]/[44-47]/[28-31], by Station. 1 = Enables PRBS sequence generation/checking on SerDes[12-15]/[44-47]/[28-31], by Station. The corresponding SerDes quad will transmit the PRBS 7 data pattern. ***Notes:*** ***Bits [19:16 and 31:28] (SerDes Quad x PRBS Enable and SerDes Quad x User Test Pattern Enable, respectively) are mutually exclusive functions and must not be enabled together for the same SerDes quad. In each Station register (Ports 0, 16, and 20), the logical result of bits [19:16] ANDed with bits [31:28] must be 0000b.*** ***PRBS transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet state and the corresponding Port's Port Control register Hold Port x Quiet bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 234h[23:20]) is Set.***		RW	Yes	0

Register 13-79. 228h Physical Layer Test (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
20	**SerDes Quad 0 Serial Loopback Path Enable** Serial *Loopback* Path enable for SerDes[0-3]/[32-35]/[16-19], by Station. 1 = Corresponding SerDes quad enables the Serial *Loopback* (Master) path, regardless of the LTSSM state		RW	Yes	0
21	**SerDes Quad 1 Serial Loopback Path Enable** Serial *Loopback* Path enable for SerDes[4-7]/[36-39]/[20-23], by Station. 1 = Corresponding SerDes quad enables the Serial *Loopback* (Master) path, regardless of the LTSSM state		RW	Yes	0
22	**SerDes Quad 2 Serial Loopback Path Enable** Serial *Loopback* Path enable for SerDes[8-11]/[40-43]/[24-27], by Station. 1 = Corresponding SerDes quad enables the Serial *Loopback* (Master) path, regardless of the LTSSM state		RW	Yes	0
23	**SerDes Quad 3 Serial Loopback Path Enable** Serial *Loopback* Path enable for SerDes[12-15]/[44-47]/[28-31], by Station. 1 = Corresponding SerDes quad enables the Serial *Loopback* (Master) path, regardless of the LTSSM state		RW	Yes	0
24	**SerDes Quad 0 Parallel Loopback Path Enable** Parallel *Loopback* Path enable for SerDes[0-3]/[32-35]/[16-19], by Station. 1 = SerDes Quad 0 enables the Parallel *Loopback* (Slave) path, regardless of the LTSSM state. If bit 4 (*Skip Timer Test Mode Enable*) is Set, the *Loopback* path is located before the Elastic buffer. Otherwise, the *Loopback* path is located after the 8b/10b decoder.		RW	Yes	0
25	**SerDes Quad 1 Parallel Loopback Path Enable** Parallel *Loopback* Path enable for SerDes[4-7]/[36-39]/[20-23], by Station. 1 = SerDes Quad 1 enables the Parallel *Loopback* (Slave) path, regardless of the LTSSM state. If bit 4 (*Skip Timer Test Mode Enable*) is Set, the *Loopback* path is located before the Elastic buffer. Otherwise, the *Loopback* path is located after the 8b/10b decoder.		RW	Yes	0
26	**SerDes Quad 2 Parallel Loopback Path Enable** Parallel *Loopback* Path enable for SerDes[8-11]/[40-43]/[24-27], by Station. 1 = SerDes Quad 2 enables the Parallel *Loopback* (Slave) path, regardless of the LTSSM state. If bit 4 (*Skip Timer Test Mode Enable*) is Set, the *Loopback* path is located before the Elastic buffer. Otherwise, the *Loopback* path is located after the 8b/10b decoder.		RW	Yes	0
27	**SerDes Quad 3 Parallel Loopback Path Enable** Parallel *Loopback* Path enable for SerDes[12-15]/[44-47]/[28-31], by Station. 1 = SerDes Quad 3 enables the Parallel *Loopback* (Slave) path, regardless of the LTSSM state. If bit 4 (*Skip Timer Test Mode Enable*) is Set, the *Loopback* path is located before the Elastic buffer. Otherwise, the *Loopback* path is located after the 8b/10b decoder.		RW	Yes	0

Register 13-79. 228h Physical Layer Test (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
28	**SerDes Quad 0 User Test Pattern Enable** User Test Pattern enable for SerDes[0-3]/[32-35]/[16-19]. 0 = Disables transmission of the 128-bit test pattern 1 = Enables transmission of the 128-bit test pattern (**Physical Layer User Test Pattern, Bytes *x* through *y*** registers (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets 210h through 21Ch)) on SerDes[0-3]/[32-35]/[16-19] in Digital Far-End Loopback Master mode ***Notes:* Bits [31:28 and 19:16] (SerDes Quad x User Test Pattern Enable and SerDes Quad x PRBS Enable, respectively) are mutually exclusive functions and must not be enabled together for the same SerDes quad. In each Station register (Ports 0, 16, and 20), the logical result of bits [31:28] ANDed with bits [19:16] must be 0000b.** ***UTP transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet state and the corresponding Port's Port Control register Hold Port x Quiet bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 234h[23:20]) is Set.*** ***The Port's Port Control register Port x Bypass UTP Alignment Pattern bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 234h[31:28]) must be Set if the Link width of the Port under test is wider than x4, the Port under test is a Loopback Master, and the Loopback Slave is in a different clock domain.***		RW	Yes	0

Register 13-79. 228h Physical Layer Test (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
29	**SerDes Quad 1 User Test Pattern Enable** User Test Pattern enable for SerDes[4-7]/[36-39]/[20-23]. 0 = Disables transmission of the 128-bit test pattern 1 = Enables transmission of the 128-bit test pattern (**Physical Layer User Test Pattern, Bytes *x* through *y*** registers (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets 210h through 21Ch)) on SerDes[4-7]/[36-39]/[20-23] in Digital Far-End Loopback Master mode ***Notes:*** ***Bits [31:28 and 19:16] (SerDes Quad x User Test Pattern Enable and SerDes Quad x PRBS Enable, respectively) are mutually exclusive functions and must not be enabled together for the same SerDes quad. In each Station register (Ports 0, 16, and 20), the logical result of bits [31:28] ANDed with bits [19:16] must be 0000b.*** ***UTP transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet state and the corresponding Port's Port Control register Hold Port x Quiet bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 234h[23:20]) is Set.*** ***The Port's Port Control register Port x Bypass UTP Alignment Pattern bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 234h[31:28]) must be Set if the Link width of the Port under test is wider than x4, the Port under test is a Loopback Master, and the Loopback Slave is in a different clock domain.***		RW	Yes	0

Register 13-79. 228h Physical Layer Test (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
30	**SerDes Quad 2 User Test Pattern Enable** User Test Pattern enable for SerDes[8-11]/[40-43]/[24-27]. 0 = Disables transmission of the 128-bit test pattern 1 = Enables transmission of the 128-bit test pattern (**Physical Layer User Test Pattern, Bytes *x* through *y*** registers (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets 210h through 21Ch)) on SerDes[8-11]/[40-43]/[24-27] in Digital Far-End Loopback Master mode ***Notes:* Bits [31:28 and 19:16] (SerDes Quad x User Test Pattern Enable and SerDes Quad x PRBS Enable, respectively) are mutually exclusive functions and must not be enabled together for the same SerDes quad. In each Station register (Ports 0, 16, and 20), the logical result of bits [31:28] ANDed with bits [19:16] must be 0000b.** ***UTP transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet state and the corresponding Port's Port Control register Hold Port x Quiet bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 234h[23:20]) is Set.*** ***The Port's Port Control register Port x Bypass UTP Alignment Pattern bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 234h[31:28]) must be Set if the Link width of the Port under test is wider than x4, the Port under test is a Loopback Master, and the Loopback Slave is in a different clock domain.***		RW	Yes	0

Register 13-79. 228h Physical Layer Test (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
31	**SerDes Quad 3 User Test Pattern Enable** User Test Pattern enable for SerDes[12-15]/[44-47]/[28-31]. 0 = Disables transmission of the 128-bit test pattern 1 = Enables transmission of the 128-bit test pattern (**Physical Layer User Test Pattern, Bytes *x* through *y*** registers (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets 210h through 21Ch)) on SerDes[12-15]/[44-47]/[28-31] in Digital Far-End Loopback Master mode ***Notes:* Bits [31:28 and 19:16] (SerDes Quad x User Test Pattern Enable and SerDes Quad x PRBS Enable, respectively) are mutually exclusive functions and must not be enabled together for the same SerDes quad. In each Station register (Ports 0, 16, and 20), the logical result of bits [31:28] ANDed with bits [19:16] must be 0000b.** ***UTP transmission should be enabled only when operating as a Loopback Master, or when the LTSSM has returned to the Detect.Quiet state and the corresponding Port's Port Control register Hold Port x Quiet bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 234h[23:20]) is Set.*** ***The Port's Port Control register Port x Bypass UTP Alignment Pattern bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 234h[31:28]) must be Set if the Link width of the Port under test is wider than x4, the Port under test is a Loopback Master, and the Loopback Slave is in a different clock domain.***		RW	Yes	0

Register 13-80. 22Ch Physical Layer Safety Bits (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	***Factory Test Only***	RWS	Yes	0
1	**Framer Filter K28 Disable** Enabling the K28 Framer Filter increases robustness of the link by not retraining the Link upon detection of a single COM symbol. 0 = Four consecutive COM symbols must be detected within a packet, to cause the Link to be retrained 1 = If a COM symbol is detected within a packet, loss of symbol lock is assumed, and the Link is immediately retrained	RWS	Yes	0
5:2	***Factory Test Only***	RWS	Yes	0h
6	**Upconfigure Capability Disable** 0 = Upconfigure capability is advertised on all Ports 1 = Upconfigure capability is not advertised on all Ports	RWS	Yes	0
25:7	***Factory Test Only***	RWS	Yes	0-0h
31:26	***Reserved***	RWS	Yes	3Ch

Register 13-81. 230h Physical Layer Port Command (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register provides the Loopback, Scrambler Disable, and Compliance Receive commands, and Ready as Loopback Master status, for each Port. ***Note:*** *The Port 0 bits are for Ports 0, 1, 2, and 3. The Port 16 bits are for Ports 16, 17, 18, and 19. The Port 20 bits are for Ports 20, 21, 22, and 23.*				
0	**Port 0, 16, or 20 Loopback Command** 0 = Corresponding PEX 8649 Port is not enabled to go to the *Loopback* Master state. 1 = Corresponding PEX 8649 Port attempts to enter the *Loopback* state as a Loopback Master. If this bit is Set before the *Configuration* state is reached, the *Configuration.Linkwidth.Start* to *Loopback* path is used. If this bit is Set later, the *Recovery.Idle* to *Loopback* path is used.	RWS	Yes	0
1	**Port 0, 16, or 20 Scrambler Disable Command** When Set, unconditionally disables the data scramblers on the corresponding Port's Lane(s), and causes the *Disable Scrambling* Training Control Bit to be Set in the transmitted Training Sets. There is one bit for each Port in the associated Station. If a serial EEPROM load Sets this bit, the scrambler is disabled in a *Configuration.Complete* state. If software Sets this bit when the Link is in the Up state, hardware disables its scrambler without executing the Link Training protocol. This scrambler disable takes effect after the Link passes through *Configuration* again. The upstream/downstream device scrambler will not be disabled. 0 = Corresponding PEX 8649 Port's scrambler is enabled 1 = Corresponding PEX 8649 Port's scrambler is disabled	RWS	Yes	0
2	**Port 0, 16, or 20 Compliance Receive Command** 0 = When the corresponding PEX 8649 Port transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is not Set during the *Polling.Active* nor *Loopback.Entry* state 1 = When the corresponding PEX 8649 Port transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is Set during the *Polling.Active* or *Loopback.Entry* state	RWS	Yes	0
3	**Port 0, 16, or 20 Ready as Loopback Master** Link Training and Status State Machine (LTSSM) established Loopback as a Master for the corresponding PEX 8649 Port. 0 = Corresponding PEX 8649 Port is not in Loopback Master mode. 1 = Indicates that the corresponding PEX 8649 Port has successfully transitioned to the *Loopback.Active* state as a Loopback Master. The LTSSM remains in this state, until bit 0 (*Port 0, 16, or 20 Loopback Command*) is Cleared. This bit is Cleared when the PEX 8649 exits the *Loopback.Active* state.	RO	No	0

Register 13-81. 230h Physical Layer Port Command (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
4	**Port 1, 17, or 21 Loopback Command** 0 = Corresponding PEX 8649 Port is not enabled to go to the *Loopback* Master state. 1 = Corresponding PEX 8649 Port attempts to enter the *Loopback* state as a Loopback Master. If this bit is Set before the *Configuration* state is reached, the *Configuration.Linkwidth.Start* to *Loopback* path is used. If this bit is Set later, the *Recovery.Idle* to *Loopback* path is used.	RWS	Yes	0
5	**Port 1, 17, or 21 Scrambler Disable Command** When Set, unconditionally disables the data scramblers on the corresponding Port's Lane(s), and causes the *Disable Scrambling* Training Control Bit to be Set in the transmitted Training Sets. There is one bit for each Port in the associated Station. If a serial EEPROM load Sets this bit, the scrambler is disabled in a *Configuration.Complete* state. If software Sets this bit when the Link is in the Up state, hardware disables its scrambler without executing the Link Training protocol. This scrambler disable takes effect after the Link passes through *Configuration* again. The upstream/downstream device scrambler will not be disabled. 0 = Corresponding PEX 8649 Port's scrambler is enabled 1 = Corresponding PEX 8649 Port's scrambler is disabled	RWS	Yes	0
6	**Port 1, 17, or 21 Compliance Receive Command** 0 = When the corresponding PEX 8649 Port transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is not Set during the *Polling.Active* nor *Loopback.Entry* state 1 = When the corresponding PEX 8649 Port transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is Set during the *Polling.Active* or *Loopback.Entry* state	RWS	Yes	0
7	**Port 1, 17, or 21 Ready as Loopback Master** LTSSM established Loopback as a Master for the corresponding PEX 8649 Port. 0 = Corresponding PEX 8649 Port is not in Loopback Master mode. 1 = Indicates that the corresponding PEX 8649 Port has successfully transitioned to the *Loopback.Active* state as a Loopback Master. The LTSSM remains in this state, until bit 4 (*Port 1, 17, or 21 Loopback Command*) is Cleared. This bit is Cleared when the PEX 8649 exits the *Loopback.Active* state.	RO	No	0

Register 13-81. 230h Physical Layer Port Command (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
8	**Port 2, 18, or 22 Loopback Command** 0 = Corresponding PEX 8649 Port is not enabled to go to the *Loopback* Master state. 1 = Corresponding PEX 8649 Port attempts to enter the *Loopback* state as a Loopback Master. If this bit is Set before the *Configuration* state is reached, the *Configuration.Linkwidth.Start* to *Loopback* path is used. If this bit is Set later, the *Recovery.Idle* to *Loopback* path is used.	RWS	Yes	0
9	**Port 2, 18, or 22 Scrambler Disable Command** When Set, unconditionally disables the data scramblers on the corresponding Port's Lane(s), and causes the *Disable Scrambling* Training Control Bit to be Set in the transmitted Training Sets. There is one bit for each Port in the associated Station. If a serial EEPROM load Sets this bit, the scrambler is disabled in a *Configuration.Complete* state. If software Sets this bit when the Link is in the Up state, hardware disables its scrambler without executing the Link Training protocol. This scrambler disable takes effect after the Link passes through *Configuration* again. The upstream/downstream device scrambler will not be disabled. 0 = Corresponding PEX 8649 Port's scrambler is enabled 1 = Corresponding PEX 8649 Port's scrambler is disabled	RWS	Yes	0
10	**Port 2, 18, or 22 Compliance Receive Command** 0 = When the corresponding PEX 8649 Port transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is not Set during the *Polling.Active* nor *Loopback.Entry* state 1 = When the corresponding PEX 8649 Port transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is Set during the *Polling.Active* or *Loopback.Entry* state	RWS	Yes	0
11	**Port 2, 18, or 22 Ready as Loopback Master** LTSSM established Loopback as a Master for the corresponding PEX 8649 Port. 0 = Corresponding PEX 8649 Port is not in Loopback Master mode. 1 = Indicates that the corresponding PEX 8649 Port has successfully transitioned to the *Loopback.Active* state as a Loopback Master. The LTSSM remains in this state, until bit 8 (*Port 2, 18, or 22 Loopback Command*) is Cleared. This bit is Cleared when the PEX 8649 exits the *Loopback.Active* state.	RO	No	0

Register 13-81. 230h Physical Layer Port Command (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
12	**Port 3, 19, or 23 Loopback Command** 0 = Corresponding PEX 8649 Port is not enabled to go to the *Loopback* Master state. 1 = Corresponding PEX 8649 Port attempts to enter the *Loopback* state as a Loopback Master. If this bit is Set before the *Configuration* state is reached, the *Configuration.Linkwidth.Start* to *Loopback* path is used. If this bit is Set later, the *Recovery.Idle* to *Loopback* path is used.	RWS	Yes	0
13	**Port 3, 19, or 23 Scrambler Disable Command** When Set, unconditionally disables the data scramblers on the corresponding Port's Lane(s), and causes the *Disable Scrambling* Training Control Bit to be Set in the transmitted Training Sets. There is one bit for each Port in the associated Station. If a serial EEPROM load Sets this bit, the scrambler is disabled in a *Configuration.Complete* state. If software Sets this bit when the Link is in the Up state, hardware disables its scrambler without executing the Link Training protocol. This scrambler disable takes effect after the Link passes through *Configuration* again. The upstream/downstream device scrambler will not be disabled. 0 = Corresponding PEX 8649 Port's scrambler is enabled 1 = Corresponding PEX 8649 Port's scrambler is disabled	RWS	Yes	0
14	**Port 3, 19, or 23 Compliance Receive Command** 0 = When the corresponding PEX 8649 Port transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is not Set during the *Polling.Active* nor *Loopback.Entry* state 1 = When the corresponding PEX 8649 Port transmits TS1 Ordered-Sets, the *Compliance Receive* Training Control Bit within these Ordered-Sets is Set during the *Polling.Active* or *Loopback.Entry* state	RWS	Yes	0
15	**Port 3, 19, or 23 Ready as Loopback Master** LTSSM established Loopback as a Master for the corresponding PEX 8649 Port. 0 = Corresponding PEX 8649 Port is not in Loopback Master mode. 1 = Indicates that the corresponding PEX 8649 Port has successfully transitioned to the *Loopback.Active* state as a Loopback Master. The LTSSM remains in this state, until bit 12 (*Port 3, 19, or 23 Loopback Command*) is Cleared. This bit is Cleared when the PEX 8649 exits the *Loopback.Active* state.	RO	No	0
31:16	***Reserved***	RsvdP	No	0000h

Register 13-82. 234h SKIP Ordered-Set Interval and Port Control (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
SKIP Ordered-Set Interval					
This register is used to adjust the distance between SKIP Ordered-Sets.					
11:0	**SKIP Ordered-Set Interval** Specifies the SKIP Ordered-Set interval (in symbol times). When a value of 000h is written, SKIP Ordered-Set transmission is disabled. 000h = SKIP Ordered-Set transmission is disabled 49Ch = Minimum interval (1,180 symbol times) 602h = Maximum interval (1,538 symbol times) ***Note:*** *A high value (such as FFFh) can cause the Link to fail.*		RWS	Yes	49Ch
15:12	***Reserved***		RsvdP	No	0h
Port Control					
This register is used to disable or enable the LTSSM in individual Ports. The Port control bits are intended to be used in lieu of placing the Port into the *Loopback.Active* state as a Loopback Master. These bits enable the test patterns to be transmitted, with or without a device attached at the far end. The recommended usage is as follows: **1.** Set the Port's *Disable Port x* and *Hold Port x Quiet* bits (bits [19:16 and 23:20], respectively), • Setting Port Disable forces the Port into the *Detect.Quiet* state. If no device is attached, it is not necessary to Set the *Disable Port x* bit. • If 5.0 GT/s is needed, also Set the Port's *Port x Test Pattern x Rate* bits (bits [27:24], respectively). **2.** If Set, Clear the Port's *Disable Port x* bit. **3.** Load the UTP registers and enable UTP transmission, or just enable PRBS transmission. ***Note:*** *The Port 0 bits are for Ports 0, 1, 2, and 3. The Port 16 bits are for Ports 16, 17, 18, and 19. The Port 20 bits are for Ports 20, 21, 22, and 23.*					
16	**Disable Port *x*** While the Port is disabled, Receiver termination is disabled and the SerDes that belong to the disabled Port are placed into the L1 Link PM state. 0 = Enables Link Training operation on the corresponding PEX 8649 Port. 1 = LTSSM remains in the *Detect.Quiet* state on the corresponding PEX 8649 Port if it is currently in, or returns to, that state. Unconditionally disables the corresponding Port. This is different from the LTSSM *Disabled* state, in that the Port does not attempt to enter this state. If the Port is idle, it ceases attempting to detect a Receiver. If the Port is up, it immediately returns to the *Detect.Quiet* state and remains there. No EIOS is sent, which could force any connected device to the *Recovery* state, and then to the LTSSM *Detect* state. The Port remains disabled until its *Disable Port x* bit is Cleared. While the Port is disabled, Receiver termination is disabled and the SerDes that belong to the disabled Port are placed into the L1 Link PM state.	0, 16, or 20	RWS	Yes	0
17		1, 17, or 21	RWS	Yes	0
18		2, 18, or 22	RWS	Yes	0
19		3, 19, or 23	RWS	Yes	0

Register 13-82. 234h SKIP Ordered-Set Interval and Port Control (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
20	**Hold Port *x* Quiet** Once in the *Detect.Quiet* state, Receiver termination is enabled and the Transmitters are placed in the L0 Link PM state. This Port can now transmit test patterns (PRBS or UTP), with or without an attached device and without being in the *Loopback.Active* state. 0 = No effect on the LTSSM. 1 = Corresponding Port remains in the *Detect.Quiet* state once it returns there. These bits do not make the LTSSM exit its current state. Receiver termination remains active, and the Transmitters are placed into the P0 state (ready to transmit data) when the *Detect.Quiet* state is reached. ***Note:*** *Use these bits when it is necessary to transmit some data pattern, without first entering the Loopback.Active state as a Loopback Master.*	0, 16, or 20	RWS	Yes	0
21		1, 17, or 21	RWS	Yes	0
22		2, 18, or 22	RWS	Yes	0
23		3, 19, or 23	RWS	Yes	0
24	**Port *x* Test Pattern *x* Rate** The corresponding Port transmits the selected test pattern (PRBS or UTP) at 5.0 GT/s, if the Port's *Hold Port x Quiet* bit (bits [23:20]) is also Set (manual rate selection is enabled only when the Port's *Hold Port x Quiet* bit is Set). 0 = UTP is transmitted at 2.5 GT/s 1 = UTP is transmitted at 5.0 GT/s ***Note:*** *If the corresponding Port's bit* ***[****31:28] (Port x Bypass UTP Alignment Pattern) is Set, this bit (for that Port) cannot be used.*	0, 16, or 20	RWS	Yes	0
25		1, 17, or 21	RWS	Yes	0
26		2, 18, or 22	RWS	Yes	0
27		3, 19, or 23	RWS	Yes	0
28	**Port *x* Bypass UTP Alignment Pattern** Must be Set if the following conditions exist: • Link width of Port being tested is wider than x4, and • Port being tested is a Loopback Master transmitting the User Test Pattern, and • Loopback Slave is in a different clock domain 0 = UTP Transmitter continuously transmits the alignment pattern until any UTP checker in the corresponding SerDes quad indicates that it has received the alignment pattern. The UTP Transmitter will then transmit one sync pattern, followed by the programmed UTP. 1 = Programmed UTP will be preceded by one alignment pattern (D3.2 D18.2 D13.2 D17.1) and one sync pattern (K28.5 D3.2 D18.2 D13.2).	0, 16, or 20	RWS	Yes	0
29		1, 17, or 21	RWS	Yes	0
30		2, 18, or 22	RWS	Yes	0
31		3, 19, or 23	RWS	Yes	0

Register 13-83. 238h SerDes Quad 0 Diagnostic Data (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
There are four **SerDes Quad *x* Diagnostic Data** (Diagnostic Data) registers, one for each SerDes quad, at offsets 238h through 244h, in each Station (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port). The contents of the Diagnostic Data registers reflect the performance of the SerDes that are selected by the registers' *SerDes Diagnostic Data Select* bits (field [25:24]). *For example*, if field [25:24] in offset 23Ch is programmed to 10b, then the information in that Diagnostic Data register is for SerDes 2 of Quad 1 of that Station (SerDes 6, 38, or 22 in Stations 0, 5, and 4, respectively). This register is used to retrieve Diagnostic Test results for SerDes[0-3]/[32-35]/[16-19]. ***Notes:*** *Refer to Table 13-7 for the relationship between the Port 0, 16, or 20 parameters and SerDes modules and Lanes.* *The Port 0 bits/fields are for Ports 0, 1, 2, and 3. The Port 16 bits/fields are for Ports 16, 17, 18, and 19. The Port 20 bits/fields are for Ports 20, 21, 22, and 23.*				
7:0	**UTP Expected Data** When User Test Pattern (UTP) is enabled, if an error is detected in the received UTP data, this field returns the expected data.	RO	No	00h
15:8	**UTP Actual Data** When UTP is enabled, if an error is detected in the received UTP data, this field returns the actual data that was received.	RO	No	00h
23:16	**UTP/PRBS Error Counter** Receiver Detected flags. Returns the number of errors detected by the UTP (bit 30 = 0) or PRBS (bit 30 = 1) Data Checkers. The Error Counter saturates at 255, and is Cleared when UTP/PRBS is disabled. **UTP Mode** To Clear the Counter, disable UTP mode by Clearing the **Physical Layer Test** register *SerDes Quad 0 User Test Pattern Enable* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 228h[28]). **PRBS Mode** To Clear the Counter, disable PRBS mode by Clearing the **Physical Layer Test** register *SerDes Quad 0 PRBS Enable* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 228h[16]).	RO	No	00h

Register 13-83. 238h SerDes Quad 0 Diagnostic Data (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
25:24	**SerDes Diagnostic Data Select** Used to select the SerDes (SerDes[0-3]/[32-35]/[16-19]) to which the diagnostic data in this SerDes quad pertains. Status selection code for the fields representing RO bits [23:0] of this register. The binary code represents a status selection for one of the SerDes Quad 0 Lanes. The test results for physical device Lanes [0-3]/[32-35]/[16-19] are selected with corresponding binary codes from 0-3. ***Note:*** *To obtain diagnostic data on all SerDes in the quad, run a test, then cycle these bits.*	RW	Yes	00b
29:26	***Reserved***	RO	No	0h
30	**PRBS Counter/-UTP Counter** 0 = Indicates that field [23:16] (*UTP/PRBS Error Counter*) is the UTP Error Counter (diagnostic data is from the UTP Data Checkers) 1 = Indicates that field [23:16] (*UTP/PRBS Error Counter*) is the PRBS Error Counter (diagnostic data is from the PRBS Data Checkers)	RO	No	0
31	***Reserved***	RsvdP	No	0

Register 13-84. 23Ch SerDes Quad 1 Diagnostic Data (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
There are four **SerDes Quad *x* Diagnostic Data** (Diagnostic Data) registers, one for each SerDes quad, at offsets 238h through 244h, in each Station (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port). The contents of the Diagnostic Data registers reflect the performance of the SerDes that are selected by the registers' *SerDes Diagnostic Data Select* bits (field [25:24]). *For example*, if field [25:24] in offset 23Ch is programmed to 10b, then the information in that Diagnostic Data register is for SerDes 2 of Quad 1 of that Station (SerDes 6, 38, or 22 in Stations 0, 5, and 4, respectively). This register is used to retrieve Diagnostic Test results for SerDes[4-7]/[36-39]/[20-23]. ***Notes:*** *Refer to Table 13-7 for the relationship between the Port 0, 16, or 20 parameters and SerDes modules and Lanes.* *The Port 0 bits/fields are for Ports 0, 1, 2, and 3. The Port 16 bits/fields are for Ports 16, 17, 18, and 19. The Port 20 bits/fields are for Ports 20, 21, 22, and 23.*				
7:0	**UTP Expected Data** When User Test Pattern (UTP) is enabled, if an error is detected in the received UTP data, this field returns the expected data.	RO	No	00h
15:8	**UTP Actual Data** When UTP is enabled, if an error is detected in the received UTP data, this field returns the actual data that was received.	RO	No	00h
23:16	**UTP/PRBS Error Counter** Receiver Detected flags. Returns the number of errors detected by the UTP (bit 30 = 0) or PRBS (bit 30 = 1) Data Checkers. The Error Counter saturates at 255, and is Cleared when UTP/PRBS is disabled. **UTP Mode** To Clear the Counter, disable UTP mode by Clearing the **Physical Layer Test** register *SerDes Quad 1 User Test Pattern Enable* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 228h[29]). **PRBS Mode** To Clear the Counter, disable PRBS mode by Clearing the **Physical Layer Test** register *SerDes Quad 1 PRBS Enable* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 228h[17]).	RO	No	00h

Register 13-84. 23Ch SerDes Quad 1 Diagnostic Data (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
25:24	**SerDes Diagnostic Data Select** Used to select the SerDes (SerDes[4-7]/[36-39]/[20-23]) to which the diagnostic data in this SerDes quad pertains. Status selection code for the fields representing RO bits [23:0] of this register. The binary code represents a status selection for one of the SerDes Quad 1 Lanes. The test results for physical device Lanes [4-7]/[36-39]/[20-23] are selected with corresponding binary codes from 0-3. ***Note:*** *To obtain diagnostic data on all SerDes in the quad, run a test, then cycle these bits.*	RW	Yes	00b
29:26	***Reserved***	RO	No	0h
30	**PRBS Counter/-UTP Counter** 0 = Indicates that field [23:16] (*UTP/PRBS Error Counter*) is the UTP Error Counter (diagnostic data is from the UTP Data Checkers) 1 = Indicates that field [23:16] (*UTP/PRBS Error Counter*) is the PRBS Error Counter (diagnostic data is from the PRBS Data Checkers)	RO	No	0
31	***Reserved***	RsvdP	No	0

Register 13-85. 240h SerDes Quad 2 Diagnostic Data (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
There are four **SerDes Quad *x* Diagnostic Data** (Diagnostic Data) registers, one for each SerDes quad, at offsets 238h through 244h, in each Station (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port). The contents of the Diagnostic Data registers reflect the performance of the SerDes that are selected by the registers' *SerDes Diagnostic Data Select* bits (field [25:24]). *For example*, if field [25:24] in offset 23Ch is programmed to 10b, then the information in that Diagnostic Data register is for SerDes 2 of Quad 1 of that Station (SerDes 6, 38, or 22 in Stations 0, 5, and 4, respectively). This register is used to retrieve Diagnostic Test results for SerDes[8-11]/[40-43]/[24-27]. ***Notes:*** *Refer to Table 13-7 for the relationship between the Port 0, 16, or 20 parameters and SerDes modules and Lanes.* *The Port 0 bits/fields are for Ports 0, 1, 2, and 3. The Port 16 bits/fields are for Ports 16, 17, 18, and 19. The Port 20 bits/fields are for Ports 20, 21, 22, and 23.*				
7:0	**UTP Expected Data** When User Test Pattern (UTP) is enabled, if an error is detected in the received UTP data, this field returns the expected data.	RO	No	00h
15:8	**UTP Actual Data** When UTP is enabled, if an error is detected in the received UTP data, this field returns the actual data that was received.	RO	No	00h
23:16	**UTP/PRBS Error Counter** Receiver Detected flags. Returns the number of errors detected by the UTP (bit 30 = 0) or PRBS (bit 30 = 1) Data Checkers. The Error Counter saturates at 255, and is Cleared when UTP/PRBS is disabled. **UTP Mode** To Clear the Counter, disable UTP mode by Clearing the **Physical Layer Test** register *SerDes Quad 2 User Test Pattern Enable* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 228h[30]). **PRBS Mode** To Clear the Counter, disable PRBS mode by Clearing the **Physical Layer Test** register *SerDes Quad 2 PRBS Enable* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 228h[18]).	RO	No	00h

Register 13-85. 240h SerDes Quad 2 Diagnostic Data (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
25:24	**SerDes Diagnostic Data Select** Used to select the SerDes (SerDes[8-11]/[40-43]/[24-27]) to which the diagnostic data in this SerDes quad pertains. Status selection code for the fields representing RO bits [23:0] of this register. The binary code represents a status selection for one of the SerDes Quad 2 Lanes. The test results for physical device Lanes [8-11]/[40-43]/[24-27] are selected with corresponding binary codes from 0-3. ***Note:*** *To obtain diagnostic data on all SerDes in the quad, run a test, then cycle these bits.*	RW	Yes	00b
29:26	***Reserved***	RO	No	0h
30	**PRBS Counter/-UTP Counter** 0 = Indicates that field [23:16] (*UTP/PRBS Error Counter*) is the UTP Error Counter (diagnostic data is from the UTP Data Checkers) 1 = Indicates that field [23:16] (*UTP/PRBS Error Counter*) is the PRBS Error Counter (diagnostic data is from the PRBS Data Checkers)	RO	No	0
31	***Reserved***	RsvdP	No	0

Register 13-86. 244h SerDes Quad 3 Diagnostic Data (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
There are four **SerDes Quad *x* Diagnostic Data** (Diagnostic Data) registers, one for each SerDes quad, at offsets 238h through 244h, in each Station (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port). The contents of the Diagnostic Data registers reflect the performance of the SerDes that are selected by the registers' *SerDes Diagnostic Data Select* bits (field [25:24]). *For example*, if field [25:24] in offset 23Ch is programmed to 10b, then the information in that Diagnostic Data register is for SerDes 2 of Quad 1 of that Station (SerDes 6, 38, or 22 in Stations 0, 5, and 4, respectively). This register is used to retrieve Diagnostic Test results for SerDes[12-15]/[44-47]/[28-31]. ***Notes:*** *Refer to Table 13-7 for the relationship between the Port 0, 16, or 20 parameters and SerDes modules and Lanes.* *The Port 0 bits/fields are for Ports 0, 1, 2, and 3. The Port 16 bits/fields are for Ports 16, 17, 18, and 19. The Port 20 bits/fields are for Ports 20, 21, 22, and 23.*				
7:0	**UTP Expected Data** When User Test Pattern (UTP) is enabled, if an error is detected in the received UTP data, this field returns the expected data.	RO	No	00h
15:8	**UTP Actual Data** When UTP is enabled, if an error is detected in the received UTP data, this field returns the actual data that was received.	RO	No	00h
23:16	**UTP/PRBS Error Counter** Receiver Detected flags. Returns the number of errors detected by the UTP (bit 30 = 0) or PRBS (bit 30 = 1) Data Checkers. The Error Counter saturates at 255, and is Cleared when UTP/PRBS is disabled. **UTP Mode** To Clear the Counter, disable UTP mode by Clearing the **Physical Layer Test** register *SerDes Quad 3 User Test Pattern Enable* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 228h[31]). **PRBS Mode** To Clear the Counter, disable PRBS mode by Clearing the **Physical Layer Test** register *SerDes Quad 3 PRBS Enable* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 228h[19]).	RO	No	00h

Register 13-86. 244h SerDes Quad 3 Diagnostic Data (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
25:24	**SerDes Diagnostic Data Select** Used to select the SerDes (SerDes[12-15]/[44-47]/[28-31]) to which the diagnostic data in this SerDes quad pertains. Status selection code for the fields representing RO bits [23:0] of this register. The binary code represents a status selection for one of the SerDes Quad 3 Lanes. The test results for physical device Lanes [12-15]/[44-47]/[28-31] are selected with corresponding binary codes from 0-3. ***Note:*** *To obtain diagnostic data on all SerDes in the quad, run a test, then cycle these bits.*	RW	Yes	00b
29:26	***Reserved***	RO	No	0h
30	**PRBS Counter/-UTP Counter** 0 = Indicates that field [23:16] (*UTP/PRBS Error Counter*) is the UTP Error Counter (diagnostic data is from the UTP Data Checkers) 1 = Indicates that field [23:16] (*UTP/PRBS Error Counter*) is the PRBS Error Counter (diagnostic data is from the PRBS Data Checkers)	RO	No	0
31	***Reserved***	RsvdP	No	0

Register 13-87. 248h Port Receiver Error Counter (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
Note: *The Port 0 fields are for Ports 0, 1, 2, and 3. The Port 16 fields are for Ports 16, 17, 18, and 19. The Port 20 fields are for Ports 20, 21, 22, and 23.*					
7:0	**Port *x* Receiver Error Counter** When read, returns the number of Receiver errors detected by the corresponding Port (Receiver Error Counter). The Error Counter saturates at 255. The Counter is Cleared with any Write to the corresponding byte in this register; otherwise, this field is RO.	0, 16, or 20	RW1C	No	00h
15:8		1, 17, or 21	RW1C	No	00h
23:16		2, 18, or 22	RW1C	No	00h
31:24		3, 19, or 23	RW1C	No	00h

Register 13-88. 24Ch Target Link Width (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I^{2}C</th><th>Default</th></tr>
<tr><td colspan="5">This register is provided to furnish software with the ability to direct Link Width Up/Down configuration.
The Port’s <i>Target Link Width</i> field in this register is initially loaded with the Port’s Negotiated Link Width (offset 78h[25:20]), the first time that the Port’s LTSSM transitions from <i>Configuration</i> (italic) to the <i>L0</i> Link PM state. The value remains 0 for Ports that are not active.
Software can be used to retrain a Link to a wider or narrower width than the current width, <i>such as</i> to conserve power when maximum bandwidth is not required. Devices advertise such support, by transmitting the appropriate value for the Data Rate Identifier symbol within TS2 Ordered-Sets.
If the Port’s <i>Port x Upconfigure Capability Received</i> bit is Set (indicating that during the previous Link training, the Port received Upconfigure Capability notification from the connected device), software can cause the Port to:
• Upconfigure the Link to a previously negotiated Link width, –or–
• Downconfigure the Link to a narrower width
by writing the needed Target Link Width value to this register, followed by Setting the Port’s <b>Link Control</b> register <i>Retrain Link</i> bit (offset 78h[5]). If the Target Link Width is not equal to the current Link width, the LTSSM transitions from <i>Recovery</i> to <i>Configuration</i>, then renegotiates the Link width.
<b><i>Note:</i></b> <i>The Port 0 bits/fields are for Ports 0, 1, 2, and 3. The Port 16 bits/fields are for Ports 16, 17, 18, and 19. The Port 20 bits/fields are for Ports 20, 21, 22, and 23.</i></td></tr>
<tr><td>4:0</td><td><b>Port 0, 16, or 20 Target Link Width</b>
Provides the capability to allow software to cause Link retraining to a wider or narrower width than the current width, <i>such as</i> to conserve power when maximum bandwidth is not required. Devices advertise such support, by transmitting the appropriate value for the Data Rate Identifier symbol within TS2 Ordered-Sets.
Written with the Target Link width for the corresponding Port, to support Link Width Upconfiguration. The initial value of this field is the Port’s Negotiated Link Width (offset 78h[25:20]).</td><td>RWS</td><td>No</td><td>Set by STRAP_STN<i>x</i>_PORTCFG<i>x</i> ball levels, or by serial EEPROM value for the <b>Port Configuration</b> register <i>Port Configuration for Station x</i> bits (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 300h[11:8, 1:0])</td></tr>
<tr><td>6:5</td><td><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>00b</td></tr>
<tr><td>7</td><td><b>Port 0, 16, or 20 Upconfigure Capability Received</b>
Set during Link training, if the corresponding Port received an Upconfigure Capability notification from the connected device.
0 = Device connected to the corresponding Port does not indicate that it is capable of Link Width Upconfiguration.
1 = Device connected to the corresponding Port indicates that it is capable of Link Width Upconfiguration. Software can cause the Port to either upconfigure the Link to a previously negotiated Link width, or downconfigure the Link to a narrower width, by writing the needed Target Link Width value to this register, followed by Setting the Port’s <b>Link Control</b> register <i>Retrain Link</i> bit (offset 78h[5]).</td><td>RO</td><td>No</td><td>0</td></tr>
</table>

Register 13-88. 24Ch Target Link Width (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) ***(Cont.)***

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
11:8	**Port 1, 17, or 21 Target Link Width** Provides the capability to allow software to cause Link retraining to a wider or narrower width than the current width, *such as* to conserve power when maximum bandwidth is not required. Devices advertise such support, by transmitting the appropriate value for the Data Rate Identifier symbol within TS2 Ordered-Sets. Written with the Target Link width for the corresponding Port, to support Link Width Upconfiguration. The initial value of this field is the Port's Negotiated Link Width (offset 78h[25:20]).	RWS	No	Set by STRAP_STN*x*_PORTCFG*x* ball levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station x* bits (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 300h[11:8, 1:0])
14:12	***Reserved***	RsvdP	No	000b
15	**Port 1, 17, or 21 Upconfigure Capability Received** Set during Link training, if the corresponding Port received an Upconfigure Capability notification from the connected device. 0 = Device connected to the corresponding Port does not indicate that it is capable of Link Width Upconfiguration. 1 = Device connected to the corresponding Port indicates that it is capable of Link Width Upconfiguration. Software can cause the Port to either upconfigure the Link to a previously negotiated Link width, or downconfigure the Link to a narrower width, by writing the needed Target Link Width value to this register, followed by Setting the Port's **Link Control** register *Retrain Link* bit (offset 78h[5]).	RO	No	0

Register 13-88. 24Ch Target Link Width (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
18:16	**Port 2, 18, or 22 Target Link Width** Provides the capability to allow software to cause Link retraining to a wider or narrower width than the current width, *such as* to conserve power when maximum bandwidth is not required. Devices advertise such support, by transmitting the appropriate value for the Data Rate Identifier symbol within TS2 Ordered-Sets. Written with the Target Link width for the corresponding Port, to support Link Width Upconfiguration. The initial value of this field is the Port's Negotiated Link Width (offset 78h[25:20]).	RWS	No	Set by STRAP_STN*x*_PORTCFG*x* ball levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station x* bits (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 300h[11:8, 1:0])
22:19	***Reserved***	RsvdP	No	0h
23	**Port 2, 18, or 22 Upconfigure Capability Received** Set during Link training, if the corresponding Port received an Upconfigure Capability notification from the connected device. 0 = Device connected to the corresponding Port does not indicate that it is capable of Link Width Upconfiguration. 1 = Device connected to the corresponding Port indicates that it is capable of Link Width Upconfiguration. Software can cause the Port to either upconfigure the Link to a previously negotiated Link width, or downconfigure the Link to a narrower width, by writing the needed Target Link Width value to this register, followed by Setting the Port's **Link Control** register *Retrain Link* bit (offset 78h[5]).	RO	No	0

Register 13-88. 24Ch Target Link Width (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
26:24	**Port 3, 19, or 23 Target Link Width** Provides the capability to allow software to cause Link retraining to a wider or narrower width than the current width, *such as* to conserve power when maximum bandwidth is not required. Devices advertise such support, by transmitting the appropriate value for the Data Rate Identifier symbol within TS2 Ordered-Sets. Written with the Target Link width for the corresponding Port, to support Link Width Upconfiguration. The initial value of this field is the Port's Negotiated Link Width (offset 78h[25:20]).	RWS	No	Set by STRAP_STN*x*_PORTCFG*x* ball levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station x* bits (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 300h[11:8, 1:0])
30:27	***Reserved***	RsvdP	No	0h
31	**Port 3, 19, or 23 Upconfigure Capability Received** Set during Link training, if the corresponding Port received an Upconfigure Capability notification from the connected device. 0 = Device connected to the corresponding Port does not indicate that it is capable of Link Width Upconfiguration. 1 = Device connected to the corresponding Port indicates that it is capable of Link Width Upconfiguration. Software can cause the Port to either upconfigure the Link to a previously negotiated Link width, or downconfigure the Link to a narrower width, by writing the needed Target Link Width value to this register, followed by Setting the Port's **Link Control** register *Retrain Link* bit (offset 78h[5]).	RO	No	0

Register 13-89. 254h Physical Layer Additional Status/Control (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
This register provides additional PHY Status and Control bits. ***Note:*** *Bits [27:16, 7:0] – The Port 0 bits are for Ports 0, 1, 2, and 3. The Port 16 bits are for Ports 16, 17, 18, and 19. The Port 20 bits are for Ports 20, 21, 22, and 23.*					
0	**Port *x* Loopback Master Entry Failed** 1 = Indicates that the corresponding PEX 8649 Port failed to enter the *Loopback* state as a Loopback Master, and abandoned the attempt by returning the LTSSM to the *Detect* state ***Note:*** *If this bit and the Port's* ***Physical Layer Port Command*** *register Port x Ready as Loopback Master bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 230h[3, 7, 11, or 15]) are both Set, the Loopback state was entered after the initial failure from the Configuration state.*	0, 16, or 20	RW1C	Yes	0
1		1, 17, or 21	RW1C	Yes	0
2		2, 18, or 22	RW1C	Yes	0
3		3, 19, or 23	RW1C	Yes	0
4	**Port *x* Internal PIPE Interface PhyStatus Signal** Internal PHY Interface for the PCI Express architecture's (PIPE) Physical Layer Status (PhyStatus) signal state. When read, returns 1 if any of the PIPE interface PhyStatus signals that are mapped to the corresponding Port are asserted. This is useful for manually changing the Link speed when the corresponding PEX 8649 Port's *Hold Port x Quiet* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 234h[23:20]) is Set. When software is used to change the Link speed, it should poll PhyStatus for assertion, then de-assertion. After PhyStatus has de-asserted, the speed change is complete and test pattern transmission can begin.	0, 16, or 20	RO	No	0
5		1, 17, or 21	RO	No	0
6		2, 18, or 22	RO	No	0
7		3, 19, or 23	RO	No	0
14:8	**Received Modified Compliance Error Counter** Returns the value received in the Modified Compliance Pattern's *ERR* field, for the Lane(s) selected by the *Port x Received Modified Compliance Lane Select* bits **(**bits [27:24]) in this register.		RO	No	0-0h
15	**Received Modified Compliance Pattern Lock** 1 = Indicates that the Modified Compliance Pattern has been locked onto by the Lane(s) selected by the *Port x Received Modified Compliance Lane Select* bits **(**bits [27:24]) in this register.		RO	No	0

Register 13-89. 254h Physical Layer Additional Status/Control (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
16	**Port *x* External Loopback Enable** 1 = Allows the corresponding PEX 8649 Port to reach Link Up status, when receiving its own Training Sets during Link training. It is necessary to Set this bit when a Port's Receivers are directly connected, externally, to its Transmitters.	0, 16, or 20	RW	Yes	0
17		1, 17, or 21	RW	Yes	0
18		2, 18, or 22	RW	Yes	0
19		3, 19, or 23	RW	Yes	0
20	**Port *x* 2nd Receiver Detect Disable** 1 = Prevents the corresponding PEX 8649 Port from waiting 12 ms and Retrying the Receiver Detect operation, when Receivers are detected on a subset of Lanes after the first Receiver Detect operation. Instead, the LTSSM progresses to the *Polling* state, and operates only on the Lanes that detected Receivers.	0, 16, or 20	RWS	Yes	0
21		1, 17, or 21	RWS	Yes	0
22		2, 18, or 22	RWS	Yes	0
23		3, 19, or 23	RWS	Yes	0
24	**Port *x* Received Modified Compliance Lane Select** Selects which Lane receives the Modified Compliance Error Counter. Status is read from the *Received Modified Compliance Pattern Lock* bit and *Received Modified Compliance Error Counter* field **(**bits [15, 14:8], respectively) in this register.	0, 16, or 20	RW	Yes	0
25		1, 17, or 21	RW	Yes	0
26		2, 18, or 22	RW	Yes	0
27		3, 19, or 23	RW	Yes	0
28	***Factory Test Only***		RW	Yes	0
31:29	***Reserved***		RsvdP	No	000b

Register 13-90. 258h PRBS Control/Status (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
This register provides Control and Status of the PRBS Generator/Checker logic. ***Note:*** *Refer to Table 13-7 for the relationship between the Port 0, 16, or 20 parameters and SerDes modules and Lanes.*				
0	**PRBS Pattern Sync Status Device Lane 0, 32, or 16** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane’s PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
1	**PRBS Pattern Sync Status Device Lane 1, 33, or 17** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane’s PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
2	**PRBS Pattern Sync Status Device Lane 2, 34, or 18** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane’s PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
3	**PRBS Pattern Sync Status Device Lane 3, 35, or 19** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane’s PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0

Register 13-90. 258h PRBS Control/Status (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4	**PRBS Pattern Sync Status Device Lane 4, 36, or 20** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane’s PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
5	**PRBS Pattern Sync Status Device Lane 5, 37, or 21** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane’s PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
6	**PRBS Pattern Sync Status Device Lane 6, 38, or 22** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane’s PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
7	**PRBS Pattern Sync Status Device Lane 7, 39, or 23** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane’s PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0

Register 13-90. 258h PRBS Control/Status
(Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) ***(Cont.)***

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
8	**PRBS Pattern Sync Status Device Lane 8, 40, or 24** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane’s PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
9	**PRBS Pattern Sync Status Device Lane 9, 41, or 25** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane’s PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
10	**PRBS Pattern Sync Status Device Lane 10, 42, or 26** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane’s PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
11	**PRBS Pattern Sync Status Device Lane 11, 43, or 27** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane’s PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0

Register 13-90. 258h PRBS Control/Status (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
12	**PRBS Pattern Sync Status Device Lane 12, 44, or 28** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
13	**PRBS Pattern Sync Status Device Lane 13, 45, or 29** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
14	**PRBS Pattern Sync Status Device Lane 14, 46, or 30** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
15	**PRBS Pattern Sync Status Device Lane 15, 47, or 31** 0 = Causes the PRBS pattern generator, when enabled, to output the PRBS7 sequence 1 = Indicates that the corresponding Lane's PRBS Data Checker has synchronized to the incoming PRBS data pattern – the Receiver has acquired its first match on two sequentially received words	RO	No	0
16	**PRBS Pattern Invert Enable** 1 = Causes the PRBS pattern generator, when enabled, to transmit the one's complement of the selected PRBS data pattern	RW	Yes	0
31:17	***Reserved***	RsvdP	No	0-0h

Register 13-91. 25Ch Physical Layer Error Injection Control (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
This register provides 1-bit error injection control. ***Note:*** *The Port 0 bits are for Ports 0, 1, 2, and 3. The Port 16 bits are for Ports 16, 17, 18, and 19. The Port 20 bits are for Ports 20, 21, 22, and 23.*				
0	**Port 0, 16, or 20 1-Bit Error Injection Enable** 1 = One bit of a symbol being transmitted by the corresponding PEX 8649 Port is corrupted	RW	Yes	0
1	**Port 0, 16, or 20 1-Bit Error Injection Period** 0 = If error injection is enabled for the corresponding PEX 8649 Port, error injection occurs once every 1 µs 1 = If error injection is enabled for the corresponding PEX 8649 Port, error injection occurs once every 1 ms	RW	Yes	0
3:2	***Reserved***	RsvdP	No	00b
4	**Port 1, 17, or 21 1-Bit Error Injection Enable** 1 = One bit of a symbol being transmitted by the corresponding PEX 8649 Port is corrupted	RW	Yes	0
5	**Port 1, 17, or 21 1-Bit Error Injection Period** 0 = If error injection is enabled for the corresponding PEX 8649 Port, error injection occurs once every 1 µs 1 = If error injection is enabled for the corresponding PEX 8649 Port, error injection occurs once every 1 ms	RW	Yes	0
7:6	***Reserved***	RsvdP	No	00b
8	**Port 2, 18, or 22 1-Bit Error Injection Enable** 1 = One bit of a symbol being transmitted by the corresponding PEX 8649 Port is corrupted	RW	Yes	0
9	**Port 2, 18, or 22 1-Bit Error Injection Period** 0 = If error injection is enabled for the corresponding PEX 8649 Port, error injection occurs once every 1 µs 1 = If error injection is enabled for the corresponding PEX 8649 Port, error injection occurs once every 1 ms	RW	Yes	0
11:10	***Reserved***	RsvdP	No	00b
12	**Port 3, 19, or 23 1-Bit Error Injection Enable** 1 = One bit of a symbol being transmitted by the corresponding PEX 8649 Port is corrupted	RW	Yes	0
13	**Port 3, 19, or 23 1-Bit Error Injection Period** 0 = If error injection is enabled for the corresponding PEX 8649 Port, error injection occurs once every 1 µs 1 = If error injection is enabled for the corresponding PEX 8649 Port, error injection occurs once every 1 ms	RW	Yes	0
15:14	***Reserved***	RsvdP	No	00b
31:16	***Reserved***	RsvdP	No	0000h

13.15.4 Device-Specific Registers – Serial EEPROM (Offsets 260h – 26Ch)

This section details the Device-Specific Serial EEPROM registers. Table 13-23 defines the register map.

Table 13-23. Device-Specific Serial EEPROM Register Map (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then these registers exist in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Status Data from Serial EEPROM	Serial EEPROM Status	Serial EEPROM Control		260h
Serial EEPROM Buffer				264h
Serial EEPROM Clock Frequency				268h
Expansion ROM Base Address		***Reserved***	Serial EEPROM 3rd Address Byte	26Ch

Register 13-92. 260h Serial EEPROM Status and Control (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then these registers exist in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	Serial EEPROM Control			
12:0	**EepBlkAddr** Serial EEPROM Block Address for 32 KB.	RW	Yes	000h
15:13	**EepCmd[2:0]** Commands to the Serial EEPROM Controller. 000b = ***Reserved*** 001b = Data from bits [31:24] (**Status Data from Serial EEPROM** register) is written to the serial EEPROM's internal **Status** register 010b = Write four bytes of data from the *EepBuf* into the memory location pointed to by the *EepBlkAddr* field 011b = Read four bytes of data from the memory location pointed to by the *EepBlkAddr* field into the *EepBuf* 100b = Reset Write Enable latch 101b = Data from the serial EEPROM's internal **Status** register is written to bits [31:24] (**Status Data from Serial EEPROM** register) 110b = Set Write Enable latch 111b = ***Reserved*** ***Note:*** *For value of 001b, only bits [31, 27:26] can be written into the serial EEPROM's internal* ***Status*** *register.*	RW	Yes	000b

Register 13-92. 260h Serial EEPROM Status and Control (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then these registers exist in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
	Serial EEPROM Status			
17:16	**EepPrsnt[1:0]** Serial EEPROM Present status. 00b = Not present 01b = Serial EEPROM is present – validation signature verified 10b = ***Reserved*** 11b = Serial EEPROM is present – validation signature not verified	RO	No	00b
18	**EepCmdStatus** Serial EEPROM Command status. 0 = Serial EEPROM Command is complete 1 = Serial EEPROM Command is not complete	RO	No	0
19	***Reserved***	RsvdP	No	0
20	**EepBlkAddr Upper Bit** Serial EEPROM Block Address upper bit 13. Extends the serial EEPROM to 64 KB.	RW	Yes	0
21	**EepAddrWidth Override** 0 = Field [23:22] (*EepAddrWidth*) is RO 1 = Field [23:22] (*EepAddrWidth*) is software-writable	RW	Yes	0
23:22	**EepAddrWidth** Serial EEPROM Address width. If the addressing width cannot be determined, 00b is returned. A non-zero value is reported only if the validation signature (5Ah) is successfully read from the first serial EEPROM location. This field is usually RO; however, it is RW if bit 21 (*EepAddrWidth Override*) is Set. 00b = Undetermined 01b = 1 byte 10b = 2 bytes 11b = 3 bytes	RO/RW	No	00b

Register 13-92. 260h Serial EEPROM Status and Control (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then these registers exist in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I²C</th><th>Default</th></tr>
<tr><td colspan="5">Status Data from Serial EEPROM[a]</td></tr>
<tr><td>24</td><td><b>EepRdy</b>
Serial EEPROM RDY#.
0 = Serial EEPROM is ready to transmit data
1 = Write cycle is in-progress</td><td>RW</td><td>Yes</td><td>0</td></tr>
<tr><td>25</td><td><b>EepWen</b>
Serial EEPROM Write Enable.
0 = Serial EEPROM Write is disabled
1 = Serial EEPROM Write is enabled</td><td>RW</td><td>Yes</td><td>0</td></tr>
<tr><td>27:26</td><td><b>EepBp[1:0]</b>
Serial EEPROM Block-Write Protect bits. Block Protection options protect the top ¼, top ½, or the entire serial EEPROM. PEX 8649 Configuration data is stored in the lower addresses; therefore, when using Block Protection, the entire serial EEPROM should be protected with BP[1:0]=11b.
<table>
<tr><th rowspan="2">BP[1:0]</th><th rowspan="2">Level</th><th colspan="4">Array Addresses Protected</th></tr>
<tr><th>8-KB Device</th><th>16-KB Device</th><th>32-KB Device</th><th>64-KB Device</th></tr>
<tr><td>00b</td><td>0</td><td>None</td><td>None</td><td>None</td><td>None</td></tr>
<tr><td>01b</td><td>1
(top ¼)</td><td>1800h – 1FFFh</td><td>3000h – 3FFFh</td><td>6000h – 7FFFh</td><td>–</td></tr>
<tr><td>10b</td><td>2
(top ½)</td><td>1000h – 1FFFh</td><td>2000h – 3FFFh</td><td>4000h – 7FFFh</td><td>–</td></tr>
<tr><td>11b</td><td>3
(All)</td><td>0000h – 1FFFh</td><td>0000h – 3FFFh</td><td>0000h – 7FFFh</td><td>–</td></tr>
</table></td><td>RW</td><td>Yes</td><td>00b</td></tr>
</table>

Register 13-92. 260h Serial EEPROM Status and Control (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then these registers exist in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
30:28	**EepWrStatus** Serial EEPROM Write status. Value is 000b when the serial EEPROM is not in an internal Write cycle. ***Note:*** *Definition of this field varies among serial EEPROM manufacturers. Reads of the serial EEPROM's internal* ***Status*** *register can return 000b or 111b, depending upon the serial EEPROM that is used.*	RW	No	000b
31	**EepWpen** Serial EEPROM Write Protect Enable. Overrides the internal serial EEPROM Write Protect WP# input and enables/disables Writes to the **Serial EEPROM Status** register: • When WP# is High or *EepWpen* = 0, and *EepWen* = 1, the **Serial EEPROM Status** register is writable • When WP# is Low and *EepWpen* = 1, or *EepWen* = 0, the **Serial EEPROM Status** register is protected ***Notes:*** *If the internal serial EEPROM Write Protect WP# input is Low, after software Sets the EepWen bit to write-protect the* ***Serial EEPROM Status*** *register, the EepWen value cannot be changed to 0, nor can the EepBp[1:0] field be Cleared to disable Block Protection, until WP# is High.* *This bit is* ***not*** *implemented in certain serial EEPROMs. Refer to the serial EEPROM manufacturer's data sheet.*	RW	Yes	0

a. *Within the serial EEPROM's internal* ***Status*** *register, only bits [31, 27:26] can be written.*

Register 13-93. 264h Serial EEPROM Buffer (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then these registers exist in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**EepBuf** Serial EEPROM RW buffer. Read/Write command to the **Serial EEPROM Control** register (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then these registers exist in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 260h) results in a 4-byte Read/Write from/to the serial EEPROM device.	RW	Yes	0000_0000h

Register 13-94. 268h Serial EEPROM Clock Frequency (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then these registers exist in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
2:0	**EepFreq[2:0]** Serial EEPROM clock (EE_SK) frequency control. 000b = 1 MHz (default) 001b = 1.98 MHz 010b = 5 MHz 011b = 9.62 MHz 100b = 12.5 MHz 101b = 15.6 MHz 110b = 17.86 MHz 111b = ***Reserved***	RW	Yes	000b
7:3	***Reserved***	RsvdP	No	0-0h
10:8	**EepCsStHld[2:0]** CS to SCLK setup and hold timing, provided as a number of ½ EE_SK Clock cycles. 000b = Use default timing for EE_CS# setup and EE_CS# hold timing to the serial EEPROM, for EE_CS# active to EE_SK active delay, and EE_SK inactive to EE_CS# inactive delay, respectively 001b = Non-zero value adds that number of ½ EE_SK clocks delay to the default setup and hold timing, between EE_CS# active and EE_SK active, and between EE_SK inactive and EE_CS# inactive	RW	Yes	000b
15:11	***Reserved***	RsvdP	No	0-0h
16	**Expansion ROM Size** 0 = 16 KB 1 = 32 KB	RW	Yes	0
31:17	***Reserved***	RsvdP	No	0-0h

Register 13-95. 26Ch Serial EEPROM 3rd Address Byte (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then these registers exist in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
7:0	**Serial EEPROM 3rd Address Byte**	RW	Yes	00h
15:8	***Reserved***	RsvdP	No	00h
31:16	**Expansion ROM Base Address** Expansion ROM Base address within the serial EEPROM. Value is dependent upon the **Serial EEPROM Clock Frequency** register *Expansion ROM Size* bit (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 268h[16]) value. The lower six bits, [21:16], map to serial EEPROM byte Address bits [15:10] (aligned to a 256-DWord (1-KB) boundary). The Expansion ROM must not straddle a 64-KB boundary within the serial EEPROM. 0020h = Default Base address in serial EEPROM for a 16-KB Expansion ROM (*Expansion ROM Size* bit is Cleared) is 2000h (8 KB). The serial EEPROM size must be at least 32 KB. 0040h = Default Base address in serial EEPROM for 32-KB Expansion ROM (*Expansion ROM Size* bit is Set) is 4000h (16 KB). The serial EEPROM size must be at least 64 KB.	RW	Yes	20h

13.15.5 Device-Specific Registers – I^{2}C and SMBus Slave Interfaces (Offsets 290h – 2FCh)

This section details the Device-Specific I^{2}C and SMBus Slave Interface registers. Table 13-24 defines the register map.

The I^{2}C and SMBus Slave Interfaces are described, in detail, in Chapter 7, “I^{2}C/SMBus Slave Interface Operation.”

Table 13-24. Device-Specific I^{2}C and SMBus Slave Interfaces Register Map (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Factory Test Only	290h
I^{2}C Configuration	294h
Factory Test Only	298h – 2C4h
SMBus Configuration	2C8h
Reserved	2CCh – 2FCh

Register 13-96. 294h I^{2}C Configuration (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default	
2:0	**Slave Address** Bits [6:0] comprise the I^{2}C/SMBus Slave address, 1Fh. The value is determined by bits [2:0] (which reflect the I2C_ADDR[2:0] ball states, and default to 111b, by virtue of weak internal pull-up resistors), combined with the value of bits [6:3] (which default to 0011b). When I2C_ADDR2=H, Address Resolution Protocol (ARP) is disabled ***and*** bit 2 defaults to a value of 1. ***Note: The I^{2}C/SMBus Slave address must not be changed by an I^{2}C/SMBus Write command.***	HwInit	Yes	111b	1Fh
6:3		RWS	Yes	0011b	
9:7	***Reserved***	RsvdP	No	000b	
10	***Factory Test Only***	RWS	Yes	0	
30:11	***Reserved***	RWS	Yes	0-0h	
31	***Factory Test Only***	RW	No	0	

Register 13-97. 2C8h SMBus Configuration (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**SMBus Enable** Initially loaded from the STRAP_SMBUS_EN# input state. Value can later be changed by serial EEPROM or Configuration Space register Read Write. 0 = Disables SMBus for device configuration (I^2C mode is enabled) 1 = Enables SMBus for device configuration (SMBus mode is enabled)	RWS	Yes	0 (STRAP_SMBUS_EN#=H) 1 (STRAP_SMBUS_EN#=L)
7:1	**SMBus Device Address** Set by the Address Resolution Protocol (ARP), if the ARP is enabled. If the ARP is disabled through I2C_ADDR2=H, defaults to 1Bh, with Address bits [1:0] values loaded from the I2C_ADDR[1:0] inputs.	RWS	Yes	00h (I2C_ADDR2=L) 1Bh (I2C_ADDR2=H)
8	**ARP Disable** 0 = Device under test is able to respond to ARP commands 1 = Device under test is unable to respond to ARP commands	RWS	Yes	0 (I2C_ADDR2=L) 1 (I2C_ADDR2=H)
9	**PEC Check Disable** 0 = Enable PEC checking on all packets 1 = Disables Packet Error Checks (PECs) checking on all packets; packets with the wrong PECs are accepted	RWS	Yes	0
10	**AV Flag** Address Valid (AV) flag. Set, by default, when ARP is disabled (I2C_ADDR2=H).	RWS	Yes	0 (I2C_ADDR2=L) 1 (I2C_ADDR2=H)
11	**AR Flag** Address Resolved (AR) flag.	RWS	Yes	0
13:12	**UDID Address Type** Unique Device Identifier (UDID) Address type. 00b = I2C_ADDR2=H (ARP is disabled) 10b = I2C_ADDR2=L (ARP is enabled) All other encodings are ***reserved***.	RWS	Yes	00b (I2C_ADDR2=H) 10b (I2C_ADDR2=L)
14	**UDID PEC Support** 1 = Sets the *PEC Support* bit in the UDID	RWS	Yes	1
15	**SMBus Parameter Reload** Set this bit if bits [10, 8, or 7:1] (*AV Flag*, *ARP Disable*, or *SMBus Device Address*, respectively) are changed after a serial EEPROM load. Effective only when bit 28 (*SMBus Command In-Progress*) is Cleared.	RO	No	0

Register 13-97. 2C8h SMBus Configuration (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
23:16	**UDID Vendor-Specific ID** Sets the MSB of the UDID Vendor-Specific ID. Bits [23:20] of this field are Set by the I2C_ADDR[1:0] inputs. The four combinations provide the following ID values: 00b = 7000_0000h 01b = B000_0000h 10b = D000_0000h 11b = E000_0000h	RWS	Yes	Set by I2C_ADDR[1:0] ball levels
26:24	**UDID Revision ID** Programmed to 001b for Silicon Revision AA.	RWS	Yes	001b
27	***Factory Test Only***	RWS	Yes	0
28	**SMBus Command In-Progress** 0 = SMBus state machine is idle 1 = SMBus state machine is active (not idle)	RO	No	0
29	**PEC Check Failed** 0 = PEC check successfully completed when receiving a packet 1 = PEC check failed when receiving a packet	RW1C	No	0
30	**Unsupported SMBus Command** 0 = Command received from SMBus is a supported command 1 = Command received from SMBus is an unsupported command	RW1C	No	0
31	**SMBus Error Detected** 0 = No error detected in STOP condition (as generated by the SMBus Master, to terminate the Data transfer) 1 = STOP detected was not on a byte boundary	RW1C	Yes	0

13.15.6 Device-Specific Registers – Port Configuration (Offsets 300h – 31Ch)

This section details the Device-Specific Port Configuration registers located at offsets 300h through 31Ch. Table 13-25 defines the register map.

Other Device-Specific Port Configuration registers are detailed in Section 13.15.8, "Device-Specific Registers – Port Configuration (Offsets 354h – 3ACh)."

Table 13-25. Device-Specific Port Configuration Register Map (Offsets 300h – 31Ch) (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then these registers exist in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Port Configuration			300h
Reserved	x1 Port Configuration		304h
Reserved	x2 Port Configuration	***Reserved***	308h
Reserved			30Ch
Factory Test Only			310h
Clock Enable			314h
Reserved			318h
Factory Test Only			31Ch

Register 13-98. 300h Port Configuration (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Note: *Table 13-5 lists the Port configuration for each Station.*				
1:0	**Port Configuration for Station 0** Port Configuration Link width, per Port, for Station 0. The serial EEPROM bit values always override the STRAP_STN0_PORTCFG[1:0] Strapping inputs (if the serial EEPROM values are loaded; refer to Table 13-5). This register is reset only by a Fundamental Reset (PEX_PERST# and/or VS*x*_PERST# assertion). 00b = x4, x4, x4, x4 01b = x16 10b = x8, x8 11b = x8, x4, x4	RO	Yes	Set by STRAP_STN0_PORTCFG[1:0] input levels
7:2	***Reserved***	RsvdP	No	0-0h
9:8	**Port Configuration for Station 4** Port Configuration Link width, per Port, for Station 4. The serial EEPROM bit values always override the STRAP_STN4_PORTCFG[1:0] Strapping inputs (if the serial EEPROM values are loaded; refer to Table 13-5). This register is reset only by a Fundamental Reset (PEX_PERST# and/or VS*x*_PERST# assertion). 00b = x4, x4, x4, x4 01b = x16 10b = x8, x8 11b = x8, x4, x4	RO	Yes	Set by STRAP_STN4_PORTCFG[1:0] input levels
11:10	**Port Configuration for Station 5** Port Configuration Link width, per Port, for Station 5. The serial EEPROM bit values always override the STRAP_STN5_PORTCFG[1:0] Strapping inputs (if the serial EEPROM values are loaded; refer to Table 13-5). This register is reset only by a Fundamental Reset (PEX_PERST# and/or VS*x*_PERST# assertion). 00b = x4, x4, x4, x4 01b = x16 10b = x8, x8 11b = x8, x4, x4	RO	Yes	Set by STRAP_STN5_PORTCFG[1:0] input levels
31:12	***Reserved***	RsvdP	No	0000_0h

Register 13-99. 304h x1 Port Configuration (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Forces the corresponding Port to linkup with a x1 negotiated Link width, regardless of the quantity of Lanes connected to the Port.				
3:0	**x1 Only for Station 0** 0000b = Indicates that none of the Ports are configured as x1 only, and x1 operation is allowed XXX1b = Indicates that Port 0 is configured as x1 only XX1Xb = Indicates that Port 1 is configured as x1 only X1XXb = Indicates that Port 2 is configured as x1 only 1XXXb = Indicates that Port 3 is configured as x1 only ***Note:*** *"X" is "Don't Care."*	RO	Yes	0000b
15:4	***Reserved***	RsvdP	No	000h
19:16	**x1 Only for Station 4** 0000b = Indicates that none of the Ports are configured as x1 only, and x1 operation is allowed XXX1b = Indicates that Port 16 is configured as x1 only XX1Xb = Indicates that Port 17 is configured as x1 only X1XXb = Indicates that Port 18 is configured as x1 only 1XXXb = Indicates that Port 19 is configured as x1 only ***Note:*** *"X" is "Don't Care."*	RO	Yes	0000b
23:20	**x1 Only for Station 5** 0000b = Indicates that none of the Ports are configured as x1 only, and x1 operation is allowed XXX1b = Indicates that Port 20 is configured as x1 only XX1Xb = Indicates that Port 21 is configured as x1 only X1XXb = Indicates that Port 22 is configured as x1 only 1XXXb = Indicates that Port 23 is configured as x1 only ***Note:*** *"X" is "Don't Care."*	RO	Yes	0000b
31:24	***Reserved***	RsvdP	No	00h

Register 13-100. 308h x2 Port Configuration (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Forces the corresponding Port to linkup with a x2 negotiated Link width, regardless of the quantity of Lanes connected to the Port.				
15:0	***Reserved***	RsvdP	No	0000h
19:16	**x2 Only for Station 4** 0000b = Indicates that none of the Ports are configured as x2 only, and x2 operation is allowed XXX1b = Indicates that Port 16 is configured as x2 only XX1Xb = Indicates that Port 17 is configured as x2 only X1XXb = Indicates that Port 18 is configured as x2 only 1XXXb = Indicates that Port 19 is configured as x2 only ***Note:*** *"X" is "Don't Care."*	RO	Yes	0000b
23:20	**x2 Only for Station 5** 0000b = Indicates that none of the Ports are configured as x2 only, and x2 operation is allowed XXX1b = Indicates that Port 20 is configured as x2 only XX1Xb = Indicates that Port 21 is configured as x2 only X1XXb = Indicates that Port 22 is configured as x2 only 1XXXb = Indicates that Port 23 is configured as x2 only ***Note:*** *"X" is "Don't Care."*	RO	Yes	0000b
31:24	***Reserved***	RsvdP	No	00h

Register 13-101. 314h Clock Enable (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Ports and Stations are automatically enabled, according to the Port configuration defined by the STRAP_STN*x*_PORTCFG*x* signals, which can be overridden by programming the **Port Configuration** register *Port Configuration for Station x* bits (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then these registers exist in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 300h[11:8, 1:0]). An enabled Port can be selectively disabled, however, by Clearing the Port's *Port x Clock Enable* bit in this register. Port 0 must always remain enabled, and Ports 16 and 20 (containing Station registers) must remain enabled, if other Ports in the respective Stations are enabled. ***Note:*** *It is not possible to enable more Ports than the maximum specified for the device.*				
0	**Port 0 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	1
1	**Port 1 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	Set by STRAP_STN0_PORTCFG[1:0] input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 0* field (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 300h[1:0])
2	**Port 2 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	
3	**Port 3 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	
15:4	***Reserved***	RsvdP	No	000h

Register 13-101. 314h Clock Enable (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
16	**Port 16 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	1
17	**Port 17 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	Set by STRAP_STN4_PORTCFG[1:0] input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 4* field (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 300h[9:8])
18	**Port 18 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	
19	**Port 19 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	
20	**Port 20 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	1
21	**Port 21 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	Set by STRAP_STN5_PORTCFG[1:0] input levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 5* field (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 300h[11:10])
22	**Port 22 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	
23	**Port 23 Clock Enable** 0 = Disables 1 = Enables	RWS	Yes	
26:24	***Reserved***	RsvdP	No	000b
27	**Station 4 Root Clock Enable**	RWS	Yes	1
28	**Station 5 Root Clock Enable**	RWS	Yes	1
31:29	***Reserved***	RsvdP	No	000b

13.15.7 Device-Specific Registers – Error Checking and Debug (Offsets 320h – 350h)

This section details Device-Specific Error Checking and Debug registers at offsets 320h through 350h. Table 13-26 defines the register map.

Other Device-Specific Error Checking and Debug registers are detailed in:

- Section 13.15.10, "Device-Specific Registers – Error Checking and Debug (Offsets 700h – 75Ch)"
- Section 13.19.3, "Device-Specific Registers – Error Checking and Debug (Offsets F70h – FB0h)"

Table 13-26. Device-Specific Error Checking and Debug Register Map (Offsets 320h – 350h) (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then these registers exist in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

<table>
<tr><th colspan="2">31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16</th><th colspan="2">15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th><th></th></tr>
<tr><td colspan="4"><em><strong>Factory Test Only</strong></em></td><td>320h – 328h</td></tr>
<tr><td colspan="4"><em><strong>Reserved</strong></em></td><td>32Ch</td></tr>
<tr><td colspan="2"><em><strong>Reserved</strong></em></td><td colspan="2">Station 0 Lane Status</td><td>330h</td></tr>
<tr><td colspan="4"><em><strong>Reserved</strong></em></td><td>334h</td></tr>
<tr><td colspan="4">Station 4/5 Lane Status</td><td>338h</td></tr>
<tr><td colspan="4"><em><strong>Reserved</strong></em></td><td>33Ch</td></tr>
<tr><td colspan="4"><em><strong>Factory Test Only</strong></em></td><td>340h – 344h</td></tr>
<tr><td colspan="4"><em><strong>Reserved</strong></em></td><td>348h – 34Ch</td></tr>
<tr><td><em><strong>Factory Test Only/Reserved</strong></em></td><td colspan="2">Debug Control</td><td><em><strong>Factory Test Only/Reserved</strong></em></td><td>350h</td></tr>
</table>

Notes: *In this section, the term "SerDes quad" or "quad" refers to assembling SerDes modules into groups of four contiguous Lanes for testing purposes.*

The Station register Port Numbers – Ports 0, 16, and 20 – are listed in addition to the individual Ports within the Station. Table 13-7 defines the Station, Station register Port Number, physical Port, physical Lane and SerDes module, and SerDes quad relationships, when all Ports are enabled.

Register 13-102. 330h Station 0 Lane Status (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
Note: *Table 13-7 defines the Port/Physical Lane/SerDes Module/Station to SerDes quad relationship.*				
0	**Lane 0 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
1	**Lane 1 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
2	**Lane 2 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
3	**Lane 3 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
4	**Lane 4 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
5	**Lane 5 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
6	**Lane 6 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
7	**Lane 7 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
8	**Lane 8 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
9	**Lane 9 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
10	**Lane 10 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
11	**Lane 11 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1

Register 13-102. 330h Station 0 Lane Status (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
12	**Lane 12 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
13	**Lane 13 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
14	**Lane 14 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
15	**Lane 15 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
31:16	***Reserved***	RsvdP	Yes	0000h

Register 13-103. 338h Station 4/5 Lane Status (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Note: *Table 13-7 defines the Port/Physical Lane/SerDes Module/Station to SerDes Quad relationship.*				
0	**Lane 32 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
1	**Lane 33 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
2	**Lane 34 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
3	**Lane 35 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
4	**Lane 36 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
5	**Lane 37 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
6	**Lane 38 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
7	**Lane 39 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
8	**Lane 40 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
9	**Lane 41 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
10	**Lane 42 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
11	**Lane 43 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1

Register 13-103. 338h Station 4/5 Lane Status (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
12	**Lane 44 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
13	**Lane 45 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
14	**Lane 46 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
15	**Lane 47 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
16	**Lane 16 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
17	**Lane 17 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
18	**Lane 18 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
19	**Lane 19 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
20	**Lane 20 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
21	**Lane 21 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
22	**Lane 22 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
23	**Lane 23 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1

Register 13-103. 338h Station 4/5 Lane Status (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
24	**Lane 24 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
25	**Lane 25 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
26	**Lane 26 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
27	**Lane 27 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
28	**Lane 28 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
29	**Lane 29 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
30	**Lane 30 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1
31	**Lane 31 Up Status** 0 = Lane is down 1 = Lane is up	RWS	Yes	1

Register 13-104. 350h Debug Control (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
Note: *If this register is programmed by the serial EEPROM, it must be the first serial EEPROM entry, at locations 4h through 9h, as listed in Table 6-1, "Serial EEPROM Data." If Port 0 is the Legacy NT Port, this register is loaded from the NT Port Virtual Interface register offset 350h location in the serial EEPROM.*				
3:0	***Factory Test Only***	RO	No	Fh
7:4	***Reserved***	RsvdP	No	0h
8	***Factory Test Only***	RWS	Yes	1
9	**Hardware/Software Configuration Mode Control** Allows software to configure which Port(s) is (are) the upstream Port(s), as well as which Port is the NT Port. 0 = Upstream Port(s) and NT Port selection by the STRAP_UPSTRM_PORTSEL[3:0] and STRAP_NT_UPSTRM_PORTSEL[4, 2:0] balls, respectively, which can be overridden by the serial EEPROM and/or I^{2}C Configuration mechanism. Cannot be changed by in-band software at runtime. 1 = In-band software can change which Port(s) is (are) is configured to be the upstream Port(s) and NT Port. The **Virtual Switch Debug** register *Upstream Port and NT-Link Port DL_Down Reset Propagation Disable* bit (Upstream Port(s), offset A30h[4]) must be Cleared.	RWS	Yes	0
10	***Factory Test Only***	RWS	Yes	0
11	**Cut-Thru Enable** 0 = Disables Cut-Thru support 1 = Enables Cut-Thru support	RWS	Yes	1

Register 13-104. 350h Debug Control (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
13:12	***Factory Test Only***	RWS	Yes	00b
14	**Base Mode** **NT P2P Enable** Reflects the STRAP_NT_P2P_EN# input state. This bit and its corresponding signal must ***not*** be toggled at runtime. 0 = NT PCI-to-PCI bridge mode is disabled (STRAP_NT_P2P_EN#=H) (Legacy NT mode is enabled) 1 = NT PCI-to-PCI bridge mode is enabled (STRAP_NT_P2P_EN#=L)	RWS	Yes	0 (STRAP_NT_P2P_EN#=H) 1 (STRAP_NT_P2P_EN#=L)
	Virtual Switch Mode ***Reserved***	RsvdP	No	0
21:15	***Factory Test Only***	RWS	Yes	0-0h
22	**Base Switch Mode** ***Reserved***	RsvdP	No	0
	Virtual Switch Mode **Port Reset EEP Load** 1 = Causes a serial EEPROM reload after the **Port Reset** register *Reset Port x Vector* bit(s) that corresponds to the Transparent downstream Port(s) (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 3A0h[23:16, 3:0]) is toggled from 1 to 0	RWS	Yes	0
23	***Reserved***	RsvdP	No	0
26:24	***Factory Test Only***	RWS	Yes	000b
31:27	***Reserved***	RsvdP	No	0-0h

13.15.8 Device-Specific Registers – Port Configuration (Offsets 354h – 3ACh)

This section details the Device-Specific Port Configuration registers located at offsets 354h through 3ACh. In particular, these registers are related to the Management Port and Virtual Switches. Table 13-27 defines the register map.

Additional information regarding programming of the Virtual Switch Table, as it relates to these registers, is provided in Section 5.5.3.2, "Virtual Switch Table Programming Sequence."

Other Device-Specific Port Configuration registers are detailed in Section 13.15.6, "Device-Specific Registers – Port Configuration (Offsets 300h – 31Ch)."

Table 13-27. Device-Specific Port Configuration Register Map (Offsets 354h – 3ACh)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved (Base Mode) Management Port Control (Virtual Switch Mode)				354h
Reserved			Virtual Switch Enable	358h
Reserved				35Ch
VS0 Upstream				360h
Reserved (Base Mode) VS1 Upstream (Virtual Switch Mode)				364h
Reserved (Base Mode) VS2 Upstream (Virtual Switch Mode)				368h
Reserved (Base Mode) VS3 Upstream (Virtual Switch Mode)				36Ch
Reserved				370h – 37Ch
Reserved	VS0 Port Vector			380h
Reserved	***Reserved*** (Base Mode) VS1 Port Vector (Virtual Switch Mode)			384h
Reserved	***Reserved*** (Base Mode) VS2 Port Vector (Virtual Switch Mode)			388h
Reserved	***Reserved*** (Base Mode) VS3 Port Vector (Virtual Switch Mode)			38Ch
Reserved				390h – 39Ch
Reserved	Port Reset			3A0h
Reserved	Parallel Hot Plug Control		***Reserved***	3A4h
Reserved		***Reserved*** (Base Mode) VSx_PERST# Status (Virtual Switch Mode)		3A8h
Configuration Release				3ACh

Register 13-105. 354h Management Port Control (Virtual Switch mode – Port 0, accessible through the Management Port and Redundant Management Port)

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I²C</th><th>Default</th></tr>
<tr><td colspan="5">This register can be accessed by Management-capable Ports (Active and Redundant Management Ports), Strapping balls, or the I²C Bus. The <b><i>reserved</i></b> register bits return zeros (0) during Reads. Writes to <b><i>reserved</i></b> register bits do not affect the register.
This register, in combination with the <b>VS<i>x</i> Upstream</b> and <b>VS<i>x</i> Port Vector</b> registers (offsets 360h through 36Ch, and 380h through 38Ch, respectively), comprises the Virtual Switch Table. For further details, refer to Section 5.5.3, “Virtual Switch Table.”</td></tr>
<tr><td>4, 2:0</td><td><b>Active Management Port</b>
Indicates the Port Number of the Active Management Port. The value of this field is latched in, upon reset de-assertion, from the STRAP_UPSTRM_PORTSEL[3:0] inputs, respectively. The upper two bits [4, 2] of this field map to STRAP_UPSTRM_PORTSEL[3:2], to select the Station, and the lower two bits [1:0] map to STRAP_UPSTRM_PORTSEL[1:0], to select the Port within that Station.
<table>
<tr><th>Field Value</th><th>Strapping Ball Value</th><th>Port Number</th></tr>
<tr><td>0h</td><td>0000b (LLLL)</td><td>0</td></tr>
<tr><td>1h</td><td>0001b (LLLH)</td><td>1</td></tr>
<tr><td>2h</td><td>0010b (LLHL)</td><td>2</td></tr>
<tr><td>3h</td><td>0011b (LLHH)</td><td>3</td></tr>
<tr><td>4h</td><td>0100b (LHLL)</td><td>16</td></tr>
<tr><td>5h</td><td>0101b (LHLH)</td><td>17</td></tr>
<tr><td>6h</td><td>0110b (LHHL)</td><td>18</td></tr>
<tr><td>7h</td><td>0111b (LHHH)</td><td>19</td></tr>
<tr><td>8h</td><td>1000b (HLLL)</td><td>20</td></tr>
<tr><td>9h</td><td>1001b (HLLH)</td><td>21</td></tr>
<tr><td>Ah</td><td>1010b (HLHL)</td><td>22</td></tr>
<tr><td>Bh</td><td>1011b (HLHH)</td><td>23</td></tr>
</table>
All other encodings are <b><i>reserved</i></b>.</td><td>RWS</td><td>Yes</td><td>Port Number Set by STRAP_UPSTRM_PORTSEL[3:0] input levels</td></tr>
<tr><td>3</td><td><b><i>Not used, internally tied Low. Must be 0.</i></b></td><td>RsvdP</td><td>Yes</td><td>0</td></tr>
<tr><td>5</td><td><b>Active Management Port Enable</b>
Enables the Active Management Port. The value of this bit is latched in, upon reset de-assertion, from the STRAP_NT_ENABLE# input.
0 = STRAP_NT_ENABLE#=H
1 = STRAP_NT_ENABLE#=L</td><td>RWS</td><td>Yes</td><td>Set by STRAP_NT_ENABLE# input level</td></tr>
</table>

Register 13-105. 354h Management Port Control (Virtual Switch mode – Port 0, accessible through the Management Port and Redundant Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
6	**Active Management Port EEPROM Load on Hot Reset for Chip and Station Registers Enable** ***Valid only for the Management Port.*** After the Management Port receives a Hot Reset or DL_Down condition, the serial EEPROM reloads registers, as described below. 0 = Serial EEPROM reloads Management Port Port-specific registers (default) 1 = Serial EEPROM reloads: • Chip-specific registers (might affect all virtual switches), • Station-specific registers for the Station that contains the Management Port (might affect other virtual switches in that Station), and, • Management Port Port-specific registers	RWS	Yes	0
7	***Reserved***	RsvdP	No	0
12, 10:8	**Redundant Management Port** Indicates the Port Number of the Redundant Management Port. 0h = Port 0 (default) 6h = Port 18 1h = Port 1 7h = Port 19 2h = Port 2 8h = Port 20 3h = Port 3 9h = Port 21 4h = Port 16 Ah = Port 22 5h = Port 17 Bh = Port 23	RWS	Yes	0h
11	***Reserved***	RsvdP	No	0
13	**Redundant Management Port Enable** Enables the Redundant Management Port.	RWS	Yes	0
31:14	***Reserved***	RsvdP	No	0-0h

Register 13-106. 358h Virtual Switch Enable (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then these registers exist in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register indicates which virtual switches are enabled. The initial value of this register corresponds to the Setting of the STRAP_VS_MODE[1:0] inputs. *For example*, if STRAP_VS_MODE[1:0]=HH, bits [3:0] are programmed to 1111b – both indicate that the first four virtual switches are enabled. Table 13-6 lists the default upstream and downstream Port assignments of each virtual switch. In Virtual Switch mode (STRAP_VS_MODE[1:0] not equal to 00b), this register can be programmed to enable or disable virtual switches, prior to linkup, using any of the following methods: • Serial EEPROM, • I^2C, if STRAP_I2C_CFG_EN#=L, followed by an I^2C Write that Sets the **Configuration Release** register *Initiate Configuration* bit (Port 0, offset 3ACh[0]), • Software, followed by a Hot Reset. ***Note:*** *For Base mode, the STRAP_VS_MODE[1:0] inputs must be Low. For Virtual Switch mode, the STRAP_VS_MODE[1:0] inputs must be strapped to a non-zero value. If the STRAP_VS_MODE[1:0] inputs are strapped Low to enable Base mode, the serial EEPROM, I^2C/SMBus, and software* ***cannot*** *override the straps to enable Virtual Switch mode. Similarly, if the STRAP_VS_MODE[1:0] inputs are strapped to a non-zero value to enable Virtual Switch mode, the serial EEPROM, I^2C/SMBus, and software* ***cannot*** *override the straps to enable Base mode. However, in Virtual Switch mode, the serial EEPROM, I^2C/SMBus, and/or software can change the Virtual Switch Table, including the quantity of enabled virtual switches. (Refer to Section 5.5.3, "Virtual Switch Table.")* *If a design must support both Base mode and Virtual Switch mode, without changing the STRAP_VS_MODE[1:0] input values, strap the STRAP_VS_MODE[1:0] inputs to a non-zero value. Then, if Base mode is needed, the serial EEPROM, I^2C/SMBus, and/or software can assign all Ports to VS0 (with no Ports assigned to other virtual switches).*				
0	**VS0 Enable** 0 = Disables VS0 1 = Enables VS0 ***Note:*** *VS0 must remain enabled in Base mode.*	RWS	Yes	1
1	**VS1 Enable** 0 = Disables VS1 1 = Enables VS1	RWS	Yes	Based upon STRAP_VS_MODE[1:0] input Settings
2	**VS2 Enable** 0 = Disables VS2 1 = Enables VS2	RWS	Yes	Based upon STRAP_VS_MODE[1:0] input Settings
3	**VS3 Enable** 0 = Disables VS3 1 = Enables VS3	RWS	Yes	Based upon STRAP_VS_MODE[1:0] input Settings
7:4	***Reserved***	RsvdP	No	0h
31:8	***Reserved***	RsvdP	No	0000_00h

Register 13-107. 360h VS0 Upstream (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I^{2}C</th><th>Default</th></tr>
<tr><td colspan="5">This register can be programmed, prior to linkup, using any of the following methods:
• Serial EEPROM,
• I^{2}C, if STRAP_I2C_CFG_EN#=L, followed by an I^{2}C Write that Sets the <b>Configuration Release</b> register <i>Initiate Configuration</i> bit (Port 0, offset 3ACh[0]),
• Software, followed by a Hot Reset.

In Base mode, this register defines the upstream Port and NT Port, and enables NT mode. In Virtual Switch mode, this register defines the VS0 upstream Port.
In Virtual Switch mode, the <b>VS<i>x</i> Upstream</b> register(s) (offsets 360h through 36Ch), in combination with the <b>Virtual Switch Enable</b> and <b>VS<i>x</i> Port Vector</b> registers (offsets 354h and 380h through 38Ch, respectively), comprise the Virtual Switch Table. For further details, refer to Section 5.5.3, “Virtual Switch Table.”</td></tr>
<tr><td>4, 2:0</td><td><b>Base Mode</b>
<b>Upstream Port</b>
Identifies the upstream Port, based upon the STRAP_UPSTRM_PORTSEL[3:0] input levels, respectively. The upper two bits [4, 2] of this field map to STRAP_UPSTRM_PORTSEL[3:2], to select the Station, and the lower two bits [1:0] map to STRAP_UPSTRM_PORTSEL[1:0], to select the Port within that Station.
<table>
<tr><th>Field Value</th><th>Strapping Ball Value</th><th>Port Number</th></tr>
<tr><td>0h</td><td>0000b (LLLL)</td><td>0</td></tr>
<tr><td>1h</td><td>0001b (LLLH)</td><td>1</td></tr>
<tr><td>2h</td><td>0010b (LLHL)</td><td>2</td></tr>
<tr><td>3h</td><td>0011b (LLHH)</td><td>3</td></tr>
<tr><td>4h</td><td>0100b (LHLL)</td><td>16</td></tr>
<tr><td>5h</td><td>0101b (LHLH)</td><td>17</td></tr>
<tr><td>6h</td><td>0110b (LHHL)</td><td>18</td></tr>
<tr><td>7h</td><td>0111b (LHHH)</td><td>19</td></tr>
<tr><td>8h</td><td>1000b (HLLL)</td><td>20</td></tr>
<tr><td>9h</td><td>1001b (HLLH)</td><td>21</td></tr>
<tr><td>Ah</td><td>1010b (HLHL)</td><td>22</td></tr>
<tr><td>Bh</td><td>1011b (HLHH)</td><td>23</td></tr>
</table>
All other encodings are <b><i>reserved</i></b>.</td><td>RWS</td><td>Yes</td><td>Set by STRAP_UPSTRM_PORTSEL[3:0] input levels</td></tr>
<tr><td>3</td><td><b>Base Mode</b>
<b><i>Not used, internally tied Low. Must be 0.</i></b></td><td>RsvdP</td><td>Yes</td><td>0</td></tr>
<tr><td>4, 2:0</td><td><b>Virtual Switch Mode</b>
<b>VS0 Upstream Port</b>
Table 13-6 lists the default upstream and downstream Port assignments of each virtual switch.</td><td>RWS</td><td>Yes</td><td>0h</td></tr>
<tr><td>3</td><td><b>Virtual Switch Mode</b>
<b><i>Not used, internally tied Low</i></b></td><td>RsvdP</td><td>Yes</td><td>0</td></tr>
</table>

Register 13-107. 360h VS0 Upstream (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I²C</th><th>Default</th></tr>
<tr><td>7:5</td><td><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>000b</td></tr>
<tr><td rowspan="2">12, 10:8</td><td><b>Base Mode</b>
<b>NT Port</b>
The NT Port Number value is selected by the STRAP_NT_UPSTRM_PORTSEL[4, 2:0] Strapping balls, respectively.
<table>
<tr><th>Field Value</th><th>Strapping Ball Value</th><th>Port Number</th></tr>
<tr><td>0h</td><td>0000b (LLLL)</td><td>0</td></tr>
<tr><td>1h</td><td>0001b (LLLH)</td><td>1</td></tr>
<tr><td>2h</td><td>0010b (LLHL)</td><td>2</td></tr>
<tr><td>3h</td><td>0011b (LLHH)</td><td>3</td></tr>
<tr><td>8h</td><td>1000b (HLLL)</td><td>16</td></tr>
<tr><td>9h</td><td>1001b (HLLH)</td><td>17</td></tr>
<tr><td>Ah</td><td>1010b (HLHL)</td><td>18</td></tr>
<tr><td>Bh</td><td>1011b (HLHH)</td><td>19</td></tr>
<tr><td>Ch</td><td>1100b (HHLL)</td><td>20</td></tr>
<tr><td>Dh</td><td>1101b (HHLH)</td><td>21</td></tr>
<tr><td>Eh</td><td>1110b (HHHL)</td><td>22</td></tr>
<tr><td>Fh</td><td>1111b (HHHH)</td><td>23</td></tr>
</table>
All other encodings are <b><i>reserved</i></b>.</td><td>RWS</td><td>Yes</td><td>Set by STRAP_NT_UPSTRM_PORTSEL[4, 2:0] ball levels</td></tr>
<tr><td><b>Virtual Switch Mode</b>
<b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>0-0h</td></tr>
<tr><td>11</td><td><b><i>Reserved</i></b></td><td>RsvdP</td><td>Yes</td><td>0</td></tr>
<tr><td rowspan="2">13</td><td><b>Base Mode</b>
<b>NT Enable</b>
0 = NT mode is disabled
1 = NT mode is enabled</td><td>RWS</td><td>Yes</td><td>Set by STRAP_NT_ENABLE# ball level</td></tr>
<tr><td><b>Virtual Switch Mode</b>
<b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>0</td></tr>
<tr><td>31:14</td><td><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>0-0h</td></tr>
</table>

Register 13-108. 364h VS1 Upstream (Virtual Switch mode – Port 0, accessible through the Management Port)

This register can be programmed, prior to linkup, using any of the following methods:

- Serial EEPROM,
- I^{2}C, if STRAP_I2C_CFG_EN#=L, followed by an I^{2}C Write that Sets the **Configuration Release** register *Initiate Configuration* bit (Port 0, offset 3ACh[0]),
- Software, followed by a Hot Reset.

The **VS*x* Upstream** register(s) (offsets 360h through 36Ch), in combination with the **Virtual Switch Enable** and **VS*x* Port Vector** registers (offsets 354h and 380h through 38Ch, respectively), comprise the Virtual Switch Table. For further details, refer to Section 5.5.3, "Virtual Switch Table."

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
4, 2:0	**VS1 Upstream Port** Table 13-6 lists the default upstream and downstream Port assignments of each virtual switch.	RWS	Yes	Set by STRAP_NT_UPSTRM_PORTSEL[4, 2:0] ball levels
3	***Reserved***	RsvdP	No	0
31:5	***Reserved***	RsvdP	No	0-0h

Register 13-109. 368h VS2 Upstream (Virtual Switch mode – Port 0, accessible through the Management Port)

This register can be programmed, prior to linkup, using any of the following methods:

- Serial EEPROM,
- I^{2}C, if STRAP_I2C_CFG_EN#=L, followed by an I^{2}C Write that Sets the **Configuration Release** register *Initiate Configuration* bit (Port 0, offset 3ACh[0]),
- Software, followed by a Hot Reset.

The **VS*x* Upstream** register(s) (offsets 360h through 36Ch), in combination with the **Virtual Switch Enable** and **VS*x* Port Vector** registers (offsets 354h and 380h through 38Ch, respectively), comprise the Virtual Switch Table. For further details, refer to Section 5.5.3, "Virtual Switch Table."

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
4, 2:0	**VS2 Upstream Port** Table 13-6 lists the default upstream and downstream Port assignments of each virtual switch.	RWS	Yes	Set by STRAP_NT_UPSTRM_PORTSEL[4, 2:0] ball levels
3	***Reserved***	RsvdP	No	0
31:5	***Reserved***	RsvdP	No	0-0h

Register 13-110. 36Ch VS3 Upstream (Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register can be programmed, prior to linkup, using any of the following methods: • Serial EEPROM, • I^2C, if STRAP_I2C_CFG_EN#=L, followed by an I^2C Write that Sets the **Configuration Release** register *Initiate Configuration* bit (Port 0, offset 3ACh[0]), • Software, followed by a Hot Reset. The **VS*x* Upstream** register(s) (offsets 360h through 36Ch), in combination with the **Virtual Switch Enable** and **VS*x* Port Vector** registers (offsets 354h and 380h through 38Ch, respectively), comprise the Virtual Switch Table. For further details, refer to Section 5.5.3, "Virtual Switch Table."				
4, 2:0	**VS3 Upstream Port** Table 13-6 lists the default upstream and downstream Port assignments of each virtual switch.	RWS	Yes	Set by STRAP_NT_UPSTRM_PORTSEL[4, 2:0] ball levels
3	***Reserved***	RsvdP	No	0
31:5	***Reserved***	RsvdP	No	0-0h

Register 13-111. 380h VS0 Port Vector (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I^{2}C</th><th>Default</th></tr>
<tr><td colspan="5">This register can be programmed, prior to linkup, using any of the following methods:<ul><li>Serial EEPROM,</li><li>I^{2}C, if STRAP_I2C_CFG_EN#=L, followed by an I^{2}C Write that Sets the <b>Configuration Release</b> register <i>Initiate Configuration</i> bit (Port 0, offset 3ACh[0]),</li><li>Software, followed by a Hot Reset.</li></ul>Bits [23:16, 3:0] correspond to Ports 23 through 16 and 3 through 0, respectively.
In Base mode the default value of this register is 00FF_FFFFh.
In Virtual Switch mode:<ul><li><b>VS<i>x</i> Port Vector</b> register(s) (offsets 380h through 38Ch), in combination with the <b>Virtual Switch Enable</b> and <b>VS<i>x</i> Upstream</b> registers (offsets 354h and 360h through 36Ch, respectively), comprise the Virtual Switch Table. For further details, refer to Section 5.5.3, “Virtual Switch Table.”</li><li>If the Virtual Switch Table is the default configuration programmed by the STRAP_VS_MODE[1:0] straps, or is programmed by serial EEPROM, then this register defines which Ports (upstream and downstream) are active for VS0. If instead the Virtual Switch Table is programmed by the Management Port (STRAP_NT_UPSTRM_PORTSEL0=L) and/or I^{2}C (STRAP_I2C_CFG_EN#=L), then the default value of this register is 00FF_FFFFh.</li><li>Attempted access through virtual switch upstream Ports, that are not the Management Port, is handled as NOP (Reads return 0h, Writes have no effect).</li></ul>Table 13-6 lists the default upstream and downstream Port assignments of each virtual switch.</td></tr>
<tr><td>23:16, 3:0</td><td><b>VS0 Active Ports</b></td><td>RWS</td><td>Yes</td><td>Based upon STRAP_VS_MODE[1:0] input Settings</td></tr>
<tr><td>15:4</td><td><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>000h</td></tr>
<tr><td>31:24</td><td><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>00h</td></tr>
</table>

Register 13-112. 384h VS1 Port Vector (Virtual Switch mode – Port 0, accessible through the Management Port)

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I^2C</th><th>Default</th></tr>
<tr><td colspan="5">This register defines which Ports (upstream and downstream) are associated with VS1. The initial value of this register corresponds to the Setting of the STRAP_VS_MODE[1:0] inputs.
Attempted access through virtual switch upstream Ports, that are not the Management Port, is handled as NOP (Reads return 0h, Writes have no effect).
Bits [23:16, 3:0] correspond to Ports 23 through 16 and 3 through 0, respectively.
Table 13-6 lists the default upstream and downstream Port assignments of each virtual switch.
This register can be programmed, prior to linkup, using any of the following methods:
• Serial EEPROM,
• I^2C, if STRAP_I2C_CFG_EN#=L, followed by an I^2C Write that Sets the <b>Configuration Release</b> register <i>Initiate Configuration</i> bit (Port 0, offset 3ACh[0]),
• Software, followed by a Hot Reset.
The <b>VS<i>x</i> Port Vector</b> register(s) (offsets 380h through 38Ch), in combination with the <b>Virtual Switch Enable</b> and <b>VS<i>x</i> Upstream</b> registers (offsets 354h and 360h through 36Ch, respectively), comprise the Virtual Switch Table. For further details, refer to Section 5.5.3, “Virtual Switch Table.”</td></tr>
<tr><td>23:16, 3:0</td><td><b>VS1 Active Ports</b></td><td>RWS</td><td>Yes</td><td>Based upon STRAP_VS_MODE[1:0] input Settings</td></tr>
<tr><td>15:4</td><td><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>000h</td></tr>
<tr><td>31:24</td><td><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>00h</td></tr>
</table>

Register 13-113. 388h VS2 Port Vector (Virtual Switch mode – Port 0, accessible through the Management Port)

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I^2C</th><th>Default</th></tr>
<tr><td colspan="5">This register defines which Ports (upstream and downstream) are associated with VS2. The initial value of this register corresponds to the Setting of the STRAP_VS_MODE[1:0] inputs.
Attempted access through virtual switch upstream Ports, that are not the Management Port, is handled as NOP (Reads return 0h, Writes have no effect).
Bits [23:16, 3:0] correspond to Ports 23 through 16 and 3 through 0, respectively.
Table 13-6 lists the default upstream and downstream Port assignments of each virtual switch.
This register can be programmed, prior to linkup, using any of the following methods:
• Serial EEPROM,
• I^2C, if STRAP_I2C_CFG_EN#=L, followed by an I^2C Write that Sets the <b>Configuration Release</b> register <i>Initiate Configuration</i> bit (Port 0, offset 3ACh[0]),
• Software, followed by a Hot Reset.
The <b>VS<i>x</i> Port Vector</b> register(s) (offsets 380h through 38Ch), in combination with the <b>Virtual Switch Enable</b> and <b>VS<i>x</i> Upstream</b> registers (offsets 354h and 360h through 36Ch, respectively), comprise the Virtual Switch Table. For further details, refer to Section 5.5.3, “Virtual Switch Table.”</td></tr>
<tr><td>23:16, 3:0</td><td><b>VS2 Active Ports</b></td><td>RWS</td><td>Yes</td><td>Based upon STRAP_VS_MODE[1:0] input Settings</td></tr>
<tr><td>15:4</td><td><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>000h</td></tr>
<tr><td>31:24</td><td><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>00h</td></tr>
</table>

Register 13-114. 38Ch VS3 Port Vector (Virtual Switch mode – Port 0, accessible through the Management Port)

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I^{2}C</th><th>Default</th></tr>
<tr><td colspan="5">This register defines which Ports (upstream and downstream) are associated with VS3. The initial value of this register corresponds to the Setting of the STRAP_VS_MODE[1:0] inputs.
Attempted access through virtual switch upstream Ports, that are not the Management Port, is handled as NOP (Reads return 0h, Writes have no effect).
Bits [23:16, 3:0] correspond to Ports 23 through 16 and 3 through 0, respectively.
Table 13-6 lists the default upstream and downstream Port assignments of each virtual switch.
This register can be programmed, prior to linkup, using any of the following methods:
• Serial EEPROM,
• I^{2}C, if STRAP_I2C_CFG_EN#=L, followed by an I^{2}C Write that Sets the <b>Configuration Release</b> register <i>Initiate Configuration</i> bit (Port 0, offset 3ACh[0]),
• Software, followed by a Hot Reset.
The <b>VS<i>x</i> Port Vector</b> register(s) (offsets 380h through 38Ch), in combination with the <b>Virtual Switch Enable</b> and <b>VS<i>x</i> Upstream</b> registers (offsets 354h and 360h through 36Ch, respectively), comprise the Virtual Switch Table. For further details, refer to Section 5.5.3, “Virtual Switch Table.”</td></tr>
<tr><td>23:16, 3:0</td><td><b>VS3 Active Ports</b></td><td>RWS</td><td>Yes</td><td>Based upon STRAP_VS_MODE[1:0] input Settings</td></tr>
<tr><td>15:4</td><td><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>000h</td></tr>
<tr><td>31:24</td><td><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>00h</td></tr>
</table>

Register 13-115. 3A0h Port Reset (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Port	Type	Serial EEPROM and I^{2}C	Default
When driven with a value of 1, this register holds the Port in reset, including the Port PCI-to-PCI bridge and the hierarchy below it. A value of 0 indicates to un-reset the PCI-to-PCI bridge and the hierarchy below it. ***Note:*** *The upstream Port bits are* ***reserved****, RsvdP, not serial EEPROM nor I^{2}C writable, and have a default value of 0.*					
0	***Reserved***	Upstream	RsvdP	No	0
	Reset Port 0 Vector 0 = Port is not reset 1 = Port is reset	Downstream	RWS	Yes	0
1	***Reserved***	Upstream	RsvdP	No	0
	Reset Port 1 Vector 0 = Port is not reset 1 = Port is reset	Downstream	RWS	Yes	0
2	***Reserved***	Upstream	RsvdP	No	0
	Reset Port 2 Vector 0 = Port is not reset 1 = Port is reset	Downstream	RWS	Yes	0
3	***Reserved***	Upstream	RsvdP	No	0
	Reset Port 3 Vector 0 = Port is not reset 1 = Port is reset	Downstream	RWS	Yes	0
15:4	***Reserved***		RsvdP	No	000h
16	***Reserved***	Upstream	RsvdP	No	0
	Reset Port 16 Vector 0 = Port is not reset 1 = Port is reset	Downstream	RWS	Yes	0
17	***Reserved***	Upstream	RsvdP	No	0
	Reset Port 17 Vector 0 = Port is not reset 1 = Port is reset	Downstream	RWS	Yes	0
18	***Reserved***	Upstream	RsvdP	No	0
	Reset Port 18 Vector 0 = Port is not reset 1 = Port is reset	Downstream	RWS	Yes	0
19	***Reserved***	Upstream	RsvdP	No	0
	Reset Port 19 Vector 0 = Port is not reset 1 = Port is reset	Downstream	RWS	Yes	0

Register 13-115. 3A0h Port Reset (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Port	Type	Serial EEPROM and I^2C	Default
20	***Reserved***	Upstream	RsvdP	No	0
	Reset Port 20 Vector 0 = Port is not reset 1 = Port is reset	Downstream	RWS	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	Reset Port 21 Vector 0 = Port is not reset 1 = Port is reset	Downstream	RWS	Yes	0
22	***Reserved***	Upstream	RsvdP	No	0
	Reset Port 22 Vector 0 = Port is not reset 1 = Port is reset	Downstream	RWS	Yes	0
23	***Reserved***	Upstream	RsvdP	No	0
	Reset Port 23 Vector 0 = Port is not reset 1 = Port is reset	Downstream	RWS	Yes	0
31:24	***Reserved***		RsvdP	No	00h

Register 13-116. 3A4h Parallel Hot Plug Control (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Any downstream Transparent Port can be configured as a Parallel Hot Plug Port or Serial Hot Plug Port. An upstream Port can be assigned to be a Parallel Hot Plug Port (although non-compliant to the *PCI Express Base r2.0*), by Setting the upstream Port's **Power Management Hot Plug User Configuration** register *Upstream Hot Plug Enable* bit (offset F70h[14]), in which case the upstream Port's **Slot Capability** and **Slot Status and Control** registers (offsets 7Ch and 80h, respectively) provide the same Hot Plug functionality and control that is usually restricted to downstream Ports.				
7:0	***Reserved***	RsvdP	No	00h
12:8	**Parallel Hot Plug Port B** Value specifies which Port is assigned Parallel Hot Plug Controller B. 0 = Selects Serial Hot Plug, if the Port is both Parallel- and Serial Hot Plug-capable 1 = Defaults to Parallel Hot Plug, if the Port is both Parallel- and Serial Hot Plug-capable	RWS	Yes	10h
14:13	***Reserved***	RsvdP	No	00b
15	**Parallel Hot Plug Port B Enable** 0 = Hot Plug Port B is not enabled 1 = Hot Plug Port B is enabled	RWS	Yes	1
20:16	**Parallel Hot Plug Port C** Value specifies which Port is assigned Parallel Hot Plug Controller C. 0 = Selects Serial Hot Plug, if the Port is both Parallel- and Serial Hot Plug-capable 1 = Defaults to Parallel Hot Plug, if the Port is both Parallel- and Serial Hot Plug-capable	RWS	Yes	14h
22:21	***Reserved***	RsvdP	No	00b
23	**Parallel Hot Plug Port C Enable** 0 = Hot Plug Port C is not enabled 1 = Hot Plug Port C is enabled	RWS	Yes	1
31:24	***Reserved***	RsvdP	No	00h

Register 13-117. 3A8h VS*x*_PERST# Status (Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**VS0_PERST# Ball Value** 0 = VS0_PERST# is Low 1 = VS0_PERST# is High	RO	No	Reflects the value of the VS0_PERST# ball
1	**VS1_PERST# Ball Value** 0 = VS1_PERST# is Low 1 = VS1_PERST# is High	RO	No	Reflects the value of the VS1_PERST# ball
2	**VS2_PERST# Ball Value** 0 = VS2_PERST# is Low 1 = VS2_PERST# is High	RO	No	Reflects the value of the VS2_PERST# ball
3	**VS3_PERST# Ball Value** 0 = VS3_PERST# is Low 1 = VS3_PERST# is High	RO	No	Reflects the value of the VS3_PERST# ball
7:4	***Reserved***	RsvdP	No	0h
8	**VS0_PERST# Control** 0 = Writing 0 Clears the VS0_PERST# reset condition 1 = Causes VS0_PERST# to receive a *Fundamental* Reset	RWS	Yes	0
9	**VS1_PERST# Control** 0 = Writing 0 Clears the VS1_PERST# reset condition 1 = Causes VS1_PERST# Reset	RWS	Yes	0
10	**VS2_PERST# Control** 0 = Writing 0 Clears the VS2_PERST# reset condition 1 = Causes VS2_PERST# Reset	RWS	Yes	0
11	**VS3_PERST# Control** 0 = Writing 0 Clears the VS3_PERST# reset condition 1 = Causes VS3_PERST# Reset	RWS	Yes	0
15:12	***Reserved***	RsvdP	No	0h
31:16	***Reserved***	RsvdP	No	0000h

Register 13-118. 3ACh Configuration Release (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
0	**Initiate Configuration** 1 = Releases the hold that prevents the Links from coming up **Base Mode** If the STRAP_I2C_CFG_EN# ball is Low, I^{2}C is being used to configure the PEX 8649. After I^{2}C has completed its configuration, it must write to this bit, to release the hold that is preventing the Links from coming up. **Virtual Switch Mode** The STRAP_NT_UPSTRM_PORTSEL0 ball is used to control Bring-Up Options 1 and 2: • **Option 1** – STRAP_NT_UPSTRM_PORTSEL0=L. After the serial EEPROM is loaded, the Management Port comes up first, to configure the PEX 8649. When the Management Port has completed its configuration, it must write to this bit, to release the hold that is preventing the remaining Links from coming up. • **Option 2** – STRAP_NT_UPSTRM_PORTSEL0=H. After the serial EEPROM is loaded, all Ports come up concurrently.	RWS	Yes	0
31:1	***Reserved***	RsvdP	No	0-0h

13.15.9 Device-Specific Registers – General-Purpose Input/Output (Offsets 600h – 68Ch)

This section details the Device-Specific General-Purpose Input/Output (GPIO) registers. Table 13-28 defines the register map.

Table 13-28. Device-Specific GPIO Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
GPIO 0_9 Direction Control				600h
GPIO 10_11 Direction Control				604h
Reserved				608h
Reserved	GPIO 24_31 Direction Control			60Ch
Reserved				610h
GPIO 0_11 Input De-Bounce				614h
GPIO 24_31 Input De-Bounce				618h
GPIO 0_11 Input Data				61Ch
Reserved			GPIO 24_31 Input Data	620h
GPIO 0_11 Output Data				624h
Reserved			GPIO 24_31 Output Data	628h
GPIO 0_11 Interrupt Polarity				62Ch
Reserved			GPIO 24_31 Interrupt Polarity	630h
GPIO 0_11 Interrupt Status				634h
Reserved			GPIO 24_31 Interrupt Status	638h
GPIO 0_11 Interrupt Mask				63Ch
Reserved			GPIO 24_31 Interrupt Mask	640h
Reserved				644h – 648h
Reserved (Base Mode) Virtual Switch GPIO Update (Virtual Switch Mode)				64Ch
Reserved (Base Mode) VS0 GPIO_PG 0_11 Assignment (Virtual Switch Mode)				650h
Reserved (Base Mode) VS1 GPIO_PG 0_11 Assignment (Virtual Switch Mode)				654h
Reserved (Base Mode) VS2 GPIO_PG 0_11 Assignment (Virtual Switch Mode)				658h
Reserved (Base Mode) VS3 GPIO_PG 0_11 Assignment (Virtual Switch Mode)				65Ch
Reserved				660h – 66Ch

Table 13-28. Device-Specific GPIO Register Map *(Cont.)*

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved	***Reserved*** (Base Mode) VS0 GPIO_SHP 0_7 Assignment (Virtual Switch Mode)	670h
Reserved	***Reserved*** (Base Mode) VS1 GPIO_SHP 0_7 Assignment (Virtual Switch Mode)	674h
Reserved	***Reserved*** (Base Mode) VS2 GPIO_SHP 0_7 Assignment (Virtual Switch Mode)	678h
Reserved	***Reserved*** (Base Mode) VS3 GPIO_SHP 0_7 Assignment (Virtual Switch Mode)	67Ch
Reserved		680h – 68Ch

Register 13-119. 600h GPIO 0_9 Direction Control (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
The GPIO 0_9 **Direction Control** registers control the direction, source, and destination of the PEX_PORT_GOOD[0:3, 16:21]# balls, respectively. ***Note:*** *Register offsets 61Ch and 624h, referenced in this register, are located as follows – Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port.*				
1:0	**PEX_PORT_GOOD0# Source/Destination** **As Input:** 00b = To **PEX_PORT_GOOD0# Input Data** register (offset 61Ch[0]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **PEX_PORT_GOOD0# Output Data** register (offset 624h[0]) 01b = PEX_PORT_GOOD0# 10b, 11b = ***Reserved***	RWS	Yes	Default is 01b when STRAP_TESTMODE[3:0]=1011b or 1101b, and the Port is enabled Otherwise, default is 00b
2	**PEX_PORT_GOOD0# Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0]=1011b or 1101b, and the Port is enabled Otherwise, default is 0

Register 13-119. 600h GPIO 0_9 Direction Control (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4:3	**PEX_PORT_GOOD1# Source/Destination** **As Input:** 00b = To **PEX_PORT_GOOD1# Input Data** register (offset 61Ch[1]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **PEX_PORT_GOOD1# Output Data** register (offset 624h[1]) 01b = **PEX_PORT_GOOD1#** 10b, 11b = ***Reserved***	RWS	Yes	Default is 01b when STRAP_TESTMODE[3:0]=1011b or 1101b, and the Port is enabled Otherwise, default is 00b
5	**PEX_PORT_GOOD1# Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0]=1011b or 1101b, and the Port is enabled Otherwise, default is 0
7:6	**PEX_PORT_GOOD2# Source/Destination** **As Input:** 00b = To **PEX_PORT_GOOD2# Input Data** register (offset 61Ch[2]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **PEX_PORT_GOOD2# Output Data** register (offset 624h[2]) 01b = PEX_PORT_GOOD2# 10b, 11b = ***Reserved***	RWS	Yes	Default is 01b when STRAP_TESTMODE[3:0]=1011b or 1101b, and the Port is enabled Otherwise, default is 00b
8	**PEX_PORT_GOOD2# Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0]=1011b or 1101b, and the Port is enabled Otherwise, default is 0

Register 13-119. 600h GPIO 0_9 Direction Control (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
10:9	**PEX_PORT_GOOD3# Source/Destination** **As Input:** 00b = To **PEX_PORT_GOOD3# Input Data** register (offset 61Ch[3]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **PEX_PORT_GOOD3# Output Data** register (offset 624h[3]) 01b = PEX_PORT_GOOD3# 10b, 11b = ***Reserved***	RWS	Yes	Default is 01b when STRAP_TESTMODE[3:0]=1011b or 1101b, and the Port is enabled Otherwise, default is 00b
11	**PEX_PORT_GOOD3# Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0]=1011b or 1101b, and the Port is enabled Otherwise, default is 0
13:12	**PEX_PORT_GOOD16# Source/Destination** **As Input:** 00b = To **PEX_PORT_GOOD16# Input Data** register (offset 61Ch[4]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **PEX_PORT_GOOD16# Output Data** register (offset 624h[4]) 01b = PEX_PORT_GOOD16# 10b, 11b = ***Reserved***	RWS	Yes	Default is 01b when STRAP_TESTMODE[3:0]=1011b or 1101b, and the Port is enabled Otherwise, default is 00b
14	**PEX_PORT_GOOD16# Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0]=1011b or 1101b, and the Port is enabled Otherwise, default is 0

Register 13-119. 600h GPIO 0_9 Direction Control (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
16:15	**PEX_PORT_GOOD17# Source/Destination** **As Input:** 00b = To **PEX_PORT_GOOD17# Input Data** register (offset 61Ch[5]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **PEX_PORT_GOOD17# Output Data** register (offset 624h[5]) 01b = PEX_PORT_GOOD17# 10b, 11b = ***Reserved***	RWS	Yes	Default is 01b when STRAP_TESTMODE[3:0]=1011b or 1101b, and the Port is enabled Otherwise, default is 00b
17	**PEX_PORT_GOOD17# Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0]=1011b or 1101b, and the Port is enabled Otherwise, default is 0
19:18	**PEX_PORT_GOOD18# Source/Destination** **As Input:** 00b = To **PEX_PORT_GOOD18# Input Data** register (offset 61Ch[6]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **PEX_PORT_GOOD18# Output Data** register (offset 624h[6]) 01b = PEX_PORT_GOOD18# 10b, 11b = ***Reserved***	RWS	Yes	Default is 01b when STRAP_TESTMODE[3:0]=1011b or 1101b, and the Port is enabled Otherwise, default is 00b
20	**PEX_PORT_GOOD18# Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0]=1011b or 1101b, and the Port is enabled Otherwise, default is 0

Register 13-119. 600h GPIO 0_9 Direction Control (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
22:21	**PEX_PORT_GOOD19# Source/Destination** **As Input:** 00b = To **PEX_PORT_GOOD19# Input Data** register (offset 61Ch[7]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **PEX_PORT_GOOD19# Output Data** register (offset 624h[7]) 01b = PEX_PORT_GOOD19# 10b, 11b = ***Reserved***	RWS	Yes	Default is 01b when STRAP_TESTMODE[3:0]=1011b or 1101b, and the Port is enabled Otherwise, default is 00b
23	**PEX_PORT_GOOD19# Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0]=1011b or 1101b, and the Port is enabled Otherwise, default is 0
25:24	**PEX_PORT_GOOD20# Source/Destination** **As Input:** 00b = To **PEX_PORT_GOOD20# Input Data** register (offset 61Ch[8]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **PEX_PORT_GOOD20# Output Data** register (offset 624h[8]) 01b = PEX_PORT_GOOD20# 10b, 11b = ***Reserved***	RWS	Yes	Default is 01b when STRAP_TESTMODE[3:0]=1011b or 1101b, and the Port is enabled Otherwise, default is 00b
26	**PEX_PORT_GOOD20# Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0]=1011b or 1101b, and the Port is enabled Otherwise, default is 0

Register 13-119. 600h GPIO 0_9 Direction Control (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
28:27	**PEX_PORT_GOOD21# Source/Destination** **As Input:** 00b = To **PEX_PORT_GOOD21# Input Data** register (offset 61Ch[9]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **PEX_PORT_GOOD21# Output Data** register (offset 624h[9]) 01b = PEX_PORT_GOOD21# 10b, 11b = ***Reserved***	RWS	Yes	Default is 01b when STRAP_TESTMODE[3:0]=1011b or 1101b, and the Port is enabled Otherwise, default is 00b
29	**PEX_PORT_GOOD21# Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0]=1011b or 1101b, and the Port is enabled Otherwise, default is 0
31:30	***Reserved***	RsvdP	No	00b

Register 13-120. 604h GPIO 10_11 Direction Control (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The GPIO 10_11 **Direction Control** registers control the direction, source, and destination of the PEX_PORT_GOOD[22:23]# balls, respectively. ***Note:*** *Register offsets 61Ch and 624h, referenced in this register, are located as follows – Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port.*				
1:0	**PEX_PORT_GOOD22# Source/Destination** **As Input:** 00b = To **PEX_PORT_GOOD22# Input Data** register (offset 61Ch[10]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **PEX_PORT_GOOD22# Output Data** register (offset 624h[10]) 01b = PEX_PORT_GOOD22# 10b, 11b = ***Reserved***	RWS	Yes	Default is 01b when STRAP_TESTMODE[3:0]=1011b or 1101b, and the Port is enabled Otherwise, default is 00b
2	**PEX_PORT_GOOD22# Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0]=1011b or 1101b, and the Port is enabled Otherwise, default is 0
4:3	**PEX_PORT_GOOD23# Source/Destination** 00b = To **PEX_PORT_GOOD23# Input Data** register (offset 61Ch[11]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **PEX_PORT_GOOD23# Output Data** register (offset 624h[11]) 01b = PEX_PORT_GOOD23# 10b, 11b = ***Reserved***	RWS	Yes	Default is 01b when STRAP_TESTMODE[3:0]=1011b or 1101b, and the Port is enabled Otherwise, default is 00b
5	**PEX_PORT_GOOD23# Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0]=1011b or 1101b, and the Port is enabled Otherwise, default is 0
31:6	***Reserved***	RsvdP	No	0-0h

Register 13-121. 60Ch GPIO 24_31 Direction Control (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
The GPIO 24_31 **Direction Control** registers control the direction, source, and destination of the GPIO[24:31] balls, respectively. ***Note:*** *Register offsets 620h and 628h, referenced in this register, are located as follows – Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port.*				
1:0	**GPIO24 Source/Destination** **As Input:** 00b = To **GPIO24 Input Data** register (offset 620h[0]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **GPIO24 Output Data** register (offset 628h[0]) 10b = Serial Hot Plug PERST# output 01b, 11b = ***Reserved***	RWS	Yes	Default is 10b when STRAP_TESTMODE[3:0]= 1100b or 1101b Otherwise, default is 00b
2	**GPIO24 Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0]= 1100b or 1101b Otherwise, default is 0
4:3	**GPIO25 Source/Destination** **As Input:** 00b = To **GPIO25 Input Data** register (offset 620h[1]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **GPIO25 Output Data** register (offset 628h[1]) 10b = Serial Hot Plug PERST# output 01b, 11b = ***Reserved***	RWS	Yes	Default is 10b when STRAP_TESTMODE[3:0]= 1100b or 1101b Otherwise, default is 00b
5	**GPIO25 Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0]= 1100b or 1101b Otherwise, default is 0

Register 13-121. 60Ch GPIO 24_31 Direction Control (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
7:6	**GPIO26 Source/Destination** **As Input:** 00b = To **GPIO26 Input Data** register (offset 620h[2]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **GPIO26 Output Data** register (offset 628h[2]) 10b = Serial Hot Plug PERST# output 01b, 11b = ***Reserved***	RWS	Yes	Default is 10b when STRAP_TESTMODE[3:0]= 1100b or 1101b Otherwise, default is 00b
8	**GPIO26 Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0]= 1100b or 1101b Otherwise, default is 0
10:9	**GPIO27 Source/Destination** **As Input:** 00b = To **GPIO27 Input Data** register (offset 620h[3]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **GPIO27 Output Data** register (offset 628h[3]) 10b = Serial Hot Plug PERST# output 01b, 11b = ***Reserved***	RWS	Yes	Default is 10b when STRAP_TESTMODE[3:0]= 1100b or 1101b Otherwise, default is 00b
11	**GPIO27 Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0]= 1100b or 1101b Otherwise, default is 0

Register 13-121. 60Ch GPIO 24_31 Direction Control (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
13:12	**GPIO28 Source/Destination** **As Input:** 00b = To **GPIO28 Input Data** register (offset 620h[4]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **GPIO28 Output Data** register (offset 628h[4]) 10b = Serial Hot Plug PERST# output 01b, 11b = ***Reserved***	RWS	Yes	Default is 10b when STRAP_TESTMODE[3:0]= 1100b or 1101b Otherwise, default is 00b
14	**GPIO28 Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0]= 1100b or 1101b Otherwise, default is 0
16:15	**GPIO29 Source/Destination** **As Input:** 00b = To **GPIO29 Input Data** register (offset 620h[5]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **GPIO29 Output Data** register (offset 628h[5]) 10b = Serial Hot Plug PERST# output 01b, 11b = ***Reserved***	RWS	Yes	Default is 10b when STRAP_TESTMODE[3:0]= 1100b or 1101b Otherwise, default is 00b
17	**GPIO29 Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0]= 1100b or 1101b Otherwise, default is 0

Register 13-121. 60Ch GPIO 24_31 Direction Control (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
19:18	**GPIO30 Source/Destination** **As Input:** 00b = To **GPIO30 Input Data** register (offset 620h[6]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **GPIO30 Output Data** register (offset 628h[6]) 10b = Serial Hot Plug PERST# output 01b, 11b = ***Reserved***	RWS	Yes	Default is 10b when STRAP_TESTMODE[3:0]= 1100b or 1101b Otherwise, default is 00b
20	**GPIO30 Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0]= 1100b or 1101b Otherwise, default is 0
22:21	**GPIO31 Source/Destination** **As Input:** 00b = To **GPIO31 Input Data** register (offset 620h[7]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **GPIO31 Output Data** register (offset 628h[7]) 10b = Serial Hot Plug PERST# output 01b, 11b = ***Reserved***	RWS	Yes	Default is 10b when STRAP_TESTMODE[3:0]= 1100b or 1101b Otherwise, default is 00b
23	**GPIO31 Direction Control** 0 = Input 1 = Output	RWS	Yes	Default is 1 when STRAP_TESTMODE[3:0]= 1100b or 1101b Otherwise, default is 0
31:24	***Reserved***	RsvdP	No	00h

Register 13-122. 614h GPIO 0_11 Input De-Bounce (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The PEX_PORT_GOOD[0:3, 16:23]# balls are de-bounced, using the GPIO 0_11 **Input De-Bounce** registers, respectively. ***Note:*** *Register offsets 600h and 604h, referenced in this register, are located as follows – Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port.*				
0	**PEX_PORT_GOOD0# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD0# is configured as an input (offset 600h[2], is Cleared). 0 = PEX_PORT_GOOD0# input is not de-bounced 1 = PEX_PORT_GOOD0# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
1	**PEX_PORT_GOOD1# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD1# is configured as an input (offset 600h[5], is Cleared). 0 = PEX_PORT_GOOD1# input is not de-bounced 1 = PEX_PORT_GOOD1# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
2	**PEX_PORT_GOOD2# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD2# is configured as an input (offset 600h[8], is Cleared). 0 = PEX_PORT_GOOD2# input is not de-bounced 1 = PEX_PORT_GOOD2# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
3	**PEX_PORT_GOOD3# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD3# is configured as an input (offset 600h[11], is Cleared). 0 = PEX_PORT_GOOD3# input is not de-bounced 1 = PEX_PORT_GOOD3# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0

Register 13-122. 614h GPIO 0_11 Input De-Bounce (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4	**PEX_PORT_GOOD16# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD16# is configured as an input (offset 600h[14], is Cleared). 0 = PEX_PORT_GOOD16# input is not de-bounced 1 = PEX_PORT_GOOD16# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
5	**PEX_PORT_GOOD17# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD17# is configured as an input (offset 600h[17], is Cleared). 0 = PEX_PORT_GOOD17# input is not de-bounced 1 = PEX_PORT_GOOD17# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
6	**PEX_PORT_GOOD18# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD18# is configured as an input (offset 600h[20], is Cleared). 0 = PEX_PORT_GOOD18# input is not de-bounced 1 = PEX_PORT_GOOD18# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
7	**PEX_PORT_GOOD19# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD19# is configured as an input (offset 600h[23], is Cleared). 0 = PEX_PORT_GOOD19# input is not de-bounced 1 = PEX_PORT_GOOD19# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0

Register 13-122. 614h GPIO 0_11 Input De-Bounce (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
8	**PEX_PORT_GOOD20# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD20# is configured as an input (offset 600h[26], is Cleared). 0 = PEX_PORT_GOOD20# input is not de-bounced 1 = PEX_PORT_GOOD20# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
9	**PEX_PORT_GOOD21# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD21# is configured as an input (offset 600h[29], is Cleared). 0 = PEX_PORT_GOOD21# input is not de-bounced 1 = PEX_PORT_GOOD21# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
10	**PEX_PORT_GOOD22# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD22# is configured as an input (offset 604h[2], is Cleared). 0 = PEX_PORT_GOOD22# input is not de-bounced 1 = PEX_PORT_GOOD22# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
11	**PEX_PORT_GOOD23# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD23# is configured as an input (offset 604h[5], is Cleared). 0 = PEX_PORT_GOOD23# input is not de-bounced 1 = PEX_PORT_GOOD23# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
31:12	***Reserved***	RsvdP	No	0000_0h

Register 13-123. 618h GPIO 24_31 Input De-Bounce (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The GPIO[24:31] balls are de-bounced, using the GPIO 24_31 **Input De-Bounce** registers, respectively. ***Note:*** *Register offset 60Ch, referenced in this register, is located as follows – Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port.*				
0	**GPIO24 Input De-Bounce Control** Controls de-bounce when GPIO24 is configured as an input (offset 60Ch[2], is Cleared). 0 = GPIO24 input is not de-bounced 1 = GPIO24 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
1	**GPIO25 Input De-Bounce Control** Controls de-bounce when GPIO25 is configured as an input (offset 60Ch[5], is Cleared). 0 = GPIO25 input is not de-bounced 1 = GPIO25 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
2	**GPIO26 Input De-Bounce Control** Controls de-bounce when GPIO26 is configured as an input (offset 60Ch[8], is Cleared). 0 = GPIO26 input is not de-bounced 1 = GPIO26 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
3	**GPIO27 Input De-Bounce Control** Controls de-bounce when GPIO27 is configured as an input (offset 60Ch[11], is Cleared). 0 = GPIO27 input is not de-bounced 1 = GPIO27 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0

Register 13-123. 618h GPIO 24_31 Input De-Bounce (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
4	**GPIO28 Input De-Bounce Control** Controls de-bounce when GPIO28 is configured as an input (offset 60Ch[14], is Cleared). 0 = GPIO28 input is not de-bounced 1 = GPIO28 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
5	**GPIO29 Input De-Bounce Control** Controls de-bounce when GPIO29 is configured as an input (offset 60Ch[17], is Cleared). 0 = GPIO29 input is not de-bounced 1 = GPIO29 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
6	**GPIO30 Input De-Bounce Control** Controls de-bounce when GPIO30 is configured as an input (offset 60Ch[20], is Cleared). 0 = GPIO30 input is not de-bounced 1 = GPIO30 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
7	**GPIO31 Input De-Bounce Control** Controls de-bounce when GPIO31 is configured as an input (offset 60Ch[23], is Cleared). 0 = GPIO31 input is not de-bounced 1 = GPIO31 input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
31:8	***Reserved***	RsvdP	No	0000_00h

Register 13-124. 61Ch GPIO 0_11 Input Data (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The PEX_PORT_GOOD[0:3, 16:23]# input values are updated into the GPIO 0_11 **Input Data** registers, respectively. ***Note:*** *Register offsets 600h and 604h, referenced in this register, are located as follows – Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port.*				
0	**PEX_PORT_GOOD0# Input Data** If PEX_PORT_GOOD0# is configured as an output (offset 600h[2], is Set), Reads return 0. If PEX_PORT_GOOD0# is configured as an input (offset 600h[2], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD0#.	RO	No	0
1	**PEX_PORT_GOOD1# Input Data** If PEX_PORT_GOOD1# is configured as an output (offset 600h[5], is Set), Reads return 0. If PEX_PORT_GOOD1# is configured as an input (offset 600h[5], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD1#.	RO	No	0
2	**PEX_PORT_GOOD2# Input Data** If PEX_PORT_GOOD2# is configured as an output (offset 600h[8], is Set), Reads return 0. If PEX_PORT_GOOD2# is configured as an input (offset 600h[8], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD2#.	RO	No	0
3	**PEX_PORT_GOOD3# Input Data** If PEX_PORT_GOOD3# is configured as an output (offset 600h[11], is Set), Reads return 0. If PEX_PORT_GOOD3# is configured as an input (offset 600h[11], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD3#.	RO	No	0

Register 13-124. 61Ch GPIO 0_11 Input Data (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
4	**PEX_PORT_GOOD16# Input Data** If PEX_PORT_GOOD16# is configured as an output (offset 600h[14], is Set), Reads return 0. If PEX_PORT_GOOD16# is configured as an input (offset 600h[14], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD16#.	RO	No	0
5	**PEX_PORT_GOOD17# Input Data** If PEX_PORT_GOOD17# is configured as an output (offset 600h[17], is Set), Reads return 0. If PEX_PORT_GOOD17# is configured as an input (offset 600h[17], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD17#.	RO	No	0
6	**PEX_PORT_GOOD18# Input Data** If PEX_PORT_GOOD18# is configured as an output (offset 600h[20], is Set), Reads return 0. If PEX_PORT_GOOD18# is configured as an input (offset 600h[20], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD18#.	RO	No	0
7	**PEX_PORT_GOOD19# Input Data** If PEX_PORT_GOOD19# is configured as an output (offset 600h[23], is Set), Reads return 0. If PEX_PORT_GOOD19# is configured as an input (offset 600h[23], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD19#.	RO	No	0

Register 13-124. 61Ch GPIO 0_11 Input Data (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
8	**PEX_PORT_GOOD20# Input Data** If PEX_PORT_GOOD20# is configured as an output (offset 600h[26], is Set), Reads return 0. If PEX_PORT_GOOD20# is configured as an input (offset 600h[26], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD20#.	RO	No	0
9	**PEX_PORT_GOOD21# Input Data** If PEX_PORT_GOOD21# is configured as an output (offset 600h[29], is Set), Reads return 0. If PEX_PORT_GOOD21# is configured as an input (offset 600h[29], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD21#.	RO	No	0
10	**PEX_PORT_GOOD22# Input Data** If PEX_PORT_GOOD22# is configured as an output (offset 604h[2], is Set), Reads return 0. If PEX_PORT_GOOD22# is configured as an input (offset 604h[2], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD22#.	RO	No	0
11	**PEX_PORT_GOOD23# Input Data** If PEX_PORT_GOOD23# is configured as an output (offset 604h[5], is Set), Reads return 0. If PEX_PORT_GOOD23# is configured as an input (offset 604h[5], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD23#.	RO	No	0
31:12	***Reserved***	RsvdP	No	0000_0h

Register 13-125. 620h GPIO 24_31 Input Data (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
The GPIO[24:31] input values are updated into the GPIO 24_31 **Input Data** registers, respectively. ***Note:*** *Register offset 60Ch, referenced in this register, is located as follows – Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port.*				
0	**GPIO24 Input Data** If GPIO24 is configured as an output (offset 60Ch[2], is Set), Reads return 0. If GPIO24 is configured as an input (offset 60Ch[2], is Cleared), Reads return the logic value of the voltage on GPIO24.	RO	No	0
1	**GPIO25 Input Data** If GPIO25 is configured as an output (offset 60Ch[5], is Set), Reads return 0. If GPIO25 is configured as an input (offset 60Ch[5], is Cleared), Reads return the logic value of the voltage on GPIO25.	RO	No	0
2	**GPIO26 Input Data** If GPIO26 is configured as an output (offset 60Ch[8], is Set), Reads return 0. If GPIO26 is configured as an input (offset 60Ch[8], is Cleared), Reads return the logic value of the voltage on GPIO26.	RO	No	0
3	**GPIO27 Input Data** If GPIO27 is configured as an output (offset 60Ch[11], is Set), Reads return 0. If GPIO27 is configured as an input (offset 60Ch[11], is Cleared), Reads return the logic value of the voltage on GPIO27.	RO	No	0
4	**GPIO28 Input Data** If GPIO28 is configured as an output (offset 60Ch[14], is Set), Reads return 0. If GPIO28 is configured as an input (offset 60Ch[14], is Cleared), Reads return the logic value of the voltage on GPIO28.	RO	No	0
5	**GPIO29 Input Data** If GPIO29 is configured as an output (offset 60Ch[17], is Set), Reads return 0. If GPIO29 is configured as an input (offset 60Ch[17], is Cleared), Reads return the logic value of the voltage on GPIO29.	RO	No	0
6	**GPIO30 Input Data** If GPIO30 is configured as an output (offset 60Ch[20], is Set), Reads return 0. If GPIO30 is configured as an input (offset 60Ch[20], is Cleared), Reads return the logic value of the voltage on GPIO30.	RO	No	0
7	**GPIO31 Input Data** If GPIO31 is configured as an output (offset 60Ch[23], is Set), Reads return 0. If GPIO31 is configured as an input (offset 60Ch[23], is Cleared), Reads return the logic value of the voltage on GPIO31.	RO	No	0
31:8	***Reserved***	RsvdP	No	0000_00h

Register 13-126. 624h GPIO 0_11 Output Data (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The GPIO 0_11 **Output Data** registers control the value of the PEX_PORT_GOOD[0:3, 16:23]# outputs, respectively. ***Note:*** *Register offsets 600h and 604h, referenced in this register, are located as follows – Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port.*				
0	**PEX_PORT_GOOD0# Output Data** If PEX_PORT_GOOD0# is configured as an output (offset 600h[2], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD0# output. Reads return the value written.	RWS	Yes	0
1	**PEX_PORT_GOOD1# Output Data** If PEX_PORT_GOOD1# is configured as an output (offset 600h[5], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD1# output. Reads return the value written.	RWS	Yes	0
2	**PEX_PORT_GOOD2# Output Data** If PEX_PORT_GOOD2# is configured as an output (offset 600h[8], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD2# output. Reads return the value written.	RWS	Yes	0
3	**PEX_PORT_GOOD3# Output Data** If PEX_PORT_GOOD3# is configured as an output (offset 600h[11], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD3# output. Reads return the value written.	RWS	Yes	0
4	**PEX_PORT_GOOD16# Output Data** If PEX_PORT_GOOD16# is configured as an output (offset 600h[14], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD16# output. Reads return the value written.	RWS	Yes	0
5	**PEX_PORT_GOOD17# Output Data** If PEX_PORT_GOOD17# is configured as an output (offset 600h[17], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD17# output. Reads return the value written.	RWS	Yes	0
6	**PEX_PORT_GOOD18# Output Data** If PEX_PORT_GOOD18# is configured as an output (offset 600h[20], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD18# output. Reads return the value written.	RWS	Yes	0
7	**PEX_PORT_GOOD19# Output Data** If PEX_PORT_GOOD19# is configured as an output (offset 600h[23], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD19# output. Reads return the value written.	RWS	Yes	0

Register 13-126. 624h GPIO 0_11 Output Data (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
8	**PEX_PORT_GOOD20# Output Data** If PEX_PORT_GOOD20# is configured as an output (offset 600h[26], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD20# output. Reads return the value written.	RWS	Yes	0
9	**PEX_PORT_GOOD21# Output Data** If PEX_PORT_GOOD21# is configured as an output (offset 600h[29], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD21# output. Reads return the value written.	RWS	Yes	0
10	**PEX_PORT_GOOD22# Output Data** If PEX_PORT_GOOD22# is configured as an output (offset 604h[2], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD22# output. Reads return the value written.	RWS	Yes	0
11	**PEX_PORT_GOOD23# Output Data** If PEX_PORT_GOOD23# is configured as an output (offset 604h[5], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD23# output. Reads return the value written.	RWS	Yes	0
31:12	***Reserved***	RsvdP	No	0000_0h

Register 13-127. 628h GPIO 24_31 Output Data (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The GPIO 24_31 **Output Data** registers control the value of the GPIO[24:31] outputs, respectively. ***Note:*** *Register offset 60Ch, referenced in this register, is located as follows – Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port.*				
0	**GPIO24 Output Data** If GPIO24 is configured as an output (offset 60Ch[2], is Set), the value written to this bit is immediately driven to the GPIO24 output. Reads return the value written.	RWS	Yes	0
1	**GPIO25 Output Data** If GPIO25 is configured as an output (offset 60Ch[5], is Set), the value written to this bit is immediately driven to the GPIO25 output. Reads return the value written.	RWS	Yes	0
2	**GPIO26 Output Data** If GPIO26 is configured as an output (offset 60Ch[8], is Set), the value written to this bit is immediately driven to the GPIO26 output. Reads return the value written.	RWS	Yes	0
3	**GPIO27 Output Data** If GPIO27 is configured as an output (offset 60Ch[11], is Set), the value written to this bit is immediately driven to the GPIO27 output. Reads return the value written.	RWS	Yes	0
4	**GPIO28 Output Data** If GPIO28 is configured as an output (offset 60Ch[14], is Set), the value written to this bit is immediately driven to the GPIO28 output. Reads return the value written.	RWS	Yes	0
5	**GPIO29 Output Data** If GPIO29 is configured as an output (offset 60Ch[17], is Set), the value written to this bit is immediately driven to the GPIO29 output. Reads return the value written.	RWS	Yes	0
6	**GPIO30 Output Data** If GPIO30 is configured as an output (offset 60Ch[20], is Set), the value written to this bit is immediately driven to the GPIO30 output. Reads return the value written.	RWS	Yes	0
7	**GPIO31 Output Data** If GPIO31 is configured as an output (offset 60Ch[23], is Set), the value written to this bit is immediately driven to the GPIO31 output. Reads return the value written.	RWS	Yes	0
31:8	***Reserved***	RsvdP	No	0000_00h

Register 13-128. 62Ch GPIO 0_11 Interrupt Polarity (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The GPIO 0_11 **Interrupt Polarity** registers control the PEX_PORT_GOOD[0:3, 16:23]# Interrupt input polarities, respectively.				
0	**PEX_PORT_GOOD0# Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = PEX_PORT_GOOD0# Interrupt input is Active-Low 1 = PEX_PORT_GOOD0# Interrupt input is Active-High	RWS	Yes	0
1	**PEX_PORT_GOOD1# Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = PEX_PORT_GOOD1# Interrupt input is Active-Low 1 = PEX_PORT_GOOD1# Interrupt input is Active-High	RWS	Yes	0
2	**PEX_PORT_GOOD2# Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = PEX_PORT_GOOD2# Interrupt input is Active-Low 1 = PEX_PORT_GOOD2# Interrupt input is Active-High	RWS	Yes	0
3	**PEX_PORT_GOOD3# Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = PEX_PORT_GOOD3# Interrupt input is Active-Low 1 = PEX_PORT_GOOD3# Interrupt input is Active-High	RWS	Yes	0
4	**PEX_PORT_GOOD16# Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = PEX_PORT_GOOD16# Interrupt input is Active-Low 1 = PEX_PORT_GOOD16# Interrupt input is Active-High	RWS	Yes	0
5	**PEX_PORT_GOOD17# Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = PEX_PORT_GOOD17# Interrupt input is Active-Low 1 = PEX_PORT_GOOD17# Interrupt input is Active-High	RWS	Yes	0
6	**PEX_PORT_GOOD18# Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = PEX_PORT_GOOD18# Interrupt input is Active-Low 1 = PEX_PORT_GOOD18# Interrupt input is Active-High	RWS	Yes	0
7	**PEX_PORT_GOOD19# Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = PEX_PORT_GOOD19# Interrupt input is Active-Low 1 = PEX_PORT_GOOD19# Interrupt input is Active-High	RWS	Yes	0

Register 13-128. 62Ch GPIO 0_11 Interrupt Polarity (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) ***(Cont.)***

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
8	**PEX_PORT_GOOD20# Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = PEX_PORT_GOOD20# Interrupt input is Active-Low 1 = PEX_PORT_GOOD20# Interrupt input is Active-High	RWS	Yes	0
9	**PEX_PORT_GOOD21# Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = PEX_PORT_GOOD21# Interrupt input is Active-Low 1 = PEX_PORT_GOOD21# Interrupt input is Active-High	RWS	Yes	0
10	**PEX_PORT_GOOD22# Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = PEX_PORT_GOOD22# Interrupt input is Active-Low 1 = PEX_PORT_GOOD22# Interrupt input is Active-High	RWS	Yes	0
11	**PEX_PORT_GOOD23# Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = PEX_PORT_GOOD23# Interrupt input is Active-Low 1 = PEX_PORT_GOOD23# Interrupt input is Active-High	RWS	Yes	0
31:12	***Reserved***	RsvdP	No	0000_0h

Register 13-129. 630h GPIO 24_31 Interrupt Polarity (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
The GPIO 24_31 **Interrupt Polarity** registers control the GPIO[24:31] Interrupt input polarities, respectively.				
0	**GPIO24 Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = GPIO24 Interrupt input is Active-Low 1 = GPIO24 Interrupt input is Active-High	RWS	Yes	0
1	**GPIO25 Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = GPIO25 Interrupt input is Active-Low 1 = GPIO25 Interrupt input is Active-High	RWS	Yes	0
2	**GPIO26 Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = GPIO26 Interrupt input is Active-Low 1 = GPIO26 Interrupt input is Active-High	RWS	Yes	0
3	**GPIO27 Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = GPIO27 Interrupt input is Active-Low 1 = GPIO27 Interrupt input is Active-High	RWS	Yes	0
4	**GPIO28 Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = GPIO28 Interrupt input is Active-Low 1 = GPIO28 Interrupt input is Active-High	RWS	Yes	0
5	**GPIO29 Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = GPIO29 Interrupt input is Active-Low 1 = GPIO29 Interrupt input is Active-High	RWS	Yes	0
6	**GPIO30 Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = GPIO30 Interrupt input is Active-Low 1 = GPIO30 Interrupt input is Active-High	RWS	Yes	0
7	**GPIO31 Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High. 0 = GPIO31 Interrupt input is Active-Low 1 = GPIO31 Interrupt input is Active-High	RWS	Yes	0
31:8	***Reserved***	RsvdP	No	0000_00h

Register 13-130. 634h GPIO 0_11 Interrupt Status (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
The PEX_PORT_GOOD[0:3, 16:23]# Interrupt input status values are updated into the GPIO 0_11 **Interrupt Status** registers, respectively. Interrupt status remains Set, as long the corresponding PEX_PORT_GOOD*x*# signal is asserted, and Clears on its own when the corresponding PEX_PORT_GOOD*x*# input de-asserts to the inactive state. The active state of each interrupt is controlled by its respective **GPIO 0_11 Interrupt Polarity** register bit (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 62Ch). ***Note:*** *The bits in this register can be masked by their respective **GPIO 0_11 Interrupt Mask** register bits (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 63Ch).*				
0	**PEX_PORT_GOOD0# Interrupt Status** Indicates whether GPIO interrupts are inactive or active. 0 = PEX_PORT_GOOD0# interrupt is inactive 1 = PEX_PORT_GOOD0# interrupt is active	RO	No	0
1	**PEX_PORT_GOOD1# Interrupt Status** Indicates whether GPIO interrupts are inactive or active. 0 = PEX_PORT_GOOD1# interrupt is inactive 1 = PEX_PORT_GOOD1# interrupt is active	RO	No	0
2	**PEX_PORT_GOOD2# Interrupt Status** Indicates whether GPIO interrupts are inactive or active. 0 = PEX_PORT_GOOD2# interrupt is inactive 1 = PEX_PORT_GOOD2# interrupt is active	RO	No	0
3	**PEX_PORT_GOOD3# Interrupt Status** Indicates whether GPIO interrupts are inactive or active. 0 = PEX_PORT_GOOD3# interrupt is inactive 1 = PEX_PORT_GOOD3# interrupt is active	RO	No	0

Register 13-130. 634h GPIO 0_11 Interrupt Status
(Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) ***(Cont.)***

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
4	**PEX_PORT_GOOD16# Interrupt Status** Indicates whether GPIO interrupts are inactive or active. 0 = PEX_PORT_GOOD16# interrupt is inactive 1 = PEX_PORT_GOOD16# interrupt is active	RO	No	0
5	**PEX_PORT_GOOD17# Interrupt Status** Indicates whether GPIO interrupts are inactive or active. 0 = PEX_PORT_GOOD17# interrupt is inactive 1 = PEX_PORT_GOOD17# interrupt is active	RO	No	0
6	**PEX_PORT_GOOD18# Interrupt Status** Indicates whether GPIO interrupts are inactive or active. 0 = PEX_PORT_GOOD18# interrupt is inactive 1 = PEX_PORT_GOOD18# interrupt is active	RO	No	0
7	**PEX_PORT_GOOD19# Interrupt Status** Indicates whether GPIO interrupts are inactive or active. 0 = PEX_PORT_GOOD19# interrupt is inactive 1 = PEX_PORT_GOOD19# interrupt is active	RO	No	0
8	**PEX_PORT_GOOD20# Interrupt Status** Indicates whether GPIO interrupts are inactive or active. 0 = PEX_PORT_GOOD20# interrupt is inactive 1 = PEX_PORT_GOOD20# interrupt is active	RO	No	0
9	**PEX_PORT_GOOD21# Interrupt Status** Indicates whether GPIO interrupts are inactive or active. 0 = PEX_PORT_GOOD21# interrupt is inactive 1 = PEX_PORT_GOOD21# interrupt is active	RO	No	0
10	**PEX_PORT_GOOD22# Interrupt Status** Indicates whether GPIO interrupts are inactive or active. 0 = PEX_PORT_GOOD22# interrupt is inactive 1 = PEX_PORT_GOOD22# interrupt is active	RO	No	0
11	**PEX_PORT_GOOD23# Interrupt Status** Indicates whether GPIO interrupts are inactive or active. 0 = PEX_PORT_GOOD23# interrupt is inactive 1 = PEX_PORT_GOOD23# interrupt is active	RO	No	0
31:12	***Reserved***	RsvdP	No	0000_0h

Register 13-131. 638h GPIO 24_31 Interrupt Status (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
The GPIO[24:31] Interrupt input status values are updated into the GPIO 24_31 **Interrupt Status** registers, respectively. Interrupt status remains Set, as long the corresponding GPIO*x* signal is asserted, and Clears on its own when the corresponding GPIO*x* input de-asserts to the inactive state. The active state of each interrupt is controlled by its respective **GPIO 24_31 Interrupt Polarity** register bit (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 630h). ***Note:*** *The bits in this register can be masked by their respective **GPIO 24_31 Interrupt Mask** register bits (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 640h).*				
0	**GPIO24 Interrupt Status** Indicates whether GPIO interrupts are inactive or active. 0 = GPIO24 interrupt is inactive 1 = GPIO24 interrupt is active	RO	No	0
1	**GPIO25 Interrupt Status** Indicates whether GPIO interrupts are inactive or active. 0 = GPIO25 interrupt is inactive 1 = GPIO25 interrupt is active	RO	No	0
2	**GPIO26 Interrupt Status** Indicates whether GPIO interrupts are inactive or active. 0 = GPIO26 interrupt is inactive 1 = GPIO26 interrupt is active	RO	No	0
3	**GPIO27 Interrupt Status** Indicates whether GPIO interrupts are inactive or active. 0 = GPIO27 interrupt is inactive 1 = GPIO27 interrupt is active	RO	No	0

Register 13-131. 638h GPIO 24_31 Interrupt Status (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4	**GPIO28 Interrupt Status** Indicates whether GPIO interrupts are inactive or active. 0 = GPIO28 interrupt is inactive 1 = GPIO28 interrupt is active	RO	No	0
5	**GPIO29 Interrupt Status** Indicates whether GPIO interrupts are inactive or active. 0 = GPIO29 interrupt is inactive 1 = GPIO29 interrupt is active	RO	No	0
6	**GPIO30 Interrupt Status** Indicates whether GPIO interrupts are inactive or active. 0 = GPIO30 interrupt is inactive 1 = GPIO30 interrupt is active	RO	No	0
7	**GPIO31 Interrupt Status** Indicates whether GPIO interrupts are inactive or active. 0 = GPIO31 interrupt is inactive 1 = GPIO31 interrupt is active	RO	No	0
31:8	***Reserved***	RsvdP	No	0000_00h

Register 13-132. 63Ch GPIO 0_11 Interrupt Mask (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
The PEX_PORT_GOOD[0:3, 16:23]# Interrupt inputs are masked, using the GPIO 0_11 **Interrupt Mask** registers, respectively. ***Note:*** *The bits in this register can be used to mask their respective* ***GPIO 0_11 Interrupt Status*** *register bits (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 634h).*				
0	**PEX_PORT_GOOD0# Interrupt Mask** Indicates whether GPIO interrupts are masked or not masked. 0 = PEX_PORT_GOOD0# interrupt is not masked. 1 = PEX_PORT_GOOD0# interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
1	**PEX_PORT_GOOD1# Interrupt Mask** Indicates whether GPIO interrupts are masked or not masked. 0 = PEX_PORT_GOOD1# interrupt is not masked. 1 = PEX_PORT_GOOD1# interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
2	**PEX_PORT_GOOD2# Interrupt Mask** Indicates whether GPIO interrupts are masked or not masked. 0 = PEX_PORT_GOOD2# interrupt is not masked. 1 = PEX_PORT_GOOD2# interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
3	**PEX_PORT_GOOD3# Interrupt Mask** Indicates whether GPIO interrupts are masked or not masked. 0 = PEX_PORT_GOOD3# interrupt is not masked. 1 = PEX_PORT_GOOD3# interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1

Register 13-132. 63Ch GPIO 0_11 Interrupt Mask (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4	**PEX_PORT_GOOD16# Interrupt Mask** Indicates whether GPIO interrupts are masked or not masked. 0 = PEX_PORT_GOOD16# interrupt is not masked. 1 = PEX_PORT_GOOD16# interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
5	**PEX_PORT_GOOD17# Interrupt Mask** Indicates whether GPIO interrupts are masked or not masked. 0 = PEX_PORT_GOOD17# interrupt is not masked. 1 = PEX_PORT_GOOD17# interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
6	**PEX_PORT_GOOD18# Interrupt Mask** Indicates whether GPIO interrupts are masked or not masked. 0 = PEX_PORT_GOOD18# interrupt is not masked. 1 = PEX_PORT_GOOD18# interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
7	**PEX_PORT_GOOD19# Interrupt Mask** Indicates whether GPIO interrupts are masked or not masked. 0 = PEX_PORT_GOOD19# interrupt is not masked. 1 = PEX_PORT_GOOD19# interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
8	**PEX_PORT_GOOD20# Interrupt Mask** Indicates whether GPIO interrupts are masked or not masked. 0 = PEX_PORT_GOOD20# interrupt is not masked. 1 = PEX_PORT_GOOD20# interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
9	**PEX_PORT_GOOD21# Interrupt Mask** Indicates whether GPIO interrupts are masked or not masked. 0 = PEX_PORT_GOOD21# interrupt is not masked. 1 = PEX_PORT_GOOD21# interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
10	**PEX_PORT_GOOD22# Interrupt Mask** Indicates whether GPIO interrupts are masked or not masked. 0 = PEX_PORT_GOOD22# interrupt is not masked. 1 = PEX_PORT_GOOD22# interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
11	**PEX_PORT_GOOD23# Interrupt Mask** Indicates whether GPIO interrupts are masked or not masked. 0 = PEX_PORT_GOOD23# interrupt is not masked. 1 = PEX_PORT_GOOD23# interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
31:12	***Reserved***	RsvdP	No	0000_0h

Register 13-133. 640h GPIO 24_31 Interrupt Mask (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port)

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I^2C</th><th>Default</th></tr>
<tr><td colspan="5">The GPIO[24:31] Interrupt inputs are masked, using the GPIO 24_31 <b>Interrupt Mask</b> registers, respectively.
<b><i>Note:</i></b> <i>The bits in this register can be used to mask their respective <b>GPIO 24_31 Interrupt Status</b> register bits (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 638h).</i></td></tr>
<tr><td>0</td><td><b>GPIO24 Interrupt Mask</b>
Indicates whether GPIO interrupts are masked or not masked.
0 = GPIO24 interrupt is not masked.
1 = GPIO24 interrupt is masked. When an interrupt is masked, the corresponding <b>Interrupt Status</b> register is not updated.</td><td>RWS</td><td>Yes</td><td>1</td></tr>
<tr><td>1</td><td><b>GPIO25 Interrupt Mask</b>
Indicates whether GPIO interrupts are masked or not masked.
0 = GPIO25 interrupt is not masked.
1 = GPIO25 interrupt is masked. When an interrupt is masked, the corresponding <b>Interrupt Status</b> register is not updated.</td><td>RWS</td><td>Yes</td><td>1</td></tr>
<tr><td>2</td><td><b>GPIO26 Interrupt Mask</b>
Indicates whether GPIO interrupts are masked or not masked.
0 = GPIO26 interrupt is not masked.
1 = GPIO26 interrupt is masked. When an interrupt is masked, the corresponding <b>Interrupt Status</b> register is not updated.</td><td>RWS</td><td>Yes</td><td>1</td></tr>
<tr><td>3</td><td><b>GPIO27 Interrupt Mask</b>
Indicates whether GPIO interrupts are masked or not masked.
0 = GPIO27 interrupt is not masked.
1 = GPIO27 interrupt is masked. When an interrupt is masked, the corresponding <b>Interrupt Status</b> register is not updated.</td><td>RWS</td><td>Yes</td><td>1</td></tr>
</table>

Register 13-133. 640h GPIO 24_31 Interrupt Mask (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
4	**GPIO28 Interrupt Mask** Indicates whether GPIO interrupts are masked or not masked. 0 = GPIO28 interrupt is not masked. 1 = GPIO28 interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
5	**GPIO29 Interrupt Mask** Indicates whether GPIO interrupts are masked or not masked. 0 = GPIO29 interrupt is not masked. 1 = GPIO29 interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
6	**GPIO30 Interrupt Mask** Indicates whether GPIO interrupts are masked or not masked. 0 = GPIO30 interrupt is not masked. 1 = GPIO30 interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
7	**GPIO31 Interrupt Mask** Indicates whether GPIO interrupts are masked or not masked. 0 = GPIO31 interrupt is not masked. 1 = GPIO31 interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
31:8	***Reserved***	RsvdP	No	0000_00h

Register 13-134. 64Ch Virtual Switch GPIO Update (Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
0	**VS GPIOs Update** After the Management Port, serial EEPROM, and/or I²C/SMBus configures the PEX_PORT_GOOD*x*# and GPIO*x* signals, and assigns these individual signals to various virtual switches, by programming the **VS*x* GPIO_PG 0_11 Assignment** and **VS*x* GPIO_SHP 0_7 Assignment** registers (Port 0, accessible through the Management Port, offsets 650h through 65Ch, and 670h through 67Ch, respectively), Set this bit to cause the GPIO assignments to take effect.	RW1CS	Yes	0
31:1	***Reserved***	RsvdP	No	0-0h

Register 13-135. 650h VS0 GPIO_PG 0_11 Assignment (Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
The LSB that is Set is assigned to GPIO_PG 0 of VS0, the next lowest LSB that is Set is assigned to GPIO_PG 1 of VS0, and so forth. A maximum of 12 GPIO_PG signals can be assigned to any virtual switch. A single GPIO_PG signal cannot be assigned to more than one virtual switch. The PEX_PORT_GOOD[0:3, 16:23]# signals correspond to GPIO_PG 0_11, respectively.				
0	**VS0 GPIO_PG 0 Assignment** 0 = PEX_PORT_GOOD0# is not assigned to VS0 1 = PEX_PORT_GOOD0# is assigned to VS0	RWS	Yes	BALL
1	**VS0 GPIO_PG 1 Assignment** 0 = PEX_PORT_GOOD1# is not assigned to VS0 1 = PEX_PORT_GOOD1# is assigned to VS0	RWS	Yes	BALL
2	**VS0 GPIO_PG 2 Assignment** 0 = PEX_PORT_GOOD2# is not assigned to VS0 1 = PEX_PORT_GOOD2# is assigned to VS0	RWS	Yes	BALL
3	**VS0 GPIO_PG 3 Assignment** 0 = PEX_PORT_GOOD3# is not assigned to VS0 1 = PEX_PORT_GOOD3# is assigned to VS0	RWS	Yes	BALL
4	**VS0 GPIO_PG 4 Assignment** 0 = PEX_PORT_GOOD16# is not assigned to VS0 1 = PEX_PORT_GOOD16# is assigned to VS0	RWS	Yes	BALL
5	**VS0 GPIO_PG 5 Assignment** 0 = PEX_PORT_GOOD17# is not assigned to VS0 1 = PEX_PORT_GOOD17# is assigned to VS0	RWS	Yes	BALL
6	**VS0 GPIO_PG 6 Assignment** 0 = PEX_PORT_GOOD18# is not assigned to VS0 1 = PEX_PORT_GOOD18# is assigned to VS0	RWS	Yes	BALL
7	**VS0 GPIO_PG 7 Assignment** 0 = PEX_PORT_GOOD19# is not assigned to VS0 1 = PEX_PORT_GOOD19# is assigned to VS0	RWS	Yes	BALL

Register 13-135. 650h VS0 GPIO_PG 0_11 Assignment (Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
8	**VS0 GPIO_PG 8 Assignment** 0 = PEX_PORT_GOOD20# is not assigned to VS0 1 = PEX_PORT_GOOD20# is assigned to VS0	RWS	Yes	BALL
9	**VS0 GPIO_PG 9 Assignment** 0 = PEX_PORT_GOOD21# is not assigned to VS0 1 = PEX_PORT_GOOD21# is assigned to VS0	RWS	Yes	BALL
10	**VS0 GPIO_PG 10 Assignment** 0 = PEX_PORT_GOOD22# is not assigned to VS0 1 = PEX_PORT_GOOD22# is assigned to VS0	RWS	Yes	BALL
11	**VS0 GPIO_PG 11 Assignment** 0 = PEX_PORT_GOOD23# is not assigned to VS0 1 = PEX_PORT_GOOD23# is assigned to VS0	RWS	Yes	BALL
31:12	***Reserved***	RsvdP	No	0000_0h

Register 13-136. 654h VS1 GPIO_PG 0_11 Assignment (Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The LSB that is Set is assigned to GPIO_PG 0 of VS1, the next lowest LSB that is Set is assigned to GPIO_PG 1 of VS1, and so forth. A maximum of 12 GPIO_PG signals can be assigned to any virtual switch. A single GPIO_PG signal cannot be assigned to more than one virtual switch. The PEX_PORT_GOOD[0:3, 16:23]# signals correspond to GPIO_PG 0_11, respectively.				
0	**VS1 GPIO_PG 0 Assignment** 0 = PEX_PORT_GOOD0# is not assigned to VS1 1 = PEX_PORT_GOOD0# is assigned to VS1	RWS	Yes	BALL
1	**VS1 GPIO_PG 1 Assignment** 0 = PEX_PORT_GOOD1# is not assigned to VS1 1 = PEX_PORT_GOOD1# is assigned to VS1	RWS	Yes	BALL
2	**VS1 GPIO_PG 2 Assignment** 0 = PEX_PORT_GOOD2# is not assigned to VS1 1 = PEX_PORT_GOOD2# is assigned to VS1	RWS	Yes	BALL
3	**VS1 GPIO_PG 3 Assignment** 0 = PEX_PORT_GOOD3# is not assigned to VS1 1 = PEX_PORT_GOOD3# is assigned to VS1	RWS	Yes	BALL
4	**VS1 GPIO_PG 4 Assignment** 0 = PEX_PORT_GOOD16# is not assigned to VS1 1 = PEX_PORT_GOOD16# is assigned to VS1	RWS	Yes	BALL
5	**VS1 GPIO_PG 5 Assignment** 0 = PEX_PORT_GOOD17# is not assigned to VS1 1 = PEX_PORT_GOOD17# is assigned to VS1	RWS	Yes	BALL
6	**VS1 GPIO_PG 6 Assignment** 0 = PEX_PORT_GOOD18# is not assigned to VS1 1 = PEX_PORT_GOOD18# is assigned to VS1	RWS	Yes	BALL
7	**VS1 GPIO_PG 7 Assignment** 0 = PEX_PORT_GOOD19# is not assigned to VS1 1 = PEX_PORT_GOOD19# is assigned to VS1	RWS	Yes	BALL
8	**VS1 GPIO_PG 8 Assignment** 0 = PEX_PORT_GOOD20# is not assigned to VS1 1 = PEX_PORT_GOOD20# is assigned to VS1	RWS	Yes	BALL
9	**VS1 GPIO_PG 9 Assignment** 0 = PEX_PORT_GOOD21# is not assigned to VS1 1 = PEX_PORT_GOOD21# is assigned to VS1	RWS	Yes	BALL
10	**VS1 GPIO_PG 10 Assignment** 0 = PEX_PORT_GOOD22# is not assigned to VS1 1 = PEX_PORT_GOOD22# is assigned to VS1	RWS	Yes	BALL
11	**VS1 GPIO_PG 11 Assignment** 0 = PEX_PORT_GOOD23# is not assigned to VS1 1 = PEX_PORT_GOOD23# is assigned to VS1	RWS	Yes	BALL
31:12	***Reserved***	RsvdP	No	0000_0h

Register 13-137. 658h VS2 GPIO_PG 0_11 Assignment (Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The LSB that is Set is assigned to GPIO_PG 0 of VS2, the next lowest LSB that is Set is assigned to GPIO_PG 1 of VS2, and so forth. A maximum of 12 GPIO_PG signals can be assigned to any virtual switch. A single GPIO_PG signal cannot be assigned to more than one virtual switch. The PEX_PORT_GOOD[0:3, 16:23]# signals correspond to GPIO_PG 0_11, respectively.				
0	**VS2 GPIO_PG 0 Assignment** 0 = PEX_PORT_GOOD0# is not assigned to VS2 1 = PEX_PORT_GOOD0# is assigned to VS2	RWS	Yes	BALL
1	**VS2 GPIO_PG 1 Assignment** 0 = PEX_PORT_GOOD1# is not assigned to VS2 1 = PEX_PORT_GOOD1# is assigned to VS2	RWS	Yes	BALL
2	**VS2 GPIO_PG 2 Assignment** 0 = PEX_PORT_GOOD2# is not assigned to VS2 1 = PEX_PORT_GOOD2# is assigned to VS2	RWS	Yes	BALL
3	**VS2 GPIO_PG 3 Assignment** 0 = PEX_PORT_GOOD3# is not assigned to VS2 1 = PEX_PORT_GOOD3# is assigned to VS2	RWS	Yes	BALL
4	**VS2 GPIO_PG 4 Assignment** 0 = PEX_PORT_GOOD16# is not assigned to VS2 1 = PEX_PORT_GOOD16# is assigned to VS2	RWS	Yes	BALL
5	**VS2 GPIO_PG 5 Assignment** 0 = PEX_PORT_GOOD17# is not assigned to VS2 1 = PEX_PORT_GOOD17# is assigned to VS2	RWS	Yes	BALL
6	**VS2 GPIO_PG 6 Assignment** 0 = PEX_PORT_GOOD18# is not assigned to VS2 1 = PEX_PORT_GOOD18# is assigned to VS2	RWS	Yes	BALL
7	**VS2 GPIO_PG 7 Assignment** 0 = PEX_PORT_GOOD19# is not assigned to VS2 1 = PEX_PORT_GOOD19# is assigned to VS2	RWS	Yes	BALL
8	**VS2 GPIO_PG 8 Assignment** 0 = PEX_PORT_GOOD20# is not assigned to VS2 1 = PEX_PORT_GOOD20# is assigned to VS2	RWS	Yes	BALL
9	**VS2 GPIO_PG 9 Assignment** 0 = PEX_PORT_GOOD21# is not assigned to VS2 1 = PEX_PORT_GOOD21# is assigned to VS2	RWS	Yes	BALL
10	**VS2 GPIO_PG 10 Assignment** 0 = PEX_PORT_GOOD22# is not assigned to VS2 1 = PEX_PORT_GOOD22# is assigned to VS2	RWS	Yes	BALL
11	**VS2 GPIO_PG 11 Assignment** 0 = PEX_PORT_GOOD23# is not assigned to VS2 1 = PEX_PORT_GOOD23# is assigned to VS2	RWS	Yes	BALL
31:12	***Reserved***	RsvdP	No	0000_0h

Register 13-138. 65Ch VS3 GPIO_PG 0_11 Assignment (Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The LSB that is Set is assigned to GPIO_PG 0 of VS3, the next lowest LSB that is Set is assigned to GPIO_PG 1 of VS3, and so forth. A maximum of 12 GPIO_PG signals can be assigned to any virtual switch. A single GPIO_PG signal cannot be assigned to more than one virtual switch. The PEX_PORT_GOOD[0:3, 16:23]# signals correspond to GPIO_PG 0_11, respectively.				
0	**VS3 GPIO_PG 0 Assignment** 0 = PEX_PORT_GOOD0# is not assigned to VS3 1 = PEX_PORT_GOOD0# is assigned to VS3	RWS	Yes	BALL
1	**VS3 GPIO_PG 1 Assignment** 0 = PEX_PORT_GOOD1# is not assigned to VS3 1 = PEX_PORT_GOOD1# is assigned to VS3	RWS	Yes	BALL
2	**VS3 GPIO_PG 2 Assignment** 0 = PEX_PORT_GOOD2# is not assigned to VS3 1 = PEX_PORT_GOOD2# is assigned to VS3	RWS	Yes	BALL
3	**VS3 GPIO_PG 3 Assignment** 0 = PEX_PORT_GOOD3# is not assigned to VS3 1 = PEX_PORT_GOOD3# is assigned to VS3	RWS	Yes	BALL
4	**VS3 GPIO_PG 4 Assignment** 0 = PEX_PORT_GOOD16# is not assigned to VS3 1 = PEX_PORT_GOOD16# is assigned to VS3	RWS	Yes	BALL
5	**VS3 GPIO_PG 5 Assignment** 0 = PEX_PORT_GOOD17# is not assigned to VS3 1 = PEX_PORT_GOOD17# is assigned to VS3	RWS	Yes	BALL
6	**VS3 GPIO_PG 6 Assignment** 0 = PEX_PORT_GOOD18# is not assigned to VS3 1 = PEX_PORT_GOOD18# is assigned to VS3	RWS	Yes	BALL
7	**VS3 GPIO_PG 7 Assignment** 0 = PEX_PORT_GOOD19# is not assigned to VS3 1 = PEX_PORT_GOOD19# is assigned to VS3	RWS	Yes	BALL
8	**VS3 GPIO_PG 8 Assignment** 0 = PEX_PORT_GOOD20# is not assigned to VS3 1 = PEX_PORT_GOOD20# is assigned to VS3	RWS	Yes	BALL
9	**VS3 GPIO_PG 9 Assignment** 0 = PEX_PORT_GOOD21# is not assigned to VS3 1 = PEX_PORT_GOOD21# is assigned to VS3	RWS	Yes	BALL
10	**VS3 GPIO_PG 10 Assignment** 0 = PEX_PORT_GOOD22# is not assigned to VS3 1 = PEX_PORT_GOOD22# is assigned to VS3	RWS	Yes	BALL
11	**VS3 GPIO_PG 11 Assignment** 0 = PEX_PORT_GOOD23# is not assigned to VS3 1 = PEX_PORT_GOOD23# is assigned to VS3	RWS	Yes	BALL
31:12	***Reserved***	RsvdP	No	0000_0h

Register 13-139. 670h VS0 GPIO_SHP 0_7 Assignment (Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The LSB that is Set is assigned to GPIO_SHP 0 of VS0, the next lowest LSB that is Set is assigned to GPIO_SHP 1 of VS0, and so forth. A maximum of eight GPIO_SHP signals can be assigned to any virtual switch. A single GPIO_SHP signal cannot be assigned to more than one virtual switch. The GPIO[24:31] signals correspond to GPIO_SHP 0_7, respectively.				
0	**VS0 GPIO_SHP 0 Assignment** 0 = GPIO24 is not assigned to VS0 1 = GPIO24 is assigned to VS0	RWS	Yes	BALL
1	**VS0 GPIO_SHP 1 Assignment** 0 = GPIO25 is not assigned to VS0 1 = GPIO25 is assigned to VS0	RWS	Yes	BALL
2	**VS0 GPIO_SHP 2 Assignment** 0 = GPIO26 is not assigned to VS0 1 = GPIO26 is assigned to VS0	RWS	Yes	BALL
3	**VS0 GPIO_SHP 3 Assignment** 0 = GPIO27 is not assigned to VS0 1 = GPIO27 is assigned to VS0	RWS	Yes	BALL
4	**VS0 GPIO_SHP 4 Assignment** 0 = GPIO28 is not assigned to VS0 1 = GPIO28 is assigned to VS0	RWS	Yes	BALL
5	**VS0 GPIO_SHP 5 Assignment** 0 = GPIO29 is not assigned to VS0 1 = GPIO29 is assigned to VS0	RWS	Yes	BALL
6	**VS0 GPIO_SHP 6 Assignment** 0 = GPIO30 is not assigned to VS0 1 = GPIO30 is assigned to VS0	RWS	Yes	BALL
7	**VS0 GPIO_SHP 7 Assignment** 0 = GPIO31 is not assigned to VS0 1 = GPIO31 is assigned to VS0	RWS	Yes	BALL
31:8	***Reserved***	RsvdP	No	0000_00h

Register 13-140. 674h VS1 GPIO_SHP 0_7 Assignment (Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The LSB that is Set is assigned to GPIO_SHP 0 of VS1, the next lowest LSB that is Set is assigned to GPIO_SHP 1 of VS1, and so forth. A maximum of eight GPIO_SHP signals can be assigned to any virtual switch. A single GPIO_SHP signal cannot be assigned to more than one virtual switch. The GPIO[24:31] signals correspond to GPIO_SHP 0_7, respectively.				
0	**VS1 GPIO_SHP 0 Assignment** 0 = GPIO24 is not assigned to VS1 1 = GPIO24 is assigned to VS1	RWS	Yes	BALL
1	**VS1 GPIO_SHP 1 Assignment** 0 = GPIO25 is not assigned to VS1 1 = GPIO25 is assigned to VS1	RWS	Yes	BALL
2	**VS1 GPIO_SHP 2 Assignment** 0 = GPIO26 is not assigned to VS1 1 = GPIO26 is assigned to VS1	RWS	Yes	BALL
3	**VS1 GPIO_SHP 3 Assignment** 0 = GPIO27 is not assigned to VS1 1 = GPIO27 is assigned to VS1	RWS	Yes	BALL
4	**VS1 GPIO_SHP 4 Assignment** 0 = GPIO28 is not assigned to VS1 1 = GPIO28 is assigned to VS1	RWS	Yes	BALL
5	**VS1 GPIO_SHP 5 Assignment** 0 = GPIO29 is not assigned to VS1 1 = GPIO29 is assigned to VS1	RWS	Yes	BALL
6	**VS1 GPIO_SHP 6 Assignment** 0 = GPIO30 is not assigned to VS1 1 = GPIO30 is assigned to VS1	RWS	Yes	BALL
7	**VS1 GPIO_SHP 7 Assignment** 0 = GPIO31 is not assigned to VS1 1 = GPIO31 is assigned to VS1	RWS	Yes	BALL
31:8	***Reserved***	RsvdP	No	0000_00h

Register 13-141. 678h VS2 GPIO_SHP 0_7 Assignment (Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
The LSB that is Set is assigned to GPIO_SHP 0 of VS2, the next lowest LSB that is Set is assigned to GPIO_SHP 1 of VS2, and so forth. A maximum of eight GPIO_SHP signals can be assigned to any virtual switch. A single GPIO_SHP signal cannot be assigned to more than one virtual switch. The GPIO[24:31] signals correspond to GPIO_SHP 0_7, respectively.				
0	**VS2 GPIO_SHP 0 Assignment** 0 = GPIO24 is not assigned to VS2 1 = GPIO24 is assigned to VS2	RWS	Yes	BALL
1	**VS2 GPIO_SHP 1 Assignment** 0 = GPIO25 is not assigned to VS2 1 = GPIO25 is assigned to VS2	RWS	Yes	BALL
2	**VS2 GPIO_SHP 2 Assignment** 0 = GPIO26 is not assigned to VS2 1 = GPIO26 is assigned to VS2	RWS	Yes	BALL
3	**VS2 GPIO_SHP 3 Assignment** 0 = GPIO27 is not assigned to VS2 1 = GPIO27 is assigned to VS2	RWS	Yes	BALL
4	**VS2 GPIO_SHP 4 Assignment** 0 = GPIO28 is not assigned to VS2 1 = GPIO28 is assigned to VS2	RWS	Yes	BALL
5	**VS2 GPIO_SHP 5 Assignment** 0 = GPIO29 is not assigned to VS2 1 = GPIO29 is assigned to VS2	RWS	Yes	BALL
6	**VS2 GPIO_SHP 6 Assignment** 0 = GPIO30 is not assigned to VS2 1 = GPIO30 is assigned to VS2	RWS	Yes	BALL
7	**VS2 GPIO_SHP 7 Assignment** 0 = GPIO31 is not assigned to VS2 1 = GPIO31 is assigned to VS2	RWS	Yes	BALL
31:8	***Reserved***	RsvdP	No	0000_00h

Register 13-142. 67Ch VS3 GPIO_SHP 0_7 Assignment (Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The LSB that is Set is assigned to GPIO_SHP 0 of VS3, the next lowest LSB that is Set is assigned to GPIO_SHP 1 of VS3, and so forth. A maximum of eight GPIO_SHP signals can be assigned to any virtual switch. A single GPIO_SHP signal cannot be assigned to more than one virtual switch. The GPIO[24:31] signals correspond to GPIO_SHP 0_7, respectively.				
0	**VS3 GPIO_SHP 0 Assignment** 0 = GPIO24 is not assigned to VS3 1 = GPIO24 is assigned to VS3	RWS	Yes	BALL
1	**VS3 GPIO_SHP 1 Assignment** 0 = GPIO25 is not assigned to VS3 1 = GPIO25 is assigned to VS3	RWS	Yes	BALL
2	**VS3 GPIO_SHP 2 Assignment** 0 = GPIO26 is not assigned to VS3 1 = GPIO26 is assigned to VS3	RWS	Yes	BALL
3	**VS3 GPIO_SHP 3 Assignment** 0 = GPIO27 is not assigned to VS3 1 = GPIO27 is assigned to VS3	RWS	Yes	BALL
4	**VS3 GPIO_SHP 4 Assignment** 0 = GPIO28 is not assigned to VS3 1 = GPIO28 is assigned to VS3	RWS	Yes	BALL
5	**VS3 GPIO_SHP 5 Assignment** 0 = GPIO29 is not assigned to VS3 1 = GPIO29 is assigned to VS3	RWS	Yes	BALL
6	**VS3 GPIO_SHP 6 Assignment** 0 = GPIO30 is not assigned to VS3 1 = GPIO30 is assigned to VS3	RWS	Yes	BALL
7	**VS3 GPIO_SHP 7 Assignment** 0 = GPIO31 is not assigned to VS3 1 = GPIO31 is assigned to VS3	RWS	Yes	BALL
31:8	***Reserved***	RsvdP	No	0000_00h

13.15.10 Device-Specific Registers – Error Checking and Debug (Offsets 700h – 75Ch)

This section details the Device-Specific Error Checking and Debug registers located at offsets 700h through 75Ch. Table 13-29 defines the register map.

Other Device-Specific Error Checking and Debug registers are detailed in:

- Section 13.15.7, “Device-Specific Registers – Error Checking and Debug (Offsets 320h – 350h)”
- Section 13.19.3, “Device-Specific Registers – Error Checking and Debug (Offsets F70h – FB0h)”

Table 13-29. Device-Specific Error Checking and Debug Register Map (Offsets 700h – 75Ch) (Ports[a])

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Device-Specific Error Status 1		700h
Device-Specific Error Mask 1		704h
Device-Specific Error Status 2		708h
Device-Specific Error Mask 2		70Ch
Reserved	Device-Specific Error Status 3	710h
Reserved	Device-Specific Error Mask 3	714h
Reserved	Device-Specific Error Status 4	718h
Reserved	Device-Specific Error Mask 4	71Ch
ECC Error Check Disable		720h
Reserved		724h – 75Ch

[a] *Certain registers are Port-specific, others are Station-specific or Chip-specific; all are Device-specific.*

Register 13-143. 700h Device-Specific Error Status 1 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

ECC is checked by the egress Port, and any ECC error is reported by the egress Station (containing the egress Port), when that Port reads the Packet data from the ingress Station RAM. *For example*, when Port 16 receives a packet, the data is stored in Station 4 RAM; then, if the egress Port is in Station 0 and an ECC error is detected when the Port reads the Station 4 RAM, the error is flagged in the Port 0 register bit that reflects Station 4 error status.

Notes: *The bits in this register can be masked by their respective* ***Device-Specific Error Mask 1*** *register bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 704h, with the exception of bit 0, which is in all Ports).*

All errors in this register generate ERR_FATAL or ERR_NONFATAL Messages, if enabled by the following:

- ***Device-Specific Error Mask 1*** *register (Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface, offset 704h*
- ***Uncorrectable Error Status*** *register Uncorrectable Internal Error Status bit (All Ports, offset FB8h[22], is Set)*
- ***Device Status*** *register Fatal Error Reporting Enable and Non-Fatal Error Reporting Enable bits (All Ports, offset 70h[2:1], respectively)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
0	**Completion FIFO Overflow Status** 0 = No overflow is detected 1 = Completion FIFO Overflow is detected when 4-deep Completion FIFO for ingress, or 1-deep Completion FIFO for egress, overflows	All	RW1CS	Yes	0
1	***Factory Test Only***	0	RW1CS	No	0
2	**Station 0 Egress Packet Link List RAM 1-Bit ECC Error Detected** 0 = No 1-Bit ECC error is detected 1 = Soft error is detected		RW1CS	Yes	0
5:3	***Reserved***		RsvdP	No	000b
6	**Station 4 Egress Packet Link List RAM 1-Bit ECC Error Detected** 0 = No 1-Bit ECC error is detected 1 = Soft error is detected		RW1CS	Yes	0
7	**Station 5 Egress Packet Link List RAM 1-Bit ECC Error Detected** 0 = No 1-Bit ECC error is detected 1 = Soft error is detected		RW1CS	Yes	0
8	**Station 0 Header RAM Soft Error Counter Overflow Detected** 0 = No overflow is detected 1 = Soft error is detected		RW1CS	Yes	0
11:9	***Reserved***		RsvdP	No	000b

Register 13-143. 700h Device-Specific Error Status 1 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
12	**Station 4 Header RAM Soft Error Counter Overflow Detected** 0 = No overflow is detected 1 = Soft error is detected		RW1CS	Yes	0
13	**Station 5 Header RAM Soft Error Counter Overflow Detected** 0 = No overflow is detected 1 = Soft error is detected		RW1CS	Yes	0
14	**Destination Queue Link List RAM 1-Bit ECC Error Detected** 0 = No 1-Bit ECC error is detected 1 = Soft error is detected		RW1CS	Yes	0
15	**Source Queue Link List RAM 1-Bit ECC Error Detected** 0 = No 1-Bit ECC error is detected 1 = Soft error is detected		RW1CS	Yes	0
16	**Retry Buffer 1-Bit ECC Error Detected** 0 = No 1-Bit ECC error is detected 1 = Soft error is detected		RW1CS	Yes	0
17	**Ingress Link List RAM Soft Error Counter Overflow Detected** 0 = No overflow is detected 1 = Soft error is detected		RW1CS	Yes	0
18	**Source Queue Link List RAM2 Soft Error Counter Overflow Detected** 0 = No overflow is detected 1 = Soft error is detected		RW1CS	Yes	0
19	**Destination Queue Data RAM Soft Error Counter Overflow Detected** 0 = No overflow is detected 1 = Soft error is detected		RW1CS	Yes	0
31:20	***Reserved***		RsvdP	No	000h

Register 13-144. 704h Device-Specific Error Mask 1 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
Note: *The bits in this register can be used to mask their respective* ***Device-Specific Error Status 1*** *register bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 700h, with the exception of bit 0, which is in all Ports).*					
0	**Completion FIFO Overflow Mask** 0 = If enabled, error generates MSI/INT*x* interrupt 1 = *Completion FIFO Overflow Status* bit is masked/disabled	All	RWS	Yes	1
1	***Factory Test Only***	0	RWS	Yes	1
2	**Station 0 Egress Packet Link List RAM 1-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Station 0 Egress Packet Link List RAM 1-Bit ECC Error Detected* bit is masked/disabled		RWS	Yes	1
5:3	***Reserved***		RsvdP	No	000b
6	**Station 4 Egress Packet Link List RAM 1-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Station 4 Egress Packet Link List RAM 1-Bit ECC Error Detected* bit is masked/disabled		RWS	Yes	1
7	**Station 5 Egress Packet Link List RAM 1-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Station 5 Egress Packet Link List RAM 1-Bit ECC Error Detected* bit is masked/disabled		RWS	Yes	1
8	**Station 0 Header RAM Soft Error Counter Overflow Mask** 0 = No effect on reporting activity 1 = *Station 0 Header RAM Soft Error Counter Overflow Detected* bit is masked/disabled		RWS	Yes	1
11:9	***Reserved***		RsvdP	No	000b

Register 13-144. 704h Device-Specific Error Mask 1 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
12	**Station 4 Header RAM Soft Error Counter Overflow Mask** 0 = No effect on reporting activity 1 = *Station 4 Header RAM Soft Error Counter Overflow Detected* bit is masked/disabled		RWS	Yes	1
13	**Station 5 Header RAM Soft Error Counter Overflow Mask** 0 = No effect on reporting activity 1 = *Station 5 Header RAM Soft Error Counter Overflow Detected* bit is masked/disabled		RWS	Yes	1
14	**Destination Queue Link List RAM 1-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Destination Queue Link List RAM 1-Bit ECC Error Detected* bit is masked/disabled		RWS	Yes	1
15	**Source Queue Link List RAM 1-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Source Queue Link List RAM 1-Bit ECC Error Detected* bit is masked/disabled		RWS	Yes	1
16	**Retry Buffer 1-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Retry Buffer 1-Bit ECC Error Detected* bit is masked/disabled		RWS	Yes	1
17	**Ingress Link List RAM Soft Error Counter Overflow Mask** 0 = No effect on reporting activity 1 = *Ingress Link List RAM Soft Error Counter Overflow Detected* bit is masked/disabled		RWS	Yes	1
18	**Source Queue Link List RAM2 Soft Error Counter Overflow Mask** 0 = No effect on reporting activity 1 = *Source Queue Link List RAM2 Soft Error Counter Overflow Detected* bit is masked/disabled		RWS	Yes	1
19	**Destination Queue Data RAM Soft Error Counter Overflow Mask** 0 = No effect on reporting activity 1 = *Destination Queue Data RAM Soft Error Counter Overflow Detected* bit is masked/disabled		RWS	Yes	1
31:20	***Reserved***		RsvdP	No	000h

Register 13-145. 708h Device-Specific Error Status 2 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I²C</th><th>Default</th></tr>
<tr><td colspan="5">ECC is checked by the egress Port, and any ECC error is reported by the egress Station (containing the egress Port), when that Port reads the Packet data from the ingress Station RAM. <i>For example</i>, when Port 16 receives a packet, the data is stored in Station 4 RAM; then, if the egress Port is in Station 0 and an ECC error is detected when the Port reads the Station 4 RAM, the error is flagged in the Port 0 register bit that reflects Station 4 error status.

<b><i>Notes:</i></b> <i>The bits in this register can be masked by their respective <b>Device-Specific Error Mask 2</b> register bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 70Ch).</i>

<i>All errors in this register generate ERR_FATAL or ERR_NONFATAL Messages, if enabled by the following:</i>
• <i><b>Device-Specific Error Mask 2</b> register (Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface, offset 70Ch</i>
• <i><b>Uncorrectable Error Status</b> register Uncorrectable Internal Error Status bit (All Ports, offset FB8h[22], is Set)</i>
• <i><b>Device Status</b> register Fatal Error Reporting Enable and Non-Fatal Error Reporting Enable bits (All Ports, offset 70h[2:1], respectively)</i></td></tr>
<tr><td>1:0</td><td><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>00b</td></tr>
<tr><td>2</td><td><b>Station 0 Egress Packet Link List RAM 2-Bit ECC Error Detected</b>
0 = No error is detected
1 = 2-bit ECC error is detected</td><td>RW1CS</td><td>Yes</td><td>0</td></tr>
<tr><td>5:3</td><td><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>000b</td></tr>
<tr><td>6</td><td><b>Station 4 Egress Packet Link List RAM 2-Bit ECC Error Detected</b>
0 = No error is detected
1 = 2-bit ECC error is detected</td><td>RW1CS</td><td>Yes</td><td>0</td></tr>
<tr><td>7</td><td><b>Station 5 Egress Packet Link List RAM 2-Bit ECC Error Detected</b>
0 = No error is detected
1 = 2-bit ECC error is detected</td><td>RW1CS</td><td>Yes</td><td>0</td></tr>
<tr><td>8</td><td><b>Station 0 Header RAM 2-Bit ECC Error Detected</b>
0 = No error is detected
1 = 2-bit ECC error is detected</td><td>RW1CS</td><td>Yes</td><td>0</td></tr>
<tr><td>11:9</td><td><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>000b</td></tr>
<tr><td>12</td><td><b>Station 4 Header RAM 2-Bit ECC Error Detected</b>
0 = No error is detected
1 = 2-bit ECC error is detected</td><td>RW1CS</td><td>Yes</td><td>0</td></tr>
<tr><td>13</td><td><b>Station 5 Header RAM 2-Bit ECC Error Detected</b>
0 = No error is detected
1 = 2-bit ECC error is detected</td><td>RW1CS</td><td>Yes</td><td>0</td></tr>
<tr><td>14</td><td><b>Destination Queue Link List RAM 2-Bit ECC Error Detected</b>
0 = No error is detected
1 = 2-bit ECC error is detected</td><td>RW1CS</td><td>Yes</td><td>0</td></tr>
</table>

Register 13-145. 708h Device-Specific Error Status 2 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15	**Source Queue Link List RAM 2-Bit ECC Error Detected** 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
16	**Retry Buffer 2-Bit ECC Error Detected** 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
17	**Ingress Link List RAM 2-Bit ECC Error Detected** 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
18	**Source Queue Link List RAM2 2-Bit ECC Error Detected** 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
19	**Destination Queue Data RAM 2-Bit ECC Error Detected** 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
31:20	***Reserved***	RsvdP	No	000h

Register 13-146. 70Ch Device-Specific Error Mask 2 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Note: *The bits in this register can be used to mask their respective **Device-Specific Error Status 2** register bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 708h).*				
1:0	***Factory Test Only***	RsvdP	No	00b
2	**Station 0 Egress Packet Link List RAM 2-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Station 0 Egress Packet Link List RAM 2-Bit ECC Error Detected* bit is masked/disabled	RWS	Yes	1
5:3	***Reserved***	RsvdP	No	000b
6	**Station 4 Egress Packet Link List RAM 2-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Station 4 Egress Packet Link List RAM 2-Bit ECC Error Detected* bit is masked/disabled	RWS	Yes	1
7	**Station 5 Egress Packet Link List RAM 2-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Station 5 Egress Packet Link List RAM 2-Bit ECC Error Detected* bit is masked/disabled	RWS	Yes	1
8	**Station 0 Header RAM 2-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Station 0 Header RAM 2-Bit ECC Error Detected* bit is masked/disabled	RWS	Yes	1
11:9	***Reserved***	RsvdP	No	000b
12	**Station 4 Header RAM 2-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Station 4 Header RAM 2-Bit ECC Error Detected* bit is masked/disabled	RWS	Yes	1
13	**Station 5 Header RAM 2-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Station 5 Header RAM 2-Bit ECC Error Detected* bit is masked/disabled	RWS	Yes	1
14	**Destination Queue Link List RAM 2-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Destination Queue Link List RAM 2-Bit ECC Error Detected* bit is masked/disabled	RWS	Yes	1
15	**Source Queue Link List RAM 2-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Source Queue Link List RAM 2-Bit ECC Error Detected* bit is masked/disabled	RWS	Yes	1

Register 13-146. 70Ch Device-Specific Error Mask 2 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
16	**Retry Buffer 2-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Retry Buffer 2-Bit ECC Error Detected* bit is masked/disabled	RWS	Yes	1
17	**Ingress Link List RAM 2-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Ingress Link List RAM 2-Bit ECC Error Detected* bit is masked/disabled	RWS	Yes	1
18	**Source Queue Link List RAM2 2-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Source Queue Link List RAM2 2-Bit ECC Error Detected* bit is masked/disabled	RWS	Yes	1
19	**Destination Queue Data RAM 2-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Destination Queue Data RAM 2-Bit ECC Error Detected* bit is masked/disabled	RWS	Yes	1
31:20	***Reserved***	RsvdP	No	000h

Register 13-147. 710h Device-Specific Error Status 3 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I^{2}C</th><th>Default</th></tr>
<tr><td colspan="5">ECC is checked by the egress Port, and any ECC error is reported by the egress Station (containing the egress Port), when that Port reads the Packet data from the ingress Station RAM. *For example*, when Port 16 receives a packet, the data is stored in Station 4 RAM; then, if the egress Port is in Station 0 and an ECC error is detected when the Port reads the Station 4 RAM, the error is flagged in the Port 0 register bit that reflects Station 4 error status.
Notes: *The bits in this register can be masked by their respective* ***Device-Specific Error Mask 3*** *register bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 714h).*
All errors in this register generate ERR_FATAL or ERR_NONFATAL Messages, if enabled by the following:
• ***Device-Specific Error Mask 3*** *register (Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface, offset 714h*
• ***Uncorrectable Error Status*** *register Uncorrectable Internal Error Status bit (All Ports, offset FB8h[22], is Set)*
• ***Device Status*** *register Fatal Error Reporting Enable and Non-Fatal Error Reporting Enable bits (All Ports, offset 70h[2:1], respectively)*</td></tr>
<tr><td>0</td><td>**Station 0 Packet RAM0 Instance 0 Soft Error Counter Overflow Detected**
0 = No error is detected
1 = Soft error is detected</td><td>RW1CS</td><td>Yes</td><td>0</td></tr>
<tr><td>3:1</td><td>***Reserved***</td><td>RsvdP</td><td>No</td><td>000b</td></tr>
<tr><td>4</td><td>**Station 4 Packet RAM0 Instance 0 Soft Error Counter Overflow Detected**
0 = No error is detected
1 = Soft error is detected</td><td>RW1CS</td><td>Yes</td><td>0</td></tr>
<tr><td>5</td><td>**Station 5 Packet RAM0 Instance 0 Soft Error Counter Overflow Detected**
0 = No error is detected
1 = Soft error is detected</td><td>RW1CS</td><td>Yes</td><td>0</td></tr>
<tr><td>11:6</td><td>***Factory Test Only***</td><td>RW1CS</td><td>Yes</td><td>0-0h</td></tr>
<tr><td>12</td><td>**Station 0 Packet RAM1 Instance 0 Soft Error Counter Overflow Detected**
0 = No error is detected
1 = Soft error is detected</td><td>RW1CS</td><td>Yes</td><td>0</td></tr>
<tr><td>15:13</td><td>***Reserved***</td><td>RsvdP</td><td>No</td><td>000b</td></tr>
<tr><td>16</td><td>**Station 4 Packet RAM1 Instance 0 Soft Error Counter Overflow Detected**
0 = No error is detected
1 = Soft error is detected</td><td>RW1CS</td><td>Yes</td><td>0</td></tr>
<tr><td>17</td><td>**Station 5 Packet RAM1 Instance 0 Soft Error Counter Overflow Detected**
0 = No error is detected
1 = Soft error is detected</td><td>RW1CS</td><td>Yes</td><td>0</td></tr>
<tr><td>23:18</td><td>***Factory Test Only***</td><td>RW1CS</td><td>Yes</td><td>0-0h</td></tr>
<tr><td>31:24</td><td>***Reserved***</td><td>RsvdP</td><td>No</td><td>00h</td></tr>
</table>

Register 13-148. 714h Device-Specific Error Mask 3 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
Note: *The bits in this register can be used to mask their respective* ***Device-Specific Error Status 3*** *register bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 710h).*				
0	**Station 0 Packet RAM0 Instance 0 Soft Error Counter Overflow Mask** 0 = No effect on reporting activity 1 = *Station 0 Packet RAM0 Instance 0 Soft Error Counter Overflow Detected* bit is masked/disabled	RWS	Yes	1
3:1	***Reserved***	RsvdP	No	000b
4	**Station 4 Packet RAM0 Instance 0 Soft Error Counter Overflow Mask** 0 = No effect on reporting activity 1 = *Station 4 Packet RAM0 Instance 0 Soft Error Counter Overflow Detected* bit is masked/disabled	RWS	Yes	1
5	**Station 5 Packet RAM0 Instance 0 Soft Error Counter Overflow Mask** 0 = No effect on reporting activity 1 = *Station 5 Packet RAM0 Instance 0 Soft Error Counter Overflow Detected* bit is masked/disabled	RWS	Yes	1
11:6	***Factory Test Only***	RW1CS	Yes	0-0h
12	**Station 0 Packet RAM1 Instance 0 Soft Error Counter Overflow Mask** 0 = No effect on reporting activity 1 = *Station 0 Packet RAM1 Instance 0 Soft Error Counter Overflow Detected* bit is masked/disabled	RWS	Yes	1
15:13	***Reserved***	RsvdP	No	000b
16	**Station 4 Packet RAM1 Instance 0 Soft Error Counter Overflow Mask** 0 = No effect on reporting activity 1 = *Station 4 Packet RAM1 Instance 0 Soft Error Counter Overflow Detected* bit is masked/disabled	RWS	Yes	1
17	**Station 5 Packet RAM1 Instance 0 Soft Error Counter Overflow Mask** 0 = No effect on reporting activity 1 = *Station 5 Packet RAM1 Instance 0 Soft Error Counter Overflow Detected* bit is masked/disabled	RWS	Yes	1
23:18	***Factory Test Only***	RW1CS	Yes	0-0h
31:24	***Reserved***	RsvdP	No	00h

Register 13-149. 718h Device-Specific Error Status 4 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
ECC is checked by the egress Port, and any ECC error is reported by the egress Station (containing the egress Port), when that Port reads the Packet data from the ingress Station RAM. *For example*, when Port 16 receives a packet, the data is stored in Station 4 RAM; then, if the egress Port is in Station 0 and an ECC error is detected when the Port reads the Station 4 RAM, the error is flagged in the Port 0 register bit that reflects Station 4 error status. ***Notes:*** *The bits in this register can be masked by their respective* ***Device-Specific Error Mask 4*** *register bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 71Ch).* *All errors in this register generate ERR_FATAL or ERR_NONFATAL Messages, if enabled by the following:* • ***Device-Specific Error Mask 4*** *register (Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface, offset 71Ch* • ***Uncorrectable Error Status*** *register Uncorrectable Internal Error Status bit (All Ports, offset FB8h[22], is Set)* • ***Device Status*** *register Fatal Error Reporting Enable and Non-Fatal Error Reporting Enable bits (All Ports, offset 70h[2:1], respectively)*				
0	**Station 0 Packet RAM0 Instance 0 2-Bit ECC Error Detected** 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
3:1	***Reserved***	RsvdP	No	000b
4	**Station 4 Packet RAM0 Instance 0 2-Bit ECC Error Detected** 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
5	**Station 5 Packet RAM0 Instance 0 2-Bit ECC Error Detected** 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
11:6	***Factory Test Only***	RW1CS	Yes	0-0h
12	**Station 0 Packet RAM1 Instance 0 2-Bit ECC Error Detected** 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
15:13	***Reserved***	RsvdP	No	000b
16	**Station 4 Packet RAM1 Instance 0 2-Bit ECC Error Detected** 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
17	**Station 5 Packet RAM1 Instance 0 2-Bit ECC Error Detected** 0 = No error is detected 1 = 2-bit ECC error is detected	RW1CS	Yes	0
23:18	***Factory Test Only***	RW1CS	Yes	0-0h
31:24	***Reserved***	RsvdP	No	00h

Register 13-150. 71Ch Device-Specific Error Mask 4 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The bits in this register can be used to mask their respective* ***Device-Specific Error Status 4*** *register bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 718h).*				
0	**Station 0 Packet RAM0 Instance 0 2-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Station 0 Packet RAM0 Instance 0 2-Bit ECC Error Detected* bit is masked/disabled	RWS	Yes	1
3:1	***Reserved***	RsvdP	No	000b
4	**Station 4 Packet RAM0 Instance 0 2-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Station 4 Packet RAM0 Instance 0 2-Bit ECC Error Detected* bit is masked/disabled	RWS	Yes	1
5	**Station 5 Packet RAM0 Instance 0 2-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Station 5 Packet RAM0 Instance 0 2-Bit ECC Error Detected* bit is masked/disabled	RWS	Yes	1
11:6	***Factory Test Only***	RW1CS	Yes	0-0h
12	**Station 0 Packet RAM1 Instance 0 2-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Station 0 Packet RAM1 Instance 0 2-Bit ECC Error Detected* bit is masked/disabled	RWS	Yes	1
15:13	***Reserved***	RsvdP	No	000b
16	**Station 4 Packet RAM1 Instance 0 2-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Station 4 Packet RAM1 Instance 0 2-Bit ECC Error Detected* bit is masked/disabled	RWS	Yes	1
17	**Station 5 Packet RAM1 Instance 0 2-Bit ECC Error Mask** 0 = No effect on reporting activity 1 = *Station 5 Packet RAM1 Instance 0 2-Bit ECC Error Detected* bit is masked/disabled	RWS	Yes	1
23:18	***Factory Test Only***	RW1CS	Yes	0-0h
31:24	***Reserved***	RsvdP	No	00h

Register 13-151. 720h ECC Error Check Disable (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
0	**ECC 1-Bit Error Check Disable** 0 = RAM 1-Bit Soft Error Check enabled 1 = Disables RAM 1-Bit Soft Error Check	**Base Mode** 0, 16, 20 **Virtual Switch Mode** 0, 16, 20, accessible through the Management Port	RWS	Yes	0
1	**ECC 2-Bit Error Check Disable** 0 = RAM 2-Bit Soft Error Check enabled 1 = Disables RAM 2-Bit Soft Error Check	**Base Mode** 0, 16, 20 **Virtual Switch Mode** 0, 16, 20, accessible through the Management Port	RWS	Yes	0
2	**Software Force Error Enable** 1 = **Correctable Error Status** and **Uncorrectable Error Status** registers (offsets FC4h and FB8h, respectively) change from RW1CS to RW		RWS	Yes	0
3	**Software Force Non-Posted Request** Used to select software-forced errors to be associated with Posted or Non-Posted TLPs, because some errors are handled differently, depending upon the TLP type (Posted or Non-Posted). 0 = Handle software-forced errors as if the errors are associated with Posted TLPs 1 = Enables handling of errors associated with Posted TLPs as if those errors are associated with Non-Posted TLPs		RWS	Yes	0

Register 13-151. 720h ECC Error Check Disable (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
4	**Enable PEX_INTA# and/or VS*x*_PEX_INTA# Interrupt Output(s) for Hot Plug or Link State Event-Triggered Interrupt** 0 = Hot Plug or Link State Event Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA# nor VS*x*_PEX_INTA#) 1 = Hot Plug or Link State Event Interrupt Requests assert PEX_INTA# and/or VS*x*_PEX_INTA# (and do not send an INT*x* Message)		RWS	Yes	0
5	**Enable PEX_INTA# Interrupt Output(s) for Device-Specific NT-Link Port Event-Triggered Interrupt** ***This bit is valid only in NT mode.*** Enables PEX_INTA# or INT*x* interrupt signaling for the following NT-Link Interface events, defined in the **Link Error Status Virtual** and **Link Error Mask Virtual** registers (NT Port Virtual Interface, offsets FE0h and FE4h, respectively): • NT-Link Port Correctable error (NT Port Link Interface, offset FC4h) • NT-Link Port Uncorrectable error (NT Port Link Interface, offset FB8h) • NT-Link Port Data Link Layer State change • NT-Link Port received (and consequently dropped) a Fatal or Non-Fatal Error Message 0 = Device-Specific NT-Link Port Event Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA#) 1 = Device-Specific NT-Link Port Event Interrupt Requests assert PEX_INTA# (and do not send an INT*x* Message)	0, NT Port Virtual Interface	RWS	Yes	0
	Reserved	Otherwise	RsvdP	No	0
6	**Enable PEX_INTA# and/or VS*x*_PEX_INTA# Interrupt Output(s) for GPIO-Generated Interrupts** 0 = General-Purpose Input/Output (GPIO) Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA# nor VS*x*_PEX_INTA#) 1 = GPIO Interrupt Requests assert PEX_INTA# and/or VS*x*_PEX_INTA# (and do not send an INT*x* Message)	**Base Mode** 0 **Virtual Switch Mode** 0, accessible through the Management Port	RWS	Yes	0
7	**Base Mode** **Enable PEX_INTA# Interrupt Output(s) for NT-Virtual Doorbell-Generated Interrupts** ***This bit is valid only in NT mode.*** Enables either PEX_INTA# or INT*x* Messages for NT-Virtual Doorbell interrupts (NT Port Virtual Interface, offsets C4Ch through C58h). 0 = NT-Virtual Doorbell Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA#) 1 = NT-Virtual Doorbell Interrupt Requests assert PEX_INTA# (and do not send an INT*x* Message)	0, NT Port Virtual Interface	RWS	Yes	0
	Reserved	Otherwise	RsvdP	No	0
	Virtual Switch Mode ***Reserved***		RsvdP	No	0

Register 13-151. 720h ECC Error Check Disable (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
8	**Base Mode** ***Reserved***		RsvdP	No	0
	Virtual Switch Mode **Enable PEX_INTA# and/or VS*x*_PEX_INTA# Interrupt Output(s) for Management Port Doorbell-Generated Interrupts** 0 = Management Port Doorbell Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA# nor VS*x*_PEX_INTA#) 1 = Management Port Doorbell Interrupt Requests assert PEX_INTA# and/or VS*x*_PEX_INTA# (and do not send an INT*x* Message)	0, accessible through the Management Port	RWS	Yes	0
9	**Base Mode** ***Reserved***		RsvdP	No	0
	Virtual Switch Mode **Enable PEX_INTA# and/or VS*x*_PEX_INTA# Interrupt Output(s) for Management Link Status Event-Generated Interrupts** 0 = Management Link Status Event Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA# nor VS*x*_PEX_INTA#) 1 = Management Link Status Event Interrupt Requests assert PEX_INTA# and/or VS*x*_PEX_INTA# (and do not send an INT*x* Message)	0, accessible through the Management Port	RWS	Yes	0
10	**Disable Sending MSI if MSI Is Enabled after Interrupt Status Set** 0 = Does not disable sending an MSI, if MSIs are enabled after an *Interrupt Status* bit is Set 1 = Disables sending an MSI, if MSIs are enabled after an *Interrupt Status* bit is Set ***Note:*** *This bit must remain Cleared, for compliance to specifications governing the MSI Capability.*		RWS	Yes	0
31:11	***Reserved***		RsvdP	No	0-0h

13.15.11 Device-Specific Registers – Control (Offsets 760h – 774h), Base Mode Only

Note: *In Virtual Switch mode, this entire structure is* ***reserved****, RsvdP, not serial EEPROM nor I^{2}C writable, and has a default value of 0h.*

This section details the Device-Specific Control registers. Table 13-30 defines the register map.

Table 13-30. Device-Specific Control Register Map (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Station-Based Control	760h
Ingress Chip Control	764h
Factory Test Only 768h –	770h
Reserved	774h

Register 13-152. 760h Station-Based Control (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
0	**Link List RAM 1-Bit Error Injection** The ECC Counter for this bit is located in the **Ingress PLL RAM ECC 1-Bit Counter** register *1-Bit ECC Counter for PLL RAM Read from Ingress Block* field (Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface, offset 778h[7:0]).	RWS	Yes	0
1	**Link List RAM 2-Bit Error Injection**	RWS	Yes	0
2	**Link List RAM Error Injection Field** 0 = Error injection is in the *ECC Code* field 1 = Error injection is in the *Data* field	RWS	Yes	0
4:3	**Link List RAM Port Selector for Error Injection**	RWS	Yes	00b
7:5	***Not used***	RWS	Yes	000b
8	**Header RAM 1-Bit Error Injection**	RWS	Yes	0
9	**Header RAM 2-Bit Error Injection**	RWS	Yes	0
10	**Header RAM Error Injection Field** 0 = Error injection is in the *ECC Code* field 1 = Error injection is in the *Data* field	RWS	Yes	0
12:11	**Header RAM Port Selector for Error Injection**	RWS	Yes	00b
15:13	***Factory Test Only***	RWS	Yes	000b

Register 13-152. 760h Station-Based Control (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
16	**Payload RAM 1-Bit Error Injection**	RWS	Yes	0
17	**Payload RAM 2-Bit Error Injection**	RWS	Yes	0
18	**Payload RAM Error Injection Field** 0 = Error injection is in the *ECC Code* field 1 = Error injection is in the *Data* field	RWS	Yes	0
19	**Payload RAM Selector for Error Injection**	RWS	Yes	0
20	**Source Queue Link List RAM 1-Bit Error Injection**	RWS	Yes	0
21	**Source Queue Link List RAM 2-Bit Error Injection**	RWS	Yes	0
22	**Source Queue Link List RAM Error Injection Field** 0 = Error injection is in the *ECC Code* field 1 = Error injection is in the *Data* field	RWS	Yes	0
23	**Source Queue Link List RAM Selector for Error Injection** 0 = Port-A, normal traffic 1 = Port-B, Read-Pacing traffic	RWS	Yes	0
24	**Disable Credit Re-Balancing** 1 = No Credit re-balancing	RWS	Yes	0
25	**Use Serial EEPROM Values for Ingress Credit Initialization** 0 = Use default values for ingress credit initialization 1 = Use serial EEPROM values for ingress credit initialization	RWS	Yes	0
26	**INCH Credit Reserve Flag** A transition from 0 to 1 indicates that I^{2}C has finished with all CSR to INCH Initialization registers, and credit reservation can proceed.	RWS	Yes	0
28:27	***Factory Test Only***	RWS	Yes	00b
29	**No Special Treatment for Relaxed Ordering Traffic** The PEX 8649 supports Relaxed Ordering for Completions. By default, if the RO attribute is Set within a Completion, then that Completion can bypass Posted transactions, if Posted TLPs are blocked at the egress Port (due to insufficient Posted credits from the connected device). This behavior can be disabled by Setting this bit, in each Station. 1 = Device-Specific Relaxed Ordering Completion will not be flagged to the Egress block	RWS	Yes	0
30	***Factory Test Only***	RWS	Yes	0
31	***Not used***	RWS	Yes	0

Register 13-153. 764h Ingress Chip Control (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**Expansion ROM Virtual Side** 0 = Expansion ROM is located on the NT Port Link Interface 1 = Expansion ROM is located on the NT Port Virtual Interface	RWS	Yes	0
1	**NT Error Message Drop** 0 = If the NT Port Link Interface receives an Uncorrectable Error Message that is routed to the Root Complex, the NT Port Link Interface reports a Malformed TLP error. 1 = Do not malform a Fatal Error Message received on the NT Port Link Interface with routing equal to 0, and instead, drop the packet and log the error in the **Link Error Status Virtual** register *Link Side Uncorrectable Error Message Drop Status* bit (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE0h[3]). If the corresponding **Link Error Mask Virtual** register *Link Side Uncorrectable Error Message Drop Mask* bit (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE4h[3]) is Set, the NT Port Virtual Interface signals an Interrupt (INT*x*, MSI, or PEX_INTA#) to the Local Host through the upstream Port, if interrupts are enabled.	RWS	Yes	0
2	**Virtual LUT Toggle** NT Port Virtual Interface Look-up Table (LUT) toggle between 8- and 32-Entry modes. (Refer to Section 15.15.1, "NT Port Virtual Interface NT Bridging-Specific Registers – Requester ID Translation Lookup Table Entry (Addresses D94h – DD0h)," for further details.) ***Note:*** *Legacy NT mode is enabled when the **Debug Control** register NT P2P Enable bit (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 350h[14]) is Set (default value is the inverse of the STRAP_NT_P2P_EN# input state).* *NT PCI-to-PCI Bridge mode is enabled when the NT P2P Enable bit is Cleared.* 0 = LUT is eight 32-bit entries in Legacy NT mode (offsets D94h to DB0h), and 32 16-bit entries in NT PCI-to-PCI mode (offsets D94h to DD0h) 1 = LUT is 32 16-bit entries in Legacy NT mode (offsets D94h to DD0h), and eight 32-bit entries in NT PCI-to-PCI mode (offsets D94h to DB0h)	RWS	Yes	0
19:3	***Not used***	RWS	Yes	0-0h
20	**Ingress MWr32 Counter Disable** 0 = Enables Ingress Memory Write 32-Bit Counter 1 = Disables Ingress Memory Write 32-Bit Counter	RWS	Yes	0
21	**Ingress MWr64 Counter Disable** 0 = Enables Ingress Memory Write 64-Bit Counter 1 = Disables Ingress Memory Write 64-Bit Counter	RWS	Yes	0
22	**Ingress MSG Counter Disable** 0 = Enables Ingress Message Counter 1 = Disables Ingress Message Counter	RWS	Yes	0
23	**Ingress MRd32 Counter Disable** 0 = Enables Ingress Memory Read 32-Bit Counter 1 = Disables Ingress Memory Read 32-Bit Counter	RWS	Yes	0

Register 13-153. 764h Ingress Chip Control (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
24	**Ingress MRd64 Counter Disable** 0 = Enables Ingress Memory Read 64-Bit Counter 1 = Disables Ingress Memory Read 64-Bit Counter	RWS	Yes	0
25	**Ingress Other Non-Posted Counter Disable** 0 = Enables Ingress Other Non-Posted Counter 1 = Disables Ingress Other Non-Posted Counter	RWS	Yes	0
26	**Ingress and Egress DLLP ACK Counter Disable** 0 = Enables Ingress and Egress DLLP ACK Counter 1 = Disables Ingress and Egress DLLP ACK Counter	RWS	Yes	0
27	**Ingress and Egress DLLP UpdateFC-P Counter Disable** 0 = Enables Ingress and Egress Data Link Layer Packet (DLLP) UpdateFC-Posted Counter 1 = Disables Ingress and Egress DLLP UpdateFC-Posted Counter	RWS	Yes	0
28	**Ingress and Egress DLLP UpdateFC-NP Counter Disable** 0 = Enables Ingress and Egress DLLP UpdateFC-Non-Posted Counter 1 = Disables Ingress and Egress DLLP UpdateFC-Non-Posted Counter	RWS	Yes	0
29	**Ingress and Egress DLLP UpdateFC-CPL Counter Disable** 0 = Enables Ingress and Egress DLLP UpdateFC-Completion Counter 1 = Disables Ingress and Egress DLLP UpdateFC-Completion Counter	RWS	Yes	0
30	***Not used***	RWS	Yes	0
31	***Factory Test Only***	RO	Yes	0

13.15.12 Device-Specific Registers – Soft Error (Offsets 778h – 8FCh)

This section details the Device-Specific Soft Error registers. Table 13-31 defines the register map.

Table 13-31. Device-Specific Soft Error Register Map
(Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved			Ingress PLL RAM ECC 1-Bit Counter	778h
Reserved				77Ch – 7FCh
Egress Station 0 Payload RAM Soft Error Counters				800h
Reserved				804h – 80Ch
Egress Station 4 Payload RAM Soft Error Counters				810h
Egress Station 5 Payload RAM Soft Error Counters				814h
Reserved			Egress Header RAM Soft Error Counters 1	818h
Reserved		Egress Header RAM Soft Error Counters 2		81Ch
Factory Test Only/Reserved				820h – 828h
Soft Error Injection				82Ch
Reserved				830h – 8FCh

Register 13-154. 778h Ingress PLL RAM ECC 1-Bit Counter (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
7:0	**1-Bit ECC Counter for PLL RAM Read from Ingress Block** A Write of 0 to bit 0 Clears the ECC Counter.	RO	No	00h
31:8	***Reserved***	RsvdP	No	0000_00h

Register 13-155. 800h Egress Station 0 Payload RAM Soft Error Counters (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
7:0	**Station 0 Payload RAM0 Instance 0 1-Bit Soft Error Counter Value**	RO	No	00h
15:8	**Station 0 Payload RAM0 Instance 1 1-Bit Soft Error Counter Value**	RO	No	00h
23:16	**Station 0 Payload RAM1 Instance 0 1-Bit Soft Error Counter Value**	RO	No	00h
31:24	**Station 0 Payload RAM1 Instance 1 1-Bit Soft Error Counter Value**	RO	No	00h

Register 13-156. 810h Egress Station 4 Payload RAM Soft Error Counters (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
7:0	**Station 4 Payload RAM0 Instance 0 1-Bit Soft Error Counter Value**	RO	No	00h
15:8	**Station 4 Payload RAM0 Instance 1 1-Bit Soft Error Counter Value**	RO	No	00h
23:16	**Station 4 Payload RAM1 Instance 0 1-Bit Soft Error Counter Value**	RO	No	00h
31:24	**Station 4 Payload RAM1 Instance 1 1-Bit Soft Error Counter Value**	RO	No	00h

Register 13-157. 814h Egress Station 5 Payload RAM Soft Error Counters (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
7:0	**Station 5 Payload RAM0 Instance 0 1-Bit Soft Error Counter Value**	RO	No	00h
15:8	**Station 5 Payload RAM0 Instance 1 1-Bit Soft Error Counter Value**	RO	No	00h
23:16	**Station 5 Payload RAM1 Instance 0 1-Bit Soft Error Counter Value**	RO	No	00h
31:24	**Station 5 Payload RAM1 Instance 1 1-Bit Soft Error Counter Value**	RO	No	00h

Register 13-158. 818h Egress Header RAM Soft Error Counters 1 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
7:0	**Station 0 Header RAM 1-Bit Soft Error Counter Value**	RO	No	00h
31:8	***Reserved***	RO	No	0000_00h

Register 13-159. 81Ch Egress Header RAM Soft Error Counters 2 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
7:0	**Station 4 Header RAM 1-Bit Soft Error Counter Value**	RO	No	00h
15:8	**Station 5 Header RAM 1-Bit Soft Error Counter Value**	RO	No	00h
31:16	***Reserved***	RO	No	0000h

Register 13-160. 82Ch Soft Error Injection (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**Destination Queue Data RAM 1-Bit Soft Error Injection** Writing 1 injects one error.	RWS	Yes	0
1	**Destination Queue Data RAM 2-Bit Soft Error Injection** Writing 1 injects one error.	RWS	Yes	0
2	**Destination Queue Data RAM Error Injection Select** 0 = Inject Soft error in *ECC code* field 1 = Inject Soft error in *Data* field	RWS	Yes	0
3	**Destination Queue Link List RAM Port A 1-Bit Soft Error Injection** Writing 1 injects one error.	RWS	Yes	0
4	**Destination Queue Link List RAM Port A 2-Bit Soft Error Injection** Writing 1 injects one error.	RWS	Yes	0
5	**Destination Queue Link List RAM Port A Error Injection Select** 0 = Inject Soft error in *ECC code* field 1 = Inject Soft error in *Data* field	RWS	Yes	0
6	**Retry Buffer 1-Bit Soft Error Injection** Writing 1 injects one error.	RWS	Yes	0
7	**Retry Buffer 2-Bit Soft Error Injection** Writing 1 injects one error.	RWS	Yes	0
8	**Retry Buffer Error Injection Select** 0 = Inject Soft error in ECC code 1 = Inject Soft error in data	RWS	Yes	0
9	**Destination Queue Link List RAM Port B 1-Bit Soft Error Injection** Writing 1 injects one error.	RWS	Yes	0
10	**Destination Queue Link List RAM Port B 2-Bit Soft Error Injection** Writing 1 injects one error.	RWS	Yes	0
11	**Destination Queue Link List RAM Port B Error Injection Select** 0 = Inject Soft error in *ECC code* field 1 = Inject Soft error in *Data* field	RWS	Yes	0
19:12	***Reserved***	RsvdP	No	00h

Register 13-160. 82Ch Soft Error Injection (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
20	**Ingress Payload RAM0 Instance 0 ECC Counter Reset** Writing 1 Clears the Counter in the **Egress Station *x* Payload RAM Soft Error Counters** register *Station x Payload RAM0 Instance 0 1-Bit Soft Error Counter Value* field(s) (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets 800h, 810h, and 814h[7:0]). Reads always return 0.	RZ	Yes	0
21	**Ingress Payload RAM0 Instance 1 ECC Counter Reset** Writing 1 Clears the Counter in the **Egress Station *x* Payload RAM Soft Error Counters** register *Station x Payload RAM0 Instance 1 1-Bit Soft Error Counter Value* field(s) (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets 800h, 810h, and 814h[15:8]). Reads always return 0.	RZ	Yes	0
22	**Ingress Payload RAM1 Instance 0 ECC Counter Reset** Writing 1 Clears the Counter in the **Egress Station *x* Payload RAM Soft Error Counters** register *Station x Payload RAM1 Instance 0 1-Bit Soft Error Counter Value* field(s) (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets 800h, 810h, and 814h[23:16]). Reads always return 0.	RZ	Yes	0
23	**Ingress Payload RAM1 Instance 1 ECC Counter Reset** Writing 1 Clears the Counter in the **Egress Station *x* Payload RAM Soft Error Counters** register *Station x Payload RAM1 Instance 1 1-Bit Soft Error Counter Value* field(s) (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets 800h, 810h, and 814h[31:24]). Reads always return 0.	RZ	Yes	0
24	**Header RAM ECC Counter Reset** Writing 1 Clears the Counter in the **Egress Header RAM Soft Error Counters *x*** register *Station x Header RAM 1-Bit Soft Error Counter Value* field(s) (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets 818h[7:0] and 81Ch[7:0, 15:8], respectively). Reads always return 0.	RZ	Yes	0
28:25	***Factory Test Only***	RZ	Yes	0h
31:29	**Station Number to Reset the ECC Counter** Selects the ECC Counter that corresponds to the Station Number. 000b = Station 0 (default) 100b = Station 4 101b = Station 5 All other encodings are ***Reserved***.	RZ	Yes	000b

13.15.13 Device-Specific Registers – Virtual Switch (Offsets 900h – 9ECh), Virtual Switch Mode Only

Note: *In Base mode, this entire structure is* ***reserved****, RsvdP, not serial EEPROM nor I^{2}C writable, and has a default value of 0h.*

This section details the Device-Specific Virtual Switch Support registers located at offsets 900h through 9ECh. These registers are implemented only in Virtual Switch mode. Additionally, the registers are implemented only in Port 0, accessible through the Management Port (offsets 900h through 90Ch), or VS Upstream Port(s) and Management Port (offsets 910h through 93Ch), as indicated in the registers that follow. Table 13-32 defines the register map.

Other Device-Specific Virtual Switch registers are detailed in Section 13.17, “Device-Specific Registers – Virtual Switch (Offset F20h), Virtual Switch Mode Only.”

Table 13-32. Device-Specific Virtual Switch Register Map (Offsets 900h – 9ECh)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved	Switch Link Up	900h
Reserved	Switch Link Down	904h
Reserved	Switch Link Event Mask	908h
Reserved	Switch Link Status	90Ch
VS Upstream to Management Upstream Doorbell Request		910h
VS Upstream to Management Upstream Doorbell Mask		914h
VS Upstream to Management Upstream Scratchpad 1		918h
VS Upstream to Management Upstream Scratchpad 2		91Ch
VS Upstream to Management Upstream Scratchpad 3		920h
VS Upstream to Management Upstream Scratchpad 4		924h
Management Upstream to VS Upstream Doorbell Request		928h
Management Upstream to VS Upstream Doorbell Mask		92Ch
Management Upstream to VS Upstream Scratchpad 1		930h
Management Upstream to VS Upstream Scratchpad 2		934h
Management Upstream to VS Upstream Scratchpad 3		938h
Management Upstream to VS Upstream Scratchpad 4		93Ch
Reserved		940h – 9ECh

Register 13-161. 900h Switch Link Up (Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
0	**Port 0 Link Up** 1 = Port 0 Link transitioned from the *DL_Inactive* state to the *DL_Active* state	0, accessible through the Management Port	RW1C	Yes	0
	Reserved	Otherwise	RsvdP	No	0
1	**Port 1 Link Up** 1 = Port 1 Link transitioned from the *DL_Inactive* state to the *DL_Active* state	0, accessible through the Management Port	RW1C	Yes	0
	Reserved	Otherwise	RsvdP	No	0
2	**Port 2 Link Up** 1 = Port 2 Link transitioned from the *DL_Inactive* state to the *DL_Active* state	0, accessible through the Management Port	RW1C	Yes	0
	Reserved	Otherwise	RsvdP	No	0
3	**Port 3 Link Up** 1 = Port 3 Link transitioned from the *DL_Inactive* state to the *DL_Active* state	0, accessible through the Management Port	RW1C	Yes	0
	Reserved	Otherwise	RsvdP	No	0
15:4	***Reserved***		RsvdP	No	000h

Register 13-161. 900h Switch Link Up (Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
16	**Port 16 Link Up** 1 = Port 16 Link transitioned from the *DL_Inactive* state to the *DL_Active* state	0, accessible through the Management Port	RW1C	Yes	0
	Reserved	Otherwise	RsvdP	No	0
17	**Port 17 Link Up** 1 = Port 17 Link transitioned from the *DL_Inactive* state to the *DL_Active* state	0, accessible through the Management Port	RW1C	Yes	0
	Reserved	Otherwise	RsvdP	No	0
18	**Port 18 Link Up** 1 = Port 18 Link transitioned from the *DL_Inactive* state to the *DL_Active* state	0, accessible through the Management Port	RW1C	Yes	0
	Reserved	Otherwise	RsvdP	No	0
19	**Port 19 Link Up** 1 = Port 19 Link transitioned from the *DL_Inactive* state to the *DL_Active* state	0, accessible through the Management Port	RW1C	Yes	0
	Reserved	Otherwise	RsvdP	No	0
20	**Port 20 Link Up** 1 = Port 20 Link transitioned from the *DL_Inactive* state to the *DL_Active* state	0, accessible through the Management Port	RW1C	Yes	0
	Reserved	Otherwise	RsvdP	No	0
21	**Port 21 Link Up** 1 = Port 21 Link transitioned from the *DL_Inactive* state to the *DL_Active* state	0, accessible through the Management Port	RW1C	Yes	0
	Reserved	Otherwise	RsvdP	No	0
22	**Port 22 Link Up** 1 = Port 22 Link transitioned from the *DL_Inactive* state to the *DL_Active* state	0, accessible through the Management Port	RW1C	Yes	0
	Reserved	Otherwise	RsvdP	No	0
23	**Port 23 Link Up** 1 = Port 23 Link transitioned from the *DL_Inactive* state to the *DL_Active* state	0, accessible through the Management Port	RW1C	Yes	0
	Reserved	Otherwise	RsvdP	No	0
31:24	***Reserved***		RsvdP	No	00h

Register 13-162. 904h Switch Link Down (Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
0	**Port 0 Link Down** 1 = Port 0 Link transitioned from the *DL_Active* state to the *DL_Inactive* state	0, accessible through the Management Port	RW1C	Yes	0
	Reserved	Otherwise	RsvdP	No	0
1	**Port 1 Link Down** 1 = Port 1 Link transitioned from the *DL_Active* state to the *DL_Inactive* state	0, accessible through the Management Port	RW1C	Yes	0
	Reserved	Otherwise	RsvdP	No	0
2	**Port 2 Link Down** 1 = Port 2 Link transitioned from the *DL_Active* state to the *DL_Inactive* state	0, accessible through the Management Port	RW1C	Yes	0
	Reserved	Otherwise	RsvdP	No	0
3	**Port 3 Link Down** 1 = Port 3 Link transitioned from the *DL_Active* state to the *DL_Inactive* state	0, accessible through the Management Port	RW1C	Yes	0
	Reserved	Otherwise	RsvdP	No	0
15:4	***Reserved***		RsvdP	No	000h

Register 13-162. 904h Switch Link Down (Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
16	**Port 16 Link Down** 1 = Port 16 Link transitioned from the *DL_Active* state to the *DL_Inactive* state	0, accessible through the Management Port	RW1C	Yes	0
	Reserved	Otherwise	RsvdP	No	0
17	**Port 17 Link Down** 1 = Port 17 Link transitioned from the *DL_Active* state to the *DL_Inactive* state	0, accessible through the Management Port	RW1C	Yes	0
	Reserved	Otherwise	RsvdP	No	0
18	**Port 18 Link Down** 1 = Port 18 Link transitioned from the *DL_Active* state to the *DL_Inactive* state	0, accessible through the Management Port	RW1C	Yes	0
	Reserved	Otherwise	RsvdP	No	0
19	**Port 19 Link Down** 1 = Port 19 Link transitioned from the *DL_Active* state to the *DL_Inactive* state	0, accessible through the Management Port	RW1C	Yes	0
	Reserved	Otherwise	RsvdP	No	0
20	**Port 20 Link Down** 1 = Port 20 Link transitioned from the *DL_Active* state to the *DL_Inactive* state	0, accessible through the Management Port	RW1C	Yes	0
	Reserved	Otherwise	RsvdP	No	0
21	**Port 21 Link Down** 1 = Port 21 Link transitioned from the *DL_Active* state to the *DL_Inactive* state	0, accessible through the Management Port	RW1C	Yes	0
	Reserved	Otherwise	RsvdP	No	0
22	**Port 22 Link Down** 1 = Port 22 Link transitioned from the *DL_Active* state to the *DL_Inactive* state	0, accessible through the Management Port	RW1C	Yes	0
	Reserved	Otherwise	RsvdP	No	0
23	**Port 23 Link Down** 1 = Port 23 Link transitioned from the *DL_Active* state to the *DL_Inactive* state	0, accessible through the Management Port	RW1C	Yes	0
	Reserved	Otherwise	RsvdP	No	0
31:24	***Reserved***		RsvdP	No	00h

Register 13-163. 908h Switch Link Event Mask (Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
Note: *The bits in this register can be used to mask their respective* ***Switch Link Status*** *register bits (Port 0, accessible through the Management Port, offset 90Ch).*					
0	**Port 0 Link Event Mask** 0 = Interrupt for Port 0 due to a Link Up or Link Down event is not masked 1 = Interrupt for Port 0 due to a Link Up or Link Down event is masked	0, accessible through the Management Port	RWS	Yes	1
	Reserved	Otherwise	RsvdP	No	0
1	**Port 1 Link Event Mask** 0 = Interrupt for Port 1 due to a Link Up or Link Down event is not masked 1 = Interrupt for Port 1 due to a Link Up or Link Down event is masked	0, accessible through the Management Port	RWS	Yes	1
	Reserved	Otherwise	RsvdP	No	0
2	**Port 2 Link Event Mask** 0 = Interrupt for Port 2 due to a Link Up or Link Down event is not masked 1 = Interrupt for Port 2 due to a Link Up or Link Down event is masked	0, accessible through the Management Port	RWS	Yes	1
	Reserved	Otherwise	RsvdP	No	0
3	**Port 3 Link Event Mask** 0 = Interrupt for Port 3 due to a Link Up or Link Down event is not masked 1 = Interrupt for Port 3 due to a Link Up or Link Down event is masked	0, accessible through the Management Port	RWS	Yes	1
	Reserved	Otherwise	RsvdP	No	0
15:4	***Reserved***		RsvdP	No	000h

Register 13-163. 908h Switch Link Event Mask (Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
16	**Port 16 Link Event Mask** 0 = Interrupt for Port 16 due to a Link Up or Link Down event is not masked 1 = Interrupt for Port 16 due to a Link Up or Link Down event is masked	0, accessible through the Management Port	RWS	Yes	1
	Reserved	Otherwise	RsvdP	No	0
17	**Port 17 Link Event Mask** 0 = Interrupt for Port 17 due to a Link Up or Link Down event is not masked 1 = Interrupt for Port 17 due to a Link Up or Link Down event is masked	0, accessible through the Management Port	RWS	Yes	1
	Reserved	Otherwise	RsvdP	No	0
18	**Port 18 Link Event Mask** 0 = Interrupt for Port 18 due to a Link Up or Link Down event is not masked 1 = Interrupt for Port 18 due to a Link Up or Link Down event is masked	0, accessible through the Management Port	RWS	Yes	1
	Reserved	Otherwise	RsvdP	No	0
19	**Port 19 Link Event Mask** 0 = Interrupt for Port 19 due to a Link Up or Link Down event is not masked 1 = 1 = Interrupt for Port 19 due to a Link Up or Link Down event is masked	0, accessible through the Management Port	RWS	Yes	1
	Reserved	Otherwise	RsvdP	No	0

Register 13-163. 908h Switch Link Event Mask (Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
20	**Port 20 Link Event Mask** 0 = Interrupt for Port 20 due to a Link Up or Link Down event is not masked 1 = 1 = Interrupt for Port 20 due to a Link Up or Link Down event is masked	0, accessible through the Management Port	RWS	Yes	1
	Reserved	Otherwise	RsvdP	No	0
21	**Port 21 Link Event Mask** 0 = Interrupt for Port 21 due to a Link Up or Link Down event is not masked 1 = 1 = Interrupt for Port 21 due to a Link Up or Link Down event is masked	0, accessible through the Management Port	RWS	Yes	1
	Reserved	Otherwise	RsvdP	No	0
22	**Port 22 Link Event Mask** 0 = Interrupt for Port 22 due to a Link Up or Link Down event is not masked 1 = 1 = Interrupt for Port 22 due to a Link Up or Link Down event is masked	0, accessible through the Management Port	RWS	Yes	1
	Reserved	Otherwise	RsvdP	No	0
23	**Port 23 Link Event Mask** 0 = Interrupt for Port 23 due to a Link Up or Link Down event is not masked 1 = Interrupt for Port 23 due to a Link Up or Link Down event is masked	0, accessible through the Management Port	RWS	Yes	1
	Reserved	Otherwise	RsvdP	No	0
31:24	***Reserved***		RsvdP	No	00h

Register 13-164. 90Ch Switch Link Status (Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
Note: *The bits in this register can be masked by their respective* ***Switch Link Event Mask*** *register bits (Port 0, accessible through the Management Port, offset 908h).*					
0	**Port 0 Link Status** 0 = Indicates that Port 0 is in a *DL_Inactive* state 1 = Indicates that Port 0 is in a *DL_Active* state	0, accessible through the Management Port	RO	Yes	0
	Reserved	Otherwise	RsvdP	No	0
1	**Port 1 Link Status** 0 = Indicates that Port 1 is in a *DL_Inactive* state 1 = Indicates that Port 1 is in a *DL_Active* state	0, accessible through the Management Port	RO	Yes	0
	Reserved	Otherwise	RsvdP	No	0
2	**Port 2 Link Status** 0 = Indicates that Port 2 is in a *DL_Inactive* state 1 = Indicates that Port 2 is in a *DL_Active* state	0, accessible through the Management Port	RO	Yes	0
	Reserved	Otherwise	RsvdP	No	0
3	**Port 3 Link Status** 0 = Indicates that Port 3 is in a *DL_Inactive* state 1 = Indicates that Port 3 is in a *DL_Active* state	0, accessible through the Management Port	RO	Yes	0
	Reserved	Otherwise	RsvdP	No	0
15:4	***Reserved***		RsvdP	No	000h
16	**Port 16 Link Status** 0 = Indicates that Port 16 is in a *DL_Inactive* state 1 = Indicates that Port 16 is in a *DL_Active* state	0, accessible through the Management Port	RO	Yes	0
	Reserved	Otherwise	RsvdP	No	0
17	**Port 17 Link Status** 0 = Indicates that Port 17 is in a *DL_Inactive* state 1 = Indicates that Port 17 is in a *DL_Active* state	0, accessible through the Management Port	RO	Yes	0
	Reserved	Otherwise	RsvdP	No	0
18	**Port 18 Link Status** 0 = Indicates that Port 18 is in a *DL_Inactive* state 1 = Indicates that Port 18 is in a *DL_Active* state	0, accessible through the Management Port	RO	Yes	0
	Reserved	Otherwise	RsvdP	No	0
19	**Port 19 Link Status** 0 = Indicates that Port 19 is in a *DL_Inactive* state 1 = Indicates that Port 19 is in a *DL_Active* state	0, accessible through the Management Port	RO	Yes	0
	Reserved	Otherwise	RsvdP	No	0

Register 13-164. 90Ch Switch Link Status (Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
20	**Port 20 Link Status** 0 = Indicates that Port 20 is in a *DL_Inactive* state 1 = Indicates that Port 20 is in a *DL_Active* state	0, accessible through the Management Port	RO	Yes	0
	Reserved	Otherwise	RsvdP	No	0
21	**Port 21 Link Status** 0 = Indicates that Port 21 is in a *DL_Inactive* state 1 = Indicates that Port 21 is in a *DL_Active* state	0, accessible through the Management Port	RO	Yes	0
	Reserved	Otherwise	RsvdP	No	0
22	**Port 22 Link Status** 0 = Indicates that Port 22 is in a *DL_Inactive* state 1 = Indicates that Port 22 is in a *DL_Active* state	0, accessible through the Management Port	RO	Yes	0
	Reserved	Otherwise	RsvdP	No	0
23	**Port 23 Link Status** 0 = Indicates that Port 23 is in a *DL_Inactive* state 1 = Indicates that Port 23 is in a *DL_Active* state	0, accessible through the Management Port	RO	Yes	0
	Reserved	Otherwise	RsvdP	No	0
31:24	***Reserved***		RsvdP	No	00h

Register 13-165. 910h VS Upstream to Management Upstream Doorbell Request (Virtual Switch mode – VS Upstream Port(s) and Management Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
3:0	**Doorbell** Writing 1 to any bit in this field, in the Non-Management VS upstream Port(s), signals an interrupt to the Management upstream Port. The Management Port Clears the interrupt(s), by writing 1 to the bit(s) that are Set.	Non-Management VS Upstream Port	RW	Yes	0h
		Management Port	RW1C	Yes	0h
	Reserved	Otherwise	RsvdP	No	0h
31:4	***Reserved***		RsvdP	No	0000_000h

Register 13-166. 914h VS Upstream to Management Upstream Doorbell Mask (Virtual Switch mode – VS Upstream Port(s) and Management Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
3:0	**Doorbell Interrupt Mask** 0 = Doorbell interrupts to the Management upstream Port are not masked 1 = Doorbell interrupts to the Management upstream Port are masked	Non-Management VS Upstream Port	RW	Yes	Fh
		Management Port	RW1C	Yes	Fh
	Reserved	Otherwise	RsvdP	No	0h
31:4	***Reserved***		RsvdP	No	0000_000h

Register 13-167. 918h VS Upstream to Management Upstream Scratchpad 1 (Virtual Switch mode – VS Upstream Port(s) and Management Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
31:0	**Scratchpad 1** 32-bit Scratchpad 1 register.	Non-Management VS Upstream Port	RWS	Yes	0000_0000h
		Management Port	ROS	Yes	0000_0000h
	Reserved	Otherwise	RsvdP	No	0000_0000h

Register 13-168. 91Ch VS Upstream to Management Upstream Scratchpad 2 (Virtual Switch mode – VS Upstream Port(s) and Management Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
31:0	**Scratchpad 2** 32-bit Scratchpad 2 register.	Non-Management VS Upstream Port	RWS	Yes	0000_0000h
		Management Port	ROS	Yes	0000_0000h
	Reserved	Otherwise	RsvdP	No	0000_0000h

Register 13-169. 920h VS Upstream to Management Upstream Scratchpad 3 (Virtual Switch mode – VS Upstream Port(s) and Management Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
31:0	**Scratchpad 3** 32-bit Scratchpad 3 register.	Non-Management VS Upstream Port	RWS	Yes	0000_0000h
		Management Port	ROS	Yes	0000_0000h
	Reserved	Otherwise	RsvdP	No	0000_0000h

Register 13-170. 924h VS Upstream to Management Upstream Scratchpad 4 (Virtual Switch mode – VS Upstream Port(s) and Management Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
31:0	**Scratchpad 4** 32-bit Scratchpad 4 register.	Non-Management VS Upstream Port	RWS	Yes	0000_0000h
		Management Port	ROS	Yes	0000_0000h
	Reserved	Otherwise	RsvdP	No	0000_0000h

Register 13-171. 928h Management Upstream to VS Upstream Doorbell Request (Virtual Switch mode – VS Upstream Port(s) and Management Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
3:0	**Doorbell** Writing 1 to any bit in this field, in the Management Port, signals an interrupt to the VS upstream Port(s). The Non-Management VS upstream Port(s) Clear(s) the interrupt(s), by writing 1 to the bit(s) that are Set.	Non-Management VS Upstream Port	RW1C	Yes	0h
		Management Port	RW	Yes	0h
	Reserved	Otherwise	RsvdP	No	0h
31:4	***Reserved***		RsvdP	No	0000_000h

Register 13-172. 92Ch Management Upstream to VS Upstream Doorbell Mask (Virtual Switch mode – VS Upstream Port(s) and Management Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
3:0	**Doorbell Interrupt Mask** 0 = Doorbell interrupts to the VS upstream Ports are not masked 1 = Doorbell interrupts to the VS upstream Ports are masked	Non-Management VS Upstream Port	RW1C	Yes	Fh
		Management Port	RW	Yes	Fh
	Reserved	Otherwise	RsvdP	No	0h
31:4	***Reserved***		RsvdP	No	0000_000h

Register 13-173. 930h Management Upstream to VS Upstream Scratchpad 1 (Virtual Switch mode – VS Upstream Port(s) and Management Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
31:0	**Scratchpad 1** 32-bit Scratchpad 1 register.	Non-Management VS Upstream Port	ROS	Yes	0000_0000h
		Management Port	RWS	Yes	0000_0000h
	Reserved	Otherwise	RsvdP	No	0000_0000h

Register 13-174. 934h Management Upstream to VS Upstream Scratchpad 2 (Virtual Switch mode – VS Upstream Port(s) and Management Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
31:0	**Scratchpad 2** 32-bit Scratchpad 2 register.	Non-Management VS Upstream Port	ROS	Yes	0000_0000h
		Management Port	RWS	Yes	0000_0000h
	Reserved	Otherwise	RsvdP	No	0000_0000h

Register 13-175. 938h Management Upstream to VS Upstream Scratchpad 3 (Virtual Switch mode – VS Upstream Port(s) and Management Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
31:0	**Scratchpad 3** 32-bit Scratchpad 3 register.	Non-Management VS Upstream Port	ROS	Yes	0000_0000h
		Management Port	RWS	Yes	0000_0000h
	Reserved	Otherwise	RsvdP	No	0000_0000h

Register 13-176. 93Ch Management Upstream to VS Upstream Scratchpad 4 (Virtual Switch mode – VS Upstream Port(s) and Management Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
31:0	**Scratchpad 4** 32-bit Scratchpad 4 register.	Non-Management VS Upstream Port	ROS	Yes	0000_0000h
		Management Port	RWS	Yes	0000_0000h
	Reserved	Otherwise	RsvdP	No	0000_0000h

13.15.14 Device-Specific Registers – Ingress Credit Handler (Offsets 9F0h – A2Ch)

This section details the Device-Specific Ingress Credit Handler (INCH) registers. Table 13-33 defines the register map.

Table 13-33. Device-Specific INCH Register Map (Ports[a])

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
INCH Station Pool Values		9F0h
Factory Test Only		9F4h
INCH Reserve Pool		9F8h
Reserved	INCH Port Pool	9FCh
INCH Threshold VC0 Posted		A00h
Factory Test Only	INCH Threshold VC0 Non-Posted	A04h
INCH Threshold VC0 Completion		A08h
Reserved		A0Ch – A2Ch

a. Certain registers are Port-specific, others are Station-specific; all are Device-specific.

Register 13-177. 9F0h INCH Station Pool Values (Base mode – Ports 0, 16, and 20; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
INCH Reserve pool.				
7:0	**Current Value of Header Pool for the Station**	RO	Yes	–
15:8	***Reserved***	RsvdP	No	00h
24:16	**Current Value of Payload Link Pool for the Station**	RO	Yes	–
31:25	***Reserved***	RsvdP	No	0-0h

Register 13-178. 9F8h INCH Reserve Pool (Base mode – Ports 0, 16, and 20; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
7:0	**Header Counter to Remove from Station Header Pool** Value of Header to remove from the initial Header pool.	RW	Yes	00h
15:8	***Reserved***	RsvdP	No	00h
24:16	**Payload Link Counter to Remove from Station Payload Pool** Value of Payload Links to remove from the initial Payload Link pool.	RW	Yes	0-0h
31:25	***Reserved***	RsvdP	No	0-0h

Register 13-179. 9FCh INCH Port Pool (Base mode – All Ports; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
Note: ***Consider the INCH Port Pool register to be reserved and only change the credit settings, using the INCH Threshold registers (Base mode – All Ports; Virtual Switch mode – Port 0, accessible through the Management Port, offsets A00h through A08h). Do not change the INCH Port Pool register from its default value, unless directed otherwise by PLX Technical Support.***				
2:0	**Port Payload Pool** Payload credits (other than the initial credits) for Posted/Completion TLPs that are dedicated to the corresponding PEX 8649 Port. 000b = 0 001b = 32 010b = 64 011b = 96 100b = 128 101b = 192 110b, 111b = 256	RWS	Yes	000b
3	**Unused 0** Keep value at 0. Additional bit for the Port Payload Pool.	RWS	Yes	0
6:4	**Port Header Pool** Combined Header credits (other than the initial credits) that are dedicated to the corresponding PEX 8649 Port. 000b = 0 TLP 001b = 4 TLPs 010b = 8 TLPs 011b = 16 TLPs 100b = 32 TLPs 101b = 48 TLPs 110b, 111b = 64 TLPs	RWS	Yes	000b
7	**Unused 1** Keep value at 0. Additional bit for the Port Header Pool.	RWS	Yes	0
31:8	***Reserved***	RsvdP	No	0000_00h

Register 13-180. A00h INCH Threshold VC0 Posted (Base mode – All Ports; Virtual Switch mode – Port 0, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default	
Posted credits are used for VC0 Memory Write and Message transactions. ***Note:*** ***Changing credit values from default register values must be done carefully; otherwise the PEX 8649 will not properly function.***					
2:0	***Reserved***	RsvdP	No	Upstream: 80h Downstream: x16: 110h x8: 90h x4: 80h	Upstream: x16: 2080h x8: 1080h x4: 0880h Downstream: x16: 2110h x8: 1790h x4: 0C80h
8:3	**Posted Payload Credit** Default advertised Posted Payload credit. Actual value is dependent upon Link width and Port configuration. Bit resolution is in units of 8. Each increment provides 8 Posted Payload credits (*for example*, Ah = 80 Posted Payload credits). Each credit means that 16 bytes of storage are reserved for Posted TLP Payload data.	RWS	Yes		
15:9	**Posted Header Credit** Default advertised Posted Header credit. Actual value is dependent upon Link width and Port configuration. Bit resolution is 1 for 1. Each increment provides 1 Posted Header credit (*for example*, Ah = 10 Posted Header credits). Each credit means that storage is reserved for the entire Header of a Posted TLP.	RWS	Yes	Upstream: x16: 40h x8: 20h x4: 10h Downstream: x16: 58h x8: 2Eh x4: 19h	
17:16	**UpdateFC High-Priority Threshold for Posted Payload Credit** 00b = 75% (default) 01b = 50% 10b = 25% 11b = 100%	RWS	Yes	00b	
19:18	**UpdateFC High-Priority Threshold for Posted Header Credit** 00b = 75% (default) 01b = 50% 10b = 25% 11b = 100%	RWS	Yes	00b	

Register 13-180. A00h INCH Threshold VC0 Posted (Base mode – All Ports; Virtual Switch mode – Port 0, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
22:20	**Congested Port Weight** If the effective rate setting times the negotiated Port Link width equates to less than x1 or greater than x8, the internal Credit Allocation logic rounds to x1 or x8, respectively. 000b = Request is weighted, based upon the Port’s Link width relative to the effective Link widths of the other Stations’ Ports 001b = Increases the weight of a Request by 2x 010b = Increases the weight of a Request by 4x 011b = Increases the weight of a Request by 8x 100b = Port receives no credit out of the common pool, until a decongested state is reached 101b = Decreases the weight of a Request by 2x 110b = Decreases the weight of a Request by 4x 111b = Decreases the weight of a Request by 8x	RWS	Yes	000b
31:23	***Reserved***	RsvdP	No	0-0h

Register 13-181. A04h INCH Threshold VC0 Non-Posted (Base mode – All Ports; Virtual Switch mode – Port 0, accessible through the Management Port)

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I^2C</th><th colspan="2">Default</th></tr>
<tr><td colspan="6">Non-Posted credits are used for VC0 Memory Read, I/O Read, I/O Write, Configuration Read, and Configuration Write transactions.
<b><i>Note: Changing credit values from default register values must be done carefully; otherwise the PEX 8649 will not properly function.</i></b></td></tr>
<tr><td>8:0</td><td><b>Non-Posted Payload Credit</b>
The Non-Posted Payload is stored with the Non-Posted Header; therefore Non-Posted Payload credit is always available. Because of this, the PEX 8649 hardwires this field to 000h (infinite credits).</td><td>RsvdP</td><td>No</td><td>Upstream:
000h
Downstream:
000h</td><td rowspan="2">Upstream:
x16: 1000h
x8: 0800h
x4: 0600h
Downstream:
x16: 1B00h
x8: 0E00h
x4: 0800h</td></tr>
<tr><td>15:9</td><td><b>Non-Posted Header Credit</b>
Default advertised Posted Header credit. Actual value is dependent upon Link width and Port configuration.
Bit resolution is 1 for 1. Each increment provides 1 Non-Posted Header credit (<i>for example</i>, Ah = 10 Non-Posted Header credits). Each credit means that storage is reserved for the entire Header of a Non-Posted TLP.</td><td>RWS</td><td>Yes</td><td>Upstream:
x16: 20h
x8: 16h
x4: 0Ch
Downstream:
x16: 37h
x8: 1Dh
x4: 10h</td></tr>
<tr><td>17:16</td><td><b>UpdateFC High-Priority Threshold for Non-Posted Payload Credit</b>
00b = 75% (default)
01b = 50%
10b = 25%
11b = 100%</td><td>RWS</td><td>Yes</td><td colspan="2">00b</td></tr>
<tr><td>19:18</td><td><b>UpdateFC High-Priority Threshold for Non-Posted Header Credit</b>
00b = 75% (default)
01b = 50%
10b = 25%
11b = 100%</td><td>RWS</td><td>Yes</td><td colspan="2">00b</td></tr>
<tr><td>22:20</td><td><b><i>Not used</i></b></td><td>RWS</td><td>Yes</td><td colspan="2">000b</td></tr>
<tr><td>23</td><td><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td colspan="2">0</td></tr>
<tr><td>29:24</td><td><b><i>Factory Test Only</i></b></td><td>RWS</td><td>Yes</td><td colspan="2">0-0h</td></tr>
<tr><td>31:30</td><td><b><i>Factory Test Only</i></b></td><td>RW1C</td><td>No</td><td colspan="2">00b</td></tr>
</table>

Register 13-182. A08h INCH Threshold VC0 Completion (Base mode – All Ports; Virtual Switch mode – Port 0, accessible through the Management Port)

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I^2C</th><th colspan="2">Default</th></tr>
<tr><td colspan="6">Completion credits are used for VC0 Memory Read, I/O Read, I/O Write, Configuration Read, and Configuration Write transaction Completions.
<b><i>Note: Changing credit values from default register values must be done carefully; otherwise the PEX 8649 will not properly function.</i></b></td></tr>
<tr><td>2:0</td><td><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td rowspan="2">Upstream:
x16: 100h
x8: 90h
x4: 80h
Downstream:
x16: 80h
x8: 80h
x4: 80h</td><td rowspan="3">Upstream:
x16: 2100h
x8: 1090h
x4: 0C80h
Downstream:
x16: 1080h
x8: 0B80h
x4: 0680h</td></tr>
<tr><td>8:3</td><td><b>Completion Payload Credit</b>
Default advertised Completion Payload credit. Actual value is dependent upon Link width and Port configuration.
Bit resolution is in units of 8. Each increment provides 8 Completion Payload credits (<i>for example</i>, Ah = 80 Completion Payload credits). Each credit means that 16 bytes of storage are reserved for Completion TLP Payload data.</td><td>RWS</td><td>Yes</td></tr>
<tr><td>15:9</td><td><b>Completion Header Credit</b>
Default advertised Completion Header credit. Actual value is dependent upon Link width and Port configuration.
Bit resolution is 1 for 1. Each increment provides 1 Completion Header credit (<i>for example</i>, Ah = 10 Completion Header credits). Each credit means that storage is reserved for the entire Header of a Completion TLP.</td><td>RWS</td><td>Yes</td><td>Upstream:
x16: 40h
x8: 20h
x4: 18h
Downstream:
x16: 20h
x8: 16h
x4: 0Ch</td></tr>
<tr><td>17:16</td><td><b>UpdateFC High-Priority Threshold for Completion Payload Credit</b>
00b = 75% (default)
01b = 50%
10b = 25%
11b = 100%</td><td>RWS</td><td>Yes</td><td colspan="2">00b</td></tr>
<tr><td>19:18</td><td><b>UpdateFC High-Priority Threshold for Completion Header Credit</b>
00b = 75% (default)
01b = 50%
10b = 25%
11b = 100%</td><td>RWS</td><td>Yes</td><td colspan="2">00b</td></tr>
<tr><td>22:20</td><td><b><i>Not used</i></b></td><td>RWS</td><td>Yes</td><td colspan="2">000b</td></tr>
<tr><td>31:23</td><td><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td colspan="2">0-0h</td></tr>
</table>

13.15.15 Device-Specific Registers – Virtual Switch Debug and GPIO Status and Control (Offsets A30h – B6Ch)

This section details the Device-Specific Virtual Switch Debug and GPIO Status and Control registers located at offsets A30h through B6Ch. These registers are implemented only in the upstream Port(s). Table 13-34 defines the register map.

Table 13-34. Device-Specific Virtual Switch Debug and GPIO Status and Control Register Map (Offsets A30h – B6Ch) (Upstream Port(s))

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Virtual Switch Debug		A30h
Reserved (Base Mode) Virtual Switch GPIO_PG 0_9 Direction Control (Virtual Switch Mode)		A34h
Reserved (Base Mode) Virtual Switch GPIO_PG 10_11 Direction Control (Virtual Switch Mode)		A38h
Reserved (Base Mode) Virtual Switch GPIO_PG 0_11 Availability (Virtual Switch Mode)		A3Ch
Reserved (Base Mode) Virtual Switch GPIO_PG 0_11 Input De-Bounce (Virtual Switch Mode)		A40h
Reserved (Base Mode) Virtual Switch GPIO_PG 0_11 Input Data (Virtual Switch Mode)		A44h
Reserved (Base Mode) Virtual Switch GPIO_PG 0_11 Output Data (Virtual Switch Mode)		A48h
Reserved (Base Mode) Virtual Switch GPIO_PG 0_11 Interrupt Polarity (Virtual Switch Mode)		A4Ch
Reserved (Base Mode) Virtual Switch GPIO_PG 0_11 Interrupt Status (Virtual Switch Mode)		A50h
Reserved (Base Mode) Virtual Switch GPIO_PG 0_11 Interrupt Mask (Virtual Switch Mode)		A54h
Reserved	***Reserved*** (Base Mode) Virtual Switch GPIO_SHP 0_7 Direction Control (Virtual Switch Mode)	A58h
Reserved (Base Mode) Virtual Switch GPIO_SHP 0_7 Availability (Virtual Switch Mode)		A5Ch

Table 13-34. Device-Specific Virtual Switch Debug and GPIO Status and Control Register Map (Offsets A30h – B6Ch) (Upstream Port(s)) ***(Cont.)***

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved	***Reserved*** (Base Mode) Virtual Switch GPIO_SHP 0_7 Input De-Bounce (Virtual Switch Mode)	A60h
Reserved	***Reserved*** (Base Mode) Virtual Switch GPIO_SHP 0_7 Input Data (Virtual Switch Mode)	A64h
Reserved	***Reserved*** (Base Mode) Virtual Switch GPIO_SHP 0_7 Output Data (Virtual Switch Mode)	A68h
Reserved	***Reserved*** (Base Mode) Virtual Switch GPIO_SHP 0_7 Interrupt Polarity (Virtual Switch Mode)	A6Ch
Reserved	***Reserved*** (Base Mode) Virtual Switch GPIO_SHP 0_7 Interrupt Status (Virtual Switch Mode)	A70h
Reserved	***Reserved*** (Base Mode) Virtual Switch GPIO_SHP 0_7 Interrupt Mask (Virtual Switch Mode)	A74h
Reserved		A78h – B6Ch

Register 13-183. A30h Virtual Switch Debug (Upstream Port(s))

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
1:0	**Interrupt Fencing Mode Select** ***Note:*** *A Fundamental Reset is needed to recover from Fencing errors.* **Mode 1 (Default)** **1.** When the PEX 8649 receives a packet with a Fatal error (Malformed, DLL Protocol error) from an external device, or the device detects a Credit Overflow, Receiver Overflow, or Surprise Link Down, the switch logs the Header on the corresponding Port, sends a Fatal Error Message to the Host, then asserts FATAL_ERR# and/or VS*x*_FATAL_ERR#. **2.** When the PEX 8649 detects an internal Fatal error (ECC failure), the switch sends a Fatal Interrupt Message to the Host and asserts FATAL_ERR# and/or VS*x*_FATAL_ERR#. In certain situations, delivery of the interrupt is not guaranteed; however, the signal is always asserted upon a Fatal event. **Mode 2 (Generate Internal Reset) – Base Mode Only** Upon Fatal error (internal or external) detection, an internal Chip Level reset is asserted (equivalent to an In-Band Reset from the upstream Port). No Error Messages are generated, and no attempt is made to block packets in transit. **Mode 3 (Block All Packet Transmission)** Upon Fatal error (internal or external) detection, the Port logs the error in the **Uncorrectable Error Status** register (offset FB8h), then asserts FATAL_ERR# and/or VS*x*_FATAL_ERR#. This Fatal error detection blocks all the Ports from sending out TLPs. No Error Messages are generated. If a packet is already in transmission, an EDB is inserted to cancel the packet. **Mode 4 (Block All Packet Transmission and Create Surprise Down)** In addition to the Mode 3 actions, the PEX 8649 forces the upstream Link to go down, thus causing a Surprise Down event on the Link, so that the Host is notified. 00b = Mode 1 (default) 01b = Mode 2 – Generate Internal Reset 10b = Mode 3 – Block All Packet Transmission 11b = Mode 4 – Block All Packet Transmission and Create Surprise Down	Upstream	RWS	Yes	00b
	Reserved	Downstream	RsvdP	No	00b

Register 13-183. A30h Virtual Switch Debug (Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
2	**Upstream Hot Reset Control** 0 = Reset all logic, except Sticky bits and Device-Specific registers 1 = Reset only the Configuration Space registers of all Ports defined by the *PCI Express Base r2.0* ***Note:*** *Only a Fundamental Reset serial EEPROM load affects this bit.*	Upstream	RWS	Yes	0
	Reserved	Downstream	RsvdP	No	0
3	**Disable Serial EEPROM Load on Hot Reset** 0 = Enables serial EEPROM load upon VS upstream Port Hot Reset or *DL_Down* state. Port-specific registers for other virtual switches are ***not*** reloaded. (default) **Virtual Switch mode** – Chip- and Station-specific register reload from serial EEPROM (which can affect other virtual switches) can be enabled by Setting the **Management Port Control** register *Active Management Port EEPROM Load on Hot Reset for Chip and Station Registers Enable* bit (Port 0, accessible through the Management Port and Redundant Management Port, offset 354h[6]). 1 = Disables serial EEPROM load upon VS upstream Port Hot Reset or *DL_Down* state	Upstream	RWS	Yes	0
	Reserved	Downstream	RsvdP	No	0
4	**Upstream Port and NT-Link Port DL_Down Reset Propagation Disable** Setting this bit: • Enables the upstream and NT-Link Ports to ignore a Hot Reset training sequence, • Blocks the PEX 8649 from manifesting an internal reset due to a DL_Down event, • Blocks the PEX 8649 NT Port Link Interface from manifesting an internal reset due to a DL_Down event on the NT Port Link, and • Prevents the downstream Ports from issuing a Hot Reset to downstream devices when a Hot Reset or DL_Down event occurs on the upstream Link	Upstream	RWS	Yes	0
	Reserved	Downstream	RsvdP	No	0
5	***Factory Test Only***		RWS	Yes	0
23:6	***Reserved***		RsvdP	No	0-0h

Register 13-183. A30h Virtual Switch Debug (Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
24	**Base Mode** **Virtual Interface Access Enable** Used only in Base mode, for NT mode. When the serial EEPROM is not present, the default value is 1; otherwise, the default value is 0. 0 = Retries Type 0 Configuration TLP received on the NT Port Virtual Interface 1 = Accepts Type 0 Configuration TLP on the NT Port Virtual Interface ***Notes:*** *This bit does not affect the PEX 8649 in Transparent mode, nor does it affect other transaction types.* *Set this bit to enable Configuration access to the NT Port Virtual Interface.*	Upstream	RW	Yes	1
	Reserved	Downstream	RsvdP	No	0
	Virtual Switch Mode ***Reserved***		RsvdP	No	0
25	**Base Mode** **Link Interface Access Enable** Used only in Base mode, for NT mode. 0 = Retries Type 0 Configuration Request received on the NT Port Link Interface 1 = Accepts Type 0 Configuration Request on the NT Port Link Interface ***Notes:*** *This bit does not affect the PEX 8649 in Transparent mode.* *Set this bit to enable Configuration access to the NT Port Link Interface.*	Upstream	RW	Yes	0
	Reserved	Downstream	RsvdP	No	0
	Virtual Switch Mode ***Reserved***		RsvdP	No	0

Register 13-183. A30h Virtual Switch Debug (Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
26	**Base Mode** **Inhibit EEPROM NT-Link Load on Hot Reset** Used only in Base mode, for NT mode. Inhibits serial EEPROM load of NT Port Link Interface registers when any one of the following conditions exist: • **Upstream Port Hot Reset** – Bits [3:2] (*Disable Serial EEPROM Load on Hot Reset* and *Upstream Hot Reset Control*, respectively) are Cleared • **Upstream Port *DL_Down* state** – Bits [4:2] (*Upstream Port and NT-Link Port DL_Down Reset Propagation Disable*, *Disable Serial EEPROM Load on Hot Reset*, and *Upstream Hot Reset Control*, respectively) are Cleared • **NT Port Link Interface Hot Reset or *DL_Down* state** – Bit 3 (*Disable Serial EEPROM Load on Hot Reset*) is Cleared Refer also to Section 6.9, “Serial EEPROM Loading of NT Port Link Interface Registers – Base Mode Only,” for further details.	Upstream	RW	Yes	0
	Reserved	Downstream	RsvdP	No	0
	Virtual Switch Mode ***Reserved***		RsvdP	No	0
27	**Base Mode** **Load Only EEPROM NT-Link on Hot Reset** Used only in Base mode, for NT mode. Load only serial EEPROM NT Port Link Interface register entries when any one of the following conditions exist: • **Upstream Port Hot Reset** – Bits [3:2] (*Disable Serial EEPROM Load on Hot Reset* and *Upstream Hot Reset Control*, respectively) are Cleared • **Upstream Port *DL_Down* state** – Bits [4:2] (*Upstream Port and NT-Link Port DL_Down Reset Propagation Disable, Disable Serial EEPROM Load on Hot Reset*, and *Upstream Hot Reset Control*, respectively) are Cleared • **NT Port Link Interface Hot Reset or *DL_Down* state** – Bit 3 (*Disable Serial EEPROM Load on Hot Reset*) is Cleared Refer also to Section 6.9, “Serial EEPROM Loading of NT Port Link Interface Registers – Base Mode Only,” for further details.	Upstream	RW	Yes	0
	Reserved	Downstream	RsvdP	No	0
	Virtual Switch Mode ***Reserved***		RsvdP	No	0
31:28	***Reserved***		RsvdP	No	0h

Register 13-184. A34h Virtual Switch GPIO_PG 0_9 Direction Control (Virtual Switch mode – VS Upstream Port(s))

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
This register provides a virtualized copy of the **GPIO 0_9 Direction Control** register (Port 0, accessible through the Management Port, offset 600h), to support the virtual switches. The main difference is that the virtual switches have no knowledge of which PEX_PORT_GOOD*x*# (PEX_PORT_GOOD[23:16, 3:0]#) signal is being used. A single GPIO ball/signal cannot be assigned to more than one virtual switch. ***Note:*** *Register offsets A44h and A48h, referenced in this register, are located in the VS Upstream Port(s).*				
1:0	**VS GPIO_PG 0 PEX_PORT_GOOD*x*# Source/Destination** **As Input:** 00b = To **VS GPIO_PG 0 PEX_PORT_GOODx# Input Data** register (offset A44h[0]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **VS GPIO_PG 0 PEX_PORT_GOODx# Output Data** register (offset A48h[0]) 01b = PEX_PORT_GOOD*x*# 10b, 11b = ***Reserved***	RWS	Yes	00b
2	**VS GPIO_PG 0 PEX_PORT_GOOD*x*# Direction Control** 0 = Input 1 = Output	RWS	Yes	0
4:3	**VS GPIO_PG 1 PEX_PORT_GOOD*x*# Source/Destination** **As Input:** 00b = To **VS GPIO_PG 1 PEX_PORT_GOODx# Input Data** register (offset A44h[1]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **VS GPIO_PG 1 PEX_PORT_GOODx# Output Data** register (offset A48h[1]) 01b = PEX_PORT_GOOD*x*# 10b, 11b = ***Reserved***	RWS	Yes	00b
5	**VS GPIO_PG 1 PEX_PORT_GOOD*x*# Direction Control** 0 = Input 1 = Output	RWS	Yes	0

Register 13-184. A34h Virtual Switch GPIO_PG 0_9 Direction Control (Virtual Switch mode – VS Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:6	**VS GPIO_PG 2 PEX_PORT_GOOD*x*# Source/Destination** **As Input:** 00b = To **VS GPIO_PG 2 PEX_PORT_GOODx# Input Data** register (offset A44h[2]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **VS GPIO_PG 2 PEX_PORT_GOODx# Output Data** register (offset A48h[2]) 01b = PEX_PORT_GOOD*x*# 10b, 11b = ***Reserved***	RWS	Yes	00b
8	**VS GPIO_PG 2 PEX_PORT_GOOD*x*# Direction Control** 0 = Input 1 = Output	RWS	Yes	0
10:9	**VS GPIO_PG 3 PEX_PORT_GOOD*x*# Source/Destination** **As Input:** 00b = To **VS GPIO_PG 3 PEX_PORT_GOODx# Input Data** register (offset A44h[3]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **VS GPIO_PG 3 PEX_PORT_GOODx# Output Data** register (offset A48h[3]) 01b = PEX_PORT_GOOD*x*# 10b, 11b = ***Reserved***	RWS	Yes	00b
11	**VS GPIO_PG 3 PEX_PORT_GOOD*x*# Direction Control** 0 = Input 1 = Output	RWS	Yes	0
13:12	**VS GPIO_PG 4 PEX_PORT_GOOD*x*# Source/Destination** **As Input:** 00b = To **VS GPIO_PG 4 PEX_PORT_GOODx# Input Data** register (offset A44h[4]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **VS GPIO_PG 4 PEX_PORT_GOODx# Output Data** register (offset A48h[4]) 01b = PEX_PORT_GOOD*x*# 10b, 11b = ***Reserved***	RWS	Yes	00b
14	**VS GPIO_PG 4 PEX_PORT_GOOD*x*# Direction Control** 0 = Input 1 = Output	RWS	Yes	0

Register 13-184. A34h Virtual Switch GPIO_PG 0_9 Direction Control (Virtual Switch mode – VS Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
16:15	**VS GPIO_PG 5 PEX_PORT_GOOD*x*# Source/Destination** **As Input:** 00b = To **VS GPIO_PG 5 PEX_PORT_GOODx# Input Data** register (offset A44h[5]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **VS GPIO_PG 5 PEX_PORT_GOODx# Output Data** register (offset A48h[5]) 01b = PEX_PORT_GOOD*x*# 10b, 11b = ***Reserved***	RWS	Yes	00b
17	**VS GPIO_PG 5 PEX_PORT_GOOD*x*# Direction Control** 0 = Input 1 = Output	RWS	Yes	0
19:18	**VS GPIO_PG 6 PEX_PORT_GOOD*x*# Source/Destination** **As Input:** 00b = To **VS GPIO_PG 6 PEX_PORT_GOODx# Input Data** register (offset A44h[6]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **VS GPIO_PG 6 PEX_PORT_GOODx# Output Data** register (offset A48h[6]) 01b = PEX_PORT_GOOD*x*# 10b, 11b = ***Reserved***	RWS	Yes	00b
20	**VS GPIO_PG 6 PEX_PORT_GOOD*x*# Direction Control** 0 = Input 1 = Output	RWS	Yes	0
22:21	**VS GPIO_PG 7 PEX_PORT_GOOD*x*# Source/Destination** **As Input:** 00b = To **VS GPIO_PG 7 PEX_PORT_GOODx# Input Data** register (offset A44h[7]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **VS GPIO_PG 7 PEX_PORT_GOODx# Output Data** register (offset A48h[7]) 01b = PEX_PORT_GOOD*x*# 10b, 11b = ***Reserved***	RWS	Yes	00b
23	**VS GPIO_PG 7 PEX_PORT_GOOD*x*# Direction Control** 0 = Input 1 = Output	RWS	Yes	0

Register 13-184. A34h Virtual Switch GPIO_PG 0_9 Direction Control (Virtual Switch mode – VS Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
25:24	**VS GPIO_PG 8 PEX_PORT_GOOD*x*# Source/Destination** **As Input:** 00b = To **VS GPIO_PG 8 PEX_PORT_GOODx# Input Data** register (offset A44h[8]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **VS GPIO_PG 8 PEX_PORT_GOODx# Output Data** register (offset A48h[8]) 01b = PEX_PORT_GOOD*x*# 10b, 11b = ***Reserved***	RWS	Yes	00b
26	**VS GPIO_PG 8 PEX_PORT_GOOD*x*# Direction Control** 0 = Input 1 = Output	RWS	Yes	0
28:27	**VS GPIO_PG 9 PEX_PORT_GOOD*x*# Source/Destination** **As Input:** 00b = To **VS GPIO_PG 9 PEX_PORT_GOODx# Input Data** register (offset A44h[9]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **VS GPIO_PG 9 PEX_PORT_GOODx# Output Data** register (offset A48h[9]) 01b = PEX_PORT_GOOD*x*# 10b, 11b = ***Reserved***	RWS	Yes	00b
29	**VS GPIO_PG 9 PEX_PORT_GOOD*x*# Direction Control** 0 = Input 1 = Output	RWS	Yes	0
31:30	***Reserved***	RsvdP	No	00b

Register 13-185. A38h Virtual Switch GPIO_PG 10_11 Direction Control (Virtual Switch mode – VS Upstream Port(s))

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
This register provides a virtualized copy of the **GPIO 10_11 Direction Control** register GPIO 10_11-related bits (Port 0, accessible through the Management Port, offset 604h), to support the virtual switches. The main difference is that the virtual switches have no knowledge of which PEX_PORT_GOOD*x*# (PEX_PORT_GOOD[23:16, 3:0]#) signal is being used. A single GPIO ball/signal cannot be assigned to more than one virtual switch. ***Note:*** *Register offsets A44h and A48h, referenced in this register, are located in the VS Upstream Port(s).*				
1:0	**VS GPIO_PG 10 PEX_PORT_GOOD*x*# Source/Destination** **As Input:** 00b = To **VS GPIO_PG 10 PEX_PORT_GOODx# Input Data** register (offset A44h[10]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **VS GPIO_PG 10 PEX_PORT_GOODx# Output Data** register (offset A48h[10]) 01b = PEX_PORT_GOOD*x*# 10b, 11b = ***Reserved***	RWS	Yes	00b
2	**VS GPIO_PG 10 PEX_PORT_GOOD*x*# Direction Control** 0 = Input 1 = Output	RWS	Yes	0
4:3	**VS GPIO_PG 11 PEX_PORT_GOOD*x*# Source/Destination** **As Input:** 00b = To **VS GPIO_PG 11 PEX_PORT_GOODx# Input Data** register (offset A44h[11]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **VS GPIO_PG 11 PEX_PORT_GOODx# Output Data** register (offset A48h[11]) 01b = PEX_PORT_GOOD*x*# 10b, 11b = ***Reserved***	RWS	Yes	00b
5	**VS GPIO_PG 11 PEX_PORT_GOOD*x*# Direction Control** 0 = Input 1 = Output	RWS	Yes	0
31:6	***Reserved***	RsvdP	No	0-0h

Register 13-186. A3Ch Virtual Switch GPIO_PG 0_11 Availability (Virtual Switch mode – VS Upstream Port(s))

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
3:0	**Number of GPIO_PGs Available** Indicates the number of PEX_PORT_GOOD*x*# signals assigned to each virtual switch. The value corresponds to the number of bits that are Set in the **VS*x* GPIO_PG 0_11 Assignment** register(s) (Port 0, accessible through the Management Port, offsets 650h through 65Ch). A single GPIO ball/signal cannot be assigned to more than one virtual switch. 0h = 1 (GPIO_PG 0) 1h = 2 (GPIO_PG 0_1) 2h = 3 (GPIO_PG 0_2) 3h = 4 (GPIO_PG 0_3) 4h = 5 (GPIO_PG 0_4) 5h = 6 (GPIO_PG 0_5) 6h = 7 (GPIO_PG 0_6) 7h = 8 (GPIO_PG 0_7) 8h = 9 (GPIO_PG 0_8) 9h = 10 (GPIO_PG 0_9) Ah = 11 (GPIO_PG 0_10) Bh = 12 (GPIO_PG 0_11) All other encodings are ***reserved***. ***Note:* Although this register is programmable, it should not be written.**	RWS	Yes	0h
31:4	***Reserved***	RsvdP	No	0000_000h

Register 13-187. A40h Virtual Switch GPIO_PG 0_11 Input De-Bounce (Virtual Switch mode – VS Upstream Port(s))

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
This register provides virtualized copies of the **GPIO 0_11 Input De-Bounce** register (Port 0, accessible through the Management Port, offset 614h), to support the virtual switches. The main difference is that the virtual switches have no knowledge of which PEX_PORT_GOOD*x*# (PEX_PORT_GOOD[23:16, 3:0]#) signal is being used. A single GPIO ball/signal cannot be assigned to more than one virtual switch. ***Note:*** *Register offsets A34h and A38h, referenced in this register, are located in the VS Upstream Port(s).*				
0	**VS GPIO_PG 0 PEX_PORT_GOOD*x*# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD*x*# is configured as an input (offset A34h[2], is Cleared). 0 = PEX_PORT_GOOD*x*# input is not de-bounced 1 = PEX_PORT_GOOD*x*# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
1	**VS GPIO_PG 1 PEX_PORT_GOOD*x*# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD*x*# is configured as an input (offset A34h[5], is Cleared). 0 = PEX_PORT_GOOD*x*# input is not de-bounced 1 = PEX_PORT_GOOD*x*# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
2	**VS GPIO_PG 2 PEX_PORT_GOOD*x*# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD*x*# is configured as an input (offset A34h[8], is Cleared). 0 = PEX_PORT_GOOD*x*# input is not de-bounced 1 = PEX_PORT_GOOD*x*# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
3	**VS GPIO_PG 3 PEX_PORT_GOOD*x*# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD*x*# is configured as an input (offset A34h[11], is Cleared). 0 = PEX_PORT_GOOD*x*# input is not de-bounced 1 = PEX_PORT_GOOD*x*# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0

Register 13-187. A40h Virtual Switch GPIO_PG 0_11 Input De-Bounce (Virtual Switch mode – VS Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4	**VS GPIO_PG 4 PEX_PORT_GOOD*x*# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD*x*# is configured as an input (offset A34h[14], is Cleared). 0 = PEX_PORT_GOOD*x*# input is not de-bounced 1 = PEX_PORT_GOOD*x*# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
5	**VS GPIO_PG 5 PEX_PORT_GOOD*x*# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD*x*# is configured as an input (offset A34h[17], is Cleared). 0 = PEX_PORT_GOOD*x*# input is not de-bounced 1 = PEX_PORT_GOOD*x*# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
6	**VS GPIO_PG 6 PEX_PORT_GOOD*x*# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD*x*# is configured as an input (offset A34h[20], is Cleared). 0 = PEX_PORT_GOOD*x*# input is not de-bounced 1 = PEX_PORT_GOOD*x*# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
7	**VS GPIO_PG 7 PEX_PORT_GOOD*x*# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD*x*# is configured as an input (offset A34h[23], is Cleared). 0 = PEX_PORT_GOOD*x*# input is not de-bounced 1 = PEX_PORT_GOOD*x*# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0

Register 13-187. A40h Virtual Switch GPIO_PG 0_11 Input De-Bounce (Virtual Switch mode – VS Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
8	**VS GPIO_PG 8 PEX_PORT_GOOD*x*# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD*x*# is configured as an input (offset A34h[26], is Cleared). 0 = PEX_PORT_GOOD*x*# input is not de-bounced 1 = PEX_PORT_GOOD*x*# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
9	**VS GPIO_PG 9 PEX_PORT_GOOD*x*# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD*x*# is configured as an input (offset A34h[29], is Cleared). 0 = PEX_PORT_GOOD*x*# input is not de-bounced 1 = PEX_PORT_GOOD*x*# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
10	**VS GPIO_PG 10 PEX_PORT_GOOD*x*# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD*x*# is configured as an input (offset A38h[2], is Cleared). 0 = PEX_PORT_GOOD*x*# input is not de-bounced 1 = PEX_PORT_GOOD*x*# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
11	**VS GPIO_PG 11 PEX_PORT_GOOD*x*# Input De-Bounce Control** Controls de-bounce when PEX_PORT_GOOD*x*# is configured as an input (offset A38h[5], is Cleared). 0 = PEX_PORT_GOOD*x*# input is not de-bounced 1 = PEX_PORT_GOOD*x*# input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
31:12	***Reserved***	RsvdP	No	0000_0h

Register 13-188. A44h Virtual Switch GPIO_PG 0_11 Input Data (Virtual Switch mode – VS Upstream Port(s))

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
	This register provides virtualized copies of the **GPIO 0_11 Input Data** register (Port 0, accessible through the Management Port, offset 61Ch), to support the virtual switches. The main difference is that the virtual switches have no knowledge of which PEX_PORT_GOOD*x*# (PEX_PORT_GOOD[23:16, 3:0]#) signal is being used. A single GPIO ball/signal cannot be assigned to more than one virtual switch. ***Note:*** *Register offsets A34h and A38h, referenced in this register, are located in the VS Upstream Port(s).*			
0	**VS GPIO_PG 0 PEX_PORT_GOOD*x*# Input Data** If PEX_PORT_GOOD*x*# is configured as an output (offset A34h[2], is Set), Reads return 0. If PEX_PORT_GOOD*x*# is configured as an input (offset A34h[2], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD*x*#.	RO	No	0
1	**VS GPIO_PG 1 PEX_PORT_GOOD*x*# Input Data** If PEX_PORT_GOOD*x*# is configured as an output (offset A34h[5], is Set), Reads return 0. If PEX_PORT_GOOD*x*# is configured as an input (offset A34h[5], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD*x*#.	RO	No	0
2	**VS GPIO_PG 2 PEX_PORT_GOOD*x*# Input Data** If PEX_PORT_GOOD*x*# is configured as an output (offset A34h[8], is Set), Reads return 0. If PEX_PORT_GOOD*x*# is configured as an input (offset A34h[8], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD*x*#.	RO	No	0
3	**VS GPIO_PG 3 PEX_PORT_GOOD*x*# Input Data** If PEX_PORT_GOOD*x*# is configured as an output (offset A34h[11], is Set), Reads return 0. If PEX_PORT_GOOD*x*# is configured as an input (offset A34h[11], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD*x*#.	RO	No	0

Register 13-188. A44h Virtual Switch GPIO_PG 0_11 Input Data (Virtual Switch mode – VS Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
4	**VS GPIO_PG 4 PEX_PORT_GOOD*x*# Input Data** If PEX_PORT_GOOD*x*# is configured as an output (offset A34h[14], is Set), Reads return 0. If PEX_PORT_GOOD*x*# is configured as an input (offset A34h[14], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD*x*#.	RO	No	0
5	**VS GPIO_PG 5 PEX_PORT_GOOD*x*# Input Data** If PEX_PORT_GOOD*x*# is configured as an output (offset A34h[17], is Set), Reads return 0. If PEX_PORT_GOOD*x*# is configured as an input (offset A34h[17], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD*x*#.	RO	No	0
6	**VS GPIO_PG 6 PEX_PORT_GOOD*x*# Input Data** If PEX_PORT_GOOD*x*# is configured as an output (offset A34h[20], is Set), Reads return 0. If PEX_PORT_GOOD*x*# is configured as an input (offset A34h[20], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD*x*#.	RO	No	0
7	**VS GPIO_PG 7 PEX_PORT_GOOD*x*# Input Data** If PEX_PORT_GOOD*x*# is configured as an output (offset A34h[23], is Set), Reads return 0. If PEX_PORT_GOOD*x*# is configured as an input (offset A34h[23], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD*x*#.	RO	No	0
8	**VS GPIO_PG 8 PEX_PORT_GOOD*x*# Input Data** If PEX_PORT_GOOD*x*# is configured as an output (offset A34h[26], is Set), Reads return 0. If PEX_PORT_GOOD*x*# is configured as an input (offset A34h[26], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD*x*#.	RO	No	0
9	**VS GPIO_PG 9 PEX_PORT_GOOD*x*# Input Data** If PEX_PORT_GOOD*x*# is configured as an output (offset A34h[29], is Set), Reads return 0. If PEX_PORT_GOOD*x*# is configured as an input (offset A34h[29], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD*x*#.	RO	No	0
10	**VS GPIO_PG 10 PEX_PORT_GOOD*x*# Input Data** If PEX_PORT_GOOD*x*# is configured as an output (offset A38h[2], is Set), Reads return 0. If PEX_PORT_GOOD*x*# is configured as an input (offset A38h[2], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD*x*#.	RO	No	0
11	**VS GPIO_PG 11 PEX_PORT_GOOD*x*# Input Data** If PEX_PORT_GOOD*x*# is configured as an output (offset A38h[5], is Set), Reads return 0. If PEX_PORT_GOOD*x*# is configured as an input (offset A38h[5], is Cleared), Reads return the logic value of the voltage on PEX_PORT_GOOD*x*#.	RO	No	0
31:12	***Reserved***	RsvdP	No	0000_0h

Register 13-189. A48h Virtual Switch GPIO_PG 0_11 Output Data (Virtual Switch mode – VS Upstream Port(s))

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register provides virtualized copies of the **GPIO 0_11 Output Data** register (Port 0, accessible through the Management Port, offset 624h), to support the virtual switches. The main difference is that the virtual switches have no knowledge of which PEX_PORT_GOOD*x*# (PEX_PORT_GOOD[23:16, 3:0]#) signal is being used. A single GPIO ball/signal cannot be assigned to more than one virtual switch. ***Note:*** *Register offsets A34h and A38h, referenced in this register, are located in the VS Upstream Port(s).*				
0	**VS GPIO_PG 0 PEX_PORT_GOOD*x*# Output Data** If PEX_PORT_GOOD*x*# is configured as an output (offset A34h[2], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD*x*# output. Reads return the value written.	RWS	Yes	0
1	**VS GPIO_PG 1 PEX_PORT_GOOD*x*# Output Data** If PEX_PORT_GOOD*x*# is configured as an output (offset A34h[5], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD*x*# output. Reads return the value written.	RWS	Yes	0
2	**VS GPIO_PG 2 PEX_PORT_GOOD*x*# Output Data** If PEX_PORT_GOOD*x*# is configured as an output (offset A34h[8], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD*x*# output. Reads return the value written.	RWS	Yes	0
3	**VS GPIO_PG 3 PEX_PORT_GOOD*x*# Output Data** If PEX_PORT_GOOD*x*# is configured as an output (offset A34h[11], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD*x*# output. Reads return the value written.	RWS	Yes	0
4	**VS GPIO_PG 4 PEX_PORT_GOOD*x*# Output Data** If PEX_PORT_GOOD*x*# is configured as an output (offset A34h[14], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD*x*# output. Reads return the value written.	RWS	Yes	0
5	**VS GPIO_PG 5 PEX_PORT_GOOD*x*# Output Data** If PEX_PORT_GOOD*x*# is configured as an output (offset A34h[17], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD*x*# output. Reads return the value written.	RWS	Yes	0
6	**VS GPIO_PG 6 PEX_PORT_GOOD*x*# Output Data** If PEX_PORT_GOOD*x*# is configured as an output (offset A34h[20], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD*x*# output. Reads return the value written.	RWS	Yes	0
7	**VS GPIO_PG 7 PEX_PORT_GOOD*x*# Output Data** If PEX_PORT_GOOD*x*# is configured as an output (offset A34h[23], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD*x*# output. Reads return the value written.	RWS	Yes	0

Register 13-189. A48h Virtual Switch GPIO_PG 0_11 Output Data (Virtual Switch mode – VS Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
8	**VS GPIO_PG 8 PEX_PORT_GOOD*x*# Output Data** If PEX_PORT_GOOD*x*# is configured as an output (offset A34h[26], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD*x*# output. Reads return the value written.	RWS	Yes	0
9	**VS GPIO_PG 9 PEX_PORT_GOOD*x*# Output Data** If PEX_PORT_GOOD*x*# is configured as an output (offset A34h[29], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD*x*# output. Reads return the value written.	RWS	Yes	0
10	**VS GPIO_PG 10 PEX_PORT_GOOD*x*# Output Data** If PEX_PORT_GOOD*x*# is configured as an output (offset A38h[2], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD*x*# output. Reads return the value written.	RWS	Yes	0
11	**VS GPIO_PG 11 PEX_PORT_GOOD*x*# Output Data** If PEX_PORT_GOOD*x*# is configured as an output (offset A38h[5], is Set), the value written to this bit is immediately driven to the PEX_PORT_GOOD*x*# output. Reads return the value written.	RWS	Yes	0
31:12	***Reserved***	RsvdP	No	0000_0h

Register 13-190. A4Ch Virtual Switch GPIO_PG 0_11 Interrupt Polarity (Virtual Switch mode – VS Upstream Port(s))

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register provides virtualized copies of the **GPIO 0_11 Interrupt Polarity** register (Port 0, accessible through the Management Port, offset 62Ch), to support the virtual switches. The main difference is that the virtual switches have no knowledge of which PEX_PORT_GOOD*x*# (PEX_PORT_GOOD[23:16, 3:0]#) signal is being used. A single GPIO ball/signal cannot be assigned to more than one virtual switch.				
0	**VS GPIO_PG 0 PEX_PORT_GOOD*x*# Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High for the PEX_PORT_GOOD*x*# signal. 0 = GPIO Interrupt input is Active-Low 1 = GPIO Interrupt input is Active-High	RWS	Yes	0
1	**VS GPIO_PG 1 PEX_PORT_GOOD*x*# Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High for the PEX_PORT_GOOD*x*# signal. 0 = GPIO Interrupt input is Active-Low 1 = GPIO Interrupt input is Active-High	RWS	Yes	0
2	**VS GPIO_PG 2 PEX_PORT_GOOD*x*# Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High for the PEX_PORT_GOOD*x*# signal. 0 = GPIO Interrupt input is Active-Low 1 = GPIO Interrupt input is Active-High	RWS	Yes	0
3	**VS GPIO_PG 3 PEX_PORT_GOOD*x*# Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High for the PEX_PORT_GOOD*x*# signal. 0 = GPIO Interrupt input is Active-Low 1 = GPIO Interrupt input is Active-High	RWS	Yes	0

Register 13-190. A4Ch Virtual Switch GPIO_PG 0_11 Interrupt Polarity (Virtual Switch mode – VS Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
4	**VS GPIO_PG 4 PEX_PORT_GOOD*x*# Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High for the PEX_PORT_GOOD*x*# signal. 0 = GPIO Interrupt input is Active-Low 1 = GPIO Interrupt input is Active-High	RWS	Yes	0
5	**VS GPIO_PG 5 PEX_PORT_GOOD*x*# Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High for the PEX_PORT_GOOD*x*# signal. 0 = GPIO Interrupt input is Active-Low 1 = GPIO Interrupt input is Active-High	RWS	Yes	0
6	**VS GPIO_PG 6 PEX_PORT_GOOD*x*# Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High for the PEX_PORT_GOOD*x*# signal. 0 = GPIO Interrupt input is Active-Low 1 = GPIO Interrupt input is Active-High	RWS	Yes	0
7	**VS GPIO_PG 7 PEX_PORT_GOOD*x*# Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High for the PEX_PORT_GOOD*x*# signal. 0 = GPIO Interrupt input is Active-Low 1 = GPIO Interrupt input is Active-High	RWS	Yes	0
8	**VS GPIO_PG 8 PEX_PORT_GOOD*x*# Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High for the PEX_PORT_GOOD*x*# signal. 0 = GPIO Interrupt input is Active-Low 1 = GPIO Interrupt input is Active-High	RWS	Yes	0
9	**VS GPIO_PG 9 PEX_PORT_GOOD*x*# Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High for the PEX_PORT_GOOD*x*# signal. 0 = GPIO Interrupt input is Active-Low 1 = GPIO Interrupt input is Active-High	RWS	Yes	0
10	**VS GPIO_PG 10 PEX_PORT_GOOD*x*# Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High for the PEX_PORT_GOOD*x*# signal. 0 = GPIO Interrupt input is Active-Low 1 = GPIO Interrupt input is Active-High	RWS	Yes	0
11	**VS GPIO_PG 11 PEX_PORT_GOOD*x*# Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High for the PEX_PORT_GOOD*x*# signal. 0 = GPIO Interrupt input is Active-Low 1 = GPIO Interrupt input is Active-High	RWS	Yes	0
31:12	***Reserved***	RsvdP	No	0000_0h

Register 13-191. A50h Virtual Switch GPIO_PG 0_11 Interrupt Status (Virtual Switch mode – VS Upstream Port(s))

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
This register provides virtualized copies of the **GPIO 0_11 Interrupt Status** register (Port 0, accessible through the Management Port, offset 634h), to support the virtual switches. The main difference is that the virtual switches have no knowledge of which PEX_PORT_GOOD*x*# (PEX_PORT_GOOD[23:16, 3:0]#) signal is being used. Interrupt status remains Set, as long the corresponding PEX_PORT_GOOD*x*# signal is asserted, and Clears on its own when the corresponding PEX_PORT_GOOD*x*# input de-asserts to the inactive state. The active state of each interrupt is controlled by its respective **Virtual Switch GPIO_PG 0_11 Interrupt Polarity** register bit (VS Upstream Port(s), offset A4Ch). A single GPIO ball/signal cannot be assigned to more than one virtual switch. ***Note:*** *The bits in this register can be masked by their respective **Virtual Switch GPIO_PG 0_11 Interrupt Mask** register bits (VS Upstream Port(s), offset A54h).*				
0	**VS GPIO_PG 0 PEX_PORT_GOOD*x*# Interrupt Status** Indicates whether GPIO interrupts are inactive or active for the PEX_PORT_GOOD*x*# signal. 0 = GPIO interrupt is inactive 1 = GPIO interrupt is active	RO	No	0
1	**VS GPIO_PG 1 PEX_PORT_GOOD*x*# Interrupt Status** Indicates whether GPIO interrupts are inactive or active for the PEX_PORT_GOOD*x*# signal. 0 = GPIO Interrupt input is inactive 1 = GPIO Interrupt input is active	RO	No	0
2	**VS GPIO_PG 2 PEX_PORT_GOOD*x*# Interrupt Status** Indicates whether GPIO interrupts are inactive or active for the PEX_PORT_GOOD*x*# signal. 0 = GPIO Interrupt input is inactive 1 = GPIO Interrupt input is active	RO	No	0
3	**VS GPIO_PG 3 PEX_PORT_GOOD*x*# Interrupt Status** Indicates whether GPIO interrupts are inactive or active for the PEX_PORT_GOOD*x*# signal. 0 = GPIO Interrupt input is inactive 1 = GPIO Interrupt input is active	RO	No	0

Register 13-191. A50h Virtual Switch GPIO_PG 0_11 Interrupt Status (Virtual Switch mode – VS Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4	**VS GPIO_PG 4 PEX_PORT_GOOD*x*# Interrupt Status** Indicates whether GPIO interrupts are inactive or active for the PEX_PORT_GOOD*x*# signal. 0 = GPIO Interrupt input is inactive 1 = GPIO Interrupt input is active	RO	No	0
5	**VS GPIO_PG 5 PEX_PORT_GOOD*x*# Interrupt Status** Indicates whether GPIO interrupts are inactive or active for the PEX_PORT_GOOD*x*# signal. 0 = GPIO Interrupt input is inactive 1 = GPIO Interrupt input is active	RO	No	0
6	**VS GPIO_PG 6 PEX_PORT_GOOD*x*# Interrupt Status** Indicates whether GPIO interrupts are inactive or active for the PEX_PORT_GOOD*x*# signal. 0 = GPIO Interrupt input is inactive 1 = GPIO Interrupt input is active	RO	No	0
7	**VS GPIO_PG 7 PEX_PORT_GOOD*x*# Interrupt Status** Indicates whether GPIO interrupts are inactive or active for the PEX_PORT_GOOD*x*# signal. 0 = GPIO Interrupt input is inactive 1 = GPIO Interrupt input is active	RO	No	0
8	**VS GPIO_PG 8 PEX_PORT_GOOD*x*# Interrupt Status** Indicates whether GPIO interrupts are inactive or active for the PEX_PORT_GOOD*x*# signal. 0 = GPIO Interrupt input is inactive 1 = GPIO Interrupt input is active	RO	No	0
9	**VS GPIO_PG 9 PEX_PORT_GOOD*x*# Interrupt Status** Indicates whether GPIO interrupts are inactive or active for the PEX_PORT_GOOD*x*# signal. 0 = GPIO Interrupt input is inactive 1 = GPIO Interrupt input is active	RO	No	0
10	**VS GPIO_PG 10 PEX_PORT_GOOD*x*# Interrupt Status** Indicates whether GPIO interrupts are inactive or active for the PEX_PORT_GOOD*x*# signal. 0 = GPIO Interrupt input is inactive 1 = GPIO Interrupt input is active	RO	No	0
11	**VS GPIO_PG 11 PEX_PORT_GOOD*x*# Interrupt Status** Indicates whether GPIO interrupts are inactive or active for the PEX_PORT_GOOD*x*# signal. 0 = GPIO Interrupt input is inactive 1 = GPIO Interrupt input is active	RO	No	0
31:12	***Reserved***	RsvdP	No	0000_0h

Register 13-192. A54h Virtual Switch GPIO_PG 0_11 Interrupt Mask (Virtual Switch mode – VS Upstream Port(s))

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register provides virtualized copies of the **GPIO 0_11 Interrupt Mask** register (Port 0, accessible through the Management Port, offset 63Ch), to support the virtual switches. The main difference is that the virtual switches have no knowledge of which PEX_PORT_GOOD*x*# (PEX_PORT_GOOD[23:16, 3:0]#) signal is being used. A single GPIO ball/signal cannot be assigned to more than one virtual switch. ***Note:*** *The bits in this register can be used to mask their respective* ***Virtual Switch GPIO_PG 0_11 Interrupt Status*** *register bits (VS Upstream Port(s), offset A50h).*				
0	**VS GPIO_PG 0 PEX_PORT_GOOD*x*# Interrupt Mask** Indicates whether GPIO interrupts are not masked or masked for the PEX_PORT_GOOD*x*# signal. 0 = GPIO interrupt is not masked. 1 = GPIO interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
1	**VS GPIO_PG 1 PEX_PORT_GOOD*x*# Interrupt Mask** Indicates whether GPIO interrupts are not masked or masked for the PEX_PORT_GOOD*x*# signal. 0 = GPIO interrupt is not masked. 1 = GPIO interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
2	**VS GPIO_PG 2 PEX_PORT_GOOD*x*# Interrupt Mask** Indicates whether GPIO interrupts are not masked or masked for the PEX_PORT_GOOD*x*# signal. 0 = GPIO interrupt is not masked. 1 = GPIO interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
3	**VS GPIO_PG 3 PEX_PORT_GOOD*x*# Interrupt Mask** Indicates whether GPIO interrupts are not masked or masked for the PEX_PORT_GOOD*x*# signal. 0 = GPIO interrupt is not masked. 1 = GPIO interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1

Register 13-192. A54h Virtual Switch GPIO_PG 0_11 Interrupt Mask (Virtual Switch mode – VS Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
4	**VS GPIO_PG 4 PEX_PORT_GOOD*x*# Interrupt Mask** Indicates whether GPIO interrupts are not masked or masked for the PEX_PORT_GOOD*x*# signal. 0 = GPIO interrupt is not masked. 1 = GPIO interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
5	**VS GPIO_PG 5 PEX_PORT_GOOD*x*# Interrupt Mask** Indicates whether GPIO interrupts are not masked or masked for the PEX_PORT_GOOD*x*# signal. 0 = GPIO interrupt is not masked. 1 = GPIO interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
6	**VS GPIO_PG 6 PEX_PORT_GOOD*x*# Interrupt Mask** Indicates whether GPIO interrupts are not masked or masked for the PEX_PORT_GOOD*x*# signal. 0 = GPIO interrupt is not masked. 1 = GPIO interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
7	**VS GPIO_PG 7 PEX_PORT_GOOD*x*# Interrupt Mask** Indicates whether GPIO interrupts are not masked or masked for the PEX_PORT_GOOD*x*# signal. 0 = GPIO interrupt is not masked. 1 = GPIO interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1

Register 13-192. A54h Virtual Switch GPIO_PG 0_11 Interrupt Mask (Virtual Switch mode – VS Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
8	**VS GPIO_PG 8 PEX_PORT_GOOD*x*# Interrupt Mask** Indicates whether GPIO interrupts are not masked or masked for the PEX_PORT_GOOD*x*# signal. 0 = GPIO interrupt is not masked. 1 = GPIO interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
9	**VS GPIO_PG 9 PEX_PORT_GOOD*x*# Interrupt Mask** Indicates whether GPIO interrupts are not masked or masked for the PEX_PORT_GOOD*x*# signal. 0 = GPIO interrupt is not masked. 1 = GPIO interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
10	**VS GPIO_PG 10 PEX_PORT_GOOD*x*# Interrupt Mask** Indicates whether GPIO interrupts are not masked or masked for the PEX_PORT_GOOD*x*# signal. 0 = GPIO interrupt is not masked. 1 = GPIO interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
11	**VS GPIO_PG 11 PEX_PORT_GOOD*x*# Interrupt Mask** Indicates whether GPIO interrupts are not masked or masked for the PEX_PORT_GOOD*x*# signal. 0 = GPIO interrupt is not masked. 1 = GPIO interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
31:12	***Reserved***	RsvdP	No	0000_0h

Register 13-193. A58h Virtual Switch GPIO_SHP 0_7 Direction Control (Virtual Switch mode – VS Upstream Port(s))

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
This register provides virtualized copies of the **GPIO 24_31 Direction Control** register (Port 0, accessible through the Management Port, offset 60Ch), to support the virtual switches. The main difference is that the virtual switches have no knowledge of which GPIO*x* (GPIO[31:24]) signal is being used. A maximum of eight GPIO_SHP signals can be assigned to any virtual switch. A single GPIO_SHP signal cannot be assigned to more than one virtual switch. ***Note:*** *Register offsets A64h and A68h, referenced in this register, are located in the VS Upstream Port(s).*				
1:0	**VS GPIO_SHP 0 GPIO*x* Source/Destination** **As Input:** 00b = To **VS GPIO_SHP 0 GPIOx Input Data** register (offset A64h[0]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **VS GPIO_SHP 0 GPIOx Output Data** register (offset A68h[0]) 10b = Serial Hot Plug PERST# output 01b, 11b = ***Reserved***	RWS	Yes	00b
2	**VS GPIO_SHP 0 GPIO*x* Direction Control** 0 = Input 1 = Output	RWS	Yes	0
4:3	**VS GPIO_SHP 1 GPIO*x* Source/Destination** **As Input:** 00b = To **VS GPIO_SHP 1 GPIOx Input Data** register (offset A64h[1]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **VS GPIO_SHP 1 GPIOx Output Data** register (offset A68h[1]) 10b = Serial Hot Plug PERST# output 01b, 11b = ***Reserved***	RWS	Yes	00b
5	**VS GPIO_SHP 1 GPIO*x* Direction Control** 0 = Input 1 = Output	RWS	Yes	0

Register 13-193. A58h Virtual Switch GPIO_SHP 0_7 Direction Control (Virtual Switch mode – VS Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
7:6	**VS GPIO_SHP 2 GPIO*x* Source/Destination** **As Input:** 00b = To **VS GPIO_SHP 1 GPIOx Input Data** register (offset A64h[2]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **VS GPIO_SHP 1 GPIOx Output Data** register (offset A68h[2]) 10b = Serial Hot Plug PERST# output 01b, 11b = ***Reserved***	RWS	Yes	00b
8	**VS GPIO_SHP 2 GPIO*x* Direction Control** 0 = Input 1 = Output	RWS	Yes	0
10:9	**VS GPIO_SHP 3 GPIO*x* Source/Destination** **As Input:** 00b = To **VS GPIO_SHP 3 GPIOx Input Data** register (offset A64h[3]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **VS GPIO_SHP 3 GPIOx Output Data** register (offset A68h[3]) 10b = Serial Hot Plug PERST# output 01b, 11b = ***Reserved***	RWS	Yes	00b
11	**VS GPIO_SHP 3 GPIO*x* Direction Control** 0 = Input 1 = Output	RWS	Yes	0

Register 13-193. A58h Virtual Switch GPIO_SHP 0_7 Direction Control (Virtual Switch mode – VS Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
13:12	**VS GPIO_SHP 4 GPIO*x* Source/Destination** **As Input:** 00b = To **VS GPIO_SHP 4 GPIOx Input Data** register (offset A64h[4]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **VS GPIO_SHP 4 GPIOx Output Data** register (offset A68h[4]) 10b = Serial Hot Plug PERST# output 01b, 11b = ***Reserved***	RWS	Yes	00b
14	**VS GPIO_SHP 4 GPIO*x* Direction Control** 0 = Input 1 = Output	RWS	Yes	0
16:15	**VS GPIO_SHP 5 GPIO*x* Source/Destination** **As Input:** 00b = To **VS GPIO_SHP 5 GPIOx Input Data** register (offset A64h[5]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **VS GPIO_SHP 5 GPIOx Output Data** register (offset A68h[5]) 10b = Serial Hot Plug PERST# output 01b, 11b = ***Reserved***	RWS	Yes	00b
17	**VS GPIO_SHP 5 GPIO*x* Direction Control** 0 = Input 1 = Output	RWS	Yes	0

Register 13-193. A58h Virtual Switch GPIO_SHP 0_7 Direction Control (Virtual Switch mode – VS Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
19:18	**VS GPIO_SHP 6 GPIO*x* Source/Destination** **As Input:** 00b = To **VS GPIO_SHP 6 GPIOx Input Data** register (offset A64h[6]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **VS GPIO_SHP 6 GPIOx Output Data** register (offset A68h[6]) 10b = Serial Hot Plug PERST# output 01b, 11b = ***Reserved***	RWS	Yes	00b
20	**VS GPIO_SHP 6 Direction Control** 0 = Input 1 = Output	RWS	Yes	0
22:21	**VS GPIO_SHP 7 Source/Destination** **As Input:** 00b = To **VS GPIO_SHP 7 GPIOx Input Data** register (offset A64h[7]) 01b = General interrupt (INT*x*, MSI, or PEX_INTA# and/or VS*x*_PEX_INTA#) 10b, 11b = ***Reserved*** **As Output:** 00b = From **VS GPIO_SHP 7 GPIOx Output Data** register (offset A68h[7]) 10b = Serial Hot Plug PERST# output 01b, 11b = ***Reserved***	RWS	Yes	00b
23	**VS GPIO_SHP 7 Direction Control** 0 = Input 1 = Output	RWS	Yes	0
31:24	***Reserved***	RsvdP	No	00h

Register 13-194. A5Ch Virtual Switch GPIO_SHP 0_7 Availability (Virtual Switch mode – VS Upstream Port(s))

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
3:0	**Number of GPIO_SHPs Available** Indicates the number of GPIO_SHP GPIO*x* signals assigned to each virtual switch. The value corresponds to the number of bits programmed to 1 in the **VS*x* GPIO_SHP 0_7 Assignment** register(s) (Port 0, accessible through the Management Port, offsets 670h through 67Ch). A maximum of eight GPIO_SHP signals can be assigned to any virtual switch. A single GPIO_SHP signal cannot be assigned to more than one virtual switch. 0h = 1 (GPIO_SHP 0) 1h = 2 (GPIO_SHP 0_1) 2h = 3 (GPIO_SHP 0_2) 3h = 4 (GPIO_SHP 0_3) 4h = 5 (GPIO_SHP 0_4) 5h = 6 (GPIO_SHP 0_5) 6h = 7 (GPIO_SHP 0_6) 7h = 8 (GPIO_SHP 0_7) All other encodings are ***reserved***.	RWS	Yes	0h
31:4	***Reserved***	RsvdP	No	0000_000h

Register 13-195. A60h Virtual Switch GPIO_SHP 0_7 Input De-Bounce (Virtual Switch mode – VS Upstream Port(s))

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
This register provides virtualized copies of the **GPIO 24_31 Input De-Bounce** register (Port 0, accessible through the Management Port, offset 618h), to support the virtual switches. The main difference is that the virtual switches have no knowledge of which GPIO*x* (GPIO[31:24]) signal is being used. A maximum of eight GPIO_SHP signals can be assigned to any virtual switch. A single GPIO_SHP signal cannot be assigned to more than one virtual switch. ***Note:*** *Register offset A58h, referenced in this register, is located in the VS Upstream Port(s).*				
0	**VS GPIO_SHP 0 GPIO*x* Input De-Bounce Control** Controls de-bounce when GPIO*x* is configured as an input (offset A58h[2], is Cleared). 0 = GPIO*x* input is not de-bounced 1 = GPIO*x* input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
1	**VS GPIO_SHP 1 GPIO*x* Input De-Bounce Control** Controls de-bounce when GPIO*x* is configured as an input (offset A58h[5], is Cleared). 0 = GPIO*x* input is not de-bounced 1 = GPIO*x* input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
2	**VS GPIO_SHP 2 GPIO*x* Input De-Bounce Control** Controls de-bounce when GPIO*x* is configured as an input (offset A58h[8], is Cleared). 0 = GPIO*x* input is not de-bounced 1 = GPIO*x* input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
3	**VS GPIO_SHP 3 GPIO*x* Input De-Bounce Control** Controls de-bounce when GPIO*x* is configured as an input (offset A58h[11], is Cleared). 0 = GPIO*x* input is not de-bounced 1 = GPIO*x* input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0

Register 13-195. A60h Virtual Switch GPIO_SHP 0_7 Input De-Bounce (Virtual Switch mode – VS Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4	**VS GPIO_SHP 4 GPIO*x* Input De-Bounce Control** Controls de-bounce when GPIO*x* is configured as an input (offset A58h[14], is Cleared). 0 = GPIO*x* input is not de-bounced 1 = GPIO*x* input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
5	**VS GPIO_SHP 5 GPIO*x* Input De-Bounce Control** Controls de-bounce when GPIO*x* is configured as an input (offset A58h[17], is Cleared). 0 = GPIO*x* input is not de-bounced 1 = GPIO*x* input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
6	**VS GPIO_SHP 6 GPIO*x* Input De-Bounce Control** Controls de-bounce when GPIO*x* is configured as an input (offset A58h[20], is Cleared). 0 = GPIO*x* input is not de-bounced 1 = GPIO*x* input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
7	**VS GPIO_SHP 7 GPIO*x* Input De-Bounce Control** Controls de-bounce when GPIO*x* is configured as an input (offset A58h[23], is Cleared). 0 = GPIO*x* input is not de-bounced 1 = GPIO*x* input is de-bounced; de-bounce time is approximately 1.3 ms	RWS	Yes	0
31:8	***Reserved***	RsvdP	No	0000_00h

Register 13-196. A64h Virtual Switch GPIO_SHP 0_7 Input Data (Virtual Switch mode – VS Upstream Port(s))

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register provides virtualized copies of the **GPIO 24_31 Input Data** register (Port 0, accessible through the Management Port, offset 620h), to support the virtual switches. The main difference is that the virtual switches have no knowledge of which GPIO*x* (GPIO[31:24]) signal is being used. A maximum of eight GPIO_SHP signals can be assigned to any virtual switch. A single GPIO_SHP signal cannot be assigned to more than one virtual switch. ***Note:*** *Register offset A58h, referenced in this register, is located in the VS Upstream Port(s).*				
0	**VS GPIO_SHP 0 GPIO*x* Input Data** If GPIO*x* is configured as an output (offset A58h[2], is Set), Reads return 0. If GPIO*x* is configured as an input (offset A58h[2], is Cleared), Reads return the logic value of the voltage on GPIO*x*.	RO	No	0
1	**VS GPIO_SHP 1 GPIO*x* Input Data** If GPIO*x* is configured as an output (offset A58h[5], is Set), Reads return 0. If GPIO*x* is configured as an input (offset A58h[5], is Cleared), Reads return the logic value of the voltage on GPIO*x*.	RO	No	0
2	**VS GPIO_SHP 2 GPIO*x* Input Data** If GPIO*x* is configured as an output (offset A58h[8], is Set), Reads return 0. If GPIO*x* is configured as an input (offset A58h[8], is Cleared), Reads return the logic value of the voltage on GPIO*x*.	RO	No	0
3	**VS GPIO_SHP 3 GPIO*x* Input Data** If GPIO*x* is configured as an output (offset A58h[11], is Set), Reads return 0. If GPIO*x* is configured as an input (offset A58h[11], is Cleared), Reads return the logic value of the voltage on GPIO*x*.	RO	No	0

Register 13-196. A64h Virtual Switch GPIO_SHP 0_7 Input Data (Virtual Switch mode – VS Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
4	**VS GPIO_SHP 4 GPIO*x* Input Data** If GPIO*x* is configured as an output (offset A58h[14], is Set), Reads return 0. If GPIO*x* is configured as an input (offset A58h[14], is Cleared), Reads return the logic value of the voltage on GPIO*x*.	RO	No	0
5	**VS GPIO_SHP 5 GPIO*x* Input Data** If GPIO*x* is configured as an output (offset A58h[17], is Set), Reads return 0. If GPIO*x* is configured as an input (offset A58h[17], is Cleared), Reads return the logic value of the voltage on GPIO*x*.	RO	No	0
6	**VS GPIO_SHP 6 GPIO*x* Input Data** If GPIO*x* is configured as an output (offset A58h[20], is Set), Reads return 0. If GPIO*x* is configured as an input (offset A58h[20], is Cleared), Reads return the logic value of the voltage on GPIO*x*.	RO	No	0
7	**VS GPIO_SHP 7 GPIO*x* Input Data** If GPIO*x* is configured as an output (offset A58h[23], is Set), Reads return 0. If GPIO*x* is configured as an input (offset A58h[23], is Cleared), Reads return the logic value of the voltage on GPIO*x*.	RO	No	0
31:8	***Reserved***	RsvdP	No	0000_00h

Register 13-197. A68h Virtual Switch GPIO_SHP 0_7 Output Data (Virtual Switch mode – VS Upstream Port(s))

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
This register provides virtualized copies of the **GPIO 24_31 Output Data** register (Port 0, accessible through the Management Port, offset 628h), to support the virtual switches. The main difference is that the virtual switches have no knowledge of which GPIO*x* (GPIO[31:24]) signal is being used. A maximum of eight GPIO_SHP signals can be assigned to any virtual switch. A single GPIO_SHP signal cannot be assigned to more than one virtual switch. ***Note:*** *Register offset A58h, referenced in this register, is located in the VS Upstream Port(s).*				
0	**VS GPIO_SHP 0 GPIO*x* Output Data** If GPIO*x* is configured as an output (offset A58h[2], is Set), the value written to this bit is immediately driven to the GPIO*x* output.	RWS	Yes	0
1	**VS GPIO_SHP 1 GPIO*x* Output Data** If GPIO*x* is configured as an output (offset A58h[5], is Set), the value written to this bit is immediately driven to the GPIO*x* output.	RWS	Yes	0
2	**VS GPIO_SHP 2 GPIO*x* Output Data** If GPIO*x* is configured as an output (offset A58h[8], is Set), the value written to this bit is immediately driven to the GPIO*x* output.	RWS	Yes	0
3	**VS GPIO_SHP 3 GPIO*x* Output Data** If GPIO*x* is configured as an output (offset A58h[11], is Set), the value written to this bit is immediately driven to the GPIO*x* output.	RWS	Yes	0
4	**VS GPIO_SHP 4 GPIO*x* Output Data** If GPIO*x* is configured as an output (offset A58h[14], is Set), the value written to this bit is immediately driven to the GPIO*x* output.	RWS	Yes	0
5	**VS GPIO_SHP 5 GPIO*x* Output Data** If GPIO*x* is configured as an output (offset A58h[17], is Set), the value written to this bit is immediately driven to the GPIO*x* output.	RWS	Yes	0
6	**VS GPIO_SHP 6 GPIO*x* Output Data** If GPIO*x* is configured as an output (offset A58h[20], is Set), the value written to this bit is immediately driven to the GPIO*x* output.	RWS	Yes	0
7	**VS GPIO_SHP 7 GPIO*x* Output Data** If GPIO*x* is configured as an output (offset A58h[23], is Set), the value written to this bit is immediately driven to the GPIO*x* output.	RWS	Yes	0
31:8	***Reserved***	RsvdP	No	0000_00h

Register 13-198. A6Ch Virtual Switch GPIO_SHP 0_7 Interrupt Polarity (Virtual Switch mode – VS Upstream Port(s))

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register provides virtualized copies of the **GPIO 24_31 Interrupt Polarity** register (Port 0, accessible through the Management Port, offset 630h), to support the virtual switches. The main difference is that the virtual switches have no knowledge of which GPIO*x* (GPIO[31:24]) signal is being used. A maximum of eight GPIO_SHP signals can be assigned to any virtual switch. A single GPIO_SHP signal cannot be assigned to more than one virtual switch.				
0	**VS GPIO_SHP 0 GPIO*x* Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High for the GPIO*x* signal. 0 = GPIO Interrupt input is Active-Low 1 = GPIO Interrupt input is Active-High	RWS	Yes	0
1	**VS GPIO_SHP 1 GPIO*x* Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High for the GPIO*x* signal. 0 = GPIO Interrupt input is Active-Low 1 = GPIO Interrupt input is Active-High	RWS	Yes	0
2	**VS GPIO_SHP 2 GPIO*x* Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High for the GPIO*x* signal. 0 = GPIO Interrupt input is Active-Low 1 = GPIO Interrupt input is Active-High	RWS	Yes	0
3	**VS GPIO_SHP 3 GPIO*x* Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High for the GPIO*x* signal. 0 = GPIO Interrupt input is Active-Low 1 = GPIO Interrupt input is Active-High	RWS	Yes	0

Register 13-198. A6Ch Virtual Switch GPIO_SHP 0_7 Interrupt Polarity (Virtual Switch mode – VS Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4	**VS GPIO_SHP 4 GPIO*x* Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High for the GPIO*x* signal. 0 = GPIO Interrupt input is Active-Low 1 = GPIO Interrupt input is Active-High	RWS	Yes	0
5	**VS GPIO_SHP 5 GPIO*x* Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High for the GPIO*x* signal. 0 = GPIO Interrupt input is Active-Low 1 = GPIO Interrupt input is Active-High	RWS	Yes	0
6	**VS GPIO_SHP 6 GPIO*x* Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High for the GPIO*x* signal. 0 = GPIO Interrupt input is Active-Low 1 = GPIO Interrupt input is Active-High	RWS	Yes	0
7	**VS GPIO_SHP 7 GPIO*x* Interrupt Polarity** Controls whether GPIO Interrupt input is Active-Low or Active-High for the GPIO*x* signal. 0 = GPIO Interrupt input is Active-Low 1 = GPIO Interrupt input is Active-High	RWS	Yes	0
31:8	***Reserved***	RsvdP	No	0000_00h

Register 13-199. A70h Virtual Switch GPIO_SHP 0_7 Interrupt Status (Virtual Switch mode – VS Upstream Port(s))

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
This register provides virtualized copies of the **GPIO 24_31 Interrupt Status** register (Port 0, accessible through the Management Port, offset 638h), to support the virtual switches. The main difference is that the virtual switches have no knowledge of which GPIO*x* (GPIO[31:24]) signal is being used. Interrupt status remains Set, as long the corresponding GPIO*x* signal is asserted, and Clears on its own when the corresponding GPIO*x* input de-asserts to the inactive state. The active state of each interrupt is controlled by its respective **Virtual Switch GPIO_SHP 0_7 Interrupt Polarity** register bit (VS Upstream Port(s), offset A6Ch). A maximum of eight GPIO_SHP signals can be assigned to any virtual switch. A single GPIO_SHP signal cannot be assigned to more than one virtual switch. ***Note:*** *The bits in this register can be masked by their respective* ***Virtual Switch GPIO_SHP 0_7 Interrupt Mask*** *register bits (VS Upstream Port(s), offset A74h).*				
0	**VS GPIO_SHP 0 GPIO*x* Interrupt Status** Indicates whether GPIO interrupts are inactive or active for the GPIO*x* signal. 0 = GPIO Interrupt input is inactive 1 = GPIO Interrupt input is active	RO	No	0
1	**VS GPIO_SHP 1 GPIO*x* Interrupt Status** Indicates whether GPIO interrupts are inactive or active for the GPIO*x* signal. 0 = GPIO Interrupt input is inactive 1 = GPIO Interrupt input is active	RO	No	0
2	**VS GPIO_SHP 2 GPIO*x* Interrupt Status** Indicates whether GPIO interrupts are inactive or active for the GPIO*x* signal. 0 = GPIO Interrupt input is inactive 1 = GPIO Interrupt input is active	RO	No	0
3	**VS GPIO_SHP 3 GPIO*x* Interrupt Status** Indicates whether GPIO interrupts are inactive or active for the GPIO*x* signal. 0 = GPIO Interrupt input is inactive 1 = GPIO Interrupt input is active	RO	No	0

Register 13-199. A70h Virtual Switch GPIO_SHP 0_7 Interrupt Status (Virtual Switch mode – VS Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4	**VS GPIO_SHP 4 GPIO*x* Interrupt Status** Indicates whether GPIO interrupts are inactive or active for the GPIO*x* signal. 0 = GPIO Interrupt input is inactive 1 = GPIO Interrupt input is active	RO	No	0
5	**VS GPIO_SHP 5 GPIO*x* Interrupt Status** Indicates whether GPIO interrupts are inactive or active for the GPIO*x* signal. 0 = GPIO Interrupt input is inactive 1 = GPIO Interrupt input is active	RO	No	0
6	**VS GPIO_SHP 6 GPIO*x* Interrupt Status** Indicates whether GPIO interrupts are inactive or active for the GPIO*x* signal. 0 = GPIO Interrupt input is inactive 1 = GPIO Interrupt input is active	RO	No	0
7	**VS GPIO_SHP 7 GPIO*x* Interrupt Status** Indicates whether GPIO interrupts are inactive or active for the GPIO*x* signal. 0 = GPIO Interrupt input is inactive 1 = GPIO Interrupt input is active	RO	No	0
31:8	***Reserved***	RsvdP	No	0000_00h

Register 13-200. A74h Virtual Switch GPIO_SHP 0_7 Interrupt Mask (Virtual Switch mode – VS Upstream Port(s))

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register provides virtualized copies of the **GPIO 24_31 Interrupt Mask** register (Port 0, accessible through the Management Port, offset 640h), to support the virtual switches. The main difference is that the virtual switches have no knowledge of which GPIO*x* (GPIO[31:24]) signal is being used. A maximum of eight GPIO_SHP signals can be assigned to any virtual switch. A single GPIO_SHP signal cannot be assigned to more than one virtual switch. ***Note:*** *The bits in this register can be used to mask their respective* ***Virtual Switch GPIO_SHP 0_7 Interrupt Status*** *register bits (VS Upstream Port(s), offset A70h).*				
0	**VS GPIO_SHP 0 GPIO*x* Interrupt Mask** Indicates whether GPIO interrupts are not masked or masked for the GPIO*x* signal. 0 = GPIO interrupt is not masked. 1 = GPIO interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
1	**VS GPIO_SHP 1 GPIO*x* Interrupt Mask** Indicates whether GPIO interrupts are not masked or masked for the GPIO*x* signal. 0 = GPIO interrupt is not masked. 1 = GPIO interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
2	**VS GPIO_SHP 2 GPIO*x* Interrupt Mask** Indicates whether GPIO interrupts are not masked or masked for the GPIO*x* signal. 0 = GPIO interrupt is not masked. 1 = GPIO interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
3	**VS GPIO_SHP 3 GPIO*x* Interrupt Mask** Indicates whether GPIO interrupts are not masked or masked for the GPIO*x* signal. 0 = GPIO interrupt is not masked. 1 = GPIO interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1

Register 13-200. A74h Virtual Switch GPIO_SHP 0_7 Interrupt Mask (Virtual Switch mode – VS Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4	**VS GPIO_SHP 4 GPIO*x* Interrupt Mask** Indicates whether GPIO interrupts are not masked or masked for the GPIO*x* signal. 0 = GPIO interrupt is not masked. 1 = GPIO interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
5	**VS GPIO_SHP 5 GPIO*x* Interrupt Mask** Indicates whether GPIO interrupts are not masked or masked for the GPIO*x* signal. 0 = GPIO interrupt is not masked. 1 = GPIO interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
6	**VS GPIO_SHP 6 GPIO*x* Interrupt Mask** Indicates whether GPIO interrupts are not masked or masked for the GPIO*x* signal. 0 = GPIO interrupt is not masked. 1 = GPIO interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
7	**VS GPIO_SHP 7 GPIO*x* Interrupt Mask** Indicates whether GPIO interrupts are not masked or masked for the GPIO*x* signal. 0 = GPIO interrupt is not masked. 1 = GPIO interrupt is masked. When an interrupt is masked, the corresponding **Interrupt Status** register is not updated.	RWS	Yes	1
31:8	***Reserved***	RsvdP	No	0000_00h

13.15.16 Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets B70h – B7Ch)

This section details the Device-Specific Vendor-Specific Extended Capability 2 registers. Table 13-35 defines the register map.

Table 13-35. Device-Specific, Vendor-Specific Extended Capability 2 Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Next Capability Offset 2 (000h)	Capability Version 2 (1h)	PCI Express Extended Capability ID 2 (000Bh)		B70h
Vendor-Specific Header 2				B74h
Hardwired Device ID		Hardwired Vendor ID		B78h
Reserved			Hardwired Revision ID	B7Ch

Register 13-201. B70h Vendor-Specific Extended Capability 2 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
15:0	**PCI Express Extended Capability ID 2** Program to 000Bh, to indicate that the Capability structure is the **Vendor-Specific Extended Capability** structure.	RO	Yes	000Bh
19:16	**Capability Version 2**	RO	Yes	1h
31:20	**Next Capability Offset 2** 000h = This extended capability is the last extended capability in the PEX 8649 Extended Capabilities list	RO	Yes	000h

Register 13-202. B74h Vendor-Specific Header 2 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
15:0	**Vendor-Specific ID 2** ID Number of this **Vendor-Specific Extended Capability** (**VSEC**) structure.	RO	Yes	0001h
19:16	**Vendor-Specific Rev 2** Version Number of this **VSEC** structure.	RO	Yes	0h
31:20	**Vendor-Specific Rev 2** Number of bytes in the entire **VSEC** structure.	RO	Yes	010h

Register 13-203. B78h PLX Hardwired Configuration ID (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**Hardwired Vendor ID** Always returns the PLX PCI-SIG-assigned Vendor ID value, 10B5h.	RO	No	10B5h
31:16	**Hardwired Device ID** Always returns the PEX 8649 default Device ID value, 8649h.	RO	No	8649h

Register 13-204. B7Ch PLX Hardwired Revision ID (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
7:0	**Hardwired Revision ID** Always returns the PEX 8649 default Revision ID value – AAh.	RO	No	Current Rev # (AAh)
31:8	***Reserved***	RsvdP	No	0000_00h

13.15.17 Device-Specific Registers – Physical Layer (Offsets B80h – BC8h)

This section details the Device-Specific Physical Layer (PHY) registers located at offsets B80h through BC8h. Table 13-36 defines the register map.

Table 13-7 defines the relationship between the registers' Port 0, 16, or 20 parameters and SerDes modules and Lanes, when all Ports are enabled.

Other Device-Specific PHY registers are detailed in Section 13.15.3, "Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)."

Table 13-36. Device-Specific PHY Register Map (Offsets B80h – BC8h) (Ports[a])

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
SerDes Control	B80h
Synchronous Advertised N_FTS	B84h
Asynchronous Advertised N_FTS	B88h
SerDes Drive Level 0	B8Ch
SerDes Drive Level 1	B90h
SerDes Drive Level 2	B94h
Post-Cursor Emphasis Level 0	B98h
Post-Cursor Emphasis Level 1	B9Ch
Post-Cursor Emphasis Level 2	BA0h
Receiver Equalization Level 0	BA4h
Receiver Equalization Level 1	BA8h
Signal Detect Level	BACh
Factory Test Only	BB0h – BC8h

[a] *Certain registers are Port-specific, others are Station-specific; all are Device-specific.*

Register 13-205. B80h SerDes Control (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
This register controls SerDes logic parameters.				
2:0	**Receiver Detect Time Select** Selects the Receiver Detect timing. 000b = 1.0 µs 001b = 2.0 µs 010b = 4.0 µs (default) 011b = 5.0 µs 100b = 10.0 µs 101b = 20.0 µs 110b = 40.0 µs 111b = 50.0 µs	RWS	Yes	010b
3	***Reserved***	RsvdP	No	0
7:4	**Transmit Latency** Specifies the Data Transmit latency through the SerDes (in clocks; 4-ns clock period).	RWS	Yes	9h
8	**Force SerDes Out** Transmit Data (TD) [19:0] Force enable. 1 = All bits of the TD[19:0] inputs, of the SerDes in this Station, are forced to the state specified by bit 9 ***(****SerDes Out Data Force State*)	RWS	Yes	0
9	**SerDes Out Data Force State** TD[19:0] Force state. Specifies the state to which the TD[19:0] inputs are forced, when bit 8 ***(****Force SerDes Out*) is Set.	RWS	Yes	0
31:10	***Reserved***	RsvdP	No	0-0h

Register 13-206. B84h Synchronous Advertised N_FTS (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
This register advertises the Number of Fast Training Sets (N_FTS) values for synchronous clocking. **Note:** *The Port 0 fields are for Ports 0, 1, 2, and 3. The Port 16 fields are for Ports 16, 17, 18, and 19. The Port 20 fields are for Ports 20, 21, 22, and 23.*					
7:0	**Port *x* Synchronous Tx N_FTS** When clocking is synchronous, specifies the *N_FTS* field value in Training Sets transmitted by the corresponding PEX 8649 Port, when the Port's **Link Control** register *Common Clock Configuration* bit (offset 78h[6]) is Set.	0, 16, or 20	RWS	Yes	80h
15:8		1, 17, or 21	RWS	Yes	80h
23:16		2, 18, or 22	RWS	Yes	80h
31:24		3, 19, or 23	RWS	Yes	80h

Register 13-207. B88h Asynchronous Advertised N_FTS (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
This register advertises the N_FTS values for asynchronous clocking. **Note:** *The Port 0 fields are for Ports 0, 1, 2, and 3. The Port 16 fields are for Ports 16, 17, 18, and 19. The Port 20 fields are for Ports 20, 21, 22, and 23.*					
7:0	**Port *x* Asynchronous Tx N_FTS** When clocking is asynchronous, specifies the *N_FTS* field value in Training Sets transmitted by the corresponding PEX 8649 Port, when the Port's **Link Control** register *Common Clock Configuration* bit (offset 78h[6]) is Cleared.	0, 16, or 20	RWS	Yes	80h
15:8		1, 17, or 21	RWS	Yes	80h
23:16		2, 18, or 22	RWS	Yes	80h
31:24		3, 19, or 23	RWS	Yes	80h

Register 13-208. B8Ch SerDes Drive Level 0 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The default value of this register, when combined with the **Post-Cursor Emphasis Level 0** register (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset B98h) default value, provides -3.5 dB of de-emphasis when the Link speed is 2.5 GT/s. However, it is also a Status register with provisional read-back data. The power-up reset default values of this register correspond to -3.5 dB drive levels, and can be overwritten by serial EEPROM or Configuration Space register transactions. However, when read back, the returned data always represents the ***current value being applied to the Lane***. That is because the Write Data value is written into a holding register for the -3.5 dB value, but cannot be directly read from the register. The Read Data value is always sourced from an active Drive register that is loaded dynamically upon de-emphasis changes. ***Notes:*** *Refer to Table 13-7 for the relationship between the Port 0, 16, or 20 parameters and SerDes modules and Lanes.* *The Port 0 fields are for Ports 0, 1, 2, and 3. The Port 16 fields are for Ports 16, 17, 18, and 19. The Port 20 fields are for Ports 20, 21, 22, and 23.* *Refer to Section 18.7, "Transmit Drive Characteristics," for a complete breakout of the default values, and their relationship with the **Post-Cursor Emphasis Level 0** register.*				
4:0	**Port 0, 16, or 20 2.5 GT/s Drive Level** Controls the Port 0, 16, or 20 Transmitter Drive Level control when the Link speed is 2.5 GT/s.	RWS	Yes	10h
7:5	***Reserved***	RsvdP	No	000b
12:8	**Port 1, 17, or 21 2.5 GT/s Drive Level** Controls the Port 1, 17, or 21 Transmitter Drive Level control when the Link speed is 2.5 GT/s.	RWS	Yes	10h
15:13	***Reserved***	RsvdP	No	000b
20:16	**Port 2, 18, or 22 2.5 GT/s Drive Level** Controls the Port 2, 18, or 22 Transmitter Drive Level control when the Link speed is 2.5 GT/s.	RWS	Yes	10h
23:21	***Reserved***	RsvdP	No	000b
28:24	**Port 3, 19, or 23 2.5 GT/s Drive Level** Controls the Port 3, 19, or 23 Transmitter Drive Level control when the Link speed is 2.5 GT/s.	RWS	Yes	10h
31:29	***Reserved***	RsvdP	No	000b

Register 13-209. B90h SerDes Drive Level 1 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
The default value of this register, when combined with the **Post-Cursor Emphasis Level 1** register (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset B9Ch) default value, provides -6 dB of de-emphasis when the Link speed is 5.0 GT/s and the current de-emphasis flag is 0. However, it is also a Status register with provisional read-back data. The power-up reset default values of this register correspond to -6 dB drive levels, and can be overwritten by serial EEPROM or Configuration Space register transactions. However, when read back, the returned data always represents the ***current value being applied to the Lane***. That is because the Write Data value is written into a holding register for the -6 dB value, but cannot be directly read from the register. The Read Data value is always sourced from an active Drive register that is loaded dynamically upon de-emphasis changes. ***Notes:*** *Refer to Table 13-7 for the relationship between the Port 0, 16, or 20 parameters and SerDes modules and Lanes.* *The Port 0 fields are for Ports 0, 1, 2, and 3. The Port 16 fields are for Ports 16, 17, 18, and 19. The Port 20 fields are for Ports 20, 21, 22, and 23.* *Refer to Section 18.7, "Transmit Drive Characteristics," for a complete breakout of the default values, and their relationship with the* ***Post-Cursor Emphasis Level 1*** *register.*				
4:0	**Port 0, 16, or 20 5.0 GT/s -6 dB Drive Level** Controls the Port 0, 16, or 20 Transmitter Drive Level control when the Link speed is 5.0 GT/s and the current De-Emphasis flag is 0.	RWS	Yes	0Eh
7:5	***Reserved***	RsvdP	No	000b
12:8	**Port 1, 17, or 21 5.0 GT/s -6 dB Drive Level** Controls the Port 1, 17, or 21 Transmitter Drive Level control when the Link speed is 5.0 GT/s and the current De-Emphasis flag is 0.	RWS	Yes	0Eh
15:13	***Reserved***	RsvdP	No	000b
20:16	**Port 2, 18, or 22 5.0 GT/s -6 dB Drive Level** Controls the Port 2, 18, or 22 Transmitter Drive Level control when the Link speed is 5.0 GT/s and the current De-Emphasis flag is 0.	RWS	Yes	0Eh
23:21	***Reserved***	RsvdP	No	000b
28:24	**Port 3, 19, or 23 5.0 GT/s -6 dB Drive Level** Controls the Port 3, 19, or 23 Transmitter Drive Level control when the Link speed is 5.0 GT/s and the current De-Emphasis flag is 0.	RWS	Yes	0Eh
31:29	***Reserved***	RsvdP	No	000b

Register 13-210. B94h SerDes Drive Level 2 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The default value of this register, when combined with the **Post-Cursor Emphasis Level 2** register (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset BA0h) default value, provides -3.5 dB of de-emphasis when the Link speed is 5.0 GT/s and the current de-emphasis flag is 1. However, it is also a Status register with provisional read-back data. The power-up reset default values of this register correspond to -3.5 dB drive levels, and can be overwritten by serial EEPROM or Configuration Space register transactions. However, when read back, the returned data always represents the ***current value being applied to the Lane***. That is because the Write Data value is written into a holding register for the -3.5 dB value, but cannot be directly read from the register. The Read Data value is always sourced from an active Drive register that is loaded dynamically upon de-emphasis changes. ***Notes:*** *Refer to Table 13-7 for the relationship between the Port 0, 16, or 20 parameters and SerDes modules and Lanes.* *The Port 0 fields are for Ports 0, 1, 2, and 3. The Port 16 fields are for Ports 16, 17, 18, and 19. The Port 20 fields are for Ports 20, 21, 22, and 23.* *Refer to Section 18.7, "Transmit Drive Characteristics," for a complete breakout of the default values, and their relationship with the **Post-Cursor Emphasis Level 2** register.*				
4:0	**Port 0, 16, or 20 5.0 GT/s -3.5 dB Drive Level** Controls the Port 0, 16, or 20 Transmitter Drive Level control when the Link speed is 5.0 GT/s and the current De-Emphasis flag is 1.	RWS	Yes	10h
7:5	***Reserved***	RsvdP	No	000b
12:8	**Port 1, 17, or 21 5.0 GT/s -3.5 dB Drive Level** Controls the Port 1, 17, or 21 Transmitter Drive Level control when the Link speed is 5.0 GT/s and the current De-Emphasis flag is 1.	RWS	Yes	10h
15:13	***Reserved***	RsvdP	No	000b
20:16	**Port 2, 18, or 22 5.0 GT/s -3.5 dB Drive Level** Controls the Port 2, 18, or 22 Transmitter Drive Level control when the Link speed is 5.0 GT/s and the current De-Emphasis flag is 1.	RWS	Yes	10h
23:21	***Reserved***	RsvdP	No	000b
28:24	**Port 3, 19, or 23 5.0 GT/s -3.5 dB Drive Level** Controls the Port 3, 19, or 23 Transmitter Drive Level control when the Link speed is 5.0 GT/s and the current De-Emphasis flag is 1.	RWS	Yes	10h
31:29	***Reserved***	RsvdP	No	000b

Register 13-211. B98h Post-Cursor Emphasis Level 0 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
The default value of this register, when combined with the **SerDes Drive Level 0** register (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset B8Ch) default value, provides -3.5 dB of de-emphasis when the Link speed is 2.5 GT/s. The power-up value can be overwritten by serial EEPROM or Configuration Space register transactions. However, when read back, the returned data always represents the ***current value being applied to the Lane***. That is because the Write Data value is written into a holding register for the -3.5 dB value, but cannot be directly read from the register. The Read Data value is always sourced from an active Drive register that is loaded dynamically upon de-emphasis changes. ***Notes:*** *Refer to Table 13-7 for the relationship between the Port 0, 16, or 20 parameters and SerDes modules and Lanes.* *The Port 0 fields are for Ports 0, 1, 2, and 3. The Port 16 fields are for Ports 16, 17, 18, and 19. The Port 20 fields are for Ports 20, 21, 22, and 23.* *Refer to Section 18.7, "Transmit Drive Characteristics," for a complete breakout of the default values, and their relationship with the **SerDes Drive Level 0** register.*				
4:0	**Port 0, 16, or 20 Post-Cursor Emphasis Level** Controls the Port 0, 16, or 20 Post-Cursor Emphasis level when the Link speed is 2.5 GT/s.	RWS	Yes	0Dh
7:5	***Reserved***	RsvdP	No	000b
12:8	**Port 1, 17, or 21 Post-Cursor Emphasis Level** Controls the Port 1, 17, or 21 Post-Cursor Emphasis level when the Link speed is 2.5 GT/s.	RWS	Yes	0Dh
15:13	***Reserved***	RsvdP	No	000b
20:16	**Port 2, 18, or 22 Post-Cursor Emphasis Level** Controls the Port 2, 18, or 22 Post-Cursor Emphasis level when the Link speed is 2.5 GT/s.	RWS	Yes	0Dh
23:21	***Reserved***	RsvdP	No	000b
28:24	**Port 3, 19, or 23 Post-Cursor Emphasis Level** Controls the Port 3, 19, or 23 Post-Cursor Emphasis level when the Link speed is 2.5 GT/s.	RWS	Yes	0Dh
31:29	***Reserved***	RsvdP	No	000b

Register 13-212. B9Ch Post-Cursor Emphasis Level 1 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The default value of this register, when combined with the **SerDes Drive Level 1** register (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset B90h) default value, provides -6 dB of de-emphasis when the Link speed is 5.0 GT/s and the current de-emphasis flag is 0. The power-up value can be overwritten by serial EEPROM or Configuration Space register transactions. However, when read back, the returned data always represents the ***current value being applied to the Lane***. That is because the Write Data value is written into a holding register for the -6 dB value, but cannot be directly read from the register. The Read Data value is always sourced from an active Drive register that is loaded dynamically upon de-emphasis changes. ***Notes:*** *Refer to Table 13-7 for the relationship between the Port 0, 16, or 20 parameters and SerDes modules and Lanes.* *The Port 0 fields are for Ports 0, 1, 2, and 3. The Port 16 fields are for Ports 16, 17, 18, and 19. The Port 20 fields are for Ports 20, 21, 22, and 23.* *Refer to Section 18.7, “Transmit Drive Characteristics,” for a complete breakout of the default values, and their relationship with the **SerDes Drive Level 1** register.*				
4:0	**Port 0, 16, or 20 5.0 GT/s -6 dB Post-Cursor Emphasis Level** Controls the Port 0, 16, or 20 Post-Cursor Emphasis level when the Link speed is 5.0 GT/s and the current De-Emphasis flag is 0.	RWS	Yes	15h
7:5	***Reserved***	RsvdP	No	000b
12:8	**Port 1, 17, or 21 5.0 GT/s -6 dB Post-Cursor Emphasis Level** Controls the Port 1, 17, or 21 Post-Cursor Emphasis level when the Link speed is 5.0 GT/s and the current De-Emphasis flag is 0.	RWS	Yes	15h
15:13	***Reserved***	RsvdP	No	000b
20:16	**Port 2, 18, or 22 5.0 GT/s -6 dB Post-Cursor Emphasis Level** Controls the Port 2, 18, or 22 Post-Cursor Emphasis level when the Link speed is 5.0 GT/s and the current de-emphasis is -6 dB.	RWS	Yes	15h
23:21	***Reserved***	RsvdP	No	000b
28:24	**Port 3, 19, or 23 5.0 GT/s -6 dB Post-Cursor Emphasis Level** Controls the Port 3, 19, or 23 Post-Cursor Emphasis level when the Link speed is 5.0 GT/s and the current De-Emphasis flag is 0.	RWS	Yes	15h
31:29	***Reserved***	RsvdP	No	000b

Register 13-213. BA0h Post-Cursor Emphasis Level 2 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The default value of this register, when combined with the **SerDes Drive Level 2** register (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset B94h) default value, provides -3.5 dB of de-emphasis when the Link speed is 5.0 GT/s and the current de-emphasis flag is 1. The power-up value can be overwritten by serial EEPROM or Configuration Space register transactions. However, when read back, the returned data always represents the ***current value being applied to the Lane***. That is because the Write Data value is written into a holding register for the 3.5 dB value, but cannot be directly read from the register. The Read Data value is always sourced from an active Drive register that is loaded dynamically upon de-emphasis changes. ***Notes:*** *Refer to Table 13-7 for the relationship between the Port 0, 16, or 20 parameters and SerDes modules and Lanes.* *The Port 0 fields are for Ports 0, 1, 2, and 3. The Port 16 fields are for Ports 16, 17, 18, and 19. The Port 20 fields are for Ports 20, 21, 22, and 23.* *Refer to Section 18.7, “Transmit Drive Characteristics,” for a complete breakout of the default values, and their relationship with the **SerDes Drive Level 2** register.*				
4:0	**Port 0, 16, or 20 5.0 GT/s -3.5 dB Post-Cursor Emphasis Level** Controls the Port 0, 16, or 20 Post-Cursor Emphasis level when the Link speed is 5.0 GT/s and the current De-Emphasis flag is 1.	RWS	Yes	0Dh
7:5	***Reserved***	RsvdP	No	000b
12:8	**Port 1, 17, or 21 5.0 GT/s -3.5 dB Post-Cursor Emphasis Level** Controls the Port 1, 17, or 21 Post-Cursor Emphasis level when the Link speed is 5.0 GT/s and the current De-Emphasis flag is 1.	RWS	Yes	0Dh
15:13	***Reserved***	RsvdP	No	000b
20:16	**Port 2, 18, or 22 5.0 GT/s -3.5 dB Post-Cursor Emphasis Level** Controls the Port 2, 18, or 22 Post-Cursor Emphasis level when the Link speed is 5.0 GT/s and the current De-Emphasis flag is 1.	RWS	Yes	0Dh
23:21	***Reserved***	RsvdP	No	000b
28:24	**Port 3, 19, or 23 5.0 GT/s -3.5 dB Post-Cursor Emphasis Level** Controls the Port 3, 19, or 23 Post-Cursor Emphasis level when the Link speed is 5.0 GT/s and the current De-Emphasis flag is 1.	RWS	Yes	0Dh
31:29	***Reserved***	RsvdP	No	000b

Register 13-214. BA4h Receiver Equalization Level 0 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	This register provides the Receiver Equalization Level control for the lower eight SerDes within each Station.			

Rx Equalization[3:0]	Equalization	Rx Equalization[3:0]	Equalization
0h (default)	Off	7h to 9h	Medium
1h	Minimum	Ah to Dh	High to Medium
2h to 3h	Low	Eh to Fh	Maximum
4h to 6h	Low to Medium		

Note: *Refer to Table 13-7 for the relationship between the Port 0, 16, or 20 parameters and SerDes modules and Lanes.*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
3:0	**SerDes 0, 32, or 16 Receiver Equalization Level**	RWS	Yes	0h
7:4	**SerDes 1, 33, or 17 Receiver Equalization Level**	RWS	Yes	0h
11:8	**SerDes 2, 34, or 18 Receiver Equalization Level**	RWS	Yes	0h
15:12	**SerDes 3, 35, or 19 Receiver Equalization Level**	RWS	Yes	0h
19:16	**SerDes 4, 36, or 20 Receiver Equalization Level**	RWS	Yes	0h
23:20	**SerDes 5, 37, or 21 Receiver Equalization Level**	RWS	Yes	0h
27:24	**SerDes 6, 38, or 22 Receiver Equalization Level**	RWS	Yes	0h
31:28	**SerDes 7, 39, or 23 Receiver Equalization Level**	RWS	Yes	0h

Register 13-215. BA8h Receiver Equalization Level 1 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I^{2}C</th><th>Default</th></tr>
<tr><td colspan="5">This register provides the Receiver Equalization Level control for the upper eight SerDes within each Station.
<table>
<tr><th>Rx Equalization[3:0]</th><th>Equalization</th><th>Rx Equalization[3:0]</th><th>Equalization</th></tr>
<tr><td>0h (default)</td><td>Off</td><td>7h to 9h</td><td>Medium</td></tr>
<tr><td>1h</td><td>Minimum</td><td>Ah to Dh</td><td>High to Medium</td></tr>
<tr><td>2h to 3h</td><td>Low</td><td>Eh to Fh</td><td>Maximum</td></tr>
<tr><td>4h to 6h</td><td>Low to Medium</td><td></td><td></td></tr>
</table>

Note: *Refer to Table 13-7 for the relationship between the Port 0, 16, or 20 parameters and SerDes modules and Lanes.*</td></tr>
<tr><td>3:0</td><td>**SerDes 8, 40, or 24 Receiver Equalization Level**</td><td>RWS</td><td>Yes</td><td>0h</td></tr>
<tr><td>7:4</td><td>**SerDes 9, 41, or 25 Receiver Equalization Level**</td><td>RWS</td><td>Yes</td><td>0h</td></tr>
<tr><td>11:8</td><td>**SerDes 10, 42, or 26 Receiver Equalization Level**</td><td>RWS</td><td>Yes</td><td>0h</td></tr>
<tr><td>15:12</td><td>**SerDes 11, 43, or 27 Receiver Equalization Level**</td><td>RWS</td><td>Yes</td><td>0h</td></tr>
<tr><td>19:16</td><td>**SerDes 12, 44, or 28 Receiver Equalization Level**</td><td>RWS</td><td>Yes</td><td>0h</td></tr>
<tr><td>23:20</td><td>**SerDes 13, 45, or 29 Receiver Equalization Level**</td><td>RWS</td><td>Yes</td><td>0h</td></tr>
<tr><td>27:24</td><td>**SerDes 14, 46, or 30 Receiver Equalization Level**</td><td>RWS</td><td>Yes</td><td>0h</td></tr>
<tr><td>31:28</td><td>**SerDes 15, 47, or 31 Receiver Equalization Level**</td><td>RWS</td><td>Yes</td><td>0h</td></tr>
</table>

Register 13-216. BACh Signal Detect Level (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
This register provides the Receiver Signal Detect Level select. Each two-bit field in this register provides four settings for detecting Electrical Idle Analog, for the corresponding SerDes. 00b = Approximately 50 to 80 mV 01b = Approximately 65 to 175 mV (default) 10b = Approximately 75 to 200 mV 11b = Approximately 120 to 240 mV ***Note:*** *Refer to Table 13-7 for the relationship between the Port 0, 16, or 20 parameters and SerDes modules and Lanes.*				
1:0	**SerDes 0, 32, or 16 Signal Detect Level**	RWS	Yes	01b
3:2	**SerDes 1, 33, or 17 Signal Detect Level**	RWS	Yes	01b
5:4	**SerDes 2, 34, or 18 Signal Detect Level**	RWS	Yes	01b
7:6	**SerDes 3, 35, or 19 Signal Detect Level**	RWS	Yes	01b
9:8	**SerDes 4, 36, or 20 Signal Detect Level**	RWS	Yes	01b
11:10	**SerDes 5, 37, or 21 Signal Detect Level**	RWS	Yes	01b
13:12	**SerDes 6, 38, or 22 Signal Detect Level**	RWS	Yes	01b
15:14	**SerDes 7, 39, or 23 Signal Detect Level**	RWS	Yes	01b
17:16	**SerDes 8, 40, or 24 Signal Detect Level**	RWS	Yes	01b
19:18	**SerDes 9, 41, or 25 Signal Detect Level**	RWS	Yes	01b
21:20	**SerDes 10, 42, or 26 Signal Detect Level**	RWS	Yes	01b
23:22	**SerDes 11, 43, or 27 Signal Detect Level**	RWS	Yes	01b
25:24	**SerDes 12, 44, or 28 Signal Detect Level**	RWS	Yes	01b
27:26	**SerDes 13, 45, or 29 Signal Detect Level**	RWS	Yes	01b
29:28	**SerDes 14, 46, or 30 Signal Detect Level**	RWS	Yes	01b
31:30	**SerDes 15, 47, or 31 Signal Detect Level**	RWS	Yes	01b

Register 13-217. BB8h Clock/Data Recovery Control 1 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

This register provides the CDR circuit control for the upper eight SerDes within each Station. Control is provided for enabling the associated SerDes' 2nd order loop (default), and controlling the gain of the associated SerDes' 2nd order loop.

The default value of this register configures all CDR circuits to operate in an Asynchronous Clocking system. If the **Link Control** register *Common Clock Configuration* bit (offset 78h[6]) is Set, the register fields that correspond to the common clock Port are automatically loaded with the values needed to operate in a Synchronous Clocking system. These values can be overridden with a Configuration Write and/or serial EEPROM load. If a serial EEPROM load is used to Set the *Common Clock Configuration* bit, the serial EEPROM load should also load this register with the correct values.

Note: *Refer to Table 13-7 for the relationship between the Port 0, 16, or 20 parameters and SerDes modules and Lanes.*

Clock	SerDes *x* 2nd Order Loop Gain Field Value	SerDes *x* 2nd Order Loop Enable Bit Value	Link Control register *Common Clock Configuration* field, (offset 78h[6]) Value
Synchronous	00b	0	1
Asynchronous	11b	1	0

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
1:0	**SerDes 8, 40, or 24 2nd Order Loop Gain**	RWS	Yes	11b
2	***Reserved***	RsvdP	No	0
3	**SerDes 8, 40, or 24 2nd Order Loop Enable**	RWS	Yes	1
5:4	**SerDes 9, 41, or 25 2nd Order Loop Gain**	RWS	Yes	11b
6	***Reserved***	RsvdP	No	0
7	**SerDes 9, 41, or 25 2nd Order Loop Enable**	RWS	Yes	1
9:8	**SerDes 10, 42, or 26 2nd Order Loop Gain**	RWS	Yes	11b
10	***Reserved***	RsvdP	No	0
11	**SerDes 10, 42, or 26 2nd Order Loop Enable**	RWS	Yes	1
13:12	**SerDes 11, 43, or 27 2nd Order Loop Gain**	RWS	Yes	11b
14	***Reserved***	RsvdP	No	0
15	**SerDes 11, 43, or 27 2nd Order Loop Enable**	RWS	Yes	1

Register 13-217. BB8h Clock/Data Recovery Control 1 (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
17:16	**SerDes 12, 44, or 28 2nd Order Loop Gain**	RWS	Yes	11b
18	***Reserved***	RsvdP	No	0
19	**SerDes 12, 44, or 28 2nd Order Loop Enable**	RWS	Yes	1
21:20	**SerDes 13, 45, or 29 2nd Order Loop Gain**	RWS	Yes	11b
22	***Reserved***	RsvdP	No	0
23	**SerDes 13, 45, or 29 2nd Order Loop Enable**	RWS	Yes	1
25:24	**SerDes 14, 46, or 30 2nd Order Loop Gain**	RWS	Yes	11b
26	***Reserved***	RsvdP	No	0
27	**SerDes 14, 46, or 30 2nd Order Loop Enable**	RWS	Yes	1
29:28	**SerDes 15, 47, or 31 2nd Order Loop Gain**	RWS	Yes	11b
30	***Reserved***	RsvdP	No	0
31	**SerDes 15, 47, or 31 2nd Order Loop Enable**	RWS	Yes	1

13.16 Multicast Extended Capability Registers (Offsets E00h – E2Ch) – All Modes Except Legacy NT

This section details the Multicast Extended Capability registers. Table 13-37 defines the register map.

Multicast is described, in detail, in Section 8.6, "Multicast – All Modes Except Legacy NT."

Table 13-37. Multicast Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (B70h or F24h)	Capability Version (1h)	PCI Express Extended Capability ID (0012h)	E00h
Multicast Control		Multicast Extended Capability	E04h
Multicast BAR0			E08h
Multicast BAR1			E0Ch
Multicast Receive 0			E10h
Multicast Receive 1			E14h
Multicast Block All 0			E18h
Multicast Block All 1			E1Ch
Multicast Block Untranslated 0			E20h
Multicast Block Untranslated 1			E24h
Multicast Overlay BAR0			E28h
Multicast Overlay BAR1			E2Ch

Register 13-218. E00h Multicast Extended Capability Header (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
15:0	**PCI Express Extended Capability ID** Program to 0012h, to indicate that the Extended Capability structure is the **Multicast Extended Capability** structure.		RO	Yes	0012h
19:16	**Capability Version**		RO	Yes	1h
31:20	**Next Capability Offset** Next extended capability is the **Vendor-Specific Extended Capability 2** structure, offset B70h.	Upstream	RO	Yes	B70h
	Next extended capability is the **ACS Extended Capability** structure, offset F24h.	Downstream	RO	Yes	F24h

Register 13-219. E04h Multicast Extended Capability and Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
	Multicast Extended Capability			
5:0	**MC Max Group** 00h = Indicates that one Multicast Group is supported 3Fh = Indicates the maximum number of Multicast Groups that the component supports, encoded as *M*-1	RO	Yes	3Fh
14:6	***Reserved***	RsvdP	No	0-0h
15	**MC ECRC Generation Supported** 0 = End-to-end Cyclic Redundancy Check (ECRC) generation is not supported in Multicast 1 = ECRC generation is supported in Multicast	RO	Yes	1
	Multicast Control			
21:16	**MC Num Group** Indicates the number of Multicast Groups configured for use, encoded as *N*-1. The behavior of this field is undefined if its value exceeds the value indicated by field [5:0] (*MC Max Group*). This parameter indirectly defines the upper limit of the Multicast Address range. This field is ignored if bit 31 (*MC Enable)* is Cleared. 00h = Indicates that one Multicast Group is configured for use	RW	Yes	00h
30:22	***Reserved***	RsvdP	No	0-0h
31	**MC Enable** 0 = Disables Multicast 1 = Enables Multicast	RW	Yes	0

Register 13-220. E08h Multicast BAR0 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
5:0	**MC Index Position** The Multicast Group Number LSB location within the address. The behavior of this field is undefined if its value is less than 12h and the **Multicast Control** register *MC Enable* bit (offset E04h[31]) is Set.	RW	Yes	00h
11:6	***Reserved***	RsvdP	No	0-0h
31:12	**MC Base Address** Multicast Lower Base Address[31:12]. Base address of the Multicast Address range. The behavior is undefined if: • **Multicast Control** register *MC Enable* bit (offset E04h[31]) is Set, and • Bits in this field corresponding to Address bits that contain the Multicast Group number, or Address bits less than the value indicated by field [5:0] (*MC Index Position*), are non-zero.	RW	Yes	0000_0h

Register 13-221. E0Ch Multicast BAR1 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**MC Upper Base Address** Multicast Upper Base Address[63:32]. Base address of the Multicast Address range. The behavior is undefined if: • **Multicast Control** register *MC Enable* bit (offset E04h[31]) is Set, and • Bits in this field corresponding to Address bits that contain the Multicast Group number, or Address bits less than the value indicated by the **Multicast BAR0** register *MC Index Position* field (offset E04h[5:0]), are non-zero.	RW	Yes	0000_0000h

Register 13-222. E10h Multicast Receive 0 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
31:0	**MC Receive** Multicast Receive[31:0]. Provides a bit Vector that denotes to which Multicast Groups the Port should forward Multicast TLPs. For each bit that is Set, this Port receives a copy of any Multicast TLPs that exist for the associated Multicast Group. Bits above MC Num Group (**Multicast Extended Capability** register *MC Num Group* field (offset E04h[21:16])) are ignored by hardware.	RW	Yes	0000_0000h

Register 13-223. E14h Multicast Receive 1 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
31:0	**MC Receive** Multicast Receive[63:32]. Provides a bit Vector that denotes to which Multicast Groups the Port should forward Multicast TLPs. For each bit that is Set, this Port receives a copy of any Multicast TLPs that exist for the associated Multicast Group. Bits above MC Num Group (**Multicast Extended Capability** register *MC Num Group* field (offset E04h[21:16])) are ignored by hardware.	RW	Yes	0000_0000h

Register 13-224. E18h Multicast Block All 0 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
31:0	**MC Block All** Multicast Block All[31:0]. Provides a bit Vector that denotes which Multicast Groups the Multicast function should block. For each bit that is Set, this Port is blocked from sending TLPs to the associated Multicast Group. Bits above MC Num Group (**Multicast Extended Capability** register *MC Num Group* field (offset E04h[21:16])) are ignored by hardware.	RW	Yes	0000_0000h

Register 13-225. E1Ch Multicast Block All 1 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
31:0	**MC Block All** Multicast Block All[63:32]. Provides a bit Vector that denotes which Multicast Groups the Multicast function should block. For each bit that is Set, this Port is blocked from sending TLPs to the associated Multicast Group. Bits above MC Num Group (**Multicast Extended Capability** register *MC Num Group* field (offset E04h[21:16])) are ignored by hardware.	RW	Yes	0000_0000h

Register 13-226. E20h Multicast Block Untranslated 0 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**MC Block Untranslated** Multicast Block Untranslated[31:0]. Used to determine whether a TLP that includes an Untranslated Address should be blocked. For each bit that is Set, this Port is blocked from sending TLPs containing Untranslated addresses to the associated Multicast Group. Bits above MC Num Group (**Multicast Extended Capability** register *MC Num Group* field (offset E04h[21:16])) are ignored by hardware.	RW	Yes	0000_0000h

Register 13-227. E24h Multicast Block Untranslated 1 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**MC Block Untranslated** Multicast Block Untranslated[63:32]. Used to determine whether a TLP that includes an Untranslated Address should be blocked. For each bit that is Set, this Port is blocked from sending TLPs containing Untranslated addresses to the associated Multicast Group. Bits above MC Num Group (**Multicast Extended Capability** register *MC Num Group* field (offset E04h[21:16])) are ignored by hardware.	RW	Yes	0000_0000h

Register 13-228. E28h Multicast Overlay BAR0 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
Specifies the Base address of a window in Unicast space onto which Multicast TLPs output from an egress Port are overlaid by a process of address replacement. This allows a single BAR in an endpoint attached to the PEX 8649 to be used for both Unicast and Multicast traffic. At the PEX 8649 upstream Port(s), this register allows the Multicast Address range, or a portion of it, to be overlaid onto Host memory.				
5:0	**MC Overlay Size** Less than 06h = Disables the Overlay mechanism 06h or greater = Specifies the size (in bytes) of the Overlay Address range, as a power of 2	RW	Yes	0-0h
31:6	**MC Overlay BAR** Multicast Overlay Lower Base Address[31:6]. Specifies the Base address of the window onto which Multicast TLPs passing through the Multicast function will be overlaid.	RW	Yes	0-0h

Register 13-229. E2Ch Multicast Overlay BAR1 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
Specifies the Base address of a window in Unicast space onto which Multicast TLPs output from an egress Port are overlaid by a process of address replacement. This allows a single BAR in an endpoint attached to the PEX 8649 to be used for both Unicast and Multicast traffic. At the PEX 8649 upstream Port(s), this register allows the Multicast Address range, or a portion of it, to be overlaid onto Host memory.				
31:0	**MC Overlay Upper Base Address** Multicast Overlay Upper Base Address[63:32]. Specifies the Base address of the window onto which Multicast TLPs passing through the Multicast function will be overlaid.	RW	Yes	0000_0000h

13.17 Device-Specific Registers – Virtual Switch (Offset F20h), Virtual Switch Mode Only

Note: *In Base mode, this entire structure is **reserved**, RsvdP, not serial EEPROM nor I^2C writable, and has a default value of 0h.*

This section details the Device-Specific Port Cut-Thru Enable Status register, which is part of the Device-Specific Virtual Switch registers. Table 13-38 defines the register map.

Other Device-Specific Virtual Switch registers are detailed in Section 13.15.13, “Device-Specific Registers – Virtual Switch (Offsets 900h – 9ECh), Virtual Switch Mode Only.”

Other Device-Specific registers are detailed in:

- Section 13.15, “Device-Specific Registers (Offsets 1C0h – DFCh)”
- Section 13.19, “Device-Specific Registers (Offsets F30h – FB0h)”

Table 13-38. Device-Specific Virtual Switch Register Map (Offset F20h) (Virtual Switch mode – VS Upstream Port(s))

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved	Port Cut-Thru Enable Status	F20h

Register 13-230. F20h Port Cut-Thru Enable Status (Virtual Switch mode – VS Upstream Port(s))

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
0	**Port 0 Cut-Thru Enable Status** Link Up status. 0 = Cut-Thru is disabled for this Port (Link is down) 1 = Cut-Thru is enabled for this Port (Link is up)	RO	No	Set by STRAP_STN0_PORTCFG[1:0] ball levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 0* field (Port 0, accessible through the Management Port, offset 300h[1:0])
1	**Port 1 Cut-Thru Enable Status** Link Up status. 0 = Cut-Thru is disabled for this Port (Link is down) 1 = Cut-Thru is enabled for this Port (Link is up)	RO	No	
2	**Port 2 Cut-Thru Enable Status** Link Up status. 0 = Cut-Thru is disabled for this Port (Link is down) 1 = Cut-Thru is enabled for this Port (Link is up)	RO	No	
3	**Port 3 Cut-Thru Enable Status** Link Up status. 0 = Cut-Thru is disabled for this Port (Link is down) 1 = Cut-Thru is enabled for this Port (Link is up)	RO	No	
15:4	***Reserved***	RsvdP	No	000h

Register 13-230. F20h Port Cut-Thru Enable Status (Virtual Switch mode – VS Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
16	**Port 16 Cut-Thru Enable Status** Link Up status. 0 = Cut-Thru is disabled for this Port (Link is down) 1 = Cut-Thru is enabled for this Port (Link is up)	RO	No	Set by STRAP_STN4_PORTCFG[1:0] ball levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 4* field (Port 0, accessible through the Management Port, offset 300h[9:8])
17	**Port 17 Cut-Thru Enable Status** Link Up status. 0 = Cut-Thru is disabled for this Port (Link is down) 1 = Cut-Thru is enabled for this Port (Link is up)	RO	No	
18	**Port 18 Cut-Thru Enable Status** Link Up status. 0 = Cut-Thru is disabled for this Port (Link is down) 1 = Cut-Thru is enabled for this Port (Link is up)	RO	No	
19	**Port 19 Cut-Thru Enable Status** Link Up status. 0 = Cut-Thru is disabled for this Port (Link is down) 1 = Cut-Thru is enabled for this Port (Link is up)	RO	No	

Register 13-230. F20h Port Cut-Thru Enable Status (Virtual Switch mode – VS Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
20	**Port 20 Cut-Thru Enable Status** Link Up status. 0 = Cut-Thru is disabled for this Port (Link is down) 1 = Cut-Thru is enabled for this Port (Link is up)	RO	No	Set by STRAP_STN5_PORTCFG[1:0] ball levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 5* field (Port 0, accessible through the Management Port, offset 300h[11:10])
21	**Port 21 Cut-Thru Enable Status** Link Up status. 0 = Cut-Thru is disabled for this Port (Link is down) 1 = Cut-Thru is enabled for this Port (Link is up)	RO	No	
22	**Port 22 Cut-Thru Enable Status** Link Up status. 0 = Cut-Thru is disabled for this Port (Link is down) 1 = Cut-Thru is enabled for this Port (Link is up)	RO	No	
23	**Port 23 Cut-Thru Enable Status** Link Up status. 0 = Cut-Thru is disabled for this Port (Link is down) 1 = Cut-Thru is enabled for this Port (Link is up)	RO	No	
31:24	***Reserved***	RsvdP	No	00h

13.18 ACS Extended Capability Registers (Offsets F24h – F2Ch)

This section details the ACS Extended Capability registers. Table 13-39 defines the register map.

Table 13-39. ACS Extended Capability Register Map (Downstream Ports; Upstream Port(s) Always Read(s) 0)

31 30 29 28 27 26 25 24 23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved (Upstream)			F24h
Next Capability Offset (B70h) (Downstream)	Capability Version (1h) (Downstream	PCI Express Extended Capability ID (000Dh) (Downstream)	
Reserved (Upstream)			F28h
ACS Control (Downstream)		ACS Capability (Downstream)	
Reserved (Upstream) Egress Control Vector (Downstream)			F2Ch

Register 13-231. F24h ACS Extended Capability Header (Downstream Ports; Upstream Port(s) Always Read(s) 0)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
Note: *Because this register is implemented as one physical register common to all Ports, the upstream Port(s)' register (which is* ***reserved****) has the same value as the downstream Ports' registers. However, in the upstream Port(s), the ACS Extended Capability is excluded from the Linked List of PCI Express Extended Capabilities, and therefore, the upstream Port(s)' register is effectively hidden from system software and the non-zero value has no significant consequence.*					
15:0	***Reserved***	Upstream	RsvdP	No	0000h
	PCI Express Extended Capability ID	Downstream	RO	Yes	000Dh
19:16	***Reserved***	Upstream	RsvdP	No	0h
	Capability Version	Downstream	RO	Yes	1h
31:20	***Reserved***	Upstream	RsvdP	No	000h
	Next Capability Offset Program to B70h, which addresses the **Vendor-Specific Extended Capability 2** structure.	Downstream	RO	Yes	B70h

Register 13-232. F28h ACS Control and Capability (Downstream Ports; Upstream Port(s) Always Read(s) 0)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
	ACS Capability				
0	***Reserved***	Upstream	RsvdP	No	0
	ACS Source Validation	Downstream	RO	Yes	1
1	***Reserved***	Upstream	RsvdP	No	0
	ACS Translation Blocking	Downstream	RO	Yes	1
2	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Request Redirect ACS Peer-to-Peer Request redirect.	Downstream	RO	Yes	1
3	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Completion Redirect ACS Peer-to-Peer Completion redirect.	Downstream	RO	Yes	1
4	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding	Downstream	RO	Yes	1
5	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Egress Control ACS Peer-to-Peer Egress control.	Downstream	RO	Yes	1
6	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P ACS Direct Translated Peer-to-Peer.	Downstream	RO	Yes	1
7	***Reserved***		RsvdP	No	0
12:8	***Reserved***	Upstream	RsvdP	No	0
	Egress Control Vector Size Encodings 01h through FFh directly indicate the number of each downstream Port's **Egress Control Vector** register *Peer-to-Peer Port x Control* bit (Downstream Ports, offset F2Ch[23:16, 3:0]). ***Note:*** *The ACS Egress Control Vector Size value must be adjusted for the specific Port configuration.*	Downstream	HwInit	Yes	18h
15:13	***Reserved***		RsvdP	No	000b

Register 13-232. F28h ACS Control and Capability (Downstream Ports; Upstream Port(s) Always Read(s) 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
	ACS Control				
16	***Reserved***	Upstream	RsvdP	No	0
	ACS Source Validation Enable 0 = Disables 1 = Enables	Downstream	RW	Yes	0
17	***Reserved***	Upstream	RsvdP	No	0
	ACS Translation Blocking Enable 0 = Disables 1 = Enables	Downstream	RW	Yes	0
18	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Request Redirect Enable Enables or disables ACS Peer-to-Peer Request redirect. 0 = Disables 1 = Enables	Downstream	RW	Yes	0
19	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Completion Redirect Enable Enables or disables ACS Peer-to-Peer Completion redirect. 0 = Disables 1 = Enables	Downstream	RW	Yes	0
20	***Reserved***	Upstream	RsvdP	No	0
	ACS Upstream Forwarding Enable 0 = Disables 1 = Enables	Downstream	RW	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	ACS P2P Egress Control Enable Enables or disables ACS Peer-to-Peer Egress control. 0 = Disables 1 = Enables	Downstream	RW	Yes	0
22	***Reserved***	Upstream	RsvdP	No	0
	ACS Direct Translated P2P Enable Enables or disables ACS Direct Translated Peer-to-Peer. 0 = Disables 1 = Enables	Downstream	RW	Yes	0
31:23	***Reserved***		RsvdP	No	0-0h

Register 13-233. F2Ch Egress Control Vector (Downstream Ports; Upstream Port(s) Always Read(s) 0)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
0	***Reserved***	Upstream	RsvdP	No	0
	Peer-to-Peer Port 0 Control Valid when the **ACS Control** register *ACS P2P Egress Control Enable* bit (Downstream Ports, offset F28h[21]) is Set. 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
1	***Reserved***	Upstream	RsvdP	No	0
	Peer-to-Peer Port 1 Control Valid when the **ACS Control** register *ACS P2P Egress Control Enable* bit (Downstream Ports, offset F28h[21]) is Set. 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
2	***Reserved***	Upstream	RsvdP	No	0
	Peer-to-Peer Port 2 Control Valid when the **ACS Control** register *ACS P2P Egress Control Enable* bit (Downstream Ports, offset F28h[21]) is Set. 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
3	***Reserved***	Upstream	RsvdP	No	0
	Peer-to-Peer Port 3 Control Valid when the **ACS Control** register *ACS P2P Egress Control Enable* bit (Downstream Ports, offset F28h[21]) is Set. 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
15:4	***Reserved***		RsvdP	No	000h

Register 13-233. F2Ch Egress Control Vector (Downstream Ports; Upstream Port(s) Always Read(s) 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
16	***Reserved***	Upstream	RsvdP	No	0
	Peer-to-Peer Port 16 Control Valid when the **ACS Control** register *ACS P2P Egress Control Enable* bit (Downstream Ports, offset F28h[21]) is Set. 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
17	***Reserved***	Upstream	RsvdP	No	0
	Peer-to-Peer Port 17 Control Valid when the **ACS Control** register *ACS P2P Egress Control Enable* bit (Downstream Ports, offset F28h[21]) is Set. 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
18	***Reserved***	Upstream	RsvdP	No	0
	Peer-to-Peer Port 18 Control Valid when the **ACS Control** register *ACS P2P Egress Control Enable* bit (Downstream Ports, offset F28h[21]) is Set. 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
19	***Reserved***	Upstream	RsvdP	No	0
	Peer-to-Peer Port 19 Control Valid when the **ACS Control** register *ACS P2P Egress Control Enable* bit (Downstream Ports, offset F28h[21]) is Set. 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0

Register 13-233. F2Ch Egress Control Vector (Downstream Ports; Upstream Port(s) Always Read(s) 0) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
20	***Reserved***	Upstream	RsvdP	No	0
	Peer-to-Peer Port 20 Control Valid when the **ACS Control** register *ACS P2P Egress Control Enable* bit (Downstream Ports, offset F28h[21]) is Set. 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	Peer-to-Peer Port 21 Control Valid when the **ACS Control** register *ACS P2P Egress Control Enable* bit (Downstream Ports, offset F28h[21]) is Set. 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
22	***Reserved***	Upstream	RsvdP	No	0
	Peer-to-Peer Port 22 Control Valid when the **ACS Control** register *ACS P2P Egress Control Enable* bit (Downstream Ports, offset F28h[21]) is Set. 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
23	***Reserved***	Upstream	RsvdP	No	0
	Peer-to-Peer Port 23 Control Valid when the **ACS Control** register *ACS P2P Egress Control Enable* bit (Downstream Ports, offset F28h[21]) is Set. 0 = No Peer-to-Peer control 1 = ACS Peer-to-Peer control	Downstream	RW	Yes	0
31:24	***Reserved***		RsvdP	No	00h

13.19 Device-Specific Registers (Offsets F30h – FB0h)

This section details the Device-Specific registers located at offsets F30h through FB0h. Device-Specific registers are unique to the PEX 8649 and not referenced in the *PCI Express Base r2.0*. Table 13-40 defines the register map.

Other Device-Specific registers are detailed in:

- Section 13.15, "Device-Specific Registers (Offsets 1C0h – DFCh)"
- Section 13.17, "Device-Specific Registers – Virtual Switch (Offset F20h), Virtual Switch Mode Only"

***Note:* *It is recommended that these registers not be changed from their default values*.**

Table 13-40. Device-Specific Register Map (Offsets F30h – FB0h)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Device-Specific Registers – Egress Control (Offsets F30h – F44h)		F30h … F44h
Device-Specific Registers – Ingress Control and Port Enable (Offsets F48h – F6Ch)		F48h … F6Ch
Device-Specific Registers – Error Checking and Debug (Offsets F70h – FB0h)		F70h … FB0h

13.19.1 Device-Specific Registers – Egress Control (Offsets F30h – F44h)

This section details the Device-Specific Egress Control registers. Table 13-41 defines the register map.

Table 13-41. Device-Specific Egress Control Register Map (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Egress Control and Status	F30h
Reserved	F34h
Port Egress TLP Threshold	F38h
Reserved	F3Ch – F44h

Register 13-234. F30h Egress Control and Status (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
1:0	***Reserved***		RsvdP	No	00b
8:2	***Factory Test Only***		RWS	Yes	0-0h
9	**Vendor-Defined Type 0 UR** 0 = Do not generate UR Vendor-Defined Type 0 Broadcast TLP in *DL_Down* state 1 = Generate UR Vendor-Defined Type 0 Broadcast TLP in *DL_Down* state	**Base Mode** 0, 16, 20 **Virtual Switch Mode** 0, 16, 20, accessible through the Management Port	RWS	Yes	0
10	**Egress Credit Timeout Enable** 0 = Egress Credit Timeout mechanism is disabled. 1 = Egress Credit Timeout mechanism is enabled. The timeout period is selected in field [12:11] (*Egress Credit Timeout Value*). Status is reflected in bit 16 (*Egress Credit Timeout Status*). If the Egress Credit Timer is enabled and expires (due to lack of Flow Control credits from the connected device), the Port brings down its Link. This event generates a Surprise Down Uncorrectable error, for Transparent downstream Ports. For upstream Port Egress Credit Timeout, the connected upstream device detects the Surprise Down event.	**Base Mode** 0, 16, 20 **Virtual Switch Mode** 0, 16, 20, accessible through the Management Port	RWS	Yes	0
12:11	**Egress Credit Timeout Value** 00b = 1 ms 01b = 512 ms 10b = 1s 11b = ***Reserved***	**Base Mode** 0, 16, 20 **Virtual Switch Mode** 0, 16, 20, accessible through the Management Port	RWS	Yes	00b
15:13	***Reserved***		RsvdP	No	000b

Register 13-234. F30h Egress Control and Status (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
16	**Egress Credit Timeout Status** 0 = No timeout 1 = Timeout		RW1CS	No	0
18:17	**Egress Credit Timeout VC&T** Egress Credit timeout for Virtual Channel and Type. 00b = Posted 01b = Non-Posted 10b = Completion 11b = ***Reserved***		RO	No	00b
30:19	***Reserved***		RsvdP	No	0-0h
31	**Port Activity** 0 = Port is idle 1 = Port has one or more pending TLPs to transmit		RO	No	0

Register 13-235. F38h Port Egress TLP Threshold (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
Caution: ***Source Queuing and Read Pacing should not be concurrently enabled. The two features are incompatible and doing so can result in Fatal errors.***					
11:0	**Port Lower TLP Counter** When Source Scheduling is disabled due to Threshold, it is re-enabled when the Port TLP Counter goes below this Threshold value.	Upstream	RWS	Yes	003h
		Downstream	RWS	Yes	FFFh
15:12	***Reserved***		RWS	Yes	0h
27:16	**Port Upper TLP Counter** When the Port TLP Counter is greater than or equal to this value, the Source Scheduler disables TLP scheduling to this egress Port.	Upstream	RWS	Yes	006h
		Downstream	RWS	Yes	FFFh
31:28	***Reserved***		RWS	Yes	0h

13.19.2 Device-Specific Registers – Ingress Control and Port Enable (Offsets F48h – F6Ch)

This section details the Device-Specific Ingress Control and Port Enable registers, which also include the **Negotiated Link Width** registers. Table 13-42 defines the register map.

Table 13-42. Device-Specific Ingress Control and Port Enable Register Map (Base mode – All Ports; Virtual Switch mode – VS Upstream Port(s))

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Ingress Port-Based Control		F48h
Port Enable Status		F4Ch
Reserved	Negotiated Link Width for Ports 0, 1, 2, 3	F50h
Reserved		F54h
Negotiated Link Width for Ports 16, 17, 18, 19, 20, 21, 22, 23		F58h
Reserved		F5Ch
Ingress Control		F60h
Reserved	F64h –	F6Ch

Register 13-236. F48h Ingress Port-Based Control (Base mode – All Ports; Virtual Switch mode – VS Upstream Port(s))

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
1:0	**ACK TLP Counter Timeout** Sets the number of ingress TLP Acknowledges (ACKs) pending, which causes a high-priority ACK to be sent. 00b = 16 TLPs 01b = 8 TLPs 10b = 4 TLPs 11b = Feature is disabled	RWS	Yes	00b
31:2	***Reserved***	RsvdP	No	0-0h

Register 13-237. F4Ch Port Enable Status (Base mode – All Ports; Virtual Switch mode – VS Upstream Port(s))

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
The value of this register depends upon the Port configuration for each Station – Station 0 (bits [3:0]), Station 4 (bits [19:16]), and Station 5 (bits [23:20]). When a Port is enabled in the corresponding Station configuration, the bit for that Port is Set; otherwise, the bit is Cleared. The following values indicate the Link width bit settings within each 4-bit grouping, for each Station: 0001b = x16 0011b = x8, x8 0111b = x8, x4, x4 1111b = x4, x4, x4, x4 ***Note:*** *Table 13-5 lists the Port configuration for each Station.*				
0	**Port 0 Enable Status** 0 = Port is disabled 1 = Port is enabled	RO	No	Set by STRAP_STN0_PORTCFG[1:0] ball levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 0* field (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 300h[1:0])
1	**Port 1 Enable Status** 0 = Port is disabled 1 = Port is enabled	RO	No	
2	**Port 2 Enable Status** 0 = Port is disabled 1 = Port is enabled	RO	No	
3	**Port 3 Enable Status** 0 = Port is disabled 1 = Port is enabled	RO	No	
15:4	***Reserved***	RsvdP	No	000h
16	**Port 16 Enable Status** 0 = Port is disabled 1 = Port is enabled	RO	No	Set by STRAP_STN4_PORTCFG[1:0] ball levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 4* field (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 300h[9:8])
17	**Port 17 Enable Status** 0 = Port is disabled 1 = Port is enabled	RO	No	
18	**Port 18 Enable Status** 0 = Port is disabled 1 = Port is enabled	RO	No	
19	**Port 19 Enable Status** 0 = Port is disabled 1 = Port is enabled	RO	No	

Register 13-237. F4Ch Port Enable Status (Base mode – All Ports; Virtual Switch mode – VS Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
20	**Port 20 Enable Status** 0 = Port is disabled 1 = Port is enabled	RO	No	Set by STRAP_STN5_PORTCFG[1:0] ball levels, or by serial EEPROM value for the **Port Configuration** register *Port Configuration for Station 5* field (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offset 300h[11:10])
21	**Port 21 Enable Status** 0 = Port is disabled 1 = Port is enabled	RO	No	
22	**Port 22 Enable Status** 0 = Port is disabled 1 = Port is enabled	RO	No	
23	**Port 23 Enable Status** 0 = Port is disabled 1 = Port is enabled	RO	No	
28:24	**VS Upstream Port Number** Indicates which Port is the upstream Port of this virtual switch. 0_0000b = Port 0 0_0001b = Port 1 0_0010b = Port 2 0_0011b = Port 3 1_0000b = Port 16 1_0001b = Port 17 1_0010b = Port 18 1_0011b = Port 19 1_0100b = Port 20 1_0101b = Port 21 1_0110b = Port 22 1_0111b = Port 23 All other encodings are ***reserved***.	RO	No	0_0000b
31:29	***Reserved***	RsvdP	No	000b

Register 13-238. F50h Negotiated Link Width for Ports 0, 1, 2, 3 (Base mode – All Ports; Virtual Switch mode – VS Upstream Port(s))

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
2:0	**Negotiated Link Width for Port 0** If the Link is down, the value is 000b. 000b = x1, or the Port is in the *DL_Down* state 001b = x2 010b = x4 011b = x8 100b = x16 All other encodings are ***reserved***.	RO	No	000b
3	**Link Speed for Port 0** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0
6:4	**Negotiated Link Width for Port 1** If the Link is down, the value is 000b. 000b = x1, or the Port is in the *DL_Down* state 001b = x2 010b = x4 011b = x8 All other encodings are ***reserved***.	RO	No	000b
7	**Valid Negotiated Link Width for Port 1** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0
10:8	**Negotiated Link Width for Port 2** If the Link is down, the value is 000b. 000b = x1, or the Port is in the *DL_Down* state 001b = x2 010b = x4 All other encodings are ***reserved***.	RO	No	000b
11	**Valid Negotiated Link Width for Port 2** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0
14:12	**Negotiated Link Width for Port 3** If the Link is down, the value is 000b. 000b = x1, or the Port is in the *DL_Down* state 001b = x2 010b = x4 All other encodings are ***reserved***.	RO	No	000b
15	**Valid Negotiated Link Width for Port 3** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0
31:16	***Reserved***	RsvdP	No	0000h

Register 13-239. F58h Negotiated Link Width for Ports 16, 17, 18, 19, 20, 21, 22, 23 (Base mode – All Ports; Virtual Switch mode – VS Upstream Port(s))

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
2:0	**Negotiated Link Width for Port 16** If the Link is down, the value is 000b. 000b = x1, or the Port is in the *DL_Down* state 001b = x2 010b = x4 011b = x8 100b = x16 All other encodings are ***reserved***.	RO	No	000b
3	**Link Speed for Port 16** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0
6:4	**Negotiated Link Width for Port 17** If the Link is down, the value is 000b. 000b = x1, or the Port is in the *DL_Down* state 001b = x2 010b = x4 011b = x8 All other encodings are ***reserved***.	RO	No	000b
7	**Valid Negotiated Link Width for Port 17** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0
10:8	**Negotiated Link Width for Port 18** If the Link is down, the value is 000b. 000b = x1, or the Port is in the *DL_Down* state 001b = x2 010b = x4 All other encodings are ***reserved***.	RO	No	000b
11	**Valid Negotiated Link Width for Port 18** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0
14:12	**Negotiated Link Width for Port 19** If the Link is down, the value is 000b. 000b = x1, or the Port is in the *DL_Down* state 001b = x2 010b = x4 All other encodings are ***reserved***.	RO	No	000b
15	**Valid Negotiated Link Width for Port 19** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0

Register 13-239. F58h Negotiated Link Width for Ports 16, 17, 18, 19, 20, 21, 22, 23 (Base mode – All Ports; Virtual Switch mode – VS Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
18:16	**Negotiated Link Width for Port 20** If the Link is down, the value is 000b. 000b = x1, or the Port is in the *DL_Down* state 001b = x2 010b = x4 011b = x8 100b = x16 All other encodings are ***reserved***.	RO	No	000b
19	**Link Speed for Port 20** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0
22:20	**Negotiated Link Width for Port 21** If the Link is down, the value is 000b. 000b = x1, or the Port is in the *DL_Down* state 001b = x2 010b = x4 011b = x8 All other encodings are ***reserved***.	RO	No	000b
23	**Valid Negotiated Link Width for Port 21** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0
26:24	**Negotiated Link Width for Port 22** If the Link is down, the value is 000b. 000b = x1, or the Port is in the *DL_Down* state 001b = x2 010b = x4 All other encodings are ***reserved***.	RO	No	000b
27	**Valid Negotiated Link Width for Port 22** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0
30:28	**Negotiated Link Width for Port 23** If the Link is down, the value is 000b. 000b = x1, or the Port is in the *DL_Down* state 001b = x2 010b = x4 All other encodings are ***reserved***.	RO	No	000b
31	**Valid Negotiated Link Width for Port 23** 0 = Negotiated Link SerDes speed is 2.5 GT/s 1 = Negotiated Link SerDes speed is 5.0 GT/s	RO	No	0

Register 13-240. F60h Ingress Control (Base mode – All Ports; Virtual Switch mode – VS Upstream Port(s))

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
3:0	***Factory Test Only***	RWS	Yes	2h
4	***Not used***	RsvdP	No	0
5	**Base Mode** **No Special Treatment for Relaxed Ordering Traffic** The PEX 8649 supports Relaxed Ordering for Completions. By default, if the RO attribute is Set within a Completion, then that Completion can bypass Posted transactions, if Posted TLPs are blocked at the egress Port (due to insufficient Posted credits from the connected device). This behavior can be disabled by Setting this bit, in each Port. 1 = Device-Specific Relaxed Ordering Completion will not be flagged to the Egress block	RWS	Yes	0
	Virtual Switch Mode ***Reserved***	RsvdP	No	0
6	***Reserved***	RsvdP	No	0
7	***Not used***	RsvdP	No	0
8	**Drop ECRC TLPs** Drop End-to-end Cyclic Redundancy Check (ECRC) TLPs. 1 = ECRC TLP was dropped	RWS	Yes	0
9	**Drop EP TLPs** Drop Endpoint TLPs. 1 = Endpoint TLP was dropped	RWS	Yes	0
10	***Factory Test Only***	RWS	Yes	0
12:11	***Not used***	RWS	Yes	00b
14:13	***Factory Test Only***	RWS	Yes	00b
15	**Disable Expansion ROM BAR** 1 = Expansion ROM always reads 0, making the Expansion ROM not present	RWS	Yes	0
23:16	***Not used***	RWS	Yes	00h

Register 13-240. F60h Ingress Control (Base mode – All Ports; Virtual Switch mode – VS Upstream Port(s)) *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
24	**Base Mode** **Limit NT Port Link Interface Memory Accesses to NT Port Link Interface** 0 = NT Port Link Interface is allowed access to all PEX 8649 registers. 1 = Limit NT Port Link Interface Memory accesses that target PEX 8649 accesses to only the NT Port Link Interface Memory-Mapped registers. All Memory accesses that target registers in other PEX 8649 Ports are No Operation – Write data is ignored, Read operation returns zeros.	RWS	Yes	0
	Virtual Switch Mode ***Reserved***	RsvdP	No	0
25	***Factory Test Only***	RWS	Yes	0
26	**Disable Upstream Port BAR0 and BAR1** Valid for the NT Port if the upstream Port is in Station 0 (Base mode only). 0 = Enables all upstream Port **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, Upstream Port(s), offsets 10h and 14h, respectively) 1 = Disables all upstream Port **BAR0** and **BAR1**	RWS	Yes	0
27	**Flag Unexpected Completion Error** 0 = Flag unexpected Completion errors for Completions that hit the PEX 8649's internal virtual PCI Bus space 1 = Silently drop unexpected Completion errors for Completions that hit the PEX 8649's internal virtual PCI Bus space	RWS	Yes	0
28	**Disable VGA BIOS Memory Access Decoding** Valid for the NT Port if the upstream Port is in Station 0 (Base mode only). 0 = Enables the **Bridge Control** register *VGA 16-Bit Decode Enable*, *VGA Enable*, and *ISA Enable* bits (offset 3Ch[20:18], respectively), and enables decoding of PC ROM shadow addresses C_0000h to C_FFFFh (packets destined to these addresses are blocked) 1 = Disables the **Bridge Control** register *VGA 16-Bit Decode Enable*, *VGA Enable*, and *ISA Enable* bits (offset 3Ch[20:18], respectively), and disables decoding of PC ROM shadow addresses C_0000h to C_FFFFh (packets destined to these addresses are ***not*** blocked)	RWS	Yes	1
30:29	***Factory Test Only***	RWS	Yes	00b
31	***Not used***	RWS	Yes	0

13.19.3 Device-Specific Registers – Error Checking and Debug (Offsets F70h – FB0h)

This section details the Device-Specific Error Checking and Debug registers located at offsets F70h through FB0h. Table 13-43 defines the register map.

Other Device-Specific Error Checking and Debug registers are detailed in:

- Section 13.15.7, "Device-Specific Registers – Error Checking and Debug (Offsets 320h – 350h)"
- Section 13.15.10, "Device-Specific Registers – Error Checking and Debug (Offsets 700h – 75Ch)"

Table 13-43. Device-Specific Error Checking and Debug Register Map (Offsets F70h – FB0h) (All Ports)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Power Management Hot Plug User Configuration	F70h
Reserved	F74h – FA4h
ACK Transmission Latency Limit	FA8h
Bad TLP Counter	FACh
Bad DLLP Counter	FB0h

Register 13-241. F70h Power Management Hot Plug User Configuration (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
0	**L0s Entry Idle Counter** Traffic Idle time to meet, to enter the L0s Link PM state. 0 = Idle condition must last 1 µs 1 = Idle condition must last 4 µs		RWS	Yes	0
1	***Factory Test Only***		RWS	Yes	0
2	***Not enabled*** Functionality associated with this bit is enabled only on the downstream Ports.	Upstream	RWS	Yes	0
	HPC PME Turn-Off Enable 1 = PME Turn-Off Message is transmitted before the Port is turned Off on a downstream Port	Downstream	RWS	Yes	0
4:3	***Not enabled*** Functionality associated with this field is enabled only on the downstream Ports.	Upstream	RWS	Yes	00b
	HPC T_{pepv} Hot Plug Port time from Power Enable to Power Valid. Indicates the delay from when HP_PWREN_*x* is asserted High, to when power is valid at a slot. (Refer to Section 10.7.1.2, “Slot Power-Up Sequencing When Power Controller Present Bit Is Set,” for details.) 00b = Feature is disabled, and HP_PWR_GOOD_*x* input is used for Power Valid 01b = 128 ms 10b = 256 ms 11b = 512 ms	Downstream	RWS	Yes	00b
5	***Factory Test Only***		RWS	Yes	0
6	***Not enabled*** Functionality associated with this bit is enabled only on the downstream Ports.	Upstream	RWS	Yes (Serial EEPROM only)	0
	HP_PWR_GOOD_*x* Active-Low Enable Controls the HP_PWR_GOOD_*x* input polarity. (Refer to Section 10.7.1.2, “Slot Power-Up Sequencing When Power Controller Present Bit Is Set,” for details.) 0 = HP_PWR_GOOD_*x* is Active-High 1 = HP_PWR_GOOD_*x* is Active-Low	Downstream	RWS	Yes (Serial EEPROM only)	0
7	***Factory Test Only***		RWS	Yes	0

Register 13-241. F70h Power Management Hot Plug User Configuration (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
8	**DLLP Timeout Link Retrain Disable** Disable Link retraining when no Data Link Layer Packets (DLLPs) are received for more than 256 µs. 0 = Enables Link retraining when no DLLPs are received for more than 256 µs (default) 1 = DLLP Timeout is disabled		RWS	Yes	0
9	***Factory Test Only***		RWS	Yes	0
10	**L0s Entry Disable** 0 = Enables entry into the L0s Link PM state on a Port when the L0s idle conditions are met 1 = Disables entry into the L0s Link PM state on a Port when the L0s idle conditions are met		RWS	Yes	0
11	***Factory Test Only***		RWS	Yes	0
12	**Software-Controlled Hot Plug Enable** 1 = Hot Plug input functionality is disabled and software controls the input functionality		RWS	Yes	0
13	**Software-Controlled Power Good** When bit 12 (*Software-Controlled Hot Plug Enable*) is Set, the value in this bit controls HP_PWR_GOOD_*x* input to the PEX 8649		RWS	Yes	0
14	**Upstream Hot Plug Enable** 1 = Enables Presence Detect and its corresponding interrupt on the upstream Port(s)		RWS	Yes	0
15	**Port Is Serial Hot Plug Port** 1 = Indicates the Port is a Serial Hot Plug Port, using I/O Expanders		RO	No	0
16	**HPC Serial Expansion Controller Disable** 0 = Enables Serial Hot Plug capability on all Ports 1 = Disables Serial Hot Plug capability on all Ports	0	RWS	Yes	0
	Not used	Otherwise	RsvdP	No	0
17	**40-Pin I/O Expander Scan Disable** 0 = 40-pin I/O Expander scan 1 = Disables 40-pin I/O Expander scan		RWS	Yes	0
18	**Serial Hot Plug INT*x* De-Bounce Disable** 1 = Disables the 10-ms De-Bounce Counter in the Serial Hot Plug Controller, for I/O Expander Interrupt inputs		RWS	Yes	0
19	**Serial Hot Plug Override Parallel Disable** 0 = Defaults to Serial Hot Plug when a Port is both Parallel and Serial Hot Plug-capable 1 = Selects Parallel Hot Plug if a Port is both Parallel and Serial Hot Plug-capable		RWS	Yes	0

Register 13-241. F70h Power Management Hot Plug User Configuration (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
20	**HPC I/O Reload** 1 = Parallel Hot Plug Controller/Serial Hot Plug Controller (I/O Expander) Output pin values are reloaded from field [26:21] (*HPC Output Reload Value*). After the action is complete, this bit is self-clearing.		RWS	Yes	0
26:21	**HPC Output Reload Value** When bit 20 (*HPC I/O Reload*) is Set, values from this field are re-loaded to the Hot Plug Controller outputs associated with the Port. Bit 21 = HP_PWRLED_*x*# or I/O Expander PWRLED# Bit 22 = HP_ATNLED_*x*# or I/O Expander ATNLED# Bit 23 = HP_PWREN_*x* or I/O Expander PWREN Bit 24 = HP_CLKEN_*x*# or I/O Expander RECLKEN# Bit 25 = HP_PERST_*x*# or I/O Expander PERST# Bit 26 = I/O Expander INTERLOCK		RWS	Yes	0-0h
27	**Software Present Detect State Value** Presence Detect State register. Value is Set from this register when bit 14 or 12 (*Upstream Hot Plug Enable* or *Software-Controlled Hot Plug Enable*, respectively) is Set.		RWS	Yes	0
28	**Software MRL State Value** Manually operated Retention Latch (MRL) Sensor State register. Value is Set from this register when bit 14 or 12 (*Upstream Hot Plug Enable* or *Software-Controlled Hot Plug Enable*, respectively) is Set.		RWS	Yes	0
31:29	***Factory Test Only***		RWS	Yes	000b

Register 13-242. FA8h ACK Transmission Latency Limit (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
The value of this register should be valid after Link negotiation.				

11:0	**ACK Transmission Latency Limit**
	Acknowledge Control Packet (ACK) Transmission Latency Limit.
	The value of this field changes, based upon the Negotiated Link Width (offset 78h[25:20]), Current Link Speed (offset 78h[19:16]) after the Link is up, and Maximum Payload Size (offset 70h[7:5]).
	x1 = 255d
	x2 = 217d
	x4 = 118d
	x8 = 107d
	x16 = 100d
		RWS	Yes	Set by STRAP_STN*x*_PORTCFG*x* ball levels

15:12	***Reserved***	RsvdP	No	0h
23:16	**Upper 8 Bits of the Replay Timer Limit** If the serial EEPROM is not present, the value of this register changes based upon the negotiated Link width after the Link is up. The value in this field is a multiplier of the default internal timer values that are compliant to the *PCI Express Base r2.0*. These bits should normally remain the default value, 00h.	RWS	Yes	00h
30:24	***Reserved***	RsvdP	No	0-0h
31	**ACK Transmission Latency Timer Status** Indicates the written status of field [11:0] (*ACK Transmission Latency Limit*). Once the register is written, either by software and/or serial EEPROM, this bit is Set and Cleared only by a Fundamental Reset.	RO	No	0

Register 13-243. FACh Bad TLP Counter (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**Bad TLP Counter** Counts the number of TLPs received with bad Link Cyclic Redundancy Check (LCRC), or number of TLPs with a Sequence Number Mismatch error. The Counter saturates at FFFF_FFFFh and does not roll over to 0000_0000h.	RWS	Yes	0000_0000h

Register 13-244. FB0h Bad DLLP Counter (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**Bad DLLP Counter** Counts the number of DLLPs received with bad LCRC, or number of DLLPs with a Sequence Number Mismatch error. The Counter saturates at FFFF_FFFFh and does not roll over to 0000_0000h.	RWS	Yes	0000_0000h

13.20 Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)

This section details the Advanced Error Reporting Extended Capability registers. Table 13-44 defines the register map.

Table 13-44. Advanced Error Reporting Extended Capability Register Map (All Ports)

31 30 29 28 27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (138h or 148h)		Capability Version (1h)	PCI Express Extended Capability ID (0001h)	FB4h
Reserved	Uncorrectable Error Status			FB8h
Reserved	Uncorrectable Error Mask			FBCh
Reserved	Uncorrectable Error Severity			FC0h
Reserved			Correctable Error Status	FC4h
Reserved			Correctable Error Mask	FC8h
Advanced Error Capabilities and Control				FCCh
Header Log 0				FD0h
Header Log 1				FD4h
Header Log 2				FD8h
Header Log 3				FDCh

Register 13-245. FB4h Advanced Error Reporting Extended Capability Header (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
15:0	**PCI Express Extended Capability ID**		RO	Yes	0001h
19:16	**Capability Version**		RO	Yes	1h
31:20	**Next Capability Offset** Program to 138h, which addresses the upstream Port **Power Budget Extended Capability** structure.	Upstream	RO	Yes	138h
	Program to 148h, which addresses the **Virtual Channel Extended Capability** structure.	Downstream	RO	Yes	148h

Register 13-246. FB8h Uncorrectable Error Status (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
Note: *The bits in this register can be masked by their respective* ***Uncorrectable Error Mask*** *register bits (offset FBCh).*					
3:0	***Reserved***		RsvdP	No	0h
4	**Data Link Protocol Error Status** 0 = No error is detected 1 = Error is detected		RW1CS[a]	Yes	0
5	***Reserved***	Upstream	RsvdP	No	0
	Surprise Down Error Status 0 = No error is detected 1 = Error is detected	Downstream	RW1CS[a]	Yes	0
11:6	***Reserved***		RsvdP	No	0-0h
12	**Poisoned TLP Status** 0 = No error is detected 1 = Error is detected		RW1CS[a]	Yes	0
13	**Flow Control Protocol Error Status** ***Reserved/Not supported***		RsvdP	No	0
14	**Completion Timeout Status** ***Not applicable to switches.***		RsvdP	No	0
15	**Completer Abort Status**		RW1CS[a]	Yes	0

Register 13-246. FB8h Uncorrectable Error Status (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
16	**Unexpected Completion Status** 0 = No error is detected 1 = Error is detected		RW1CS[a]	Yes	0
17	**Receiver Overflow Status** 0 = No error is detected 1 = Error is detected		RW1CS[a]	Yes	0
18	**Malformed TLP Status** 0 = No error is detected 1 = Error is detected		RW1CS[a]	Yes	0
19	**ECRC Error Status** 0 = No error is detected 1 = Error is detected		RW1CS[a]	Yes	0
20	**Unsupported Request Error Status** 0 = No error is detected 1 = Error is detected		RW1CS[a]	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	ACS Violation Error Status 0 = No violation is detected 1 = Violation is detected	Downstream	RW1CS[a]	Yes	0
22	**Uncorrectable Internal Error Status** 0 = No error is detected 1 = Error is detected	**Base Mode** 0, 16, 20 **Virtual Switch Mode** 0, 16, 20, accessible through the Management Port	RW1CS[a]	Yes	0
	Reserved	Otherwise	RsvdP	No	0
23	**MC Blocked TLP Status** Multicast blocked TLP status. 0 = No error is detected 1 = Error is detected		RW1CS[a]	Yes	0
31:24	***Reserved***		RsvdP	No	00h

[a] *When the* ***ECC Error Check Disable*** *register Software Force Error Enable bit (offset 720h[2]) is Set, Type changes from RW1CS to RW.*

Register 13-247. FBCh Uncorrectable Error Mask (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
Note: *The bits in this register can be used to mask their respective* ***Uncorrectable Error Status*** *register bits (offset FB8h).*					
3:0	***Reserved***		RsvdP	No	0h
4	**Data Link Protocol Error Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
5	***Reserved***	Upstream	RsvdP	No	0
	Surprise Down Error Mask 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error	Downstream	RWS	Yes	0
11:6	***Reserved***		RsvdP	No	0-0h
12	**Poisoned TLP Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
13	**Flow Control Protocol Error Mask** ***Reserved/Not supported***		RsvdP	No	0
14	**Completion Timeout Mask** ***Not applicable to switches.***		RsvdP	No	0
15	**Completer Abort Mask**		RWS	Yes	0

Register 13-247. FBCh Uncorrectable Error Mask (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^{2}C	Default
16	**Unexpected Completion Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
17	**Receiver Overflow Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
18	**Malformed TLP Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
19	**ECRC Error Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
20	**Unsupported Request Error Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
21	***Reserved***	Upstream	RsvdP	No	0
	ACS Violation Error Mask 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error	Downstream	RWS	Yes	0
22	**Uncorrectable Internal Error Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error	**Base Mode** 0, 16, 20 **Virtual Switch Mode** 0, 16, 20, accessible through the Management Port	RWS	Yes	1
	Reserved	Otherwise	RsvdP	No	1
23	**MC Blocked TLP Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
31:24	***Reserved***		RsvdP	No	00h

Register 13-248. FC0h Uncorrectable Error Severity (All Ports)

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
3:0	***Reserved***		RsvdP	No	0h
4	**Data Link Protocol Error Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal		RWS	Yes	1
5	**Surprise Down Error Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal	Upstream	RO	No	1
		Downstream	RWS	Yes	1
11:6	***Reserved***		RsvdP	No	0-0h
12	**Poisoned TLP Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0
13	**Flow Control Protocol Error Severity** ***Reserved/Not supported***		RsvdP	No	1
14	**Completion Timeout Severity** ***Not applicable to switches.*** Because the Status and Mask are both ***reserved*** for this bit, Severity can be ignored.		RsvdP	No	0
15	**Completer Abort Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0
16	**Unexpected Completion Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0
17	**Receiver Overflow Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal		RWS	Yes	1
18	**Malformed TLP Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal		RWS	Yes	1
19	**ECRC Error Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0

Register 13-248. FC0h Uncorrectable Error Severity (All Ports) *(Cont.)*

Bit(s)	Description	Ports	Type	Serial EEPROM and I^2C	Default
20	**Unsupported Request Error Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0
21	***Reserved***	Upstream	RsvdP	Yes	0
	ACS Violation Error Severity 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal	Downstream	RWS	Yes	0
22	**Uncorrectable Internal Error Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal	**Base Mode** 0, 16, 20 **Virtual Switch Mode** 0, 16, 20, accessible through the Management Port	RWS	Yes	1
	Reserved	Otherwise	RsvdP	No	1
23	**MC Blocked TLP Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal		RWS	Yes	0
31:24	***Reserved***		RsvdP	No	00h

Register 13-249. FC4h Correctable Error Status (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
Note: *The bits in this register can be masked by their respective* ***Correctable Error Mask*** *register bits (offset FC8h).*				
0	**Receiver Error Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
5:1	***Reserved***	RsvdP	No	0-0h
6	**Bad TLP Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
7	**Bad DLLP Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
8	**REPLAY NUM Rollover Status** Replay Number Rollover status. 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
11:9	***Reserved***	RsvdP	No	000b
12	**Replay Timer Timeout Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
13	**Advisory Non-Fatal Error Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
14	**Corrected Internal Error Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
15	**Header Log Overflow Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
31:16	***Reserved***	RsvdP	No	0000h

[a] *When the* ***ECC Error Check Disable*** *register Software Force Error Enable bit (offset 720h[2]) is Set, Type changes from RW1CS to RW.*

Register 13-250. FC8h Correctable Error Mask (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
Note: *The bits in this register can be used to mask their respective* ***Correctable Error Status*** *register bits (offset FC4h).*				
0	**Receiver Error Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
5:1	***Reserved***	RsvdP	No	0-0h
6	**Bad TLP Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
7	**Bad DLLP Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
8	**REPLAY NUM Rollover Mask** Replay Number Rollover mask. 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
11:9	***Reserved***	RsvdP	No	000b
12	**Replay Timer Timeout Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
13	**Advisory Non-Fatal Error Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	1
14	**Corrected Internal Error Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	1
15	**Header Log Overflow Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	1
31:16	***Reserved***	RsvdP	No	0000h

Register 13-251. FCCh Advanced Error Capabilities and Control (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4:0	**First Error Pointer** Identifies the bit position of the first error reported in the **Uncorrectable Error Status** register (offset FB8h).	ROS	No	1Fh
5	**ECRC Generation Capable** 0 = ECRC generation is not supported 1 = ECRC generation is supported, but must be enabled	RO	Yes	1
6	**ECRC Generation Enable** 0 = ECRC generation is disabled 1 = ECRC generation is enabled	RWS	Yes	0
7	**ECRC Check Capable** 0 = ECRC checking is not supported 1 = ECRC checking is supported, but must be enabled	RO	Yes	1
8	**ECRC Check Enable** 0 = ECRC checking is disabled 1 = ECRC checking is enabled	RWS	Yes	0
31:9	***Reserved***	RsvdP	No	0-0h

Register 13-252. FD0h Header Log 0 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
31:0	**TLP Header 0** First DWord Header. TLP Header associated with error.	ROS	Yes	0000_0000h

Register 13-253. FD4h Header Log 1 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
31:0	**TLP Header 1** Second DWord Header. TLP Header associated with error.	ROS	Yes	0000_0000h

Register 13-254. FD8h Header Log 2 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
31:0	**TLP Header 2** Third DWord Header. TLP Header associated with error.	ROS	Yes	0000_0000h

Register 13-255. FDCh Header Log 3 (All Ports)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
31:0	**TLP Header 3** Fourth DWord Header. TLP Header associated with error.	ROS	Yes	0000_0000h

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Chapter 14 Non-Transparent Bridging – Base Mode Only

14.1 Introduction

Note: *Check the latest design guides, application notes and errata list for Non-Transparent (NT) usage.*

The PEX 8649 supports NT bridge functionality (NT mode) in Base mode, which is used to implement High-Availability systems or Intelligent I/O modules using PCI Express technology. The following discusses the basic NT bridging concept, as it applies to a PCI Express system.

NT bridges allow systems to isolate Address spaces, by appearing as an endpoint to the Host. The NT bridge exposes a Type 0 CSR Header and forwards transactions from one domain to the other, using address translation. The NT bridge is used to connect two independent address/Host domains. The NT bridge includes **Doorbell** registers, for transmitting interrupts from one side of the bridge to the other. The bridge also includes **Scratchpad** registers, accessible from both domains for inter-Host communication. The PEX 8649, with a single Port configured to operate in NT mode, supports the Intelligent Adapter Mode system model. NT mode is enabled/disabled by the STRAP_NT_ENABLE# ball. The STRAP_VS_MODE[1:0] inputs must be Low for NT mode.

Note: *If STRAP_NT_ENABLE# is High and software enables NT mode by Setting the* ***VS0 Upstream*** *register NT Enable bit (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 360h[13]), this register Write must be preceded by a Write that programs the NT Port Virtual Interface* ***PCI Class Code*** *register (offset 08h) to the default value for NT mode, 068000h (Other Bridge Device).*

The following are PEX 8649 Non-Transparent Bridging (NTB) key elements:

- Device Type Identification
- NT Port Features
- Intelligent Adapter Mode
- NT Port Reset
- NT Port Memory-Mapped Base Address Registers
- Doorbell Registers
- Scratchpad Registers
- NT Base Address Registers
- Address Translation

14.1.1 Device Type Identification

Devices identify themselves by way of the Conventional PCI Configuration Space register (CSR) Header **PCI Class Code** register. A Transparent PCI-to-PCI bridge identifies itself as a PCI Class Code 060400h. An NT bridge identifies itself as “Other Bridge,” 068000h, with a Type 0 Header, which is consistent with the use of other NT bridges available in the industry.

The **PCI Express Capability** register includes a *Device/Port Type* field (offset 68h[23:20]). In this register, a Transparent bridge/switch Port identifies itself as an *upstream* or *downstream Port*, while an NT bridge/switch NT Port identifies itself as a *PCI Express endpoint*.

14.1.2 NT Port Features

- Maps PEX 8649 Configuration registers into either 32- or 64-bit Memory space
- Base Address registers (BARs)
  - Implements four 32-bit, two 32-bit and one 64-bit, or two 64-bit BARs
  - Supports BAR Size programming, through the **BAR*x* Setup** register(s)
  - Allows BARs to be individually disabled, including Memory-Mapped BARs
- Supports Direct Address Translation
  - 32-to-32-bit address conversion
  - 32-to-64-bit address conversion
  - 64-to-32-bit address conversion
  - 64-to-64-bit address conversion
  - Requester ID (Bus Number, Device Number, and Function Number) conversion across the NT bridge
- **Doorbell** registers
- **Scratchpad** registers
- Supports Requester ID and Completion ID translation
- NT Port Link Interface *DL_Active* state change generates interrupt to Local Host
- Supports Cursor mechanism
- Supports Expansion ROM on either NT Port interface
- Supports End-to-end Cyclic Redundancy Check (ECRC)
- Provides ability to Clear *No Snoop* Transaction Layer Packet (TLP) attribute (if enabled)
- Programmable upstream Port and NT Port for the enabling of High Availability systems (Failover and Redundant systems)
- Brings down the NT Port Link when the Local domain is down (if enabled)
- Supports Fencing mechanism
- Signals Device-Specific interrupt to the Local Host when the NT Port Link Interface detects TLP errors
- Signals Device-Specific interrupt to the Local Host when the NT Port Link Interface receives Error Messages (Safety bit-controllable)
- Disables NT Port Link Interface Hot Reset effect (enabled, by default)
- Supports Configuration Space access control
- Option to appear behind a PCI-to-PCI bridge (refer to STRAP_NT_P2P_EN# ball description)

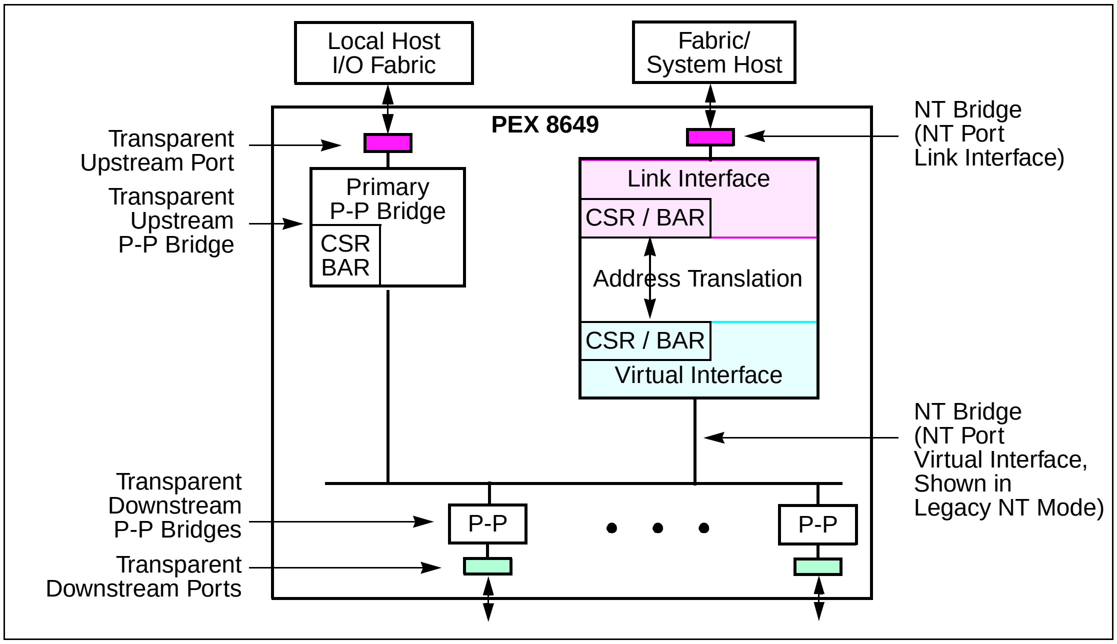
14.1.3 Intelligent Adapter Mode

The use of NT bridges in PCI systems is well-established for supporting intelligent adapters in enterprise and multi-Host systems. The same concept is used in PCI Express bridges and switches.

In Figure 14-1, there are two Type 0 CSR Headers in the NT bridge. The one nearer the internal virtual PCI Bus is referred to as the *Virtual Interface*. The one nearer the PCI Express Link is referred to as the *Link Interface*.

In Intelligent Adapter mode, the NT Port Link Interface is connected to the System Host domain. The System Host manages only the NT Port Link Interface Type 0 function. The Local Host manages all PEX 8649 Transparent Port Type 1 and NT Port Virtual Interface Type 0 functions. Cross-domain traffic is routed through an Address Translation mechanism. (Refer to Section 14.1.9.)

Figure 14-1. Intelligent Adapter Software Model



14.1.4 NT Port Reset

The section discusses NT mode exceptions and enhancements to Transparent mode PCI Express (standard) reset behavior.

14.1.4.1 Fundamental Reset (PEX_PERST#)

PEX_PERST# resets all PEX 8649 states, including NT Port states. This reset initializes all Sticky bits and Configuration registers in Virtual and Link spaces to default values.

14.1.4.2 Intelligent Adapter Mode NT Port Reset

When the Transparent upstream Port receives a Hot Reset or enters the *DL_Down* state, the PEX 8649, by default, propagates the in-band reset to all Transparent downstream Ports and connected downstream devices (to reset the downstream hierarchy), then resets the internal switch fabric and the NT Port Virtual Interface. There is no reset propagation to the NT Port Link Interface, and the Link-side remains intact.

When the NT Port Link Interface receives a Hot Reset or enters the *DL_Down* state, the NT Port Link Interface registers are reset, by default. This Soft Reset does not reset the Transparent Ports nor the NT Port Virtual Interface. Instead, when the NT Port Link Interface receives a Hot Reset (or enters the *DL_Down* state), the PEX_NT_RESET# output is asserted Low for 1 µs. The system can use this signal to trigger a reset of the entire Local subsystem.

The PEX 8649 supports an option that allows these Hot Reset conditions at its Transparent upstream Port and NT Port Link Interface to be masked (disabled) for all Ports, including the NT Port, by Setting the **Virtual Switch Debug** register *Upstream Port and NT-Link Port DL_Down Reset Propagation Disable* bit (Upstream Port, offset A30h[4]).

When software writes to the PEX 8649 upstream Port’s **Bridge Control** register *Secondary Bus Reset* bit (offset 3Ch[22]), the resulting Secondary Bus Reset is (as above) propagated to all PEX 8649 Transparent downstream Ports, and the Port states and NT Port Virtual Interface states are reset.

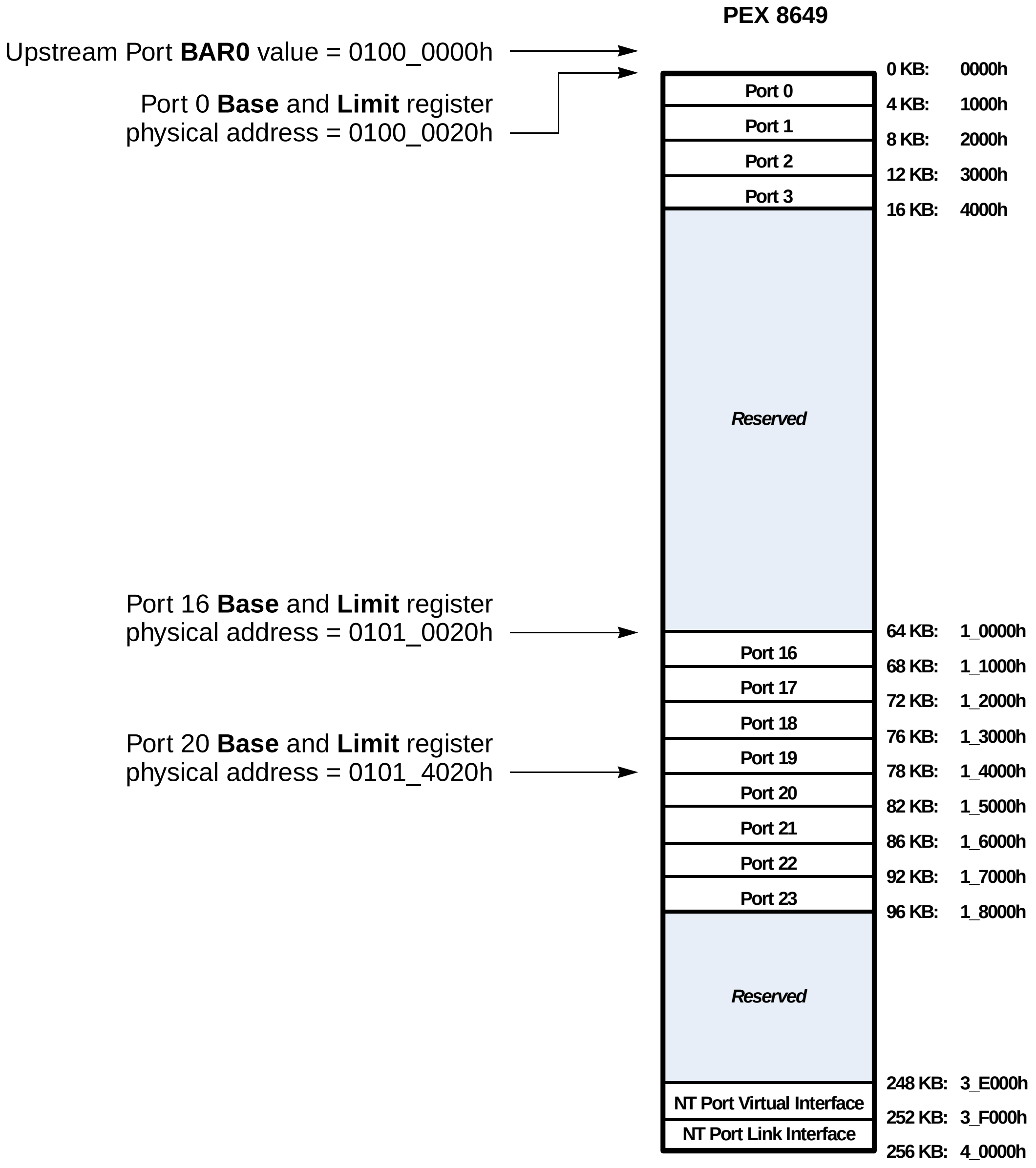
14.1.5 NT Port Memory-Mapped Base Address Registers

The NT Port Virtual and Link Interfaces individually claim 256 KB of memory, using **BAR0** and **BAR1**. The 256-KB space contains the Configuration Space registers for all PEX 8649 Ports. **BAR0** and **BAR1** can be programmed as one of the following:

- 32-bit BAR (**BAR1** is ***reserved***; default mode)
- 64-bit BAR, by programming the Configuration **BAR0/1 Setup** register (the NT Port Virtual offset is D0h; the NT Port Link Interface offset is E4h)
- **BAR0** and **BAR1** can be completely disabled

Figure 14-2 provides a memory-mapped view of the PEX 8649 Configuration Space registers. This view is the same from the upstream Port, NT Port Virtual Interface, or NT Port Link Interface.

Figure 14-2. NT Mode Configuration Register Mapping to Memory-Mapped BAR



14.1.6 Doorbell Registers

Doorbell registers are used to signal interrupts from one side of the NT bridge to the other. This section describes a typical set of Doorbell Control registers.

A 16-bit software-controlled Interrupt Request register and associated 16-bit Mask register are implemented for the NT Port Virtual and Link Interfaces. The Doorbell mechanisms consist of the following registers:

- **Virtual Interface IRQ Set**
- **Virtual Interface IRQ Clear**
- **Virtual Interface IRQ Mask Set**
- **Virtual Interface IRQ Mask Clear**
- **Link Interface IRQ Set**
- **Link Interface IRQ Clear**
- **Link Interface IRQ Mask Set**
- **Link Interface IRQ Mask Clear**

The Virtual Interface IRQ is for interrupts that exit the NT Port Virtual Interface. An interrupt is asserted on the NT Port Virtual Interface when one or more of the **Virtual Interface IRQ Set** register bits are Set by the NT Port Link Interface and their corresponding **Virtual Interface IRQ Mask Set** register bits are Cleared. An interrupt is de-asserted on the NT Port Virtual Interface when one or more of the **Virtual Interface IRQ Clear** register bits are Set from the NT Port Virtual Interface and their corresponding **Virtual Interface IRQ Mask Clear** register bits are Cleared. The interrupt is de-asserted when all Set bits are masked or Cleared.

The Link Interface IRQ is for interrupts that exit the NT Port Link Interface. An interrupt is asserted on the NT Port Link Interface when one or more of the **Link Interface IRQ Set** register bits are Set by the NT Port Virtual Interface and their corresponding **Link Interface IRQ Mask Set** register bits are Cleared. An interrupt is de-asserted on the NT Port Link Interface when one or more of the **Link Interface IRQ Clear** register bits are Set from the NT Port Link Interface and their corresponding **Link Interface IRQ Mask Clear** register bits are Cleared. The interrupt is de-asserted when all asserted bits are masked or Cleared.

Because Memory Requests can access both sets of NT-Virtual and NT-Link Doorbell registers, software in either domain can generate Doorbell interrupts to both domains.

Internally, the **Set IRQ** and **Clear IRQ** registers are the same register. One location is used to Set bits and the other is used to Clear bits. The status can be read from either register.

In a PCI Express switch, interrupt state transitions (from Setting to Clearing, or vice versa) result in packets being transmitted upstream on the appropriate side of the bridge when INT*x* is enabled (**PCI Command** register *Interrupt Disable* bit, offset 04h[10], is Cleared). Standard PCI Express Capability structures allow these interrupts to be configured as MSI or INT*x*. When MSIs are enabled (**MSI Control** register *MSI Enable* bit, offset 48h[16], is Set), packets are transmitted only when interrupts transition from Clear IRQ to Set IRQ.

NT Port Doorbell interrupts can optionally use the PEX_INTA# output for interrupt signaling, instead of the INT*x* or MSI signaling mechanisms. PEX_INTA# output can be enabled for NT Port Doorbell interrupts, by Setting the **ECC Error Check Disable** register *Enable PEX_INTA# Interrupt Output(s) for NT-Virtual Doorbell-Generated Interrupts* bit (offset 720h[7]).

The PEX 8649 Virtual interrupts are de-asserted when the NT Port goes to the *DL_Down* state.

14.1.7 Scratchpad Registers

Scratchpad registers are readable and writable from both sides of the NT bridge, providing a generic means for inter-Host communication. A block of eight registers are provided, accessible in Memory space from the NT Port Virtual and Link Interfaces. These registers pass Control and Status information between Virtual and Link Interface devices or they can be generic RW registers. Reading or writing **Scratchpad** registers does not cause interrupts to assert – **Doorbell** registers are used for that purpose. **Scratchpad** registers are reset only by a Fundamental Reset (PEX_PERST#).

14.1.8 NT Base Address Registers

There are two sets of NT Base Address registers (BARs) – one each for the NT Port Virtual and Link Interfaces. Each BAR has its own **Setup** and **Address Translation** register:

- **BAR*x* Setup** registers enable/disable the BAR and define the window size and type. Program the **BAR*x* Setup** registers prior to allowing configuration software to assign a resource for these BARs. (Discussed further in Section 14.1.8.1.)
- **Memory BAR*x* Address Translation** registers allow for an address change on the upper bits (up to the size of the space). Program the **Memory BAR*x* Address Translation** registers, before generating traffic across the NT Port. This programming is typically performed by information downloaded from I^{2}C, software, or an optional serial EEPROM (if present) on the destination side. The source side does not need to know what the Address Translation is.
- The address could change size. *For example*, the PEX 8649 NT Port allows a 32-bit device to communicate to a 64-bit device, and vice versa. (The same is true when the addresses are the same size, as well – a 32-bit device can communicate with a 32-bit device, and a 64-bit can communicate with a 64-bit device.)

14.1.8.1 NT BAR*x* Setup Registers

All NT Port Virtual and Link Interface BARs include programmable window sizes, with the exception of **BAR0** and **BAR1** (on both interfaces), which provide Memory-Mapped access to the CSRs. The **BAR*x* Setup** registers are used to program the window size of each BAR. Table 14-1 briefly describes each NT Port BAR. **BAR2**, **BAR3**, **BAR4**, and **BAR5** can be configured for accessing the Address space across the NT Port Virtual and Link Interfaces.

Each **BAR*x* Setup** register defines the size of the memory window to be assigned by a system enumerator (*that is*, BIOS or firmware). *For example*, if the size of the window needs to be 1 MB, Memory space, and cacheable region, the **BAR*x* Setup** register in 32-bit space will be FFF0_0008h (FFF0_0000h indicates the 1-MB space Request, bit 3 is the cacheable region, and bit 0 must be Memory space).

In a standard case, the **BAR*x* Setup** registers must be programmed using the serial EEPROM, before the BIOS or firmware allocates the resources (because enumeration of the resources is done before the system software can access these devices).

Table 14-1. NT Port Virtual and Link Interface BARs

BAR	NT Port Virtual Interface Description	NT Port Link Interface Description
BAR0	All PEX 8649 Port Configuration registers are mapped into Memory space, using **BAR0** and **BAR1**. The Local Host, connected to the Transparent upstream Port, can use the Transparent upstream Port **BAR0**/**1** or NT Port Virtual Interface **BAR0/1** to access the PEX 8649 Port Configuration registers. The **NT Port Virtual Interface BAR0/1 Setup** register controls the **BAR0** and **BAR1** implementation, as follows: • Disables **BAR0** and **BAR1** • Enables **BAR0** and disables **BAR1** (**BAR0** is a 32-bit BAR) • Enables **BAR0** and **BAR1** (**BAR0/1** is a 64-bit BAR) **BAR0** and **BAR1** claim 256-KB Memory space to the system.	All PEX 8649 Port Configuration registers are mapped into Memory space, using **BAR0** and **BAR1**. The System Host, connected to the NT Port, can use **BAR0**/**1** to access the PEX 8649 Port Configuration registers. The **NT Port Link Interface BAR0/1 Setup** register controls the **BAR0** and **BAR1** implementation, as follows: • Disables **BAR0** and **BAR1** • Enables **BAR0** and disables **BAR1** (**BAR0** is a 32-bit BAR) • Enables **BAR0** and **BAR1** (**BAR0/1** is a 64-bit BAR) **BAR0** and **BAR1** claim 256-KB Memory space to the system.
BAR1	Configured by the **NT Port Virtual Interface BAR0/1 Setup** register. **BAR1** is implemented as an upper 32-bit address of the NT Port Virtual Interface memory-mapped 64-bit BAR; otherwise, it is ***reserved***.	Configured by the **NT Port Link Interface BAR0/1 Setup** register. **BAR1** is implemented as an upper 32-bit address of the NT Port Link Interface memory-mapped 64-bit BAR; otherwise, it is ***reserved***.
BAR2	Configured by the **NT Port Virtual Interface Memory BAR2 Setup** register. **BAR2** can be implemented as a 32-bit BAR or lower half of a 64-bit BAR, by combining it with **BAR3** (**BAR2**/**3**). **BAR2** uses Direct Address Translation.	Configured by the **NT Port Link Interface Memory BAR2 Setup** register. **BAR2** can be implemented as a 32-bit BAR or lower half of a 64-bit BAR, by combining it with **BAR3** (**BAR2**/**3**). **BAR2** uses Direct Address Translation.
BAR3	Configured by the **NT Port Virtual Interface Memory BAR2/3 Setup** register. **BAR3** can be implemented as a 32-bit BAR or upper half of a 64-bit BAR, by combining it with **BAR2** (**BAR2**/**3**). **BAR3** uses Direct Address Translation.	Configured by the **NT Port Link Interface Memory BAR2/3 Setup** register. **BAR3** can be implemented as a 32-bit BAR or upper half of a 64-bit BAR, by combining it with **BAR2** (**BAR2**/**3**). **BAR3** uses Direct Address Translation.
BAR4	Configured by the **NT Port Virtual Interface Memory BAR4 Setup** register. **BAR4** can be implemented as a 32-bit BAR or lower half of a 64-bit BAR, by combining it with **BAR5** (**BAR4**/**5**). **BAR4** uses Direct Address Translation.	Configured by the **NT Port Link Interface Memory BAR4 Setup** register. **BAR4** can be implemented as a 32-bit BAR or lower half of a 64-bit BAR, by combining it with **BAR5** (**BAR4**/**5**). **BAR4** uses Direct Address Translation.
BAR5	Configured by the **NT Port Virtual Interface Memory BAR4/5 Setup** register. **BAR5** can be implemented as a 32-bit BAR or upper half of a 64-bit BAR, by combining it with **BAR4** (**BAR4**/**5**). **BAR5** uses Direct Address Translation.	Configured by the **NT Port Link Interface Memory BAR4/5 Setup** register. **BAR5** can be implemented as a 32-bit BAR or upper half of a 64-bit BAR, by combining it with **BAR4** (**BAR4**/**5**). **BAR5** uses Direct Address Translation.

14.1.9 Address Translation

The Transparent bridge uses **Base** and **Limit** registers in I/O space, Non-Prefetchable Memory space, and Prefetchable Memory space to map transactions downstream, across the bridge. All downstream devices must be mapped in contiguous address regions, such that a single Address range in each space is sufficient. Upstream mapping is done by way of inverse decode, relative to the same registers. A Transparent bridge does not translate the addresses of forwarded transactions/packets.

In multi-domain systems, each Host domain has its own Address space, that is different from that of other Host domain(s). Hence, any transaction crossing the inter-domain by way of NT, or other means, must support address translations as well as Requester ID translations.

Before a transaction (PCI Express packet) can go through the NT bridge (either from the Virtual-side to Link-side, or from Link-side to Virtual-side) in an inter-domain system, one or more sets of Memory resources must be assigned to the NT bridge. To request this resource from the system enumerator (BIOS or firmware), the NT bridge must be programmed with the **BAR*x* Setup** register(s). (Refer to Section 14.1.8.1.) The **BAR*x* Setup** register(s) requests the size of the window space, memory type, 32- or 64-bit space, prefetchable or non-prefetchable area and so forth. using one 32-bit register for 32-bit space or 2x the 32-bit register for 64-bit space. In return, the system enumerator assigns resources to the NT bridge in **BAR0** through **BAR5**. Any transactions that target **BAR2** through **BAR5** on the NT Port Link Interface result in a transaction across the NT bridge, to the secondary address domain.

Similarly, in NT PCI-to-PCI Bridge mode, the NT PCI-to-PCI bridge must be enumerated to accommodate the resources assigned to the NT endpoint, to allow packets to logically traverse the bridge. Its Device Number (on the Internal Virtual PCI Bus) value is the Port Number of the NT Port. Device enumeration minimally includes the **PCI Command**, **Bus Number**, and **Memory Base and Limit** and/or **Prefetchable Memory Base and Limit** registers (offsets 04h, 18h, and 20h, and/or 24h). The Internal NT Virtual Bus (connecting the NT PCI-to-PCI secondary interface and the NT endpoint) can be assigned any available Bus Number within the upstream Port’s range of Subordinate Bus Numbers.

In addition, the Lookup Table (LUT) register(s) and **Memory BAR*x* Address Translation** register(s) must be programmed. The LUTs are the Requester ID (Bus Number, Device Number, and Function Number) with the ability to disable features that allow Requester’s transaction go through the NT bridge (if enabled). This adds security to the NT bridge, limiting the devices that can generate transactions across the NT bridge. LUTs also play a crucial role, because the Requester ID is also used to complete PCI Express Read Requests – during the PCI Express Read Request to the other domain side, the NT bridge uses its own Requester ID to translate the original PCI Read Request, and when the Completion returns, the NT bridge uses the original Requester ID to complete the transaction.

The Address Translation is used to re-direct the address of the PCI Express packet to a programmer-reserved area (instead of using the same address for both Host domains). Hence, any transaction targeting **BAR2** through **BAR5** can be translated (re-mapped) on the other side of the NT bridge while maintaining the offsets. These Translation registers can be changed during runtime, as long as there are no pending transactions.

The PEX 8649 NT Port Virtual and Link Interfaces support Direct Address Translation, described in the following section.

14.1.9.1 Direct Address Translation

The **BAR*x* Setup** registers define a mask that splits the address into an upper *Base* field and a lower *Offset* field. Translation then consists of replacing, under the maskable portion of the **BAR*x* Setup** register, the Address Base register bits with the corresponding Address Translation register bits. Accordingly, the Address Translation register value must be a multiple of the size of the corresponding BAR. Figure 14-3 illustrates Direct Address Translation.

The device(s) on the originating Host domain can communicate to a single device or multiple devices mapped to consecutive Memory Address space on the Target Host domain, by using the Direct Address Translation mechanism. Figure 14-4 illustrates the entire Address map, claimed by the NT Port, mapped into the single target device. Figure 14-5 illustrates the entire Address map claimed by the NT Port, mapped into multiple target devices. Multiple devices must be in contiguous Memory ranges.

Figure 14-3. Direct Address Translation

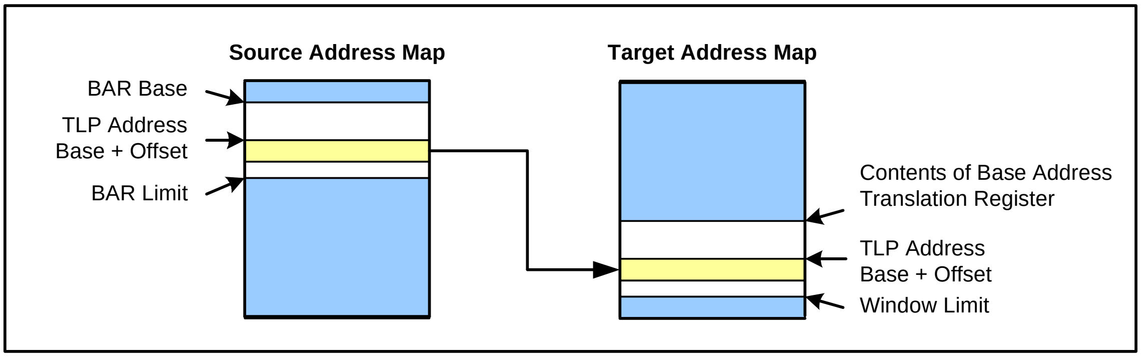


Figure 14-4. NT Port Mapped into Single Target Device

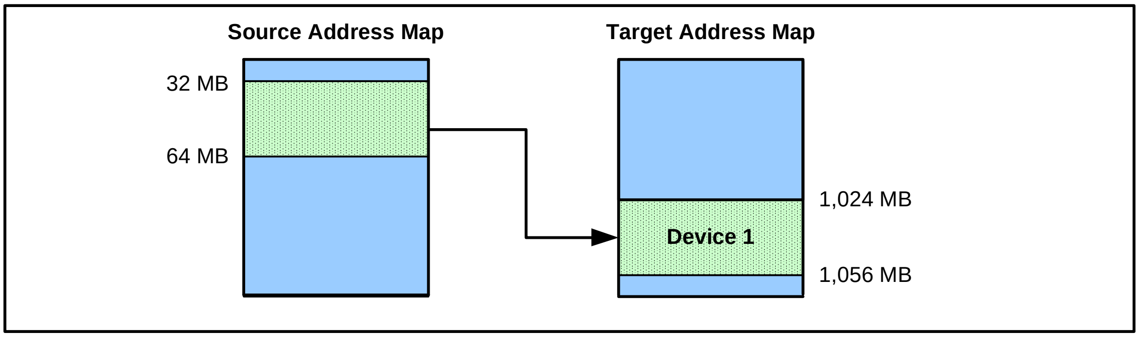
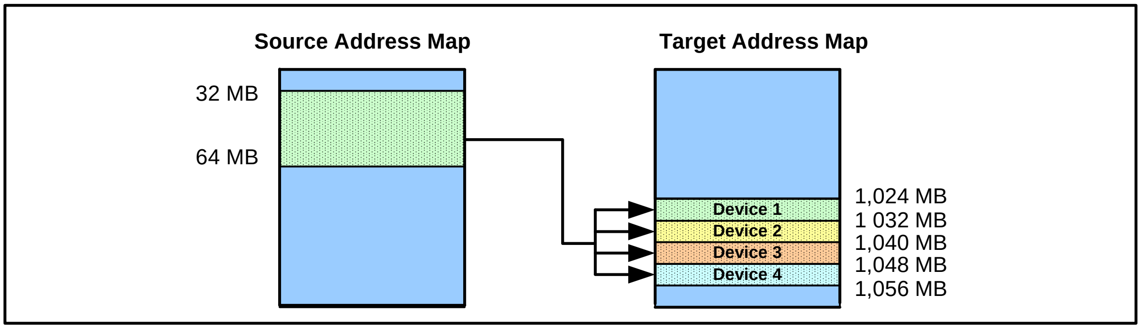


Figure 14-5. NT Port Mapped into Multiple Target Devices



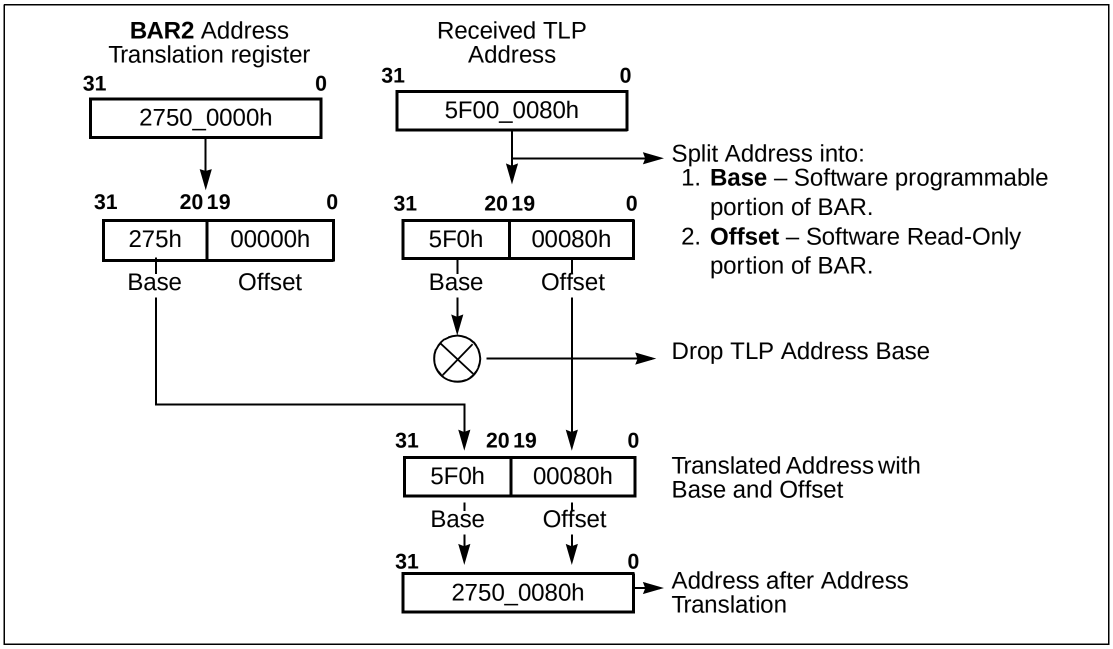
Address Translation Example

Assume the following:

1. NT Port Virtual Interface **BAR2** claims 1-MB Memory space (**BAR2 Setup** register = FFF0_0000h).
2. Configuration software assigns the 5F00_0000h address value to NT Port Virtual Interface **BAR2** and it is within the Transparent upstream Port Memory window.
3. Device driver software programs the **BAR2** Address Translation register to 2750_0000h.

The PEX 8649 receives a transaction to the NT Port Virtual Interface, with address 5F00_0080h. The received transaction address is hitting the NT Port Virtual Interface **BAR2**. The PEX 8649 claims the transaction and executes the address translation described in Figure 14-6.

Figure 14-6. Address Translation Example


BAR2 Address Translation register
31
0
2750_0000h
31
20
19
0
275h
00000h
Base
Offset
Received TLP Address
31
0
5F00_0080h
31
20
19
0
5F0h
00080h
Base
Offset
Split Address into:
1. **Base** – Software programmable portion of BAR.
2. **Offset** – Software Read-Only portion of BAR.
Drop TLP Address Base
31
20
19
0
5F0h
00080h
Base
Offset
Translated Address with Base and Offset
31
0
2750_0080h
Address after Address Translation

14.2 NT PCI-to-PCI Bridge Mode

The PEX 8649 provides an option to insert a PCI-to-PCI bridge (NT PCI-to-PCI bridge) between the NT Port Virtual Interface and internal virtual PCI Bus. Without the NT PCI-to-PCI bridge, the NT Port is parallel to other Transparent downstream bridges within the device hierarchy. This mode is referred to as *Legacy NT mode*. (Refer to Figure 14-7.) With the NT PCI-to-PCI bridge, the NT Port Virtual Interface is connected under one of the downstream bridges. (Refer to Figure 14-8.)

The NT PCI-to-PCI bridge is not connected to a physical Link; therefore, there are some minor differences in the Configuration registers, particularly in some Link control functionality. Insertion of the NT PCI-to-PCI bridge does not affect packet latency, and is controlled by the STRAP_NT_P2P_EN# input, when NT mode is enabled.

Figure 14-7. Legacy NT Mode (STRAP_NT_P2P_EN#=H)

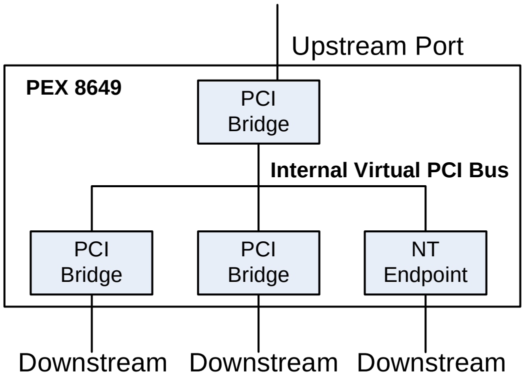
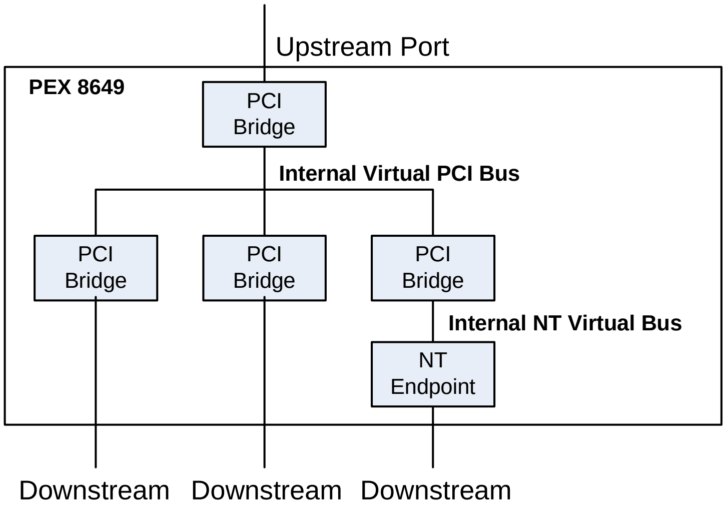


Figure 14-8. NT PCI-to-PCI Bridge Mode (STRAP_NT_P2P_EN#=L)



14.3 Requester ID Translation

Configuration, Message, and Completion transactions are ID-routed instead of address-routed. Of these, the NT Port forwards only the Completion transaction between the two Host domains. PCI Express switches and bridges use the Requester ID (defined in the Completion TLP Header) to route these packets.

The Requester ID consists of the following:

- Requester's PCI Bus Number
- Device Number
- Function Number

The Completer ID consists of the following:

- Completer's PCI Bus Number
- Device Number
- Function Number

Note: *The PCI Bus Number is unique for each Host domain.*

Figure 14-9 illustrates the Memory Request TLP Header format. Figure 14-10 illustrates the Completion TLP Header format.

Figure 14-9. Memory Request TLP Header Format

<table>
<tr><td></td><td colspan="8">Byte 0</td><td colspan="8">Byte 1</td><td colspan="8">Byte 2</td><td colspan="8">Byte 3</td></tr>
<tr><td></td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Bytes 0-3</td><td>R</td><td colspan="2">Fmtx1</td><td colspan="5">Type</td><td>R</td><td colspan="3">TC</td><td colspan="4">R</td><td>TD</td><td>EP</td><td colspan="2">Attr</td><td colspan="2">R</td><td colspan="10">Length</td></tr>
<tr><td>Bytes 4-7</td><td colspan="16">Requester ID</td><td colspan="8">Tag</td><td colspan="4">Last DW BE</td><td colspan="4">1st DW BE</td></tr>
<tr><td>Bytes 8-11</td><td colspan="32">Address[63:32]</td></tr>
<tr><td>Bytes 12-15</td><td colspan="30">Address[31:0]</td><td colspan="2">R</td></tr>
</table>

Figure 14-10. Completion TLP Header Format

<table>
<tr><td></td><td colspan="8">Byte 0</td><td colspan="8">Byte 1</td><td colspan="8">Byte 2</td><td colspan="8">Byte 3</td></tr>
<tr><td></td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Bytes 0-3</td><td>R</td><td colspan="2">Fmt</td><td colspan="5">Type</td><td>R</td><td colspan="3">TC</td><td colspan="4">R</td><td>TD</td><td>EP</td><td colspan="2">Attr</td><td colspan="2">R</td><td colspan="10">Length</td></tr>
<tr><td>Bytes 4-7</td><td colspan="16">Completer ID</td><td colspan="3">Completer Status</td><td>BCM</td><td colspan="12">Byte Count</td></tr>
<tr><td>Bytes 8-11</td><td colspan="16">Requester ID</td><td colspan="8">Tag</td><td>R</td><td colspan="7">Lower Address</td></tr>
</table>

14.3.1 Transaction Sequence

To implement a transaction sequence:

1. Requester inserts ID information into the Memory Read TLP that it generates on the initiating Host domain.
2. Switches and bridges between the transaction initiator and PEX 8649 NT Port route this Memory Read TLP, based upon the address.
3. NT Port replaces the Memory Read TLP Requester ID with its ID, and conducts the address translation before it forwards this Requester ID-translated TLP to the target Host domain, because the NT Port is the transaction initiator in the target Host domain.
4. Switches and bridges between the PEX 8649 NT Port and target device route this Memory Read TLP, based upon the address.
5. When the target device generates the Completion TLP, it copies the Memory Read TLP Requester ID into the corresponding Completion *TLP Requester ID* field and inserts its ID into the *TLP Completer ID* field.
6. Switches and bridges between the target device and PEX 8649 NT Port route the Completion TLP, based upon Requester ID (in this case, NT Bridge ID) information.
7. NT Port restores the original Requester ID value from the Configuration register and implements another Requester ID and Completer ID translation for the Completion TLP, before it forwards the Completion TLP to the Requester Host domain.
8. Switches and bridges between the PEX 8649 NT Port and Requester route the Completion TLP, based upon the Requester ID.
9. Requester accepts and processes the Completion TLP.

14.3.2 Transaction Originating in Local Host Domain

The translation of outgoing Requests from the NT Port Virtual Interface to the NT Port Link Interface uses an 8- or 32-entry LUT, as discussed in Section 15.15.1, “NT Port Virtual Interface NT Bridging-Specific Registers – Requester ID Translation Lookup Table Entry (Addresses D94h – DD0h).” Each LUT entry supports all outgoing Requests and any number of outstanding Requests made by a single device or function. If a device uses Phantom Function Numbers to increase the maximum number of outstanding transactions, each phantom function consumes an LUT entry. Configure the LUT by a serial EEPROM, I^2C, or local firmware, so it is possible to transmit Requests to the system domain, which provides a measure of security and protection.

When a Memory Request arrives at the NT Port Virtual Interface, the packet Requester ID is associated with this LUT. If it attains one of the enabled LUT entries, the corresponding entry address (TxIndex) is inserted into the *Function Number* field of the packet’s Requester ID. Conversely, if it does not match one of the enabled LUT entries, an Unsupported Request (UR) Completion is returned.

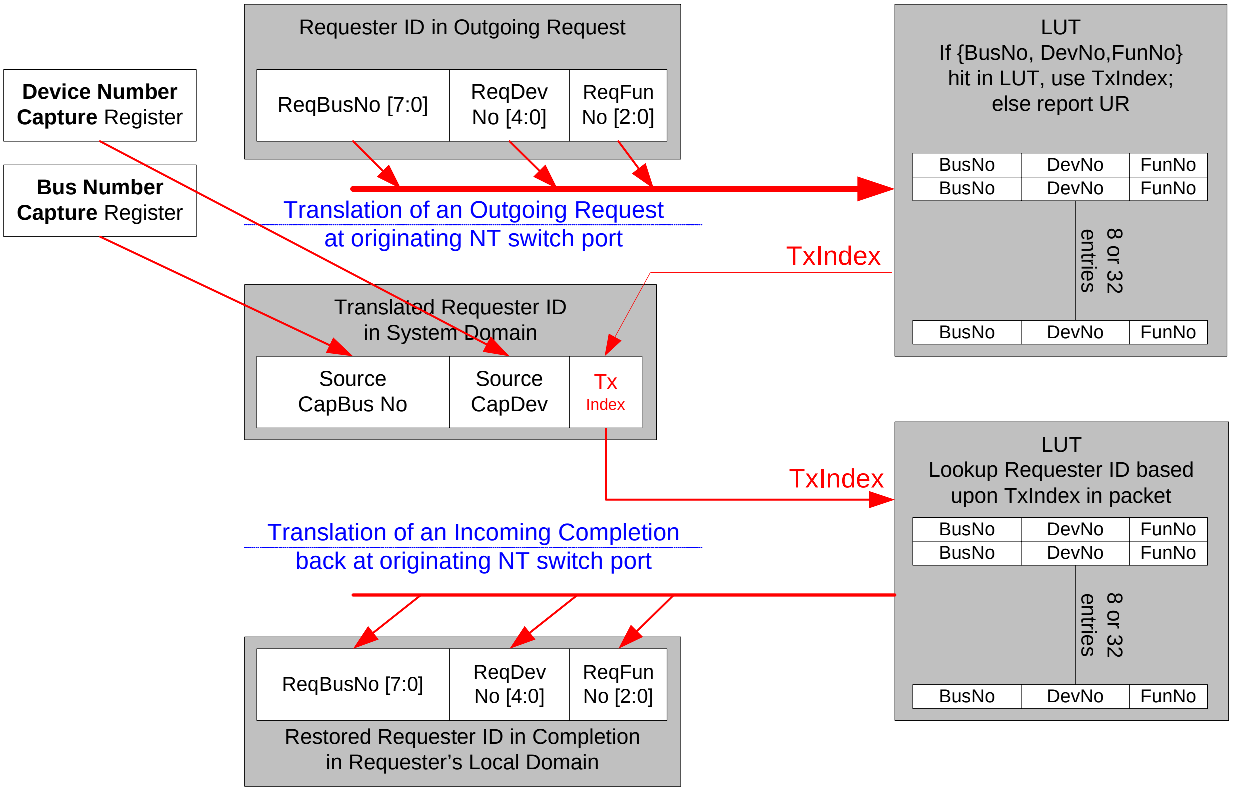
At the same time, the contents of the NT Port Link Interface **NT Captured Bus Number** and **NT Captured Device Number** registers (offsets 1DCh[7:0] and 1E0h[7:0], respectively) (the values used during the last CSR Write to the Port) are copied into the packet Requester ID’s *Bus Number* and *Device Number* fields.

A Completion, with translated Requester ID, returned from the system domain to the PEX 8649, is recognized when its Requester ID Bus Number and Device Number match the NT Port Link Interface captured Bus Number and Device Number. (Refer to Figure 14-11.)

When the original Requester ID is restored, the following occurs:

1. TxIndex is retrieved from the *Function Number* field of the Completion TLP Requester ID.
2. TxIndex is used to look up the same 8- or 32-entry LUT, to restore the original Requester ID.
3. If the selected entry is valid, the restored Requester ID is placed into the Completion *TLP Requester* field; otherwise, an Unexpected Completion is reported.
4. Completion *TLP Completer ID* field is replaced by the NT Port Virtual Interface captured Bus Number, Device Number, and Function Number.
5. Translated Completion TLP is forwarded to the original Requester, in the Local Host domain.

Figure 14-11. Requester ID Translation for Request Originating in Local Host Domain


Device Number Capture Register
Bus Number Capture Register
Requester ID in Outgoing Request
ReqBusNo [7:0]
ReqDev No [4:0]
ReqFun No [2:0]
Translation of an Outgoing Request at originating NT switch port
LUT
If {BusNo, DevNo,FunNo} hit in LUT, use TxIndex; else report UR
BusNo
DevNo
FunNo
8 or 32 entries
TxIndex
Translated Requester ID in System Domain
Source CapBus No
Source CapDev
Tx Index
TxIndex
LUT
Lookup Requester ID based upon TxIndex in packet
BusNo
DevNo
FunNo
8 or 32 entries
Translation of an Incoming Completion back at originating NT switch port
ReqBusNo [7:0]
ReqDev No [4:0]
ReqFun No [2:0]
Restored Requester ID in Completion in Requester's Local Domain

14.3.3 Transaction Originating in System Host Domain

Transactions originating in the System Host domain use a Receive LUT, with 32 entries, as discussed in Section 16.15.1, "NT Bridging-Specific Registers – Requester ID Translation Lookup Table Entry (Offsets DB4h – DF0h)." This data structure supports up to 32 devices (elsewhere in the system domain) that are transmitting Requests through the associated NT Port. Because the Function Number is not used in the LUT association, a separate LUT entry is not required for each requesting or phantom function device. Configure the LUT before transmitting Requests through the NT Port. This Requester registration process, which cannot be accomplished by a peer, is an effective security and protection mechanism.

When a Request is received from the system domain and routed to the NT Port, its Requester ID is translated again – Bus Number and Device Number, but not Function Number. The received Memory Request TLP Requester ID is associated with this LUT, and the address (RxIndex) of the corresponding matching entry is substituted into the *Device Number* field of the Memory Request's TLP *Requester ID* field.

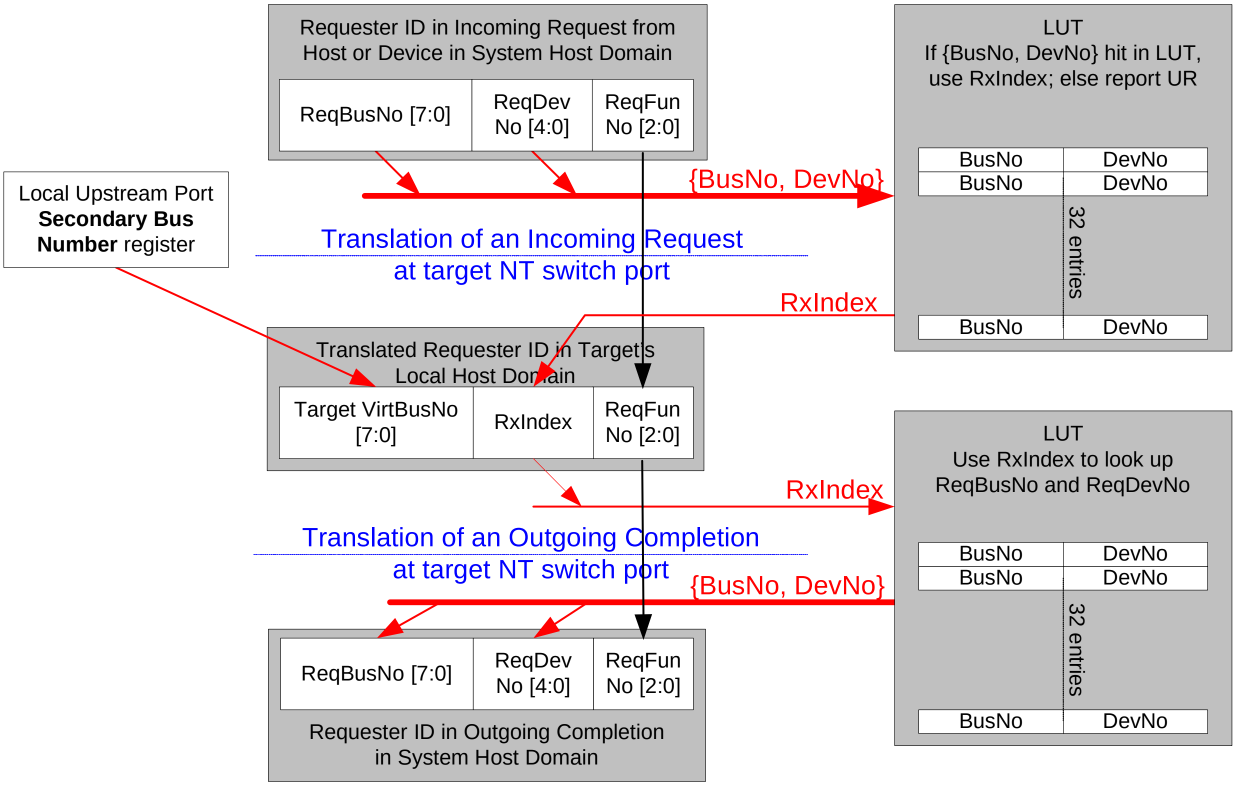
If no match is found, or the matched entry is not enabled, the Request receives a UR response. If a match is found, and matched entry is enabled, the PEX 8649 internal virtual PCI Bus Number is copied into the packet Requester ID's *Bus Number* field. The translated Memory Request TLP is address-translated and forwarded into the Local Host domain.

The PEX 8649 internal virtual PCI Bus Number is sufficient to route the Completion from the Completer back to the NT Port in the Completer's domain, because the NT Port is the only possible Requester on the switch internal virtual PCI Bus. Elsewhere in the PCI Express hierarchy, the Bus Number is sufficient to route the Completion back into the switch containing the NT Port.

The inverse translation occurs when a Completion passes through the NT bridge from the local domain to the system domain. The RxIndex is retrieved from the *Device Number* field of the received Completion *TLP Requester ID* header field, and used to look up the 32-entry LUT. The Completion TLP *Requester ID*, *Bus Number*, and *Device Number* fields are replaced by the decoded LUT-entry Bus Number and Device Number values, if the entry is valid; otherwise, an Unexpected Completion is reported.

The Completion TLP Completer ID is replaced by the NT Port Link Interface captured Bus Number, Device Number, and Function Number values before forwarding the Completion TLP to the System Host domain. (Refer to Figure 14-12.)

Figure 14-12. Requester ID Translation for Request Originating in System Host Domain


Requester ID in Incoming Request from
Host or Device in System Host Domain
ReqBusNo [7:0]
ReqDev No [4:0]
ReqFun No [2:0]
LUT
If {BusNo, DevNo} hit in LUT, use RxIndex; else report UR
BusNo
DevNo
BusNo
DevNo
32 entries
BusNo
DevNo
{BusNo, DevNo}
Local Upstream Port Secondary Bus Number register
Translation of an Incoming Request at target NT switch port
RxIndex
Translated Requester ID in Target's Local Host Domain
Target VirtBusNo [7:0]
RxIndex
ReqFun No [2:0]
LUT
Use RxIndex to look up ReqBusNo and ReqDevNo
RxIndex
Translation of an Outgoing Completion at target NT switch port
BusNo
DevNo
BusNo
DevNo
32 entries
BusNo
DevNo
{BusNo, DevNo}
ReqBusNo [7:0]
ReqDev No [4:0]
ReqFun No [2:0]
Requester ID in Outgoing Completion in System Host Domain

14.4 NT Port Power Management Handling

14.4.1 Active State Power Management

The PEX 8649 NT Port Link Interface endpoint supports the ASPM L0s and L1 Link Power Management (PM) states. The PEX 8649 NT Port Virtual Interface endpoint implements the Configuration Space registers for ASPM support. However, it does not enter into the low-power states, because there is no physical link associated with it.

14.4.2 PCI-PM and PME Turn Off Support

When NT mode is enabled, the NT Port Link Interface Type 0 Endpoint behaves as any other endpoints in the PCI Express PCI-PM D3hot Device PM state. Once in the D3hot Device PM state, the PEX 8649 NT Port Link Interface Type 0 Endpoint requests PCI-PM L1 Link PM state entry and finally settles in the L1 Link PM state. Only Configuration accesses and Messages to the NT Port Link Interface Type 0 Endpoint are supported in the D3hot Device PM state. The Root Complex transmits PME_Turn_Off Messages when the NT Host decides to turn Off the main power and Reference Clock. The PEX 8649 NT Port Link Interface Type 0 Endpoint indicates its readiness to lose power, by transmitting a PME_TO_Ack Message toward the upstream device. The PME_TO_Ack Message is transmitted when there are no pending TLPs to transmit upstream, toward the NT Port Link Interface. The Port requests the L2/L3 Ready Link PM state, by transmitting PM_Enter_L23 Data Link Layer Packets (DLLPs) to the upstream device after transmitting a PME_TO_Ack TLP. The Port settles into the L3 Link PM state when the Power Controller removes the main power and Reference Clock.

When the PME_Turn_Off Message is received on the PEX 8649 Transparent upstream Port, the Port broadcasts this Message to all PEX 8649 downstream devices, including the NT Port Virtual Interface Type 0 Endpoint. After the PME_TO_Ack Message is received from all downstream devices and the PEX 8649 NT Port Virtual Interface Type 0 Endpoint, the PEX 8649 Transparent upstream Port transmits an aggregated PME_TO_Ack Message to the upstream component after it finishes transmitting all pending TLPs to the upstream component. When NT mode is enabled, the PEX 8649 Transparent downstream Ports allow the attached devices to enter the PCI-PM-compatible L1 Link PM state. The PEX 8649 NT Port Virtual Interface Type 0 Endpoint never enters the PCI-PM L1 Link PM state.

14.4.3 Message Generation

The PEX 8649 NT Port Link Interface Type 0 Endpoint never generates PM_PME Messages. The PEX 8649 NT Port Virtual Interface Type 0 Endpoint never receives Set_Slot_Power_Limit Messages nor generates PM_PME Messages.

14.5 Expansion ROM

The NT Port Link Interface supports Expansion ROM, by default. Expansion ROM support can be moved from the NT Port Link Interface to the NT Port Virtual Interface, by Setting the **Ingress Chip Control** register *Expansion ROM Virtual Side* bit (Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface, offset 764h[0]).

The NT Port supports 16- or 32-KB-sized Expansion ROM, based upon the **Serial EEPROM Clock Frequency** register *Expansion ROM Size* bit (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 268h[16]) value.

Note: *Expansion ROM can be enabled in either the NT Port Virtual or Link Interface, but not both simultaneously. Expansion ROM is enabled, by default, in the NT Port Link Interface (**Ingress Chip Control** register Expansion ROM Virtual Side bit (Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface, offset 764h[0]) is Cleared).*

*Expansion ROM can be disabled, by Setting the Port's **Ingress Control** register Disable Expansion ROM BAR bit (offset F60h[15]).*

14.6 NT Port Interrupts

The NT Port Virtual and Link Interfaces can both generate interrupts in response to specific events. The NT Port must not receive any INT*x* Message Requests. If the NT Port receives an INT*x* Message Request, the Request is handled as a Malformed TLP error.

14.6.1 NT Port Virtual Interface Interrupts

The NT Port Virtual Interface generates interrupts to the Local Host for the following reasons (all are masked, by default, and must not be masked to be enabled):

- Doorbell interrupts
- NT Port Link Interface detected an Correctable TLP error
- NT Port Link Interface detected an Uncorrectable TLP error (option to signal Fatal, Non-Fatal, or both)
- NT Port Link Interface *DL_Active* state change
- NT Port Link Interface received an Uncorrectable Error Message

NT-Virtual Doorbell interrupts and Device-Specific errors can use the INT*x*, MSI, or PEX_INTA# signaling mechanisms (all mutually exclusive). PEX_INTA# output can be enabled for NT Port Virtual Interface Doorbell interrupts, by Setting the **ECC Error Check Disable** register *Enable PEX_INTA# Interrupt Output(s) for NT-Virtual Doorbell-Generated Interrupts* bit (offset 720h[7]). (Refer to Section 14.1.6 for Doorbell interrupt details.)

PEX_INTA# output can also be enabled for NT-Link Error and Event interrupts, by Setting the register's *Enable PEX_INTA# Interrupt Output(s) for Device-Specific NT-Link Port Event-Triggered Interrupt* bit (offset 720h[5]).

The NT Port Virtual Interface de-asserts INT*x* or PEX_INTA# interrupts in response to one or more of the following conditions:

- NT Port Virtual Interface **PCI Command** register *Interrupt Disable* bit (offset 04h[10]) is Set
- Corresponding *Interrupt Mask* bit is Set
- NT Port Link goes down (DL_Down condition) or the NT Port Link Interface receives a Hot Reset
- Software Clears the *Interrupt Status* bit, or Sets the *Doorbell Interrupt Request Clear* bit

In NT PCI-to-PCI Bridge mode, for tracking purposes, an NT Port Virtual Interface-generated interrupt is treated like an event that is external to the PCI-to-PCI bridge. If software asserts a Secondary Bus Reset from this PCI-to-PCI bridge, the PCI-to-PCI bridge de-asserts the NT Port Virtual Interface interrupt.

When the NT Port Link Interface detects Correctable TLP errors, the NT Port Virtual Interface signals the interrupt to the Local Host, if the interrupt signaling is enabled and not masked (**Link Error Status Virtual** register *Correctable Error Status on Link Side* bit is Set, and **Link Error Mask Virtual** register *Link Side Correctable Error Mask* bit is Cleared (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offsets FE0h[0] and FE4h[0], respectively).

When the NT Port Link Interface detects Uncorrectable TLP errors, the NT Port Virtual Interface signals the interrupt to the Local Host, if the interrupt signaling is enabled and not masked (**Link Error Status Virtual** register *Uncorrectable Error Status on Link Side* bit is Set, and **Link Error Mask Virtual** register *Link Side Uncorrectable Error Mask* bit is Cleared (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offsets FE0h[1] and FE4h[1], respectively).

An NT Port Link Interface *DL_Active* state change occurs upon detection of an NT Port Link Interface *DL_Down* state rise edge and fall edge. This signals the interrupt to the Local Host, if the interrupt signaling enabled and not masked (**Link Error Status Virtual** register *Link Side DL Active Change Status* bit is Set, and **Link Error Mask Virtual** register *Link Side DL Active Change Mask* bit is Cleared (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offsets FE0h[2] and FE4h[2], respectively).

When the NT Port Link Interface receives an Uncorrectable Error Message, the NT Port Virtual Interface signals the interrupt to the Local Host, if the interrupt signaling is enabled and not masked (**Link Error Status Virtual** register *Link Side Uncorrectable Error Message Drop Status* bit is Set, and **Link Error Mask Virtual** register *Link Side Uncorrectable Error Message Drop Mask* bit is Cleared (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offsets FE0h[3] and FE4h[3], respectively).

14.6.2 NT Port Link Interface Interrupts

The NT Port Link Interface generates interrupts to the System Host for NT-Link Doorbell interrupts detected at the NT Port Link Interface ingress Port (interrupts are masked, by default). The NT Port Link Interface should not detect any Device-Specific errors. (Refer to Section 14.1.6 for Doorbell interrupt details.)

NT-Link Doorbell interrupts can use the INT*x*, MSI, or PEX_INTA# signaling mechanisms (all mutually exclusive). PEX_INTA# output can be enabled for NT Port Link Interface Doorbell interrupts, by Setting the **ECC Error Check Disable** register *Enable PEX_INTA# Ball Interrupt for NT Link Doorbell-Generated Interrupts* bit (NT Port Link Interface, offset 720h[7]). (Refer to Section 14.1.6 for Doorbell interrupt details.)

The NT Port Link Interface de-asserts INT*x* or PEX_INTA# interrupts in response to one or more of the following conditions:

- NT Port Link Interface **PCI Command** register *Interrupt Disable* bit (offset 04h[10]) is Set
- Corresponding *Interrupt Mask* bit is Set
- NT Port Link goes down (DL_Down condition) or the NT Port Link Interface receives a Hot Reset
- Software Clears the *Interrupt Status* bit, or Sets the *Doorbell Interrupt Request Clear* bit

14.7 NT Port Error Handling

The PEX 8649 NT Port Virtual Interface endpoint logs TLP errors, for TLPs that travel from the NT Port Virtual Interface to the NT Port Link Interface. The PEX 8649 signals Error Messages to the Local Host (Host closest to the upstream Port). The PEX 8649 provides an option to communicate this error condition to the System Host (Host closest to the NT Port), by signaling an interrupt.

The PEX 8649 NT Port Link Interface endpoint logs TLP errors, for TLPs that travel from the NT Port Link Interface to the NT Port Virtual Interface. The PEX 8649 signals Error Messages to the System Host (Host closest to the NT Port).

When the PEX 8649 receives a TLP, it performs the following:

1. TLP integrity check,
2. Address decode,
3. Address translation,
4. Requester ID translation, and
5. ECRC re-generation,

before transmitting the TLP through the NT Port. If the PEX 8649 detects an ECRC error, it corrupts the re-generated ECRC before transmitting the TLP through the NT Port. The PEX 8649 also provides options for dropping error-detected endpoint (EP) or ECRC TLPs (**Ingress Control** register *Drop EP TLPs* and *Drop ECRC TLPs* bits, offset F60h[9:8], respectively).

The PEX 8649 does not generate the ECRC for a TLP that passes through the NT Port, if the received TLP does not have its *TD* bit Set.

The PEX 8649 drops all TLPs traveling from the NT Port Virtual Interface to the NT Port Link Interface, if the internal RAM Fatal ECC error is detected, until the PEX 8649 receives a Hot Reset from a Local Host.

14.7.1 NT Port Link Interface Error Handling

If the NT Port Link Interface receives an Uncorrectable Error message, it reports a Malformed TLP error, by default. However, if the **Ingress Chip Control** register *NT Error Message Drop* bit (Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface, offset 764h[1]) is Set, the NT Port Link Interface drops the Message, and logs the error in the **Link Error Status Virtual** register *Link Side Uncorrectable Error Message Drop Status* bit (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE0h[3]. If the corresponding **Link Error Mask Virtual** register *Link Side Uncorrectable Error Message Drop Mask* bit (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE4h[3]) is Set, the NT Port Virtual signals an interrupt (INTx, MSI, or PEX_INTA#) to the Local Host through the upstream Port, if interrupts are enabled.

14.7.2 NT PCI-to-PCI Bridge Mode Error Handling

In NT PCI-to-PCI Bridge mode, for the NT Port Virtual Interface to generate an Error Message, the following error-forwarding *Enable* bits, in both the NT PCI-to-PCI bridge and the upstream Port, must be Set:

- **PCI Command** register (offset 04h)
  - *SERR# Enable* (bit 8)
- **Bridge Control** register (offset 3Ch)
  - *SERR# Enable* (bit 17)
- **Device Control** register (offset 70h)
  - *Correctable Error Reporting Enable* (bit 0)
  - *Non-Fatal Error Reporting Enable* (bit 1)
  - *Fatal Error Reporting Enable* (bit 2)

When the NT Port Virtual Interface generates an error Message, the NT PCI-to-PCI bridge also logs the error status in the following NT PCI-to-PCI Bridge mode registers, while sending the Message upstream:

- **Secondary Status** register (offset 1Ch)
  - *Received System Error* (bit 30)
- **PCI Status** register (offset 04h)
  - *Signaled System Error* (bit 30)

14.8 Cursor Mechanism

A software application can use the Device-Specific Cursor Mechanism to access the PEX 8649 NT Port Configuration Space registers. The registers that support the Device-Specific Cursor Mechanism are the **Configuration Address Window** and **Configuration Data Window** registers (offsets F8h and FCh, respectively). A software application can also:

- Select the Configuration Register offset, by using the **Configuration Address Window** register
- Perform Read accesses to the **Configuration Data Window** register, to read to the selected Configuration register
- Perform Write accesses to the **Configuration Data Window** register, to write to the selected Configuration register

Configuration transactions have access to this Device-Specific Cursor Mechanism, if NT mode is enabled.

For details regarding the **Configuration Address Window** and **Configuration Data Window** registers, refer to:

- Section 15.10, "NT Port Virtual Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)"
- Section 16.10, "NT Port Link Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)"

14.9 Port Programmability

The PEX 8649 supports the capability of programming the upstream Port and NT Port Number. The Configuration register for the upstream Port and NT Port is in the **VS0 Upstream** register *Upstream Port* and *NT Port* fields (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 360h[4, 2:0 and 12, 10:8], respectively). This register is updated, based upon the external STRAP_NT_ENABLE# and STRAP_NT_UPSTRM_PORTSEL[4, 2:0] Strapping ball values, by default. A serial EEPROM, I^{2}C, and/or software can be used to override the external strap values.

A software application can change the upstream Port and NT Port location to another Port Number during runtime, or as part of a failover sequence. It is recommended that the PEX 8649 be in an Idle state (no traffic) when changing the upstream Port and NT Port Numbers during runtime. During a failover sequence, application software must be able to handle all spurious TLPs that it receives as a result of the failover process.

Chapter 15 NT Port Virtual Interface Registers – Base Mode Only

15.1 Introduction

Note: *Check the latest design guides, application notes and errata list for Non-Transparent (NT) usage.*

NT mode is supported in Base mode. In NT mode, the NT Port includes two sets of Configuration, Capability, Control, and Status registers, to support the Virtual and Link Interfaces. This chapter defines the PEX 8649 NT Port Virtual Interface registers. Other registers are defined in:

- Chapter 13, "Transparent Port Registers"
- Chapter 16, "NT Port Link Interface Registers – Base Mode Only"

Notes: *For Chip-specific registers (those that exist only in Port 0), if Port 0 is the Legacy NT Port, then those registers exist only in the NT Port Virtual Interface.*

For Station-specific registers (those that exist only in Port 0, 16, or 20), if Port 0, 16, or 20 is the Legacy NT Port, then those registers exist only in the NT Port Virtual Interface.

All PEX 8649 registers can be accessed by Configuration or Memory Requests.

For further details regarding register names and descriptions, refer to the following specifications:

- *PCI r3.0*
- *PCI Power Mgmt. r1.2*
- *PCI Express Base r2.0*

15.2 NT Port Virtual Interface Type 0 Register Map

Table 15-1 defines the NT Port Virtual Interface Type 0 register mapping.

Table 15-1. NT Port Virtual Interface Type 0 Register Map

31 30 29 28 27 26 25 24 23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
NT Port Virtual Interface PCI-Compatible Type 0 Configuration Header Registers (Offsets 00h – 3Ch)				00h …
			Capability Pointer (40h)	34h
				… 3Ch
		Next Capability Pointer (48h)	Capability ID (01h)	40h
NT Port Virtual Interface PCI Power Management Capability Registers (Offsets 40h – 44h)				44h
		Next Capability Pointer (68h)	Capability ID (05h)	48h
NT Port Virtual Interface MSI Capability Registers (Offsets 48h – 64h)				… 64h
		Next Capability Pointer (A4h)	Capability ID (10h)	68h
NT Port Virtual Interface PCI Express Capability Registers (Offsets 68h – A0h)				… A0h
		Next Capability Pointer (C8h)	SSID/SSVID Capability ID (0Dh)	A4h
NT Port Virtual Interface Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – C4h)				… C4h
		Next Capability Pointer (00h)	Capability ID 3 (09h)	C8h
NT Port Virtual Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)				… FCh
Next Capability Offset (FB4h)	1h	PCI Express Extended Capability ID (0003h)		100h
NT Port Virtual Interface Device Serial Number Extended Capability Registers (Offsets 100h – 134h)				… 134h
Next Capability Offset (148h)	1h	PCI Express Extended Capability ID (0004h)		138h
NT Port Virtual Interface Power Budget Extended Capability Registers (Offsets 138h – 144h)				… 144h
Next Capability Offset 2 (C34h)	1h	PCI Express Extended Capability ID (0002h)		148h
NT Port Virtual Interface Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)				… 1BCh

Table 15-1. NT Port Virtual Interface Type 0 Register Map *(Cont.)*

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16		15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
NT Port Virtual Interface Device-Specific Registers (Offsets 1C0h – C88h)			1C0h …
Next Capability Offset 2 (000h)	1h	PCI Express Extended Capability ID 2 (000Bh)	B70h
NT Port Virtual Interface Device-Specific Registers (Offsets 1C0h – C88h)			…
Next Capability Offset 4 (B70h)	1h	PCI Express Extended Capability ID 4 (000Bh)	C34h
NT Port Virtual Interface Device-Specific Registers (Offsets 1C0h – C88h)			… C88h
NT Port Virtual Interface NT Bridging-Specific Registers (Offsets C8Ch – DFCh)			C8Ch … DFCh
Reserved (Legacy NT Mode) Multicast Extended Capability Registers (Offsets E00h – E2Ch) – All Modes Except Legacy NT (NT PCI-to-PCI Mode)			E00h … E2Ch
Reserved		E30h –	F2Ch
NT Port Virtual Interface Device-Specific Registers (Offsets F30h – FB0h)			F30h … FB0h
Next Capability Offset (138h)	1h	PCI Express Extended Capability ID (0001h)	FB4h
NT Port Virtual Interface Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)			… FDCh
NT Port Virtual Interface Device-Specific Registers – Link Error (Offsets FE0h – FFCh)			FE0h … FFCh

15.3 Register Access

The PEX 8649 NT Port Virtual Interface implements a 4-KB Configuration Space. The lower 256 bytes (offsets 00h through FFh) are the PCI-compatible Configuration Space, and the upper 960 Dwords (offsets 100h through FFFh) are the PCI Express Extended Configuration Space. The PEX 8649 supports three mechanisms for accessing the NT Port Virtual Interface registers:

- PCI Express Base r2.0 Configuration Mechanism
- Device-Specific Memory-Mapped Configuration Mechanism
- Device-Specific Cursor Mechanism

15.3.1 *PCI Express Base r2.0* Configuration Mechanism

The *PCI Express Base r2.0* Configuration mechanism is divided into two mechanisms:

- **PCI r3.0-Compatible Configuration Mechanism** – Provides Conventional PCI access to the first 256 bytes (the bytes at offsets 00h through FFh) of the NT Port Virtual Interface Configuration Register space
- **PCI Express Enhanced Configuration Access Mechanism** – Provides access to the entire 4 KB Configuration Space

Both are described in the sections that follow.

15.3.1.1 *PCI r3.0*-Compatible Configuration Mechanism

The *PCI r3.0*-Compatible Configuration mechanism provides standard access to the PEX 8649 NT Port Virtual Interface's first 256 bytes (the bytes at offsets 00h through FFh) of the PCI Express Configuration Space. (Refer to Figure 15-1.)

The mechanism uses PCI Type 0 and Type 1 Configuration transactions to access the PEX 8649 Configuration registers. All Ports capture the Bus Number and Device Number assigned by the upstream device on the PCI Express Link attached to the PEX 8649 upstream Port, as required by the *PCI Express Base r2.0*.

The PEX 8649 decodes all Type 1 Configuration accesses received on its upstream Port, when any of the following conditions exist:

- If the Bus Number specified in the Configuration access is the number of the PEX 8649 internal virtual PCI Bus, the PEX 8649 automatically converts the Type 1 Configuration access into the appropriate Type 0 Configuration access for the specified device.
  - If the specified device corresponds to the NT Port Virtual Interface (or to the PCI-to-PCI bridge in one of the PEX 8649 Transparent downstream Ports), the PEX 8649 processes the Read or Write Request
  - If the specified Device Number does not correspond to any of the PEX 8649 downstream Port Device Numbers or NT Port Number, the PEX 8649 responds with an Unsupported Request (UR)

Because the mechanism is limited to the first 256 bytes of the NT Port Virtual Interface Configuration register space, one of the following must be used to access beyond Byte FFh:

- PCI Express Enhanced Configuration Access Mechanism
- Device-Specific Memory-Mapped Configuration Mechanism
- Device-Specific Cursor Mechanism

This mechanism uses the same Request format as the PCI Express Enhanced Configuration Access Mechanism. For PCI-compatible Configuration Requests, the Extended Register Address field must be all zeros (0).

15.3.1.2 PCI Express Enhanced Configuration Access Mechanism

The PCI Express Enhanced Configuration Access mechanism uses a flat, Root Complex Memory-Mapped Address space to access the device Configuration registers. In this case, the Memory address determines the Configuration register accessed, and the Memory data returns the addressed register's contents. The Root Complex converts the Memory transaction into a Configuration transaction.

This mechanism is used to access all PEX 8649 registers.

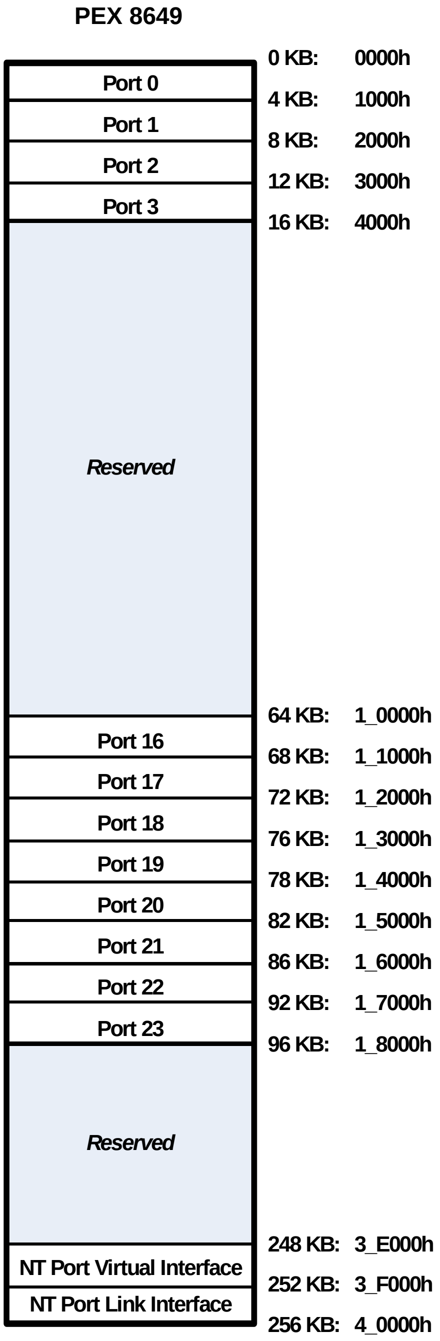
15.3.2 Device-Specific Memory-Mapped Configuration Mechanism

The Device-Specific Memory-Mapped Configuration mechanism provides a method to access the registers for all Ports within a single 256-KB Memory map, as illustrated in Figure 15-1. This Memory map is identical for Upstream Port **BAR0/1**, NT Port Virtual Interface **BAR0/1**, and NT Port Link Interface **BAR0/1**. The registers of each Port are located within a 4-KB range.

When the NT Port is enabled at Fundamental Reset, the NT Port Virtual and Link Interface registers use the *PCI r3.0* Type 0 Configuration Space Header. In NT PCI-to-PCI Bridge mode (STRAP_NT_P2P_EN# input is Low), the NT PCI-to-PCI bridge (between the NT Port Virtual Interface and internal virtual PCI Bus) registers use the *PCI r3.0* Type 1 Configuration Space Header, and are mapped to the 4-KB Address space of the Port Number that is assigned as the NT Port (indicated in the **VS0 Upstream** register *NT Port* field (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 360h[12, 10:8])).

To use this mechanism, use the PCI r3.0-Compatible Configuration Mechanism to program the PEX 8649 NT Port Virtual Interface **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, offsets 10h and 14h, respectively). After the PEX 8649 NT Port Virtual Interface Memory-Mapped register Base address is Set, the PEX 8649 Configuration Space registers are accessed, using Memory Reads and Writes to the 4-KB range, starting at offset 248 KB (3_E000h, Virtual Interface) and offset 252 KB (3_F000h, Link Interface).

Figure 15-1. Register Offset from NT Port Virtual Interface BAR0/1 Base Address



15.3.3 Device-Specific Cursor Mechanism

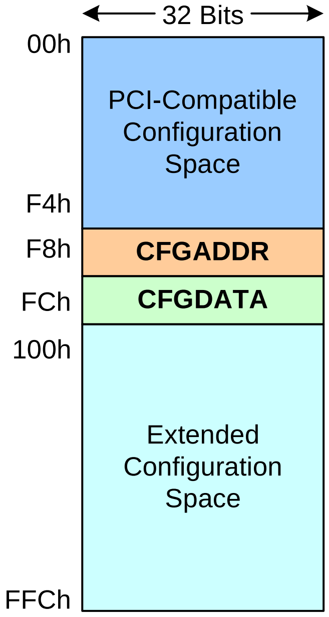
The Device-Specific Cursor mechanism is provided for use in development systems that can only generate *PCI r3.0* Configuration cycles (*that is*, the system cannot use either the Device-Specific Memory-Mapped Configuration mechanism, nor generate Extended Configuration Requests to access the Extended Configuration Space).

In Figure 15-2, the software uses the **Configuration Address Window** (CFGADDR) register (offset F8h) to point to the NT Port Virtual or Link Interface Configuration Space registers, including the PCI Express Extended Configuration Space registers (offsets 100h through FFFh).

Software uses the **Configuration Data Window** (CFGDATA) register (offset FCh) to write to or read from the selected Configuration Space registers.

Refer to Section 15.10, "NT Port Virtual Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)," for the register descriptions.

Figure 15-2. Configuration Space View


32 Bits
00h
PCI-Compatible Configuration Space
F4h
F8h
CFGADDR
FCh
CFGDATA
100h
Extended Configuration Space
FFCh

15.4 Register Descriptions

The remainder of this chapter details the PEX 8649 NT Port Virtual Interface registers, including:

- Bit/field names
- Description of register functions in the PEX 8649 NT Port Virtual and Link Interfaces
- Type (*such as* RW or HwInit; refer to Table 13-4, "Register Types, Grouped by User Accessibility," for Type descriptions)
- Whether the power-on/reset value can be modified, by way of the PEX 8649 serial EEPROM and/or I^{2}C Initialization feature
- Default power-on/reset value

15.5 NT Port Virtual Interface PCI-Compatible Type 0 Configuration Header Registers (Offsets 00h – 3Ch)

This section details the NT Port Virtual Interface PCI-Compatible Type 0 Configuration Header registers. Table 15-2 defines the register map.

Table 15-2. NT Port Virtual Interface PCI-Compatible Type 0 Configuration Header Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Device ID		Vendor ID		00h
PCI Status		PCI Command		04h
PCI Class Code			PCI Revision ID	08h
PCI BIST ***(Not Supported)***	PCI Header Type	Master Latency Timer ***(Not Supported)***	Cache Line Size	0Ch
Base Address 0				10h
Base Address 1				14h
Base Address 2				18h
Base Address 3				1Ch
Base Address 4				20h
Base Address 5				24h
Reserved				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Expansion ROM Base Address				30h
Reserved			Capability Pointer (40h)	34h
Reserved				38h
Max_Lat ***(Reserved)***	Min_Gnt ***(Reserved)***	PCI Interrupt Pin	PCI Interrupt Line	3Ch

Register 15-1. 00h PCI Configuration ID

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**Vendor ID** Identifies the device manufacturer. Defaults to the PCI-SIG-issued Vendor ID of PLX (10B5h), if not overwritten by serial EEPROM and/or I^2C.	RO	Yes	10B5h
31:16	**Device ID** Identifies the particular device. Defaults to the PLX part number for the PEX 8649, if not overwritten by serial EEPROM and/or I^2C.	RO	Yes	8649h

Register 15-2. 04h PCI Command/Status

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	PCI Command			
0	**I/O Access Enable** The PEX 8649 does not claim I/O resources, nor does it forward I/O transactions through the NT Port. The value of this register is “Don’t Care.”	RW	Yes	0
1	**Memory Access Enable** 0 = PEX 8649 ignores Memory Space Requests on the NT Port Virtual Interface 1 = PEX 8649 accepts Memory Space Requests received on the NT Port Virtual Interface	RW	Yes	0
2	**Bus Master Enable** Controls PEX 8649 forwarding of Memory Requests upstream. Does not affect Message forwarding nor Completions. 0 = PEX 8649 handles Memory Requests received on the NT Port Link Interface as Unsupported Requests (URs); for Non-Posted Requests, the PEX 8649 returns a Completion with UR Completion status 1 = PEX 8649 forwards Memory Requests upstream	RW	Yes	0
3	**Special Cycle Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
4	**Memory Write and Invalidate Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
5	**VGA Palette Snoop** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
6	**Parity Error Response Enable** Controls bit 24 (*Master Data Parity Error Detected*).	RW	Yes	0
7	**IDSEL Stepping/Wait Cycle Control** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
8	**SERR# Enable** Controls bit 30 (*Signaled System Error*). 1 = Enables reporting of Fatal and Non-Fatal errors detected by the NT Port Virtual Interface to the Root Complex	RW	Yes	0
9	**Fast Back-to-Back Transactions Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
10	**Interrupt Disable** 0 = NT Port Virtual Interface is enabled to generate INT*x* Interrupt Messages 1 = NT Port Virtual Interface is prevented from generating INT*x* Interrupt Messages	RW	Yes	0
15:11	***Reserved***	RsvdP	No	0-0h

Register 15-2. 04h PCI Command/Status *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	PCI Status			
18:16	***Reserved***	RsvdP	No	000b
19	**Interrupt Status** 0 = No INT*x* interrupt is pending 1 = INT*x* interrupt is pending internally to the NT Port Virtual Interface –or– PEX_INTA# (if enabled) is asserted	RO	No	0
20	**Capability List** Capability function is supported. Set, as required by the *PCI Express Base r2.0*.	RO	Yes	1
21	**66 MHz Capable** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
22	***Reserved***	RsvdP	No	0
23	**Fast Back-to-Back Transactions Capable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
24	**Master Data Parity Error Detected** If bit 6 (*Parity Error Response Enable*) is Set, the NT Port Virtual Interface Sets this bit when the NT Port: • Forwards the poisoned Transaction Layer Packet (TLP) Write Request from the NT Port Link Interface to the NT Port Virtual Interface, –or– • Receives a Completion marked as poisoned on the NT Port Virtual Interface If the *Parity Error Response Enable* bit is Cleared, the PEX 8649 never Sets this bit. This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
26:25	**DEVSEL# Timing** ***Not supported***	RsvdP	No	00b
27	**Signaled Target Abort** The NT Port Virtual Interface Sets this bit if any of the following conditions exist: • NT Port Virtual Interface receives a Completion (from a Transparent Port) that has a Completion status of Completer Abort (CA), –or– • NT Port Virtual Interface receives a Memory Request targeting a PEX 8649 register, and the Payload Length (indicated within the Memory Request Header) is greater than 1 DWord • NT Port Virtual Interface receives a Memory Request targeting a PEX 8649 register address within a non-existent Port • NT Port Virtual Interface receives a Memory Write Request targeting enabled Expansion ROM Address space (Expansion ROM Base Address Register (BAR), offset 30h) ***Note:*** *When Set during a forwarded Completion, the* ***Uncorrectable Error Status*** *register Completer Abort Status bit (offset FB8h[15]) is not Set.*	RW1C	Yes	0

Register 15-2. 04h PCI Command/Status *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
28	**Received Target Abort** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
29	**Received Master Abort** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
30	**Signaled System Error** If bit 8 (*SERR# Enable*) is Set, the NT Port Virtual Interface Sets this bit when transmitting an ERR_FATAL or ERR_NONFATAL Message to the upstream Port.	RW1C	Yes	0
31	**Detected Parity Error** This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility. 1 = NT Port Virtual Interface received a Poisoned TLP, regardless of the bit 6 (*Parity Error Response Enable*) state	RW1C	Yes	0

Register 15-3. 08h PCI Class Code and Revision ID

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
	PCI Revision ID			
7:0	**Revision ID** Unless overwritten by the serial EEPROM, returns the Silicon Revision (AAh), the PLX-assigned Revision ID for this version of the PEX 8649. The PEX 8649 Serial EEPROM register Initialization capability is used to replace the PLX Revision ID with another Revision ID.	RO	Yes	AAh
	PCI Class Code			**068000h**
15:8	**Register-Level Programming Interface**	RO	Yes	00h
23:16	**Sub-Class Code** Other bridge devices.	RO	Yes	80h
31:24	**Base Class Code** Bridge devices.	RO	Yes	06h

Register 15-4. 0Ch Miscellaneous Control

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
Cache Line Size				
7:0	**Cache Line Size** System Cache Line Size. Implemented as a RW field for Conventional PCI compatibility purposes and does not impact PEX 8649 functionality.	RW	Yes	00h
Master Latency Timer				
15:8	**Master Latency Timer** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	00h
PCI Header Type				
22:16	**Configuration Layout Type** Type 0 Configuration Header for the NT Port.	RO	No	00h
23	**Multi-Function Device** 0 = Single-function device 1 = Indicates multiple (up to eight) functions (logical devices), each containing its own, individually addressable Configuration Space, 256 DWords in size	RO	No	0
PCI BIST				
31:24	**PCI BIST** ***Not supported*** Built-In Self-Test (BIST) Pass or Fail.	RsvdP	No	00h

Register 15-5. 10h Base Address 0 (NT Port Virtual Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *By default, NT Port Virtual Interface* ***BAR0*** *is enabled and* ***BAR1*** *is disabled, to provide a 32-bit* ***BAR0*** *for register access.* ***BAR1*** *can be enabled (by serial EEPROM and/or I²C/SMBus), to provide a 64-bit* ***BAR0/1****, by programming the* ***NT Port Virtual Interface BAR0/1 Setup*** *register BAR0/1 Enable field (NT Port Virtual Interface, offset D0h[1:0]) to 11b (which enables both* ***BAR0*** *and* ***BAR1****).*				
0	**Memory Space Indicator** When enabled, the Base Address register maps PEX 8649 Port Configuration registers into Memory space. ***Note:*** *Hardwired to 0.*	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Base Address register maps the PEX 8649 Port Configuration registers into Non-Prefetchable Memory space	RO	Yes	0
17:4	***Reserved***	RsvdP	No	0-0h
31:18	**Base Address 0** 256-KB-aligned Base address used for Memory-Mapped access to the 256-KB block of all PEX 8649 registers (4 KB per Port).	RW	Yes	0-0h

Register 15-6. 14h Base Address 1 (NT Port Virtual Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Upper 32-Bit Address for Memory-Mapped BAR** For 64-bit addressing (**BAR0/1**), Base Address 1 (**BAR1**) extends Base Address 0 (**BAR0**) to provide the upper 32 Address bits when the **Base Address 0** register *Memory Map Type* field (offset 10h[2:1]) is programmed to 10b.	RW	Yes	0000_0000h
	RO when the **Base Address 0** (**BAR0**) register is not enabled as a 64-bit BAR (*Memory Map Type* field (offset 10h[2:1]) is not equal to 10b).	RO	Yes	0000_0000h

Register 15-7. 18h Base Address 2 (NT Port Virtual Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**Memory Space Indicator** 0 = Implemented as a Memory BAR	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
19:4	***Reserved***	RsvdP	No	0_000h
31:20	**Base Address 2** Resolution is 1 MB.	RW	Yes	000h

Register 15-8. 1Ch Base Address 3 (NT Port Virtual Interface Memory Space)

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
Note:	*This register has RW privilege if **BAR2/3** is configured as a 64-bit BAR (**Base Address 2** register Memory Map Type field, offset 18h[2:1], is programmed to 10b).*				
0	**Memory Space Indicator** **BAR3** can be used as an independent 32-bit only BAR, or as the upper 32 bits of 64-bit **BAR2/3**. 0 = Memory BAR – only value supported	Offset 18h[2:1]=00b	RsvdP	No	0
		Offset 18h[2:1]=10b	RW	Yes	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space All other encodings are ***reserved***.	Offset 18h[2:1]=00b	RsvdP	No	00b
		Offset 18h[2:1]=10b	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	Offset 18h[2:1]=00b	RsvdP	No	0
		Offset 18h[2:1]=10b	RW	Yes	0
19:4	***Reserved***	Offset 18h[2:1]=00b	RsvdP	No	0_000h
	When **BAR2/3** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset 18h[2:1]=10b	RW	Yes	0_000h
31:20	**Base Address 3**		RW	Yes	000h

Register 15-9. 20h Base Address 4 (NT Port Virtual Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
0	**Memory Space Indicator** 0 = Memory BAR – only value supported	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
19:4	***Reserved***	RsvdP	No	0_000h
31:20	**Base Address 4**	RW	Yes	000h

Register 15-10. 24h Base Address 5 (NT Port Virtual Interface Memory Space)

<table>
<tr><th>Bit(s)</th><th colspan="2">Description</th><th>Type</th><th>Serial EEPROM and I^{2}C</th><th>Default</th></tr>
<tr><td colspan="6"><i><b>Note:</b> This register has RW privilege if <b>BAR4/5</b> is configured as a 64-bit BAR (<b>Base Address 4</b> register Memory Map Type field, offset 20h[2:1], is programmed to 10b).</i></td></tr>
<tr><td rowspan="2">0</td><td rowspan="2"><b>Memory Space Indicator</b>
<b>BAR5</b> can be used as an independent 32-bit only BAR, or as the upper 32 bits of 64-bit <b>BAR4/5</b>.
0 = Memory BAR – only value supported</td><td>Offset 20h[2:1]=00b</td><td>RsvdP</td><td>No</td><td>0</td></tr>
<tr><td>Offset 20h[2:1]=10b</td><td>RW</td><td>Yes</td><td>0</td></tr>
<tr><td rowspan="2">2:1</td><td rowspan="2"><b>Memory Map Type</b>
00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space
All other encodings are <b><i>reserved</i></b>.</td><td>Offset 20h[2:1]=00b</td><td>RsvdP</td><td>No</td><td>00b</td></tr>
<tr><td>Offset 20h[2:1]=10b</td><td>RW</td><td>Yes</td><td>00b</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2"><b>Prefetchable</b>
0 = Non-Prefetchable
1 = Prefetchable</td><td>Offset 20h[2:1]=00b</td><td>RsvdP</td><td>Yes</td><td>0</td></tr>
<tr><td>Offset 20h[2:1]=10b</td><td>RW</td><td>Yes</td><td>0</td></tr>
<tr><td rowspan="2">19:4</td><td><b><i>Reserved</i></b></td><td>Offset 20h[2:1]=00b</td><td>RsvdP</td><td>No</td><td>0_000h</td></tr>
<tr><td>When <b>BAR4/5</b> are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.</td><td>Offset 20h[2:1]=10b</td><td>RW</td><td>Yes</td><td>0_000h</td></tr>
<tr><td>31:20</td><td colspan="2"><b>Base Address 5</b></td><td>RW</td><td>Yes</td><td>000h</td></tr>
</table>

Register 15-11. 2Ch Subsystem ID and Subsystem Vendor ID

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
15:0	**Subsystem Vendor ID** Identifies the device manufacturer. Defaults to the PCI-SIG-issued Vendor ID of PLX (10B5h), if not overwritten by serial EEPROM and/or I^{2}C.	RO	Yes	10B5h
31:16	**Subsystem ID** Identifies the particular device. Defaults to the PLX part number for the PEX 8649, if not overwritten by serial EEPROM and/or I^{2}C.	RO	Yes	8649h

Register 15-12. 30h Expansion ROM Base Address

<table>
<tr><th>Bit(s)</th><th colspan="2">Description</th><th>Type</th><th>Serial EEPROM and I^{2}C</th><th>Default</th></tr>
<tr><td colspan="6"><b><i>Note:</i></b> <i>Expansion ROM can be enabled in either the NT Port Virtual or Link Interface, but not both simultaneously. Expansion ROM is enabled, by default, in the NT Port Link Interface (<b>Ingress Chip Control</b> register Expansion ROM Virtual Side bit (Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface, offset 764h[0]) is Cleared).</i>
<i>Expansion ROM can be disabled, by Setting the Port's <b>Ingress Control</b> register Disable Expansion ROM BAR bit (offset F60h[15]).</i></td></tr>
<tr><td rowspan="2">0</td><td><b>Expansion ROM Enable</b>
0 = NT Port Virtual Interface Expansion ROM is disabled</td><td>Offset F60h[15]=1
–or–
NT Station
offset 764h[0]=0</td><td>RsvdP</td><td>No</td><td>0</td></tr>
<tr><td>1 = NT Port Virtual Interface Expansion ROM is enabled, and NT Port Link Interface Expansion ROM is disabled</td><td>Offset F60h[15]=0
–or–
NT Station
offset 764h[0]=1</td><td>RW</td><td>Yes</td><td>0</td></tr>
<tr><td>13:1</td><td colspan="2"><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>0-0h</td></tr>
<tr><td rowspan="2">31:14</td><td rowspan="2"><b>Expansion ROM Base Address</b>
If the <b>Serial EEPROM Clock Frequency</b> register <i>Expansion ROM Size</i> bit (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 268h[16]) value is 0, the Expansion ROM size is 16 KB (default value is FFFF_C001h). Bit 14 is RW.
If the <i>Expansion ROM Size</i> bit value is 1, the Expansion ROM size is 32 KB (default value is FFFF_8001h). Bit 14 is RO.</td><td>Offset F60h[15]=1
–or–
NT Station
offset 764h[0]=0</td><td>RsvdP</td><td>No</td><td>0-0h</td></tr>
<tr><td>Offset F60h[15]=0
–or–
NT Station
offset 764h[0]=1</td><td>RW</td><td>Yes</td><td>0-0h</td></tr>
</table>

Register 15-13. 34h Capability Pointer

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
7:0	**Capability Pointer** Default 40h points to the **PCI Power Management Capability** structure.	RO	Yes	40h
31:8	***Reserved***	RsvdP	No	0000_00h

Register 15-14. 3Ch PCI Interrupt

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
7:0	**PCI Interrupt Line** The Interrupt Line Routing value communicates interrupt line routing information. Values in this register are programmed by system software and are system architecture-specific. The value is used by device drivers and operating systems.	RW	Yes	00h
15:8	**PCI Interrupt Pin** Identifies the Conventional PCI Interrupt Message(s) the device (or device function) uses. Only value 00h or 01h is allowed in the PEX 8649. 00h = Indicates that the device does not use Conventional PCI Interrupt Message(s) 01h, 02h, 03h, and 04h = Maps to Conventional PCI Interrupt Messages for INTA#, INTB#, INTC#, and INTD#, respectively	RO	Yes	01h
23:16	**Min_Gnt** ***Reserved*** Minimum Grant. Does not apply to PCI Express.	RsvdP	No	00h
31:24	**Max_Lat** ***Reserved*** Maximum Latency. Does not apply to PCI Express.	RsvdP	No	00h

15.6 NT Port Virtual Interface PCI Power Management Capability Registers (Offsets 40h – 44h)

This section details the NT Port Virtual Interface PCI Power Management Capability registers. Table 15-3 defines the register map.

Table 15-3. NT Port Virtual Interface PCI Power Management Capability Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Power Management Capability		Next Capability Pointer (48h)	Capability ID (01h)	40h
PCI Power Management Data	PCI Power Management Control/Status Bridge Extensions *(Reserved)*	PCI Power Management Status and Control		44h

Register 15-15. 40h PCI Power Management Capability

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
7:0	**Capability ID** Default = 01h – only value allowed.	RO	Yes	01h
15:8	**Next Capability Pointer** Default 48h points to the **MSI Capability** structure.	RO	Yes	48h
18:16	**Version** Default = 011b – only value allowed.	RO	Yes	011b
19	**PME Clock** Power Management Event (PME) clock. Does not apply to PCI Express. Returns 0.	RsvdP	No	0
20	***Reserved***	RsvdP	No	0
21	**Device-Specific Initialization** 0 = Device-Specific Initialization is ***not*** required	RO	Yes	0
24:22	**AUX Current** The PEX 8649 does ***not support*** PME generation from the D3cold Device Power Management (PM) state; therefore, the serial EEPROM value for this field should be 000b.	RO	Yes	000b
25	**D1 Support** ***Not supported*** 0 = PEX 8649 does ***not support*** the D1 Device PM state	RsvdP	No	0
26	**D2 Support** ***Not supported*** 0 = PEX 8649 does ***not support*** the D2 Device PM state	RsvdP	No	0
31:27	**PME Support** The default value is applied to bits [31, 30, and 27] only. PME Messages are disabled, by default.	RO	Yes	0000_0b

Register 15-16. 44h PCI Power Management Status and Control

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
PCI Power Management Status and Control				
1:0	**Power State** Used to determine the Port's current Device PM state, and to Set the Port into a new Device PM state. 00b = D0 01b = D1 – ***Not supported*** 10b = D2 – ***Not supported*** 11b = D3hot If software attempts to write an unsupported state to this field, the Write operation completes normally; however, the data is discarded and no state change occurs.	RW	Yes	00b
2	***Reserved***	RsvdP	No	0
3	**No Soft Reset** 1 = Devices transitioning from the D3hot to D0 Device PM state, because of Power State commands, do not perform an internal reset	RO	Yes	1
7:4	***Reserved***	RsvdP	No	0h
8	**PME Enable** Tied to 0, because the PEX 8649 does ***not*** generate PME in PCI Express mode.	RsvdP	No	0
12:9	**Data Select** Initially writable by serial EEPROM and I^{2}C only[a]. This Configuration Space register (CSR) access privilege changes to RW after a Serial EEPROM and/or I^{2}C Write occurs to this register. Selects the **Data** and **Data Scale** registers (fields [31:24 and 14:13], respectively). 0h = D0 power consumed 3h = D3hot power consumed 4h = D0 power dissipated 7h = D3hot power dissipated All other encodings are ***reserved***.	RO	Yes	0h
14:13	**Data Scale** Writable by serial EEPROM and I^{2}C only[a]. Indicates the scaling factor to be used when interpreting the **Data** register value. The value and meaning of this field varies, depending upon which data value is selected by field [12:9] (*Data Select*). There are four internal **Data Scale** registers (one each, per *Data Select* values 0h, 3h, 4h and 7h). For other *Data Select* values, the **Data Scale** value returned is 0h.	RO	Yes	00b
15	**PME Status** 0 = PME is not being generated by the NT Port	RsvdP	No	0

Register 15-16. 44h PCI Power Management Status and Control *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
PCI Power Management Control/Status Bridge Extensions				
21:16	***Reserved***	RsvdP	No	0-0h
22	**B2/B3 Support** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.	RsvdP	No	0
23	**Bus Power/Clock Control Enable** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.	RsvdP	No	0
PCI Power Management Data				
31:24	**Data** Writable by serial EEPROM and I^2C only[a]. There are four supported *Data Select* values (0h, 3h, 4h and 7h). For other *Data Select* values, the **Data Scale** value returned is 0h. Selected by field [12:9] (*Data Select*).	RO	Yes	00h

[a] *With no serial EEPROM nor previous I^2C programming, Reads return 00h for the* ***Data*** *and* ***Data Scale*** *registers (for all Data Selects).*

15.7 NT Port Virtual Interface MSI Capability Registers (Offsets 48h – 64h)

The registers detailed in Section 13.9, “MSI Capability Registers (Offsets 48h – 64h),” are also applicable to the NT Port Virtual Interface, except as defined in Table 15-4 (register map), and Register 15-17 through Register 15-19.

Table 15-4. NT Port Virtual Interface MSI Capability Register Map[a]

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
MSI Control		Next Capability Pointer (68h)	Capability ID (05h)	48h
MSI Address				4Ch
MSI Upper Address				50h
Reserved		MSI Data		54h
MSI Mask				58h
MSI Status				5Ch
Reserved				60h – 64h

[a] *Offsets 54h, 58h, and 5Ch change to 50h, 54h, and 58h, respectively, when the **MSI Control** register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.*

Register 15-17. 48h MSI Capability

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
MSI Capability Header				
7:0	**Capability ID** Program to 05h, as required by the *PCI r3.0*.	RO	Yes	05h
15:8	**Next Capability Pointer** Program to 68h, to point to the **PCI Express Capability** structure.	RO	Yes	68h
MSI Control				
16	**MSI Enable** 0 = MSIs for the NT Port Virtual Interface are disabled 1 = MSIs for the NT Port Virtual Interface are enabled, and INT*x* Interrupt Messages and PEX_INTA# output assertion are disabled	RW	Yes	0
19:17	**Multiple Message Capable** 000b = NT Port Virtual Interface can request only one Vector 001b = NT Port Virtual Interface can request two Vectors 010b = NT Port Virtual Interface can request four Vectors 011b = NT Port Virtual Interface can request eight Vectors All other encodings are ***reserved***.	RO	Yes	011b
22:20	**Multiple Message Enable** 000b = NT Port Virtual Interface is allocated one Vector, by default. 001b = NT Port Virtual Interface is allocated two Vectors. 010b = NT Port Virtual Interface is allocated four Vectors. 011b = NT Port Virtual Interface is allocated eight Vectors. Up to six Vectors are used; the upper two Vectors (having the highest values of Message Data bits [2:0]) are ***not*** used.All other encodings are ***reserved***. ***Note:*** *This field should not be programmed with a value larger than that of field [19:17] (Multiple Message Capable). If the value of this field is larger than that of field [19:17], the Multiple Message Capable value takes effect.*	RW	Yes	000b
23	**MSI 64-Bit Address Capable** 0 = PEX 8649 is capable of generating MSI 32-bit addresses (**MSI Address** register, offset 4Ch, is the Message address) 1 = PEX 8649 is capable of generating MSI 64-bit addresses (**MSI Address** register, offset 4Ch, is the lower 32 bits of the Message address, and **MSI Upper Address** register, offset 50h, is the upper 32 bits of the Message address)	RO	Yes	1
24	**Per Vector Masking Capable** 0 = PEX 8649 does not have Per Vector Masking capability 1 = PEX 8649 has Per Vector Masking capability	RO	Yes	1
31:25	***Reserved***	RsvdP	No	0-0h

Register 15-18. 58h MSI Mask

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
	The interrupt sources in the NT Port are grouped into four categories – Power Management/Link State events, Device-Specific NT-Link Port events, GPIO-generated interrupts, and NT-Virtual Doorbell-generated interrupts. The number of allocated MSI Vectors is determined by the **MSI Control** register *Multiple Message Capable* and *Multiple Message Enable* fields (offset 48h[19:17 and 22:20], respectively). When the number of MSI Vectors that can be requested is: • **Four** – Each interrupt category generates its own MSI Vector • **Two** – Device-Specific NT-Link Port events generate their own MSI Vector, while the other categories are combined and generate the same Vector • **One** – All interrupt categories generate the same MSI Vector ***Note:*** *The offset for this register changes from 58h, to 54h, when the **MSI Control** register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.* *The bits in this register can be used to mask their respective **MSI Status** register bits (offset 5Ch).*				
0	**MSI Mask for Link State Events** MSI mask for Power Management event- or Link State event-generated interrupts.	Offset 48h[22:20]≥010b	RW	Yes	0
	MSI Mask for Shared Interrupt Sources MSI mask for all interrupt sources when the **MSI Control** register *Multiple Message Enable* field indicates that the Host has allocated one or two Vectors.	Offset 48h[22:20]≤001b	RW	Yes	0
1	**MSI Mask for Device-Specific NT-Link Port Events** MSI mask for Device-Specific NT-Link Port event-generated interrupts. Enables MSIs for the following NT-Link Port events, defined in the **Link Error Status Virtual** and **Link Error Mask Virtual** registers (NT Port Virtual Interface, offsets FE0h and FE4h, respectively): • NT-Link Port Correctable error (NT Port Link Interface, offset FC4h) • NT-Link Port Uncorrectable error (NT Port Link Interface, offset FB8h) • NT-Link Port Data Link Layer State change • NT-Link Port received (and consequently dropped) a Fatal or Non-Fatal Error Message	Offset 48h[22:20]≥001b	RW	Yes	0
	Reserved	Offset 48h[22:20]=000b	RsvdP	No	0
2	**MSI Mask for GPIO-Generated Interrupts**	Offset 48h[22:20]≥010b	RW	Yes	0
	Reserved	Offset 48h[22:20]≤001b	RsvdP	No	0
3	**MSI Mask for NT-Virtual Doorbell-Generated Interrupts** Refer to NT Port registers located at offsets C4Ch through C58h.	Offset 48h[22:20]≥010b	RW	Yes	0
	Reserved	Offset 48h[22:20]≤001b	RsvdP	No	0
31:4	***Reserved***		RsvdP	No	0000_000h

Register 15-19. 5Ch MSI Status

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
	The interrupt sources in the NT Port are grouped into four categories – Power Management/Link State events, Device-Specific NT-Link Port events, GPIO-generated interrupts, and NT-Virtual Doorbell-generated interrupts. The number of allocated MSI Vectors is determined by the **MSI Control** register *Multiple Message Capable* and *Multiple Message Enable* fields (offset 48h[19:17 and 22:20], respectively). When the number of MSI Vectors that can be requested is: • **Four** – Each interrupt category generates its own MSI Vector • **Two** – Device-Specific NT-Link Port events generate their own MSI Vector, while the other categories are combined and generate the same Vector • **One** – All interrupt categories generate the same MSI Vector ***Note:*** *The offset for this register changes from 5Ch, to 58h, when the **MSI Control** register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.* *The bits in this register can be masked by their respective **MSI Mask** register bits (offset 58h).*				
0	**MSI Pending Status for Link State Events** MSI pending status for Power Management event- or Link State event-generated interrupts.	Offset 48h[22:20]≥010b	RO	No	0
	MSI Pending Status for Shared Interrupt Sources MSI pending status for all interrupt sources when the **MSI Control** register *Multiple Message Enable* field indicates that the Host has allocated one or two Vectors.	Offset 48h[22:20]≤001b	RO	No	0
1	**MSI Pending Status for Device-Specific Error Triggered Event** Indicates the MSI pending status for the Device-Specific NT-Link Port event-generated interrupts defined in the **Link Error Status Virtual** and **Link Error Mask Virtual** registers (NT Port Virtual Interface, offsets FE0h and FE4h, respectively): • NT-Link Port Correctable error (NT Port Link Interface, offset FC4h) • NT-Link Port Uncorrectable error (NT Port Link Interface, offset FB8h) • NT-Link Port Data Link Layer State change • NT-Link Port received (and consequently dropped) a Fatal or Non-Fatal Error Message	Offset 48h[22:20]≥001b	RO	No	0
	Reserved	Offset 48h[22:20]=000b	RsvdP	No	0
2	**MSI Pending Status for GPIO-Generated Interrupts**	Offset 48h[22:20]≥010b	RO	No	0
	Reserved	Offset 48h[22:20]≤001b	RsvdP	No	0
3	**MSI Pending Status for NT-Virtual Doorbell-Generated Interrupts** Refer to NT Port registers located at offsets C4Ch through C58h.	Offset 48h[22:20]≥010b	RO	No	0
	Reserved	Offset 48h[22:20]≤001b	RsvdP	No	0
31:4	***Reserved***		RsvdP	No	0000_000h

15.8 NT Port Virtual Interface PCI Express Capability Registers (Offsets 68h – A0h)

The registers detailed in Section 13.10, "PCI Express Capability Registers (Offsets 68h – A0h)," are also applicable to the NT Port Virtual Interface, except as defined in Table 15-5 (register map; offsets 7Ch, 80h, 8Ch, and 90h are ***reserved***), and Register 15-20 through Register 15-25.

Table 15-5. NT Port Virtual Interface PCI Express Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Express Capability	Next Capability Pointer (A4h)	Capability ID (10h)	68h
Device Capability			6Ch
Device Status	***Not Supported/Reserved***	Device Control	70h
Link Capability			74h
Link Status	***Reserved***	Link Control	78h
Reserved			7Ch – 94h
Link Status 2	Link Control 2		98h
Reserved			9Ch – A0h

Register 15-20. 68h PCI Express Capability List and Capability

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
	PCI Express Capability List			
7:0	**Capability ID** Program to 10h, by default, as required by the *PCI Express Base r2.0*.	RO	Yes	10h
15:8	**Next Capability Pointer** Program to A4h, to point to the **Subsystem Capability** structure.	RO	Yes	A4h
	PCI Express Capability			
19:16	**Capability Version** The PEX 8649 NT Port Virtual Interface programs this field to 2h, as required by the *PCI Express Base r2.0*.	RO	Yes	2h
23:20	**Device/Port Type** Default = PCI Express endpoint device.	RO	Yes	0h
24	**Slot Implemented** ***Not valid for PCI Express endpoint devices***	RsvdP	No	0
29:25	**Interrupt Message Number** The serial EEPROM writes 00_000b, because the Base Message and MSI Messages are the same.	RO	Yes	00_000b
31:30	***Reserved***	RsvdP	No	00b

Register 15-21. 6Ch Device Capability

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
2:0	**Maximum Payload Size Supported** Maximum Payload Size Port limitations are as follows: • 2,048 bytes if the number of Ports is ≤ 6 • 1,024 bytes if the number of Ports is > 6 and ≤ 12 000b = NT Port Virtual Interface supports a 128-byte maximum payload 001b = NT Port Virtual Interface supports a 256-byte maximum payload 010b = NT Port Virtual Interface supports a 512-byte maximum payload 011b = NT Port Virtual Interface supports a 1,024-byte maximum payload 100b = NT Port Virtual Interface supports a 2,048-byte maximum payload No other encodings are supported.	HwInit	Yes	011b = > 6 and ≤ 12 Ports 100b = ≤ 6 Ports
4:3	**Phantom Functions Supported** ***Not supported***	RO	Yes	00b
5	**Extended Tag Field Supported** 0 = Maximum *Tag* field is 5 bits 1 = Maximum *Tag* field is 8 bits	RO	Yes	0
8:6	**Endpoint L0s Acceptable Latency** 111b = No Limit	RO	Yes	111b
11:9	**Endpoint L1 Acceptable Latency** 111b = No Limit	RO	Yes	111b
14:12	***Reserved***	RsvdP	No	000b
15	**Role-Based Error Reporting**	RO	Yes	1
17:16	***Reserved***	RsvdP	No	00b
25:18	**Captured Slot Power Limit Value** For the NT Port Virtual Interface, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [27:26] (*Captured Slot Power Limit Scale*).	RO	Yes	00h
27:26	**Captured Slot Power Limit Scale** For the NT Port Virtual Interface, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [25:18] (*Captured Slot Power Limit Value*). 00b = 1.0 01b = 0.1 10b = 0.01 11b = 0.001	RO	Yes	00b
31:28	***Reserved***	RsvdP	No	0h

Register 15-22. 70h Device Status and Control

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
Device Control				
0	**Correctable Error Reporting Enable** 0 = Disables 1 = Enables the NT Port Virtual Interface to report Correctable errors to the Local Host	RW	Yes	0
1	**Non-Fatal Error Reporting Enable** 0 = Disables 1 = Enables the NT Port Virtual Interface to report Non-Fatal errors to the Local Host	RW	Yes	0
2	**Fatal Error Reporting Enable** 0 = Disables 1 = Enables the NT Port Virtual Interface to report Fatal errors to the Local Host	RW	Yes	0
3	**Unsupported Request Reporting Enable** 0 = Disables 1 = Enables the NT Port Virtual Interface to report UR errors to the Local Host	RW	Yes	0
4	**Enable Relaxed Ordering** ***Not supported***	RsvdP	No	0
7:5	**Maximum Payload Size** The NT Port Virtual Interface power-on/reset value is 000b, to support a Maximum Payload Size of 128 bytes. Software can change this field to configure the NT Port Virtual Interface to support other Payload sizes; however, software cannot change this field to a value larger than that indicated by the **Device Capability** register *Maximum Payload Size Supported* field (offset 6Ch[2:0]), for the NT Port Virtual and Link Interfaces. (Requester and Completer domains must possess the same Maximum Payload Size.) 000b = NT Port Virtual Interface supports a 128-byte maximum payload 001b = NT Port Virtual Interface supports a 256-byte maximum payload 010b = NT Port Virtual Interface supports a 512-byte maximum payload 011b = NT Port Virtual Interface supports a 1,024-byte maximum payload 100b = NT Port Virtual Interface supports a 2,048-byte maximum payload No other encodings are supported. ***Note:*** *Software must halt all transactions through the NT Port before changing this field.*	RW	Yes	000b
8	**Extended Tag Field Enable** ***Not supported***	RsvdP	No	0
9	**Phantom Functions Enable** ***Not supported***	RsvdP	No	0
10	**AUX Power PM Enable** ***Not supported***	RsvdP	No	0
11	**Enable No Snoop** ***Not supported***	RsvdP	No	0
14:12	**Maximum Read Request Size** ***Not supported***	RsvdP	No	000b
15	***Reserved***	RsvdP	No	0

Register 15-22. 70h Device Status and Control *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
	Device Status			
16	**Correctable Error Detected** 0 = NT Port Virtual Interface did not detect a Correctable error 1 = NT Port Virtual Interface detected a Correctable error, regardless of the bit 0 (*Correctable Error Reporting Enable*) state	RW1C	Yes	0
17	**Non-Fatal Error Detected** 0 = NT Port Virtual Interface did not detect a Non-Fatal error 1 = NT Port Virtual Interface detected a Non-Fatal error, regardless of the bit 1 (*Non-Fatal Error Reporting Enable*) state	RW1C	Yes	0
18	**Fatal Error Detected** 0 = NT Port Virtual Interface did not detect a Fatal error 1 = NT Port Virtual Interface detected a Fatal error, regardless of the bit 2 (*Fatal Error Reporting Enable*) state	RW1C	Yes	0
19	**Unsupported Request Detected** 0 = NT Port Virtual Interface did not detect a UR 1 = NT Port Virtual Interface detected a UR, regardless of the bit 3 (*Unsupported Request Reporting Enable*) state	RW1C	Yes	0
20	**AUX Power Detected** ***Not supported***	RsvdP	No	0
21	**Transactions Pending** ***Not supported*** Because the PEX 8649 NT Port is a bridging device, it does not track Completion for the corresponding Non-Posted transactions. Therefore, the NT Port Virtual Interface does not implement Transactions Pending.	RsvdP	No	0
31:22	***Reserved***	RsvdP	No	0-0h

Register 15-23. 74h Link Capability

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
3:0	**Supported Link Speeds** Indicates the NT Port Virtual Interface's supported Link speed. 0001b = 2.5 GT/s Link speed is supported 0010b = 5.0 GT/s and 2.5 GT/s Link speeds are supported All other encodings are ***reserved***.	RO	Yes	0010b (STRAP_RESERVED17#=H) 0001b (STRAP_RESERVED17#=L)
9:4	**Maximum Link Width** The PEX 8649 maximum Link width is x16 = 01_0000b. Actual maximum Link width is Set by the STRAP_STN*x*_PORTCFG*x* balls. 00_0000b = ***Reserved*** 00_0001b = x1 00_0010b = x2 00_0100b = x4 00_1000b = x8 01_0000b = x16 All other encodings are ***not supported***.	ROS	No	Set by STRAP_STN*x*_PORTCFG*x* ball levels, or by serial EEPROM value for the **Port Configuration**-related registers (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offsets 300h through 308h)
11:10	**Active State Power Management (ASPM) Support** Active State Link PM support. Indicates the level of ASPM supported by the Port. 01b = L0s Link PM state entry is supported 11b = L0s and L1 Link PM states are supported All other encodings are ***reserved***.	RO	Yes	01b

Register 15-23. 74h Link Capability *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
14:12	**L0s Exit Latency** Indicates the L0s Link PM state exit latency for the given PCI Express Link. Value depends upon the Port's **Synchronous Advertised N_FTS** or **Asynchronous Advertised N_FTS** register (Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface, offset B84h or B88h, respectively) *Port x Advertised N_FTS* field value, Link speed, and state of the Port's **Link Control** register *Common Clock Configuration* bit (offset 78h[6]). When the *Common Clock Configuration* bit is Set, the Synchronous Advertised N_FTS register value is used; otherwise, the Asynchronous Advertised N_FTS register value is used. Exit latency is calculated, as follows: • **2.5 GHz** – Multiply *Port x Advertised N_FTS* x 4 (4 symbol times in 1 N_FTS) x 4 ns (1 symbol time at 2.5 GT/s) • **5.0 GHz** – Multiply *Port x Advertised N_FTS* x 4 (4 symbol times in 1 N_FTS) x 2 ns (1 symbol time at 5.0 GT/s) 100b = NT Port Virtual Interface L0s Link PM state Exit Latency is 512 ns to less than 1 µs at 5.0 GT/s 101b = NT Port Virtual Interface L0s Link PM state Exit Latency is 1 µs to less than 2 µs at 2.5 GT/s All other encodings are ***reserved***. ***Note:*** *The NT Port Virtual Interface never enters the L0s Link PM state, because there is no physical Link attached to it.*	RO	No	100b (5.0 GT/s) 101b (2.5 GT/s)
17:15	**L1 Exit Latency** Indicates the L1 Link PM state exit latency for the given PCI Express Link. Value depends upon the Link speed. 001b = NT Port Link Interface L1 Link PM state Exit Latency is 1 µs to less than 2 µs at 5.0 GT/s 010b = NT Port Link Interface L1 Link PM state Exit Latency is 2 µs to less than 4 µs at 2.5 GT/s All other encodings are ***reserved***. ***Note:*** *The NT Port Virtual Interface never enters the L1 Link PM state, because there is no physical Link attached to it.*	RO	Yes	001b (5.0 GT/s) 010b (2.5 GT/s)
18	**Clock Power Management**	RO	Yes	0
23:19	***Reserved***	RsvdP	No	0-0h

Register 15-23. 74h Link Capability *(Cont.)*

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I²C</th><th>Default</th></tr>
<tr><td>31:24</td><td><b>NT Port Number</b>
The NT Port Number value is selected by the STRAP_NT_UPSTRM_PORTSEL[4, 2:0] Strapping balls. All other encodings are <b><i>reserved</i></b>.
<table>
<tr><th>Field Value</th><th>Strapping Ball Value</th><th>Port Number</th></tr>
<tr><td>00h</td><td>0000b (LLLL)</td><td>0</td></tr>
<tr><td>01h</td><td>0001b (LLLH)</td><td>1</td></tr>
<tr><td>02h</td><td>0010b (LLHL)</td><td>2</td></tr>
<tr><td>03h</td><td>0011b (LLHH)</td><td>3</td></tr>
<tr><td>08h</td><td>1000b (HLLL)</td><td>16</td></tr>
<tr><td>09h</td><td>1001b (HLLH)</td><td>17</td></tr>
<tr><td>0Ah</td><td>1010b (HLHL)</td><td>18</td></tr>
<tr><td>0Bh</td><td>1011b (HLHH)</td><td>19</td></tr>
<tr><td>0Ch</td><td>1100b (HHLL)</td><td>20</td></tr>
<tr><td>0Dh</td><td>1101b (HHLH)</td><td>21</td></tr>
<tr><td>0Eh</td><td>1110b (HHHL)</td><td>22</td></tr>
<tr><td>0Fh</td><td>1111b (HHHH)</td><td>23</td></tr>
</table></td><td>ROS</td><td>No</td><td>Set by STRAP_NT_UPSTRM_PORTSEL[4, 2:0] ball levels</td></tr>
</table>

Register 15-24. 78h Link Status and Control

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Link Control				
1:0	**Active State Power Management (ASPM) Control** The NT Port Virtual Interface ignores this register value, because no external Port connection exists.	RW	Yes	00b
2	***Reserved***	RsvdP	No	0
3	**Read Request Return Parameter Control** Read Request Return Parameter “R” control. Read Completion Boundary (RCB).	RO	Yes	0
4	**Link Disable** ***Reserved*** for the NT Port Virtual Interface.	RsvdP	No	0
5	**Retrain Link** ***Reserved*** for the NT Port Virtual Interface.	RsvdP	No	0
6	**Common Clock Configuration** The NT Port Virtual Interface ignores this register value, because no external Port connection exists.	RW	Yes	0
7	**Extended Sync** The NT Port Virtual Interface ignores this register value, because no external Port connection exists.	RW	Yes	0
15:8	***Reserved***	RsvdP	No	00h

Register 15-24. 78h Link Status and Control *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	Link Status			
19:16	**Current Link Speed** Indicates the negotiated Link speed of the Port's PCI Express Link. 0001b = 2.5 GT/s Link speed 0010b = 5.0 GT/s Link speed All other encodings are ***reserved***. The value in this field is undefined when the Link is not up.	RO	No	0001b
25:20	**Negotiated Link Width** Reports the Link status of the NT Port Link Interface. Dependent upon the configuration of the physical Ports. Link width is determined by the negotiated value with the attached Lane/Port. If the Link is not up, the value of this field is undefined. 00_0000b = Link is down (default) 00_0001b = x1 00_0010b = x2 00_0100b = x4 00_1000b = x8 01_0000b = x16 All other encodings are ***not supported***.	RO	No	00_0000b
26	***Reserved***	RsvdP	No	0
27	**Link Training** ***Reserved*** for the NT Port Virtual Interface. Always read as 0.	RsvdP	No	0
28	**Slot Clock Configuration** Because there is no external connection to the NT Port Virtual Interface, this bit is always Cleared, which indicates that the PEX 8649 uses an independent clock.	HwInit	Yes	0
31:29	***Reserved***	RsvdP	No	000b

Register 15-25. 98h Link Status and Control 2

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Link Control 2				
3:0	**Target Link Speed** 0001b = 2.5 GT/s Link speed is supported 0010b = 5.0 GT/s Link speed is supported All other encodings are ***reserved***.	RWS	Yes	0010b
4	**Enter Compliance**	RWS	Yes	0
5	**Hardware Autonomous Speed Disable** ***Reserved*** Initial transition to the highest supported common Link speed is not blocked by this bit.	RsvdP	No	0
6	**Selectable De-Emphasis** ***Reserved***	RsvdP	Yes	0
9:7	**Transmit Margin** Intended for debug and compliance testing only.	RWS	Yes	000b
10	**Enter Modified Compliance**	RWS	Yes	0
11	**Compliance SOS** 1 = Link Training and Status State Machine (LTSSM) must periodically send SKIP Ordered-Sets between sequences when sending the Compliance Pattern or Modified Compliance Pattern	RWS	Yes	0
12	**Compliance De-Emphasis** Sets the de-emphasis level in the *Polling.Compliance* state, if the entry occurred due to bit 4 (*Enter Compliance*) being Set.	RWS	Yes	0
15:13	***Reserved***	RsvdP	No	000b
Link Status 2				
16	**Current De-Emphasis Level** Reflects the de-emphasis level. 0 = -6 dB (Link is operating at 5.0 GT/s) 1 = -3.5 dB	RO	Yes	0 (5.0 GT/s) 1 (2.5 GT/s)
31:17	***Reserved***	RsvdP	No	0-0h

15.9 NT Port Virtual Interface Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – C4h)

The registers detailed in Section 13.11, "Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – FCh)," are also applicable to the NT Port, except as defined in Table 15-6 (register map) and Register 15-26.

Table 15-6. NT Port Virtual Interface Subsystem ID and Subsystem Vendor ID Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved	Next Capability Pointer (C8h)	SSID/SSVID Capability ID (0Dh)	A4h
Subsystem ID	Subsystem Vendor ID		A8h
Reserved			ACh – C4h

Register 15-26. A4h Subsystem Capability

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**SSID/SSVID Capability ID** SSID/SSVID registers for the PCI-to-PCI bridge. Program to 0Dh, as required by the *PCI-to-PCI Bridge r1.2*.	RO	Yes	0Dh
15:8	**Next Capability Pointer** Program to C8h, to point to the **Vendor-Specific Capability 3** structure.	RO	Yes	C8h
31:16	***Reserved***	RsvdP	No	0000h

15.10 NT Port Virtual Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)

This section details the NT Port Virtual Interface Vendor-Specific Capability 3 registers, which include the **Memory BAR*x* Setup** registers and **Configuration Address** and **Data Window** registers. Table 15-7 defines the register map used by the NT Port Virtual Interface.

The Cursor Mechanism registers at offsets F8h and FCh provide a means for accessing PCI Express Extended Configuration Space registers (offsets 100h through FFFh) within the NT Port Virtual and Link Interfaces, when only standard PCI Configuration transactions (that do not support the *Extended Register Number* field within the Completion Request Header) are available. The Cursor Mechanism can generally access only those registers that are defined by the *PCI Express Base r2.0*, and not the Device-Specific registers. However, if Port 0 is the NT Port, the Cursor Mechanism in the NT Port Virtual Interface registers can also access the Device-Specific registers.

Table 15-7. NT Port Virtual Interface Vendor-Specific Capability 3 Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16		15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Reserved	Vendor-Specific Capability 3	Next Capability Pointer (00h)	Capability ID 3 (09h)	C8h
Vendor-Specific Header 3 ***(Reserved)***				CCh
NT Port Virtual Interface BAR0/1 Setup				D0h
NT Port Virtual Interface Memory BAR2 Setup				D4h
NT Port Virtual Interface Memory BAR2/3 Setup				D8h
NT Port Virtual Interface Memory BAR4 Setup				DCh
NT Port Virtual Interface Memory BAR4/5 Setup				E0h
Reserved				E4h – F4h
Configuration Address Window		***Reserved***		F8h
Configuration Data Window				FCh

Register 15-27. C8h Vendor-Specific Capability 3

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
7:0	**Capability ID 3**	RO	Yes	09h
15:8	**Next Capability Pointer** 00h = This capability is the last capability in the Linked List	RO	Yes	00h
23:16	**Length** Number of bytes in this Capability structure.	RO	Yes	38h
31:24	***Reserved***	RsvdP	No	00h

Register 15-28. CCh Vendor-Specific Header 3

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	***Reserved***	RO	Yes	0380_0002h

Register 15-29. D0h NT Port Virtual Interface BAR0/1 Setup

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
1:0	**BAR0/1 Enable** 00b = Disables Virtual Interface **BAR0** and **BAR1** 01b = ***Reserved*** 10b = Enables Virtual Interface **BAR0** and disables **BAR1** (**BAR0** is a 32-bit BAR) 11b = Enables Virtual Interface **BAR0** and **BAR1** (**BAR0/1** is a 64-bit BAR)	RW	Yes	10b
2	**BAR0 Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RW	Yes	0
31:3	***Reserved***	RsvdP	No	0-0h

Register 15-30. D4h NT Port Virtual Interface Memory BAR2 Setup

Bit(s)	Description		Type	Serial EEPROM and I²C	Default
0	**Type Selector**		RsvdP	No	0
2:1	**BAR2 Type** 00b = **BAR2** is implemented as a 32-bit Memory BAR 10b = **BAR2/3** is implemented as a 64-bit Memory BAR No other encodings are allowed.		RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***		RsvdP	No	0_000h
30:20	**BAR2 Size** Specifies the Address Range size requested by **BAR2**. 0 = Corresponding **BAR2** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR2** bits are RW bits ***Note:*** *If BAR[30:n] is the Base field (BAR size is* 2^n*), BAR[30:n] should have all ones (1).*		RW	Yes	0-0h
31	**BAR2 Enable** 0 = **BAR2** is disabled, all **BAR2** bits read 0 1 = **BAR2** is enabled	Field [2:1] (*BAR2 Type*) = 00b	RW	Yes	0
	BAR2 Size Included with field [30:20] when this BAR is used as a 64-bit BAR.	Field [2:1] (*BAR2 Type*) = 10b	RW	Yes	0

Register 15-31. D8h NT Port Virtual Interface Memory BAR2/3 Setup

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
0	**Type Selector**		RsvdP	No	0
2:1	**BAR3 Type** 00b = Selects 32-bit Memory BAR (**BAR3**) No other encodings are allowed.		RO	No	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***	Offset D4h[2:1] (*BAR2 Type*) = 00b	RsvdP	No	0_000h
	When **BAR2/3** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset D4h[2:1] (*BAR2 Type*) = 10b	RW	Yes	0_000h
30:20	**BAR3 Size** Specifies the Address Range size requested by **BAR3**. 0 = Corresponding **BAR3** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR3** bits are RW bits ***Note:*** *If BAR[30:n] is the Base field (BAR size is* 2^n*), BAR[30:n] should have all ones (1).*		RW	Yes	0-0h
31	**BAR3 Enable** **32-Bit BAR** 0 = **BAR3** is disabled 1 = **BAR3** is enabled as a 32-bit BAR	Offset D4h[2:1] (*BAR2 Type*) = 00b	RW	Yes	0
	64-Bit BAR 0 = **BAR2/3** is disabled, all **BAR2/3** bits read 0 1 = **BAR2/3** is enabled as a 64-bit BAR	Offset D4h[2:1] (*BAR2 Type*) = 10b	RW	Yes	0

Register 15-32. DCh NT Port Virtual Interface Memory BAR4 Setup

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
0	**Type Selector**		RsvdP	No	0
2:1	**BAR4 Type** 00b = **BAR4** is implemented as a 32-bit Memory BAR (**BAR4**) 10b = **BAR4/5** is implemented as a 64-bit Memory BAR (**BAR4/5**) No other encodings are allowed.		RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***		RsvdP	No	0_000h
30:20	**BAR4 Size** Specifies the Address Range size requested by **BAR4**. 0 = Corresponding **BAR4** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR4** bits are RW bits ***Note:*** *If BAR[30:n] is the Base field (BAR size is 2^n), BAR[30:n] should have all ones (1).*		RW	Yes	0-0h
31	**BAR4 Enable** 0 = **BAR4** is disabled, all **BAR4** bits read 0 1 = **BAR4** is enabled	Field [2:1] (*BAR4 Type*) = 00b	RW	Yes	0
	BAR4 Size Included with field [30:20] when this BAR is used as a 64-bit BAR.	Field [2:1] (*BAR4 Type*) = 10b	RW	Yes	0

Register 15-33. E0h NT Port Virtual Interface Memory BAR4/5 Setup

Bit(s)	Description		Type	Serial EEPROM and I^{2}C	Default
0	**Type Selector**		RsvdP	No	0
2:1	**BAR5 Type** 00b = Selects 32-bit Memory BAR (**BAR5**) No other encodings are allowed.		RO	No	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***	Offset DCh[2:1] (*BAR4 Type*) = 00b	RsvdP	No	0_000h
	When **BAR4/5** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset DCh[2:1] (*BAR4 Type*) = 10b	RW	Yes	0_000h
30:20	**BAR5 Size** Specifies the Address Range size requested by **BAR5**. 0 = Corresponding **BAR5** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR5** bits are RW bits ***Note:*** *If BAR[30:n] is the Base field (BAR size is* 2^n*), BAR[30:n] should have all ones (1).*		RW	Yes	0-0h
31	**BAR5 Enable** **32-Bit BAR** 0 = **BAR5** is disabled 1 = **BAR5** is enabled as a 32-bit BAR	Offset DCh[2:1] (*BAR4 Type*) = 00b	RW	Yes	0
	64-Bit BAR 0 = **BAR4/5** is disabled, all **BAR4/5** bits read 0 1 = **BAR4/5** is enabled as a 64-bit BAR	Offset DCh[2:1] (*BAR4 Type*) = 10b	RW	Yes	0

Register 15-34. F8h Configuration Address Window (Device-Specific Cursor Mechanism)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
15:0	***Reserved***	RsvdP	No	0000h
25:16	**Register Offset**	RW	Yes	0-0h
30:26	***Reserved***	RsvdP	No	0-0h
31	**Interface Select** 0 = Access is to the NT Port Link Interface Type 0 Configuration Space register 1 = Access is to the NT Port Virtual Interface Type 0 Configuration Space register	RW	Yes	0

Register 15-35. FCh Configuration Data Window (Device-Specific Cursor Mechanism)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
31:0	**Register Data** Software selects a register by writing into the NT Port Virtual Interface Configuration Address window, then reads from or writes to that register using this register.	RW	Yes	0000_0000h

15.11 NT Port Virtual Interface Device Serial Number Extended Capability Registers (Offsets 100h – 134h)

The registers detailed in Section 13.12, “Device Serial Number Extended Capability Registers (Offsets 100h – 134h),” are also applicable to the NT Port. Table 15-8 defines the register map used by all Ports.

Table 15-8. NT Port Virtual Interface Device Serial Number Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (FB4h)	Capability Version (1h)	PCI Express Extended Capability ID (0003h)	100h
Serial Number (Lower DW)			104h
Serial Number (Upper DW)			108h
Reserved		10Ch –	134h

15.12 NT Port Virtual Interface Power Budget Extended Capability Registers (Offsets 138h – 144h)

The registers detailed in Section 13.13, “Power Budget Extended Capability Registers (Offsets 138h – 144h),” are also applicable to the NT Port. Table 15-9 defines the register map used by all upstream Ports.

Table 15-9. NT Port Virtual Interface Power Budget Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Next Capability Offset (148h)	Capability Version (1h)	PCI Express Extended Capability ID (0004h)		138h
Reserved			Data Select	13Ch
Power Budget Data				140h
Power Budget Capability				144h

15.13 NT Port Virtual Interface Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)

The registers detailed in Section 13.14, "Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)," are also applicable to the NT Port Virtual Interface, except as defined in Table 15-10 (register map), and Register 15-36 and Register 15-37.

Table 15-10. NT Port Virtual Interface Virtual Channel Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16		15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset 2 (C34h)	Capability Version (1h)	PCI Express Extended Capability ID (0002h)	148h
Port VC Capability 1			14Ch
Port VC Capability 2			150h
Port VC Status ***(Reserved)***		Port VC Control	154h
VC0 Resource Capability			158h
VC0 Resource Control			15Ch
VC0 Resource Status		***Reserved***	160h
Reserved			164h – 174h
WRR Port Arbitration Table Registers (Offsets 178h – 1BCh) (Legacy NT Mode) ***Reserved*** (NT PCI-to-PCI Bridge Mode)			178h … 1BCh

Register 15-36. 148h Virtual Channel Extended Capability Header

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
15:0	**PCI Express Extended Capability ID** Program to 0002h, as required by the *PCI Express Base r2.0*.	RO	No	0002h
19:16	**Capability Version** Program to 1h, as required by the *PCI Express Base r2.0*.	RO	No	1h
31:20	**Next Capability Offset 2** Next extended capability is the **Vendor-Specific Extended Capability 2** structure, offset C34h.	RO	Yes	C34h

Register 15-37. 160h VC0 Resource Status

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	***Reserved***	RsvdP	No	0000h
16	**Port Arbitration Table Status** 0 = Hardware has finished loading values stored in the Port Arbitration Table, after software Sets the **VC0 Resource Control** register *Load Port Arbitration Table* bit (offset 15Ch[16]), or if the Port Arbitration Table is not implemented, then this bit is ***reserved*** 1 = Software updates to WRR Port Arbitration Table are pending update to the functional logic	RO	No	0
17	**VC0 Negotiation Pending** 0 = VC0 negotiation completed (NT Port Virtual Interface Link to the internal virtual PCI Bus is up) 1 = VC0 initialization is not complete for the NT Port Virtual Interface	RO	Yes	0
31:18	***Reserved***	RsvdP	No	0-0h

15.14 NT Port Virtual Interface Device-Specific Registers (Offsets 1C0h – C88h)

The registers detailed in Section 13.15, "Device-Specific Registers (Offsets 1C0h – DFCh)" (for offsets 1C0h through C88h), are unique to the PEX 8649 and not referenced in the *PCI Express Base r2.0*. These registers are also applicable to the NT Port Virtual Interface, except as defined in Table 15-11 (register map; offsets 900h through 9ECh, and A34h through B6Ch, are ***reserved***; offsets C34h through C88h are ***not*** reserved) through Table 15-16, and Register 15-38 through Register 15-61.

Other NT Port Virtual Interface Device-Specific registers are detailed in:

- Section 15.16, "NT Port Virtual Interface Device-Specific Registers (Offsets F30h – FB0h)"
- Section 15.18, "NT Port Virtual Interface Device-Specific Registers – Link Error (Offsets FE0h – FFCh)"

Note: It is recommended that these registers not be changed from their default values.

Table 15-11. NT Port Virtual Interface Device-Specific Register Map (Offsets 1C0h – C88h)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved	1C0h – 1CCh
NT Port Virtual Interface Device-Specific Registers – Read Pacing (Offsets 1D0h – 1D8h)	1D0h … 1D8h
Device-Specific Registers – Captured Bus and Device Numbers (Offsets 1DCh – 1FCh)	1DCh … 1FCh
Device-Specific Registers – Physical Layer (Offsets 200h – 25Ch)	200h … 25Ch
Device-Specific Registers – Serial EEPROM (Offsets 260h – 26Ch) (Legacy NT Mode) ***Reserved*** (NT PCI-to-PCI Bridge Mode)	260h … 26Ch
Reserved	270h – 28Ch
NT Port Virtual Interface Device-Specific Registers – I^{2}C and SMBus Slave Interfaces (Offsets 290h – 2FCh)	290h … 2FCh

Table 15-11. NT Port Virtual Interface Device-Specific Register Map (Offsets 1C0h – C88h) *(Cont.)*

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16		15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Device-Specific Registers – Port Configuration (Offsets 300h – 31Ch)			300h … 31Ch
Device-Specific Registers – Error Checking and Debug (Offsets 320h – 350h)			320h … 350h
NT Port Virtual Interface Device-Specific Registers – Port Configuration (Offsets 354h – 3ACh)			354h … 3ACh
Reserved			3B0h – 4D8h
Factory Test Only			4DCh – 5FCh
Device-Specific Registers – General-Purpose Input/Output (Offsets 600h – 68Ch) (Legacy NT Mode) ***Reserved*** (NT PCI-to-PCI Bridge Mode)			600h … 68Ch
Factory Test Only/Reserved			690h – 6FCh
Device-Specific Registers – Error Checking and Debug (Offsets 700h – 75Ch) (Legacy NT Mode) ***Reserved*** (NT PCI-to-PCI Bridge Mode)			700h … 75Ch
Device-Specific Registers – Control (Offsets 760h – 774h), Base Mode Only			760h … 774h
Device-Specific Registers – Soft Error (Offsets 778h – 8FCh)			778h … 8FCh
Reserved			900h – 9ECh
NT Port Virtual Interface Device-Specific Registers – Ingress Credit Handler (Offsets 9F0h – A2Ch)			9F0h … A2Ch
Device-Specific Registers – Virtual Switch Debug and GPIO Status and Control (Offsets A30h – B6Ch)[a]			A30h … B6Ch
Next Capability Offset 2 (000h)	1h	PCI Express Extended Capability ID 2 (000Bh)	B70h
Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets B70h – B7Ch)			… B7Ch

Table 15-11. NT Port Virtual Interface Device-Specific Register Map (Offsets 1C0h – C88h) *(Cont.)*

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16		15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Device-Specific Registers – Physical Layer (Offsets B80h – BC8h)			B80h … BC8h
Factory Test Only			BCCh – BFCh
Reserved			C00h – C30h
Next Capability Offset 4 (B70h)	1h	PCI Express Extended Capability ID 4 (000Bh)	C34h
NT Port Virtual Interface Device-Specific Registers – Vendor-Specific Extended Capability 4 (Offsets C34h – C88h)			… C88h

a. Register offsets A34h through B6Ch are reserved in NT mode.

15.14.1 NT Port Virtual Interface Device-Specific Registers – Read Pacing (Offsets 1D0h – 1D8h)

The registers detailed in Section 13.15.1, "Device-Specific Registers – Read Pacing (Offsets 1D0h – 1D8h)," are also applicable to the NT Port Virtual Interface, except as defined in Table 15-12 (register map) and Register 15-38. The registers are located in one Port, per Station, as listed in Table 13-20 in Section 13.15.1, "Device-Specific Registers – Read Pacing (Offsets 1D0h – 1D8h)."

Read Pacing is described, in detail, in Section 8.5, "Read Pacing."

Table 15-12. NT Port Virtual Interface Device-Specific Read Pacing Register Map (Refer to Table 13-20)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Read Pacing Control	1D0h
Read Pacing Threshold 1	1D4h
Read Pacing Threshold 2	1D8h

Register 15-38. 1D8h Read Pacing Threshold 2 (Refer to Table 13-20)

Bit(s)	Descriptions	Ports	Type	Serial EEPROM and I^2C	Default
Note: *For bits [19:16], the Port 0 bits are for Ports 0, 1, 2, and 3. The Port 16 bits are for Ports 16, 17, 18, and 19. The Port 20 bits are for Ports 20, 21, 22, and 23.*					
12:0	**x4 Port Memory Read Outstanding Threshold** Specified in DWords. Default value of 400h Sets the threshold to 4 KB.		RWS	Yes	400h
15:13	***Reserved***		RsvdP	No	000b
16	**Port *x* Memory Read Outstanding Counter Reset** Provides a mechanism for Clearing the Counter when an error condition occurs, with either the device that issued the Read Request, or the device that was to provide the Read Completions, where a System Level Reset will not be issued. If the Counter is not Cleared after an error condition such as this, the threshold will not be accurate. 0 = Read Outstanding Counter value increments, with each outstanding Read 1 = Resets Read Outstanding Counter	0, 16, or 20	RZ	Yes	0
17		1 17, or 21	RZ	Yes	0
18		2, 18, or 22	RZ	Yes	0
19		3, 19, or 23	RZ	Yes	0
31:20	***Reserved***		RsvdP	No	000h

15.14.2 NT Port Virtual Interface Device-Specific Registers – I^{2}C and SMBus Slave Interfaces (Offsets 290h – 2FCh)

The registers detailed in Section 13.15.5, "Device-Specific Registers – I^{2}C and SMBus Slave Interfaces (Offsets 290h – 2FCh)," are also applicable to the NT Port Virtual Interface, except as defined in Table 15-13 (register map) and Register 15-39.

The I^{2}C/SMBus Slave Interface is described, in detail, in Chapter 7, "I^{2}C/SMBus Slave Interface Operation."

Table 15-13. NT Port Virtual Interface Device-Specific I^{2}C and SMBus Slave Interfaces Register Map (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Factory Test Only	290h
I^{2}C/SMBus Configuration	294h
Factory Test Only	298h – 2C4h
SMBus Configuration	2C8h
Reserved	2CCh – 2FCh

Register 15-39. 294h I^{2}C/SMBus Configuration (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default	
2:0	**Slave Address** Bits [6:0] comprise the I^{2}C/SMBus Slave address, 1Fh. The value is determined by bits [2:0] (which reflect the I2C_ADDR[2:0] ball states, and default to 111b, by virtue of weak internal pull-up resistors), combined with the value of bits [6:3] (which default to 0011b). ***Note:*** ***The I^{2}C/SMBus Slave address must not be changed by an I^{2}C/SMBus Write command.***	HwInit	Yes	111b	1Fh
6:3		RWS	Yes	0011b	
9:7	***Reserved***	RsvdP	No	000b	
10	***Factory Test Only***	RWS	Yes	0	
31:11	***Reserved***	RWS	Yes	0-0h	

15.14.3 NT Port Virtual Interface Device-Specific Registers – Port Configuration (Offsets 354h – 3ACh)

The registers detailed in Section 13.15.8, "Device-Specific Registers – Port Configuration (Offsets 354h – 3ACh)," are also applicable to the NT Port Virtual Interface, except as defined in Table 15-14 (register map; all but offsets 358h, 360h, 3A4h, and 3ACh are ***reserved***).

Other NT Port Virtual Interface Device-Specific Port Configuration registers are detailed in Section 13.15.6, "Device-Specific Registers – Port Configuration (Offsets 300h – 31Ch)."

Table 15-14. NT Port Virtual Interface Device-Specific Port Configuration Register Map (Offsets 354h – 3ACh) (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface)

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved				354h
Virtual Switch Enable				358h
Reserved				35Ch
VS0 Upstream				360h
Reserved				364h – 3A0h
Reserved	Parallel Hot Plug Control		***Reserved***	3A4h
Reserved				3A8h
Configuration Release				3ACh

15.14.4 NT Port Virtual Interface Device-Specific Registers – Ingress Credit Handler (Offsets 9F0h – A2Ch)

The registers detailed in Section 13.15.14, "Device-Specific Registers – Ingress Credit Handler (Offsets 9F0h – A2Ch)," are also applicable to the NT Port Link Interface. These registers for the NT Port Link Interface are implemented in the NT Port Virtual Interface registers, except as defined in Table 15-15 (register map; offsets 9F0h through 9FCh are ***reserved***).

Table 15-15. NT Port Virtual Interface Device-Specific INCH Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved				9F0h – 9FCh
INCH Threshold VC0 Posted				A00h
INCH Threshold VC0 Non-Posted				A04h
INCH Threshold VC0 Completion				A08h
Reserved				A0Ch – A2Ch

15.14.5 NT Port Virtual Interface Device-Specific Registers – Vendor-Specific Extended Capability 4 (Offsets C34h – C88h)

This section details the NT Port Virtual Interface Device-Specific, Vendor-Specific Extended Capability 4 registers, which include the **Memory BAR*x* Address Translation**, **Doorbell**, and **Scratchpad** registers. Table 15-16 defines the register map used by the NT Port Virtual Interface.

Table 15-16. NT Port Virtual Interface Device-Specific, Vendor-Specific Extended Capability 4 Register Map

31 30 29 28 27 26 25 24 23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset 4 (B70h)	Capability Version 4 (1h)	PCI Express Extended Capability ID 4 (000Bh)	C34h
Vendor-Specific Header 4			C38h
Memory BAR2 Address Translation Lower			C3Ch
Memory BAR3 Address Translation Upper			C40h
Memory BAR4 Address Translation Lower			C44h
Memory BAR5 Address Translation Upper			C48h
Reserved		Virtual Interface IRQ Set	C4Ch
Reserved		Virtual Interface IRQ Clear	C50h
Reserved		Virtual Interface IRQ Mask Set	C54h
Reserved		Virtual Interface IRQ Mask Clear	C58h
Reserved		Link Interface IRQ Set	C5Ch
Reserved		Link Interface IRQ Clear	C60h
Reserved		Link Interface IRQ Mask Set	C64h
Reserved		Link Interface IRQ Mask Clear	C68h
NT Port SCRATCH0			C6Ch
NT Port SCRATCH1			C70h
NT Port SCRATCH2			C74h
NT Port SCRATCH3			C78h
NT Port SCRATCH4			C7Ch
NT Port SCRATCH5			C80h
NT Port SCRATCH6			C84h
NT Port SCRATCH7			C88h

Register 15-40. C34h Vendor-Specific Extended Capability 4

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
15:0	**PCI Express Extended Capability ID 4** Program to 000Bh, to indicate that the Extended Capability structure is the **Vendor-Specific Extended Capability** structure.	RO	Yes	000Bh
19:16	**Capability Version 4**	RO	Yes	1h
31:20	**Next Capability Offset 4** Program to B70h, which addresses the **Vendor-Specific Extended Capability 4** structure.	RO	Yes	B70h

Register 15-41. C38h Vendor-Specific Header 4

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
15:0	**Vendor-Specific ID 4** ID Number of this Extended Capability structure.	RO	Yes	0003h
19:16	**Vendor-Specific Rev 4** Version Number of this structure.	RO	Yes	0h
31:20	**Vendor-Specific Length 4** Number of bytes in the entire structure.	RO	Yes	078h

Register 15-42. C3Ch Memory BAR2 Address Translation Lower

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**NT Port Virtual-to-Link Interface BAR2 Base Translation Address** NT Port Virtual-to-Link Interface Base Translation address when **BAR2** is enabled (**NT Port Virtual Interface Memory BAR2 Setup** register *BAR2 Enable* bit, offset D4h[31], is Set).	RW	Yes	000h

Register 15-43. C40h Memory BAR3 Address Translation Upper

Bit(s)	Description		Type	Serial EEPROM and I^{2}C	Default
19:0	***Reserved***	Offset D8h[31]=0	RsvdZ	No	0_0000h
	When **BAR2/3** are used as a 64-bit BAR, bits [31:0] (including bits [19:0]) are used as the upper 32 bits.	Offset D8h[31]=1	RW	Yes	0_0000h
31:20	**NT Port Virtual-to-Link Interface BAR3 Base Translation Address** NT Port Virtual-to-Link Interface Base Translation address when **BAR3** is enabled (**NT Port Virtual Interface Memory BAR2/3 Setup** register *BAR3 Enable* bit, offset D8h[31], is Set).		RW	Yes	000h

Register 15-44. C44h Memory BAR4 Address Translation Lower

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**NT Port Virtual-to-Link Interface BAR4 Base Translation Address** NT Port Virtual-to-Link Interface Base Translation address when **BAR4** is enabled (**NT Port Virtual Interface Memory BAR4 Setup** register *BAR4 Enable* bit, offset DCh[31], is Set).	RW	Yes	000h

Register 15-45. C48h Memory BAR5 Address Translation Upper

Bit(s)	Description		Type	Serial EEPROM and I^{2}C	Default
19:0	***Reserved***	Offset E0h[31]=0	RsvdZ	No	0_0000h
	When **BAR4/5** are used as a 64-bit BAR, bits [31:0] (including bits [19:0]) are used as the upper 32 bits.	Offset E0h[31]=1	RW	Yes	0_0000h
31:20	**NT Port Virtual-to-Link Interface BAR5 Base Translation Address** NT Port Virtual-to-Link Interface Base Translation address when **BAR5** is enabled (**NT Port Virtual Interface Memory BAR4/5 Setup** register *BAR5 Enable* bit, offset E0h[31], is Set).		RW	Yes	000h

Register 15-46. C4Ch Virtual Interface IRQ Set

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The bits in this register can be masked by their respective **Virtual Interface IRQ Mask Set** register bits (offset C54h).*				
15:0	**SET_IRQ** Set Virtual IRQ. Controls the state of the Virtual Interface Doorbell Interrupt Request. Reading returns the status of the bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register Sets the corresponding Interrupt Request. The Virtual Interface interrupt is asserted if the following conditions exist: • This register (offset C4Ch or C50h) value is non-zero, and, • Corresponding **Virtual Interface IRQ Mask Set** or **Virtual Interface IRQ Mask Clear** register (offset C54h or C58h, respectively) *Interrupt Mask* bit is not Set, and, • Interrupts (either INT*x* or MSI) are enabled	RW1S	Yes	0000h
31:16	***Reserved***	RsvdP	No	0000h

Register 15-47. C50h Virtual Interface IRQ Clear

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *The bits in this register can be masked by their respective **Virtual Interface IRQ Mask Clear** register bits (offset C58h).*				
15:0	**CLR_IRQ** Clear Virtual IRQ. Controls the state of the Virtual Interface Doorbell Interrupt Request. Reading returns the status of the bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register Clears the corresponding Interrupt Request. The Virtual Interface interrupt is de-asserted if the following conditions exist: • This register (offset C50h or C4Ch) value is zero (0), –or– • **Virtual Interface IRQ Mask Set** or **Virtual Interface IRQ Mask Clear** register (offset C54h or C58h, respectively) masks all its **Set** or **Clear** register (offset C50h or C4Ch) *Set* bits, and • INT*x* interrupts are enabled	RW1C	Yes	0000h
31:16	***Reserved***	RsvdP	No	0000h

Register 15-48. C54h Virtual Interface IRQ Mask Set

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
Note:	*The bits in this register can be used to mask their respective **Virtual Interface IRQ Set** register bits (offset C4Ch).*			
15:0	**SET_IRQM** Virtual Interface interrupt IRQ Mask Set. Reading returns the state of the *Interrupt Mask* bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register Clears the corresponding *Interrupt Mask* bit. 0 = Corresponding **Virtual Interface IRQ Set** register (offset C4Ch) *Interrupt Request* bit is not masked 1 = Corresponding **Virtual Interface IRQ Set** register (offset C4Ch) *Interrupt Request* bit is masked/disabled	RW1S	Yes	FFFFh
31:16	***Reserved***	RsvdP	No	0000h

Register 15-49. C58h Virtual Interface IRQ Mask Clear

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
Note:	*The bits in this register can be used to mask their respective **Virtual Interface IRQ Clear** register bits (offset C50h).*			
15:0	**CLR_IRQM** Clear Virtual IRQ Mask. Controls the state of the Virtual Interface *Interrupt Request* bits. Reading returns the state of the *Interrupt Mask* bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register Clears the corresponding *Interrupt Mask* bit. 0 = Corresponding **Virtual Interface IRQ Clear** register (offset C50h) *Interrupt Request* bit is not masked 1 = Corresponding **Virtual Interface IRQ Clear** register (offset C50h) *Interrupt Request* bit is masked/disabled	RW1C	Yes	FFFFh
31:16	***Reserved***	RsvdP	No	0000h

Register 15-50. C5Ch Link Interface IRQ Set

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Note:	*The bits in this register can be masked by their respective* ***Link Interface IRQ Mask Set*** *register bits (offset C64h).*			
15:0	**SET_IRQ** Set Link IRQ. Controls the state of the Link Interface Doorbell Interrupt Request. Reading returns the status of the bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register Sets the corresponding Interrupt Request. The Link Interface interrupt is asserted if the following conditions exist: • This register (offset C5Ch or C60h) value is non-zero, and, • Corresponding **Link Interface IRQ Mask Set** or **Link Interface IRQ Mask Clear** register (offset C64h or C68h, respectively) *Interrupt Mask* bit is not Set, and, • Interrupts (either INT*x* or MSI) are enabled	RW1S	Yes	0000h
31:16	***Reserved***	RsvdP	No	0000h

Register 15-51. C60h Link Interface IRQ Clear

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Note:	*The bits in this register can be masked by their respective* ***Link Interface IRQ Mask Clear*** *register bits (offset C68h).*			
15:0	**CLR_IRQ** Clear Virtual IRQ. Controls the state of the Virtual Interface Doorbell Interrupt Request. Reading returns the status of the bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register Clears the corresponding Interrupt Request. The Virtual Interface interrupt is de-asserted if the following conditions exist: • This register (offset C60h or C5Ch) value is zero (0), –or– • **Link Interface IRQ Mask Set** or **Link Interface IRQ Mask Clear** register (offset C64h or C68h, respectively) masks all its **Set** or **Clear** register (offset C60h or C5Ch) *Set* bits, and • INT*x* interrupts are enabled	RW1C	Yes	0000h
31:16	***Reserved***	RsvdP	No	0000h

Register 15-52. C64h Link Interface IRQ Mask Set

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
Note: *The bits in this register can be used to mask their respective* ***Link Interface IRQ Set*** *register bits (offset C5Ch).*				
15:0	**SET_IRQM** Link Interface Interrupt IRQ Mask Set. Reading returns the state of the *Interrupt Mask* bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register Sets the corresponding *Interrupt Mask* bit. 0 = Corresponding **Link Interface IRQ Set** register (offset C5Ch) *Interrupt Request* bit is not masked 1 = Corresponding **Link Interface IRQ Set** register (offset C5Ch) *Interrupt Request* bit is masked/disabled	RW1S	Yes	FFFFh
31:16	***Reserved***	RsvdP	No	0000h

Register 15-53. C68h Link Interface IRQ Mask Clear

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
Note: *The bits in this register can be used to mask their respective* ***Link Interface IRQ Clear*** *register bits (offset C60h).*				
15:0	**CLR_IRQM** Link Interface Interrupt IRQ Mask Clear. Reading returns the state of the *Interrupt Mask* bits. Writing 0 to a bit in the register has no effect. Writing 1 to a bit in the register Clears the corresponding *Interrupt Mask* bit. 0 = Corresponding **Link Interface IRQ Clear** register (offset C60h) *Interrupt Request* bit is not masked 1 = Corresponding **Link Interface IRQ Clear** register (offset C60h) *Interrupt Request* bit is masked/disabled	RW1C	Yes	FFFFh
31:16	***Reserved***	RsvdP	No	0000h

Register 15-54. C6Ch NT Port SCRATCH0

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
31:0	**Scratchpad 0** 32-bit Scratchpad 0 register.	RW	Yes	0000_0000h

Register 15-55. C70h NT Port SCRATCH1

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
31:0	**Scratchpad 1** 32-bit Scratchpad 1 register.	RW	Yes	0000_0000h

Register 15-56. C74h NT Port SCRATCH2

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
31:0	**Scratchpad 2** 32-bit Scratchpad 2 register.	RW	Yes	0000_0000h

Register 15-57. C78h NT Port SCRATCH3

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
31:0	**Scratchpad 3** 32-bit Scratchpad 3 register.	RW	Yes	0000_0000h

Register 15-58. C7Ch NT Port SCRATCH4

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
31:0	**Scratchpad 4** 32-bit Scratchpad 4 register.	RW	Yes	0000_0000h

Register 15-59. C80h NT Port SCRATCH5

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**Scratchpad 5** 32-bit Scratchpad 5 register.	RW	Yes	0000_0000h

Register 15-60. C84h NT Port SCRATCH6

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**Scratchpad 6** 32-bit Scratchpad 6 register.	RW	Yes	0000_0000h

Register 15-61. C88h NT Port SCRATCH7

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	**Scratchpad 7** 32-bit Scratchpad 7 register.	RW	Yes	0000_0000h

15.15 NT Port Virtual Interface NT Bridging-Specific Registers (Offsets C8Ch – DFCh)

Table 15-17 defines the register map of the NT Port Virtual Interface NT Bridging-Specific registers.

Table 15-17. NT Port Virtual Interface NT Bridging-Specific Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved		C8Ch – D90h
NT Port Virtual Interface NT Bridging-Specific Registers – Requester ID Translation Lookup Table Entry (Addresses D94h – DD0h)		D94h … DD0h
Reserved		DD4h – DFCh

15.15.1 NT Port Virtual Interface NT Bridging-Specific Registers – Requester ID Translation Lookup Table Entry (Addresses D94h – DD0h)

This section describes the NT Port Virtual Interface NT Bridging-Specific Requester ID Translation Lookup Table (LUT) Entry registers, in 8- and 32-Entry modes. The NT Port uses these registers for Requester ID translation when it forwards:

- Memory Requests from the NT Port Virtual Interface to the NT Port Link Interface, –or–
- Completion TLPs from the NT Port Link Interface to the NT Port Virtual Interface

If the application needs to send traffic through the NT Port Virtual Interface:

- **Address Locations D94h through DB0h (8-Entry mode (eight 32-bit entries))** – Program the registers listed in this group with the corresponding Requester’s Requester ID, then Set the *LUT Entry_n Enable* bit (bit 31) of each register accordingly. 8-Entry mode is selected by way of the following:
  - **Legacy NT mode** – 8-Entry mode is selected, by default
  - **NT PCI-to-PCI Bridge mode** – 8-Entry mode is selected when the **Ingress Chip Control** register *Virtual LUT Toggle* bit (Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface, offset 764h[2]) is Set

  Table 15-18 defines the 8-Entry mode register and address locations, as they relate to Register 15-62.
- **Address Locations D94h through DD0h (32-Entry mode (32 16-bit entries))** – Program the registers listed in this group with the corresponding Requester’s Requester ID, then Set the *LUT Entry_n Enable* and *LUT Entry_m Enable* bits (bits 0 and 16, respectively) for each LUT entry, as needed.
  - **Legacy NT mode** – 8-Entry mode is selected when the **Ingress Chip Control** register *Virtual LUT Toggle* bit (Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface, offset 764h[2]) is Set
  - **NT PCI-to-PCI Bridge mode** – 32-Entry mode is selected, by default

  Table 15-19 defines the 32-Entry mode register and address locations, as they relate to Register 15-63.

Table 15-18. NT Port Virtual Interface NT Bridging-Specific Requester ID Translation Lookup Table Entry_*n* – 8-Entry Mode

ADDR Location	Lookup Table Entry_*n*
D94h	0
D98h	1
D9Ch	2
DA0h	3
DA4h	4
DA8h	5
DACh	6
DB0h	7

Register 15-62. D94h – DB0h NT Port Virtual Interface Requester ID Translation LUT Entry_*n* – 8-Entry Mode (where *n* = 0 through 7)

Bit(s)	Description		Type	Serial EEPROM and I^{2}C	Default
2:0	**Requester ID on Virtual Side**	**Function Number** LUT Entry_*n* Requester Function Number.	RW	Yes	000b
7:3		**Device Number** LUT Entry_*n* Requester Device Number.	RW	Yes	0000_0b
15:8		**Bus Number** LUT Entry_*n* Requester Bus Number.	RW	Yes	00h
29:16	**8-Entry Mode** ***Reserved***		RsvdP	No	0-0h
	32-Entry Mode Part of 2nd LUT in 32-Entry mode.		RW	Yes	0-0h
30	**LUT Entry_*n* No Snoop Enable** If Set, the NT Port Clears the TLP *No Snoop* attribute bit for the Memory Request, then goes from the NT Port Virtual Interface to the NT Port Link Interface, and re-calculates the End-to-end Cyclic Redundancy Check (ECRC). If the original TLP has an ECRC error, the NT Port corrupts the re-calculated ECRC before transmitting to the other Host domain. The NT Port sets the *No Snoop* attribute bit when it forwards the Completion TLP from the NT Port Link Interface to the NT Port Virtual Interface if this bit is Set for the corresponding Requester ID entry. This ECRC rule applies to Completion TLPs as well. 0 = Disables 1 = Enables		RW	Yes	0
31	**LUT Entry_*n* Enable** 0 = Disables 1 = Enables		RW	Yes	0

Table 15-19. NT Port Virtual Interface NT Bridging-Specific Requester ID Translation Lookup Table Entry_*n_m* Register Locations – 32-Entry Mode

ADDR Location	Lookup Table Entry_*n*	ADDR Location	Lookup Table Entry_*n_m*
D94h	0_1	DB4h	16_17
D98h	2_3	DB8h	18_19
D9Ch	4_5	DBCh	20_21
DA0h	6_7	DC0h	22_23
DA4h	8_9	DC4h	24_25
DA8h	10_11	DC8h	26_27
DACh	12_13	DCCh	28_29
DB0h	14_15	DD0h	30_31

Register 15-63. D94h – DD0h NT Port Virtual Interface Requester ID Translation LUT Entry_*n_m* – 32-Entry Mode (where *n_m* = 0_1 through 30_31)

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
0	**LUT Entry_*n* Enable** 0 = Disables 1 = Enables		RW	Yes	0
1	**LUT Entry_*n* No Snoop Enable** If Set, the NT Port Clears the TLP *No Snoop* attribute bit for the Memory Request, then goes from the NT Port Virtual Interface to the NT Port Link Interface, and re-calculates the ECRC. If the original TLP has an ECRC error, the NT Port corrupts the re-calculated ECRC before transmitting to the other Host domain. The NT Port sets the *No Snoop* attribute bit when it forwards the Completion TLP from the NT Port Link Interface to the NT Port Virtual Interface if this bit is Set for the corresponding Requester ID entry. This ECRC rule applies to Completion TLPs as well. 0 = Disables 1 = Enables		RW	Yes	0
2	***Reserved***		RsvdP	No	0
7:3	**Requester ID on Link Side**	**Device Number** LUT Entry_*n* Requester Device Number.	RW	Yes	0000_0b
15:8		**Bus Number** LUT Entry_*n* Requester Bus Number.	RW	Yes	00h
16	**LUT Entry_*m* Enable** 0 = Disables 1 = Enables		RW	Yes	0
17	**LUT Entry_*m* No Snoop Enable** If Set, the NT Port Clears the TLP *No Snoop* attribute bit for the Memory Request, then goes from the NT Port Virtual Interface to the NT Port Link Interface, and re-calculates the ECRC. If the original TLP has an ECRC error, the NT Port corrupts the re-calculated ECRC before transmitting to the other Host domain. The NT Port sets the *No Snoop* attribute bit when it forwards the Completion TLP from the NT Port Link Interface to the NT Port Virtual Interface if this bit is Set for the corresponding Requester ID entry. This ECRC rule applies to Completion TLPs as well. 0 = Disables 1 = Enables		RW	Yes	0
18	***Reserved***		RsvdP	No	0
23:19	**Requester ID on Link Side**	**Device Number** LUT Entry_*m* Requester Device Number.	RW	Yes	0000_0b
31:24		**Bus Number** LUT Entry_*m* Requester Bus Number.	RW	Yes	00h

15.16 NT Port Virtual Interface Device-Specific Registers (Offsets F30h – FB0h)

The registers detailed in Section 13.19, "Device-Specific Registers (Offsets F30h – FB0h)," are unique to the PEX 8649 and not referenced in the *PCI Express Base r2.0*. These registers are also applicable to the NT Port Virtual Interface, except as defined in Table 15-20 (register map) through Table 15-23, and Register 15-65.

Other NT Port Virtual Interface Device-Specific registers are detailed in:

- Section 15.14, "NT Port Virtual Interface Device-Specific Registers (Offsets 1C0h – C88h)"
- Section 15.18, "NT Port Virtual Interface Device-Specific Registers – Link Error (Offsets FE0h – FFCh)"

Note:* *It is recommended that these registers not be changed from their default values.

Table 15-20. NT Port Virtual Interface Device-Specific Register Map (Offsets F30h – FB0h)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
NT Port Virtual Interface Device-Specific Registers – Egress Control (Offsets F30h – F44h)	F30h … F44h
NT Port Virtual Interface Device-Specific Registers – Ingress Control and Port Enable (Offsets F48h – F6Ch)	F48h … F6Ch
NT Port Virtual Interface Device-Specific Registers – Error Checking and Debug (Offsets F70h – FB0h)	F70h … FB0h

15.16.1 NT Port Virtual Interface Device-Specific Registers – Egress Control (Offsets F30h – F44h)

The registers detailed in Section 13.19.1, “Device-Specific Registers – Egress Control (Offsets F30h – F44h),” are also applicable to the NT Port Virtual Interface, except as defined in Table 15-21 (register map), and Register 15-64 and Register 15-65.

Table 15-21. NT Port Virtual Interface Device-Specific Egress Control Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Egress Control and Status	F30h
Reserved	F34h
Port Egress TLP Threshold	F38h
Reserved	F3Ch – F44h

Register 15-64. F30h Egress Control and Status

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
1:0	***Reserved***	RsvdP	No	00b
8:2	***Factory Test Only***	RWS	Yes	0-0h
9	**Vendor-Defined Type 0 UR** 0 = Do not generate UR Vendor-Defined Type 0 Broadcast TLP in *DL_Down* state 1 = Generate UR Vendor-Defined Type 0 Broadcast TLP in *DL_Down* state	RWS	Yes	0
10	**Egress Credit Timeout Enable** 0 = Egress Credit Timeout mechanism is disabled. 1 = Egress Credit Timeout mechanism is enabled. The timeout period is selected in field [12:11] (*Egress Credit Timeout Value*). Status is reflected in bit 16 (*Egress Credit Timeout Status*). If the Egress Credit Timer is enabled and expires (due to lack of Flow Control credits from the device connected to the NT Port Link Interface), the NT Port Link Interface brings down its Link. This event generates a Surprise Down Uncorrectable error, on the connected device.	RWS	Yes	0
12:11	**Egress Credit Timeout Value** 00b = 1 ms 01b = 512 ms 10b = 1s 11b = ***Reserved***	RWS	Yes	00b
15:13	***Reserved***	RsvdP	No	000b
16	**Egress Credit Timeout Status** 0 = No timeout 1 = Timeout	RW1CS	No	0
18:17	**Egress Credit Timeout VC&T** Egress Credit timeout for Virtual Channel and Type. 00b = Posted 01b = Non-Posted 10b = Completion 11b = ***Reserved***	RO	No	00b
30:19	***Reserved***	RsvdP	No	0-0h
31	**Port Activity** 0 = NT Port Virtual Interface is idle 1 = NT Port Virtual Interface has one or more pending TLPs to transmit	RO	No	0

Register 15-65. F38h Port Egress TLP Threshold

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
11:0	**Port Lower TLP Counter** When Source Scheduling is disabled due to Threshold, it is re-enabled when the Port TLP Counter goes below this Threshold value.	RWS	Yes	FFFh
15:12	***Reserved***	RWS	Yes	0h
27:16	**Port Upper TLP Counter** When the Port TLP Counter is greater than or equal to this value, the Source Scheduler disables TLP scheduling to this egress Port.	RWS	Yes	FFFh
31:28	***Reserved***	RWS	Yes	0h

15.16.2 NT Port Virtual Interface Device-Specific Registers – Ingress Control and Port Enable (Offsets F48h – F6Ch)

The registers detailed in Section 13.19.2, "Device-Specific Registers – Ingress Control and Port Enable (Offsets F48h – F6Ch)," are also applicable to the NT Port Virtual Interface, except as defined in Table 15-22 (register map; offset F60h is ***reserved***).

Table 15-22. NT Port Virtual Interface Device-Specific Ingress Control and Port Enable Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Ingress Port-Based Control		F48h
Port Enable Status		F4Ch
Reserved	Negotiated Link Width for Ports 0, 1, 2, 3	F50h
Reserved		F54h
Negotiated Link Width for Ports 16, 17, 18, 19, 20, 21, 22, 23		F58h
Reserved		F5Ch – F6Ch

15.16.3 NT Port Virtual Interface Device-Specific Registers – Error Checking and Debug (Offsets F70h – FB0h)

The registers detailed in Section 13.19.3, "Device-Specific Registers – Error Checking and Debug (Offsets F70h – FB0h)," are also applicable to the NT Port Virtual Interface, except as defined in Table 15-23 (register map; offset F70h is ***reserved***).

Other NT Port Virtual Interface Device-Specific Error Checking and Debug registers are detailed in:

- Section 13.15.7, "Device-Specific Registers – Error Checking and Debug (Offsets 320h – 350h)"
- Section 13.15.10, "Device-Specific Registers – Error Checking and Debug (Offsets 700h – 75Ch)"

Table 15-23. NT Port Virtual Interface Device-Specific Error Checking and Debug Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved		F70h – FA4h
ACK Transmission Latency Limit		FA8h
Bad TLP Counter		FACh
Bad DLLP Counter		FB0h

15.17 NT Port Virtual Interface Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)

The registers detailed in Section 13.20, "Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)," are also applicable to the NT Port Virtual Interface, except as defined in Table 15-24 (register map), and Register 15-66 through Register 15-71.

Table 15-24. NT Port Virtual Interface Advanced Error Reporting Extended Capability Register Map

31 30 29 28 27 26 25 24	23 22 21 20	19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Next Capability Offset (138h)		Capability Version (1h)	PCI Express Extended Capability ID (0001h)		FB4h
Reserved	Uncorrectable Error Status				FB8h
Reserved	Uncorrectable Error Mask				FBCh
Reserved	Uncorrectable Error Severity				FC0h
Reserved			Correctable Error Status		FC4h
Reserved			Correctable Error Mask		FC8h
Advanced Error Capabilities and Control					FCCh
Header Log 0					FD0h
Header Log 1					FD4h
Header Log 2					FD8h
Header Log 3					FDCh

Register 15-66. FB8h Uncorrectable Error Status

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The following PCI Express errors are not valid for the NT Port Virtual Interface: • Data Link Protocol error • Surprise Down error ***Note:*** *The bits in this register can be masked by their respective* ***Uncorrectable Error Mask*** *register bits (offset FBCh).*				
3:0	***Reserved***	RsvdP	No	0h
4	**Data Link Protocol Error Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
5	**Surprise Down Error Status** ***Reserved***	RsvdP	No	0
11:6	***Reserved***	RsvdP	No	0-0h
12	**Poisoned TLP Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
13	**Flow Control Protocol Error Status** ***Reserved/Not supported***	RsvdP	No	0
14	**Completion Timeout Status** ***Not applicable to switches.***	RsvdP	No	0
15	**Completer Abort Status**	RW1CS[a]	Yes	0

Register 15-66. FB8h Uncorrectable Error Status *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
16	**Unexpected Completion Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
17	**Receiver Overflow Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
18	**Malformed TLP Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
19	**ECRC Error Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
20	**Unsupported Request Error Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
21	***Reserved***	RsvdP	No	0
22	**Uncorrectable Internal Error Status** ***Reserved***	RsvdP	No	0
23	**MC Blocked TLP Status** Multicast blocked TLP status. 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
31:24	***Reserved***	RsvdP	No	00h

[a] *When the* ***ECC Error Check Disable*** *register Software Force Error Enable bit (offset 720h[2]) is Set, Type changes from RW1CS to RW.*

Register 15-67. FBCh Uncorrectable Error Mask

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I²C</th><th>Default</th></tr>
<tr><td colspan="5">The following PCI Express errors are not valid for the NT Port Virtual Interface:
• Data Link Protocol error
• Surprise Down error
<b><i>Note:</i></b> <i>The bits in this register can be used to mask their respective <b>Uncorrectable Error Status</b> register bits (offset FB8h).</i></td></tr>
<tr><td>3:0</td><td><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>0h</td></tr>
<tr><td>4</td><td><b>Data Link Protocol Error Mask</b>
0 = No mask is Set
1 = Masks error reporting, first error update, and Header logging for this error</td><td>RWS</td><td>Yes</td><td>0</td></tr>
<tr><td>5</td><td><b>Surprise Down Error Mask</b>
<b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>0</td></tr>
<tr><td>11:6</td><td><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>0-0h</td></tr>
<tr><td>12</td><td><b>Poisoned TLP Mask</b>
0 = No mask is Set
1 = Masks error reporting, first error update, and Header logging for this error</td><td>RWS</td><td>Yes</td><td>0</td></tr>
<tr><td>13</td><td><b>Flow Control Protocol Error Mask</b>
<b><i>Reserved/Not supported</i></b></td><td>RsvdP</td><td>No</td><td>0</td></tr>
<tr><td>14</td><td><b>Completion Timeout Mask</b>
<b><i>Not applicable to switches.</i></b></td><td>RsvdP</td><td>No</td><td>0</td></tr>
<tr><td>15</td><td><b>Completer Abort Mask</b></td><td>RWS</td><td>Yes</td><td>0</td></tr>
</table>

Register 15-67. FBCh Uncorrectable Error Mask *(Cont.)*

Bit(s)	Description		Type	Serial EEPROM and I^{2}C	Default
16	**Unexpected Completion Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
17	**Receiver Overflow Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
18	**Malformed TLP Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
19	**ECRC Error Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
20	**Unsupported Request Error Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
21	***Reserved***		RsvdP	No	0
22	**Uncorrectable Internal Error Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error	Port 0 is NT	RWS	Yes	1
	Reserved	Otherwise	RsvdP	No	1
23	**MC Blocked TLP Mask** 0 = No mask is Set 1 = Masks error reporting, first error update, and Header logging for this error		RWS	Yes	0
31:24	***Reserved***		RsvdP	No	00h

Register 15-68. FC0h Uncorrectable Error Severity

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
The following PCI Express errors are not valid for the NT Port Virtual Interface: • Data Link Protocol error • Surprise Down error				
3:0	***Reserved***	RsvdP	No	0h
4	**Data Link Protocol Error Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal	RWS	Yes	1
5	**Surprise Down Error Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal	RWS	Yes	1
11:6	***Reserved***	RsvdP	No	0-0h
12	**Poisoned TLP Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal	RWS	Yes	0
13	**Flow Control Protocol Error Severity** ***Reserved/Not supported***	RsvdP	No	1
14	**Completion Timeout Severity** ***Not applicable to switches.*** Because the Status and Mask are both ***reserved*** for this bit, Severity can be ignored.	RsvdP	No	0
15	**Completer Abort Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal	RWS	Yes	0

Register 15-68. FC0h Uncorrectable Error Severity *(Cont.)*

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
16	**Unexpected Completion Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0
17	**Receiver Overflow Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal		RWS	Yes	1
18	**Malformed TLP Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal		RWS	Yes	1
19	**ECRC Error Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0
20	**Unsupported Request Error Severity** 0 = Error is handled as an Advisory Non-Fatal error, and reported as a Correctable error 1 = Error is reported as fatal		RWS	Yes	0
21	***Reserved***		RsvdP	No	0
22	**Uncorrectable Internal Error Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal	Port 0 is NT	RWS	Yes	1
	Reserved	Otherwise	RsvdP	No	1
23	**MC Blocked TLP Severity** 0 = Error is reported as non-fatal 1 = Error is reported as fatal		RWS	Yes	0
31:24	***Reserved***		RsvdP	No	00h

Register 15-69. FC4h Correctable Error Status

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The following PCI Express errors are not valid for the NT Port Virtual Interface: • Receiver error • Bad TLP error • Bad DLLP error • Replay Number Rollover error • Replay Timer Timeout error ***Note:*** *The bits in this register can be masked by their respective* ***Correctable Error Mask*** *register bits (offset FC8h).*				
0	**Receiver Error Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
5:1	***Reserved***	RsvdP	No	0-0h
6	**Bad TLP Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
7	**Bad DLLP Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
8	**REPLAY NUM Rollover Status** Replay Number Rollover status. 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
11:9	***Reserved***	RsvdP	No	000b
12	**Replay Timer Timeout Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
13	**Advisory Non-Fatal Error Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
14	**Legacy NT Mode** **Corrected Internal Error Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
	NT PCI-to-PCI Bridge Mode ***Reserved***	RsvdP	No	0
15	**Header Log Overflow Status** 0 = No error is detected 1 = Error is detected	RW1CS[a]	Yes	0
31:16	***Reserved***	RsvdP	No	0000h

[a] *When the* ***ECC Error Check Disable*** *register Software Force Error Enable bit (offset 720h[2]) is Set, Type changes from RW1CS to RW.*

Register 15-70. FC8h Correctable Error Mask

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
The following PCI Express errors are not valid for the NT Port Virtual Interface: • Receiver error • Bad TLP error • Bad DLLP error • Replay Number Rollover error • Replay Timer Timeout error ***Note:*** *The bits in this register can be used to mask their respective* ***Correctable Error Status*** *register bits (offset FC4h).*				
0	**Receiver Error Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
5:1	***Reserved***	RsvdP	No	0-0h
6	**Bad TLP Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
7	**Bad DLLP Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
8	**REPLAY NUM Rollover Mask** Replay Number Rollover mask. 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
11:9	***Reserved***	RsvdP	No	000b
12	**Replay Timer Timeout Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	0
13	**Advisory Non-Fatal Error Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	1
14	**Legacy NT Mode** **Corrected Internal Error Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	1
	NT PCI-to-PCI Bridge Mode ***Reserved***	RsvdP	No	0
15	**Header Log Overflow Mask** 0 = Error reporting is not masked 1 = Error reporting is masked	RWS	Yes	1
31:16	***Reserved***	RsvdP	No	0000h

Register 15-71. FCCh Advanced Error Capabilities and Control

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
4:0	**First Error Pointer** Identifies the bit position of the first error reported in the **Uncorrectable Error Status** register (offset FB8h).	ROS	No	1Fh
5	**ECRC Generation Capable** 0 = ECRC generation is not supported 1 = ECRC generation is supported, but must be enabled	RO	Yes	1
6	**ECRC Generation Enable** 0 = ECRC generation is disabled 1 = ECRC generation is enabled	RWS	Yes	0
7	**ECRC Check Capable** 0 = ECRC checking is not supported 1 = ECRC checking is supported, but must be enabled	RO	Yes	1
8	**ECRC Check Enable** 0 = ECRC checking is disabled 1 = ECRC checking is enabled	RWS	Yes	0
31:9	***Reserved***	RsvdP	No	0-0h

15.18 NT Port Virtual Interface Device-Specific Registers – Link Error (Offsets FE0h – FFCh)

This section details the NT Port Virtual Interface Device-Specific Link Error registers, located at offsets FE0h through FFCh. Device-Specific registers are unique to the NT Port Virtual Interface and not referenced in the *PCI Express Base r2.0*. Table 15-25 defines the register map used by the NT Port Virtual Interface.

Other NT Port Virtual Interface Device-Specific registers are detailed in:

- Section 15.14, "NT Port Virtual Interface Device-Specific Registers (Offsets 1C0h – C88h)"
- Section 15.16, "NT Port Virtual Interface Device-Specific Registers (Offsets F30h – FB0h)"

Note:* *It is recommended that these registers not be changed from their default values.

Table 15-25. NT Port Virtual Interface Device-Specific Link Error Register Map (Offsets FE0h – FFCh) (Port 0, when Port 0 is the NT Port, Virtual Interface Only)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Link Error Status Virtual		FE0h
Link Error Mask Virtual		FE4h
Reserved		FE8h – FFCh

Register 15-72. FE0h Link Error Status Virtual (Port 0, when Port 0 is the NT Port, Virtual Interface Only)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
Note: *The bits in this register can be masked by their respective* ***Link Error Mask Virtual*** *register bits (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE4h).*				
0	**Correctable Error Status on Link Side** 1 = NT Port Link Interface detected a Correctable TLP error, and signaled the interrupt to the Local Host	RW1CS	Yes	0
1	**Uncorrectable Error Status on Link Side** 1 = NT Port Link Interface detected an Uncorrectable TLP error, and signaled the interrupt to the Local Host	RW1CS	Yes	0
2	**Link Side DL Active Change Status** 1 = NT Port Link Interface *DL_Active* state change occurred upon detection of an NT Port Link Interface *DL_Down* state rise edge and fall edge	RW1CS	Yes	0
3	**Link Side Uncorrectable Error Message Drop Status** 1 = NT Port Link Interface received an Uncorrectable Error Message, and signaled the interrupt to the Local Host	RW1CS	Yes	0
31:4	***Reserved***	RsvdP	No	0000_000h

Register 15-73. FE4h Link Error Mask Virtual (Port 0, when Port 0 is the NT Port, Virtual Interface Only)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
Note: *The bits in this register can be used to mask their respective* ***Link Error Status Virtual*** *register bits (Port 0, when Port 0 is the NT Port, Virtual Interface Only, offset FE0h).*				
0	**Link Side Correctable Error Mask** 0 = No effect on reporting activity 1 = *Correctable Error Status on Link Side* bit is masked/disabled	RWS	Yes	1
1	**Link Side Uncorrectable Error Mask** 0 = No effect on reporting activity 1 = *Uncorrectable Error Status on Link Side* bit is masked/disabled	RWS	Yes	1
2	**Link Side DL Active Change Mask** 0 = No effect on reporting activity 1 = *Link Side DL Active Change Status* bit is masked/disabled	RWS	Yes	1
3	**Link Side Uncorrectable Error Message Drop Mask** 0 = No effect on reporting activity 1 = *Link Side Uncorrectable Error Message Drop Status* bit is masked/disabled	RWS	Yes	1
31:4	***Reserved***	RsvdP	No	0000_000h

Chapter 16 NT Port Link Interface Registers – Base Mode Only

16.1 Introduction

Note: *Check the latest design guides, application notes and errata list for Non-Transparent (NT) usage.*

NT mode is supported in Base mode. In NT mode, the NT Port includes two sets of Configuration, Capability, Control, and Status registers, to support the Link and Virtual Interfaces. This chapter defines the PEX 8649 NT Port Link Interface registers. Other registers are defined in:

- Chapter 13, "Transparent Port Registers"
- Chapter 15, "NT Port Virtual Interface Registers – Base Mode Only"

Notes: *For Chip-specific registers (those that exist only in Port 0), if Port 0 is the Legacy NT Port, then those registers exist only in the NT Port Virtual Interface.*

For Station-specific registers (those that exist only in Port 0, 16, or 20), if Port 0, 16, or 20 is the Legacy NT Port, then those registers exist only in the NT Port Virtual Interface.

All PEX 8649 registers can be accessed by Configuration or Memory Requests.

For further details regarding register names and descriptions, refer to the following specifications:

- *PCI r3.0*
- *PCI Power Mgmt. r1.2*
- *PCI Express Base r2.0*

16.2 NT Port Link Interface Type 0 Register Map

Table 16-1 defines the NT Port Link Interface Type 0 register mapping.

Table 16-1. NT Port Link Interface Type 0 Register Map

<table>
<tr><th colspan="2">31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16</th><th colspan="2">15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th><th></th></tr>
<tr><td colspan="3" rowspan="3">NT Port Link Interface PCI-Compatible Type 0 Configuration Header Registers (Offsets 00h – 3Ch)</td><td></td><td>00h
…</td></tr>
<tr><td>Capability Pointer (40h)</td><td>34h</td></tr>
<tr><td></td><td>…
3Ch</td></tr>
<tr><td colspan="2"></td><td>Next Capability Pointer (48h)</td><td>Capability ID (01h)</td><td>40h</td></tr>
<tr><td colspan="4">NT Port Link Interface PCI Power Management Capability Registers (Offsets 40h – 44h)</td><td>44h</td></tr>
<tr><td colspan="2"></td><td>Next Capability Pointer (68h)</td><td>Capability ID (05h)</td><td>48h</td></tr>
<tr><td colspan="4">NT Port Link Interface MSI Capability Registers (Offsets 48h – 64h)</td><td>…
64h</td></tr>
<tr><td colspan="2"></td><td>Next Capability Pointer (A4h)</td><td>Capability ID (10h)</td><td>68h</td></tr>
<tr><td colspan="4">NT Port Link Interface PCI Express Capability Registers (Offsets 68h – A0h)</td><td>…
A0h</td></tr>
<tr><td colspan="2"></td><td>Next Capability Pointer (C8h)</td><td>SSID/SSVID Capability ID (0Dh)</td><td>A4h</td></tr>
<tr><td colspan="4">NT Port Link Interface Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – C4h)</td><td>…
C4h</td></tr>
<tr><td colspan="2"></td><td>Next Capability Pointer (00h)</td><td>Capability ID 3 (09h)</td><td>C8h</td></tr>
<tr><td colspan="4">NT Port Link Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)</td><td>…
FCh</td></tr>
<tr><td>Next Capability Offset (FB4h)</td><td>1h</td><td colspan="2">PCI Express Extended Capability ID (0003h)</td><td>100h</td></tr>
<tr><td colspan="4">NT Port Link Interface Device Serial Number Extended Capability Registers (Offsets 100h – 134h)</td><td>…
134h</td></tr>
<tr><td>Next Capability Offset (148h)</td><td>1h</td><td colspan="2">PCI Express Extended Capability ID (0004h)</td><td>138h</td></tr>
<tr><td colspan="4">NT Port Link Interface Power Budget Extended Capability Registers (Offsets 138h – 144h)</td><td>…
144h</td></tr>
<tr><td>Next Capability Offset (C34h)</td><td>1h</td><td colspan="2">PCI Express Extended Capability ID (0002h)</td><td>148h</td></tr>
<tr><td colspan="4">NT Port Link Interface Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)</td><td>…
1BCh</td></tr>
</table>

Table 16-1. NT Port Link Interface Type 0 Register Map *(Cont.)*

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16		15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
NT Port Link Interface Device-Specific Registers (Offsets 1C0h – C88h)			1C0h …
Next Capability Offset 2 (000h)	1h	PCI Express Extended Capability ID 2 (000Bh)	B70h
NT Port Link Interface Device-Specific Registers (Offsets 1C0h – C88h)			…
Next Capability Offset 4 (B70h)	1h	PCI Express Extended Capability ID 4 (000Bh)	C34h
NT Port Link Interface Device-Specific Registers (Offsets 1C0h – C88h)			… C88h
NT Bridging-Specific Registers (Offsets C8Ch – EFCh)			C8Ch … EFCh
Reserved		F00h –	F2Ch
NT Port Link Interface Device-Specific Registers (Offsets F30h – FB0h)			F30h … FB0h
Next Capability Offset (138h)	1h	PCI Express Extended Capability ID (0001h)	FB4h
NT Port Link Interface Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)			… FDCh
Reserved		FE0h –	FFCh

16.3 Register Access

The PEX 8649 NT Port Link Interface implements a 4-KB Configuration Space. The lower 256 bytes (offsets 00h through FFh) are the PCI-compatible Configuration Space, and the upper 960 Dwords (offsets 100h through FFFh) are the PCI Express Extended Configuration Space. The PEX 8649 supports three mechanisms for accessing the NT Port Link Interface registers:

- PCI Express Base r2.0 Configuration Mechanism
- Device-Specific Memory-Mapped Configuration Mechanism
- Device-Specific Cursor Mechanism

16.3.1 *PCI Express Base r2.0* Configuration Mechanism

The *PCI Express Base r2.0* Configuration mechanism is divided into two mechanisms:

- **PCI r3.0-Compatible Configuration Mechanism** – Provides Conventional PCI access to the first 256 bytes (the bytes at offsets 00h through FFh) of the NT Port Virtual Interface Configuration Register space
- **PCI Express Enhanced Configuration Access Mechanism** – Provides access to the entire 4 KB Configuration Space

Both are described in the sections that follow.

The PEX 8649 decodes Type 0 Configuration transactions received on its NT Port Link Interface. The PEX 8649 reads from or writes to the NT Port Link Interface register, as specified in the original Type 0 Configuration access.

16.3.1.1 *PCI r3.0*-Compatible Configuration Mechanism

The *PCI r3.0*-Compatible Configuration Space consists of the first 256 bytes of the NT Port Link Interface Configuration Space. (Refer to Figure 16-1.) The *PCI r3.0*-Compatible Configuration mechanism provides standard access to the PEX 8649 NT Port Link Interface's first 256 bytes (the bytes at offsets 00h through FFh) of the PCI Express Configuration Space.

This mechanism is used to access the PEX 8649 NT Port Link Interface Type 0 (PCI endpoint) registers:

- NT Port Link Interface PCI-Compatible Type 0 Configuration Header Registers (Offsets 00h – 3Ch)
- NT Port Link Interface PCI Power Management Capability Registers (Offsets 40h – 44h)
- NT Port Link Interface MSI Capability Registers (Offsets 48h – 64h)
- NT Port Link Interface PCI Express Capability Registers (Offsets 68h – A0h)
- NT Port Link Interface Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – C4h)
- NT Port Link Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)

Because the mechanism is limited to the first 256 bytes of the NT Port Link Interface Configuration Register space, one of the following must be used to access beyond Byte FFh:

- PCI Express Enhanced Configuration Access Mechanism
- Device-Specific Memory-Mapped Configuration Mechanism
- Device-Specific Cursor Mechanism

This mechanism uses the same Request format as the Extended PCI Express Mechanism. For PCI-compatible Configuration Requests, the Extended Register Address field must be all zeros (0).

16.3.1.2 PCI Express Enhanced Configuration Access Mechanism

The PCI Express Enhanced Configuration Access mechanism uses a flat, Root Complex Memory-Mapped Address space to access the device Configuration registers. In this case, the Memory address determines the Configuration register accessed, and Memory data returns the addressed register contents. The Root Complex converts the Memory transaction into a Configuration transaction before transmitting this access to the downstream devices.

This mechanism is used to access the NT Port Link Interface Type 0 registers:

- NT Port Link Interface PCI-Compatible Type 0 Configuration Header Registers (Offsets 00h – 3Ch)
- NT Port Link Interface PCI Power Management Capability Registers (Offsets 40h – 44h)
- NT Port Link Interface MSI Capability Registers (Offsets 48h – 64h)
- NT Port Link Interface PCI Express Capability Registers (Offsets 68h – A0h)
- NT Port Link Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)
- NT Port Link Interface Device Serial Number Extended Capability Registers (Offsets 100h – 134h)
- NT Port Link Interface Power Budget Extended Capability Registers (Offsets 138h – 144h)
- NT Port Link Interface Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)
- Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets B70h – B7Ch)
- NT Port Link Interface Device-Specific Registers – Vendor-Specific Extended Capability 4 (Offsets C34h – C88h)
- NT Port Link Interface Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)

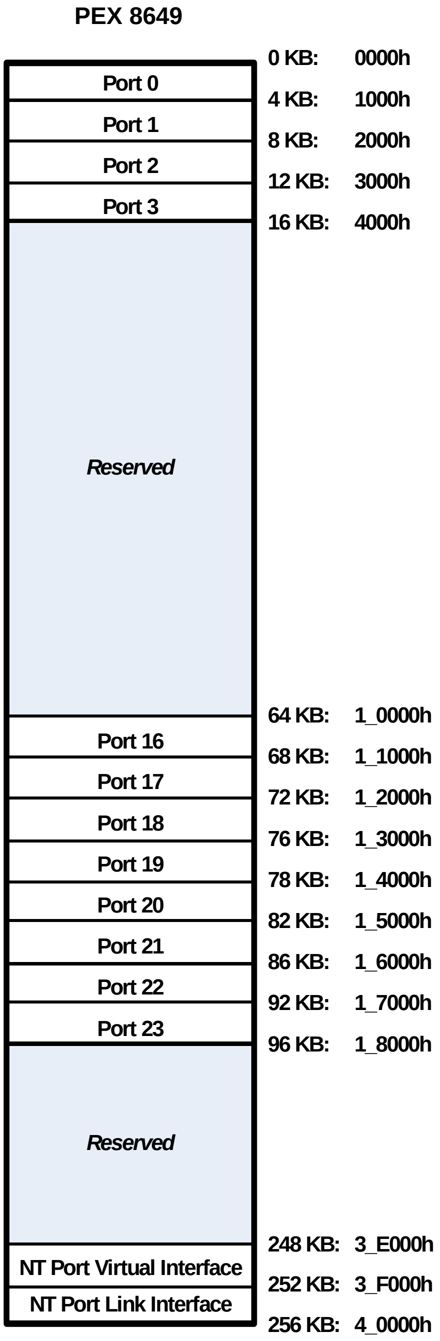
16.3.2 Device-Specific Memory-Mapped Configuration Mechanism

The Device-Specific Memory-Mapped Configuration mechanism provides a method to access the registers for all Ports within a single 256-KB Memory map, as illustrated in Figure 16-1. This Memory map is identical for Upstream Port **BAR0/1**, NT Port Virtual Interface **BAR0/1**, and NT Port Link Interface **BAR0/1**. The registers of each Port are located within a 4-KB range.

When the NT Port is enabled at Fundamental Reset, the NT Port Virtual and Link Interface registers use the *PCI r3.0* Type 0 Configuration Space Header. In NT PCI-to-PCI Bridge mode (STRAP_NT_P2P_EN# input is Low), the NT PCI-to-PCI bridge (between the NT Port Virtual Interface and internal virtual PCI Bus) registers use the *PCI r3.0* Type 1 Configuration Space Header, and are mapped to the 4-KB Address space of the Port Number that is assigned as the NT Port (indicated in the **VS0 Upstream** register *NT Port* field (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 360h[12, 10:8])).

To use this mechanism, use the PCI r3.0-Compatible Configuration Mechanism to program the PEX 8649 upstream Port **Base Address 0** and **Base Address 1** registers (**BAR0** and **BAR1**, offsets 10h and 14h, respectively). After the PEX 8649 NT Port Link Interface Memory-Mapped register Base address is Set, the PEX 8649 Configuration Space registers are accessed, using Memory Reads and Writes to the 4-KB range, starting at offset 248 KB (3_E000h, Virtual Interface) and offset 252 KB (3_F000h, Link Interface).

Figure 16-1. Register Offset from NT Port Link Interface BAR0/1 Base Address



16.3.3 Device-Specific Cursor Mechanism

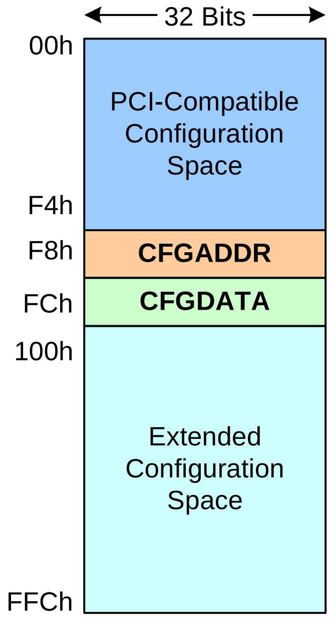
The Device-Specific Cursor mechanism is provided for use in development systems that can only generate *PCI r3.0* Configuration cycles (*that is*, the system cannot use either the Device-Specific Memory-Mapped Configuration Mechanism, nor generate Extended Configuration Requests to access the Extended Configuration Space).

In Figure 16-2, the software uses the **Configuration Address Window** (CFGADDR) register (offset F8h) to select the NT Port Virtual or Link Interface Configuration Space registers, including the PCI Express Extended Configuration Space registers (offsets 100h through FFFh).

Software uses the **Configuration Data Window** (CFGDATA) register (offset FCh) to read or write to the selected Configuration Space registers.

Refer to Section 16.10, "NT Port Link Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)," for the register descriptions.

Figure 16-2. Configuration Space View


32 Bits
00h
PCI-Compatible Configuration Space
F4h
F8h
CFGADDR
FCh
CFGDATA
100h
Extended Configuration Space
FFCh

16.4 Register Descriptions

The remainder of this chapter details the PEX 8649 NT Port Link Interface registers, including:

- Bit/field names
- Description of register functions in the PEX 8649 NT Port Link and Virtual Interfaces
- Type (*such as* RW or HwInit; refer to Table 13-4, "Register Types, Grouped by User Accessibility," for Type descriptions)
- Whether the power-on/reset value can be modified, by way of the PEX 8649 serial EEPROM and/or I^{2}C Initialization feature
- Default power-on/reset value

16.5 NT Port Link Interface PCI-Compatible Type 0 Configuration Header Registers (Offsets 00h – 3Ch)

This section details the NT Port Link Interface PCI-Compatible Type 0 Configuration Header registers. Table 16-2 defines the register map.

Table 16-2. NT Port Link Interface PCI-Compatible Type 0 Configuration Header Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Device ID		Vendor ID		00h
PCI Status		PCI Command		04h
PCI Class Code			PCI Revision ID	08h
PCI BIST ***(Not Supported)***	PCI Header Type	Master Latency Timer ***(Not Supported)***	Cache Line Size	0Ch
Base Address 0				10h
Base Address 1				14h
Base Address 2				18h
Base Address 3				1Ch
Base Address 4				20h
Base Address 5				24h
Reserved				28h
Subsystem ID		Subsystem Vendor ID		2Ch
Expansion ROM Base Address				30h
Reserved			Capability Pointer (40h)	34h
Reserved				38h
Max_Lat ***(Reserved)***	Min_Gnt ***(Reserved)***	PCI Interrupt Pin	PCI Interrupt Line	3Ch

Register 16-1. 00h PCI Configuration ID

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
15:0	**Vendor ID** Identifies the device manufacturer. Defaults to the PCI-SIG-issued Vendor ID of PLX (10B5h), if not overwritten by serial EEPROM and/or I^{2}C.	RO	Yes	10B5h
31:16	**Device ID** Identifies the particular device. Defaults to the PLX part number for the PEX 8649, if not overwritten by serial EEPROM and/or I^{2}C.	RO	Yes	8649h

Register 16-2. 04h PCI Command/Status

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	PCI Command			
0	**I/O Access Enable** The NT Port Link Interface ignores the value of this register, because it does ***not support*** I/O resources.	RW	Yes	0
1	**Memory Access Enable** 0 = PEX 8649 ignores Memory Space Requests received on the NT Port Link Interface 1 = PEX 8649 accepts Memory Space Requests received on the NT Port Link Interface	RW	Yes	0
2	**Bus Master Enable** Controls PEX 8649 forwarding of Memory Requests upstream. Does not affect Message forwarding nor Completions. 0 = PEX 8649 handles Memory Requests received on the NT Port Virtual Interface as Unsupported Requests (URs); for Non-Posted Requests, the PEX 8649 returns a Completion with UR Completion status 1 = PEX 8649 forwards Memory Requests from the NT Port Virtual Interface to the NT Port Link Interface	RW	Yes	0
3	**Special Cycle Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
4	**Memory Write and Invalidate Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
5	**VGA Palette Snoop** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
6	**Parity Error Response Enable** Controls bit 24 (*Master Data Parity Error Detected*).	RW	Yes	0
7	**IDSEL Stepping/Wait Cycle Control** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
8	**SERR# Enable** Controls bit 30 (*Signaled System Error*). 1 = Enables reporting of Fatal and Non-Fatal errors detected by the NT Port Link Interface to the Root Complex	RW	Yes	0
9	**Fast Back-to-Back Transactions Enable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
10	**Interrupt Disable** 0 = NT Port Link Interface is enabled to generate INT*x* Interrupt Messages 1 = NT Port Link Interface is prevented from generating INT*x* Interrupt Messages	RW	Yes	0
15:11	***Reserved***	RsvdP	No	0-0h

Register 16-2. 04h PCI Command/Status *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	PCI Status			
18:16	***Reserved***	RsvdP	No	000b
19	**Interrupt Status** 0 = No INT*x* interrupt is pending 1 = INT*x* interrupt is pending internally to the NT Port Link Interface –or– PEX_INTA# (if enabled) is asserted	RO	No	0
20	**Capability List** Capability function is supported. Set, as required by the *PCI Express Base r2.0*.	RO	Yes	1
21	**66 MHz Capable** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
22	***Reserved***	RsvdP	No	0
23	**Fast Back-to-Back Transactions Capable** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
24	**Master Data Parity Error Detected** If bit 6 (*Parity Error Response Enable*) is Set, the NT Port Link Interface Sets this bit when the NT Port: • Forwards the poisoned Transaction Layer Packet (TLP) Write Request from the NT Port Virtual Interface to the NT Port Link Interface, –or– • Receives a Completion marked as poisoned on the NT Port Link Interface If the *Parity Error Response Enable* bit is Cleared, the PEX 8649 never Sets this bit. This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
26:25	**DEVSEL# Timing** ***Not supported***	RsvdP	No	00b
27	**Signaled Target Abort** The NT Port Link Interface Sets this bit if any of the following conditions exist: • NT Port Link Interface receives a Completion (from a Transparent Port) that has a Completion status of Completer Abort (CA), –or– • NT Port Link Interface receives a Memory Request targeting a PEX 8649 register, and the Payload Length (indicated within the Memory Request Header) is greater than 1 DWord • NT Port Link Interface receives a Memory Request targeting a PEX 8649 register address within a non-existent Port • NT Port Link Interface receives a Memory Write Request targeting enabled Expansion ROM Address space (Expansion ROM Base Address Register (BAR), offset 30h) ***Note:*** *When Set during a forwarded Completion, the* ***Uncorrectable Error Status*** *register Completer Abort Status bit (offset FB8h[15]) is not updated, because the NT Port does not log the corresponding Requests that it forwards.*	RW1C	Yes	0

Register 16-2. 04h PCI Command/Status *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
28	**Received Target Abort** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
29	**Received Master Abort** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	0
30	**Signaled System Error** If bit 8 (*SERR# Enable*) is Set, the NT Port Link Interface Sets this bit when transmitting an ERR_FATAL or ERR_NONFATAL Message to its upstream device. This error is natively reported by the **Device Status** register *Fatal Error Detected* and *Non-Fatal Error Detected* bits (offset 70h[18:17], respectively), which are mapped to this bit for Conventional PCI backward compatibility.	RW1C	Yes	0
31	**Detected Parity Error** This error is natively reported by the **Uncorrectable Error Status** register *Poisoned TLP Status* bit (offset FB8h[12]), which is mapped to this bit for Conventional PCI backward compatibility. 1 = NT Port Link Interface received a Poisoned TLP, regardless of the bit 6 (*Parity Error Response Enable*) state	RW1C	Yes	0

Register 16-3. 08h PCI Class Code and Revision ID

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	PCI Revision ID			
7:0	**Revision ID** Unless overwritten by the serial EEPROM, returns the Silicon Revision (AAh), the PLX-assigned Revision ID for this version of the PEX 8649. The PEX 8649 Serial EEPROM register Initialization capability is used to replace the PLX Revision ID with another Revision ID.	RO	Yes	AAh
	PCI Class Code			**068000h**
15:8	**Register-Level Programming Interface** Cleared, as required by the *PCI r3.0* for other bridge devices.	RO	Yes	00h
23:16	**Sub-Class Code** Other bridge devices.	RO	Yes	80h
31:24	**Base Class Code** Bridge devices.	RO	Yes	06h

Register 16-4. 0Ch Miscellaneous Control

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Cache Line Size				
7:0	**Cache Line Size** System Cache Line Size. Implemented as a RW field for Conventional PCI compatibility purposes and does not impact PEX 8649 functionality.	RW	Yes	00h
Master Latency Timer				
15:8	**Master Latency Timer** ***Not supported*** Cleared, as required by the *PCI Express Base r2.0*.	RsvdP	No	00h
PCI Header Type				
22:16	**Configuration Layout Type** Type 0 Configuration Header for the NT Port.	RO	Yes	00h
23	**Multi-Function Device** 0 = Single-function device 1 = Indicates multiple (up to eight) functions (logical devices), each containing its own, individually addressable Configuration Space, 256 DWords in size	RO	Yes	0
PCI BIST				
31:24	**PCI BIST** ***Not supported*** Built-In Self-Test (BIST) Pass or Fail.	RsvdP	No	00h

Register 16-5. 10h Base Address 0 (NT Port Link Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
Note: *By default, NT Port Link Interface **BAR0** is enabled and **BAR1** is disabled, to provide a 32-bit **BAR0** for register access. **BAR1** can be enabled (by serial EEPROM and/or I²C/SMBus), to provide a 64-bit **BAR0/1**, by programming the **NT Port Link Interface BAR0/1 Setup** register BAR0/1 Enable field (NT Port Link Interface, offset E4h[1:0]) to 11b (which enables both **BAR0** and **BAR1**).*				
0	**Memory Space Indicator** When enabled, the Base Address register maps PEX 8649 Port Configuration registers into Memory space. ***Note:*** *Hardwired to 0.*	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Base Address register maps the PEX 8649 Port Configuration registers into Non-Prefetchable Memory space	RO	Yes	0
17:4	***Reserved***	RsvdP	No	0-0h
31:18	**Base Address 0** 256-KB-aligned Base address used for Memory-Mapped access to the 256-KB block of all PEX 8649 registers (4 KB per Port).	RW	Yes	0-0h

Register 16-6. 14h Base Address 1 (NT Port Link Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
31:0	**Upper 32-Bit Address for Memory-Mapped BAR** For 64-bit addressing (**BAR0/1**), Base Address 1 (**BAR1**) extends Base Address 0 (**BAR0**) to provide the upper 32 Address bits when the **Base Address 0** register *Memory Map Type* field (offset 10h[2:1]) is programmed to 10b.	RW	Yes	0000_0000h
	Read-Only when the **Base Address 0** (**BAR0**) register is not enabled as a 64-bit BAR (*Memory Map Type* field (offset 10h[2:1]) is not equal to 10b).	RO	Yes	0000_0000h

Register 16-7. 18h Base Address 2 (NT Port Link Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
0	**Memory Space Indicator** 0 = Implemented as a Memory BAR	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
19:4	***Reserved***	RsvdP	No	0_000h
31:20	**Base Address 2**	RW	Yes	000h

Register 16-8. 1Ch Base Address 3 (NT Port Link Interface Memory Space)

Bit(s)	Description		Type	Serial EEPROM and I^{2}C	Default
Note: *This register has RW privilege if **BAR2/3** is configured as a 64-bit BAR (**Base Address 2** register Memory Map Type field, offset 18h[2:1], is programmed to 10b).*					
0	**Memory Space Indicator** **BAR3** can be used as an independent 32-bit only BAR, or as the upper 32 bits of 64-bit **BAR2/3**. 0 = Implemented as a Memory BAR in 32-Bit mode	Offset 18h[2:1]=00b	RsvdP	No	0
		Offset 18h[2:1]=10b	RW	Yes	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space All other encodings are ***reserved***.	Offset 18h[2:1]=00b	RsvdP	No	00b
		Offset 18h[2:1]=10b	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	Offset 18h[2:1]=00b	RsvdP	No	0
		Offset 18h[2:1]=10b	RW	Yes	0
19:4	***Reserved***	Offset 18h[2:1]=00b	RsvdP	No	0_000h
	When **BAR2/3** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset 18h[2:1]=10b	RW	Yes	0_000h
31:20	**Base Address 3**		RW	Yes	000h

Register 16-9. 20h Base Address 4 (NT Port Link Interface Memory Space)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
0	**Memory Space Indicator** 0 = Implemented as a Memory BAR; otherwise, ***reserved***	RO	No	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space 10b = Base Address register is 64 bits wide and can be mapped anywhere in the 64-bit Address space All other encodings are ***reserved***.	RO	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RO	Yes	0
19:4	***Reserved***	RsvdP	No	0_000h
31:20	**Base Address 4**	RW	Yes	000h

Register 16-10. 24h Base Address 5 (NT Port Link Interface Memory Space)

Bit(s)	Description		Type	Serial EEPROM and I^{2}C	Default
Note: *This register has RW privilege if **BAR4/5** is configured as a 64-bit BAR (**Base Address 4** register Memory Map Type field, offset 20h[2:1], is programmed to 10b).*					
0	**Memory Space Indicator** **BAR5** can be used as an independent 32-bit only BAR, or as the upper 32 bits of 64-bit **BAR4/5**. 0 = Implemented as a Memory BAR in 32-Bit mode	Offset 20h[2:1]=00b	RsvdP	No	0
		Offset 20h[2:1]=10b	RW	Yes	0
2:1	**Memory Map Type** 00b = Base Address register is 32 bits wide and can be mapped anywhere in the 32-bit Memory space All other encodings are ***reserved***.	Offset 20h[2:1]=00b	RsvdP	No	00b
		Offset 20h[2:1]=10b	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	Offset 20h[2:1]=00b	RsvdP	No	0
		Offset 20h[2:1]=10b	RW	Yes	0
19:4	***Reserved***	Offset 20h[2:1]=00b	RsvdP	No	0_000h
	When **BAR4/5** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset 20h[2:1]=10b	RW	Yes	0_000h
31:20	**Base Address 5**		RW	Yes	000h

Register 16-11. 2Ch Subsystem ID and Subsystem Vendor ID

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	**Subsystem Vendor ID** Identifies the device manufacturer. Defaults to the PCI-SIG-issued Vendor ID of PLX (10B5h), if not overwritten by serial EEPROM and/or I^2C.	RO	Yes	10B5h
31:16	**Subsystem ID** Identifies the particular device. Defaults to the PLX part number for the PEX 8649, if not overwritten by serial EEPROM and/or I^2C.	RO	Yes	8649h

Register 16-12. 30h Expansion ROM Base Address

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
Note: *Expansion ROM can be enabled in either the NT Port Link or Virtual Interface, but not both simultaneously. Expansion ROM is enabled, by default, in the NT Port Link Interface (**Ingress Chip Control** register Expansion ROM Virtual Side bit (Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface, offset 764h[0]) is Cleared).* *Expansion ROM can be disabled, by Setting the Port's **Ingress Control** register Disable Expansion ROM BAR bit (offset F60h[15]).*					
0	**Expansion ROM Enable** 0 = NT Port Link Interface Expansion ROM is disabled	Offset F60h[15]=1 –or– NT Station offset 764h[0]=0	RsvdP	No	0
	1 = NT Port Link Interface Expansion ROM is enabled, and NT Port Virtual Interface Expansion ROM is disabled	Offset F60h[15]=0 –or– NT Station offset 764h[0]=1	RO	Yes	0
13:1	***Reserved***		RsvdP	No	0-0h
31:14	**Expansion ROM Base Address** If the **Serial EEPROM Clock Frequency** register *Expansion ROM Size* bit (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offset 268h[16]) value is 0, the Expansion ROM size is 16 KB (default value is FFFF_C001h). Bit 14 is RW. If the *Expansion ROM Size* bit value is 1, the Expansion ROM size is 32 KB (default value is FFFF_8001h). Bit 14 is RO.	Offset F60h[15]=1 –or– NT Station offset 764h[0]=0	RsvdP	No	0-0h
		Offset F60h[15]=0 –or– NT Station offset 764h[0]=1	RW	Yes	0-0h

Register 16-13. 34h Capability Pointer

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
7:0	**Capability Pointer** Default 40h points to the **PCI Power Management Capability** structure.	RO	Yes	40h
31:8	***Reserved***	RsvdP	No	0000_00h

Register 16-14. 3Ch PCI Interrupt

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
7:0	**PCI Interrupt Line** The Interrupt Line Routing Value communicates interrupt line routing information. Values in this register are programmed by system software and are system architecture-specific. The value is used by device drivers and operating systems.	RW	Yes	00h
15:8	**PCI Interrupt Pin** Identifies the Conventional PCI Interrupt Message(s) the device (or device function) uses. Only value 00h or 01h is allowed in the PEX 8649. 00h = Indicates that the device does not use Conventional PCI Interrupt Message(s) 01h, 02h, 03h, and 04h = Maps to Conventional PCI Interrupt Messages for INTA#, INTB#, INTC#, and INTD#, respectively	RO	Yes	01h
23:16	**Min_Gnt** Minimum Grant. ***Reserved*** Does not apply to PCI Express.	RsvdP	No	00h
31:24	**Max_Lat** Maximum Latency. ***Reserved*** Does not apply to PCI Express.	RsvdP	No	00h

16.6 NT Port Link Interface PCI Power Management Capability Registers (Offsets 40h – 44h)

This section details the NT Port Link Interface PCI Power Management Capability registers. Table 16-3 defines the register map.

Table 16-3. NT Port Link Interface PCI Power Management Capability Register Map

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Power Management Capability		Next Capability Pointer (48h)	Capability ID (01h)	40h
PCI Power Management Data	PCI Power Management Control/Status Bridge Extensions *(Reserved)*	PCI Power Management Status and Control		44h

Register 16-15. 40h PCI Power Management Capability

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
7:0	**Capability ID** Default = 01h – only value allowed.	RO	Yes	01h
15:8	**Next Capability Pointer** Default 48h points to the **MSI Capability** structure.	RO	Yes	48h
18:16	**Version** Default = 011b – only value allowed.	RO	Yes	011b
19	**PME Clock** Power Management Event (PME) clock. Does not apply to PCI Express. Returns 0.	RsvdP	No	0
20	***Reserved***	RsvdP	No	0
21	**Device-Specific Initialization** 0 = Device-Specific Initialization is ***not*** required	RO	Yes	0
24:22	**AUX Current** The PEX 8649 does ***not support*** PME generation from the D3cold Device Power Management (PM) state; therefore, the serial EEPROM value for this field should be 000b.	RO	Yes	000b
25	**D1 Support** ***Not supported*** 0 = PEX 8649 does ***not support*** the D1 Device PM state	RsvdP	No	0
26	**D2 Support** ***Not supported*** 0 = PEX 8649 does ***not support*** the D2 Device PM state	RsvdP	No	0
31:27	**PME Support** The default value is applied to bits [31, 30, and 27] only. PME Messages are disabled, by default.	RO	Yes	0000_0b

Register 16-16. 44h PCI Power Management Status and Control

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
	PCI Power Management Status and Control			
1:0	**Power State** Used to determine the Port's current Device PM state, and to Set the Port into a new Device PM state. 00b = D0 01b = D1 – ***Not supported*** 10b = D2 – ***Not supported*** 11b = D3hot If software attempts to write an unsupported state to this field, the Write operation completes normally; however, the data is discarded and no state change occurs.	RW	Yes	00b
2	***Reserved***	RsvdP	No	0
3	**No Soft Reset** 1 = Devices transitioning from the D3hot to D0 Device PM state, because of Power State commands, do not perform an internal reset	RO	Yes	1
7:4	***Reserved***	RsvdP	No	0h
8	**PME Enable** Default value of 0 indicates that PME generation is disabled.	RsvdP	No	0
12:9	**Data Select** Initially writable by serial EEPROM and I^{2}C only[a]. This Configuration Space register (CSR) access privilege changes to RW after a Serial EEPROM and/or I^{2}C Write occurs to this register. Selects the **Data** and **Data Scale** registers (fields [31:24 and 14:13], respectively). 0h = D0 power consumed 3h = D3hot power consumed 4h = D0 power dissipated 7h = D3hot power dissipated All other encodings are ***reserved***.	RO	Yes	0h
14:13	**Data Scale** Writable by serial EEPROM and I^{2}C only[a]. Indicates the scaling factor to be used when interpreting the **Data** register value. The value and meaning of this field varies, depending upon which data value is selected by field [12:9] (*Data Select*). There are four internal **Data Scale** registers (one each, per *Data Select* values 0h, 3h, 4h and 7h). For other *Data Select* values, the **Data Scale** value returned is 0h.	RO	Yes	00b
15	**PME Status** 0 = PME is not being generated by the NT Port	RsvdP	No	0

Register 16-16. 44h PCI Power Management Status and Control *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
PCI Power Management Control/Status Bridge Extensions				
21:16	***Reserved***	RsvdP	No	0-0h
22	**B2/B3 Support** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.	RsvdP	No	0
23	**Bus Power/Clock Control Enable** ***Reserved*** Cleared, as required by the *PCI Power Mgmt. r1.2*.	RsvdP	No	0
PCI Power Management Data				
31:24	**Data** Writable by serial EEPROM and I^{2}C only[a]. There are four supported *Data Select* values (0h, 3h, 4h and 7h). For other *Data Select* values, the **Data Scale** value returned is 0h. Selected by field [12:9] (*Data Select*).	RO	Yes	00h

[a] *With no serial EEPROM nor previous I^{2}C programming, Reads return 00h for the* **Data** *and* **Data Scale** *registers (for all Data Selects).*

16.7 NT Port Link Interface MSI Capability Registers (Offsets 48h – 64h)

The registers detailed in Section 13.9, "MSI Capability Registers (Offsets 48h – 64h)," are also applicable to the NT Port Link Interface, except as defined in Table 16-4 (register map), and Register 16-17 through Register 16-19.

Table 16-4. NT Port Link Interface MSI Capability Register Map[a]

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
MSI Control		Next Capability Pointer (68h)	Capability ID (05h)	48h
MSI Address				4Ch
MSI Upper Address				50h
Reserved		MSI Data		54h
MSI Mask				58h
MSI Status				5Ch
Reserved				60h – 64h

[a] *Offsets 54h, 58h, and 5Ch change to 50h, 54h, and 58h, respectively, when the* ***MSI Control*** *register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.*

Register 16-17. 48h MSI Capability

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
MSI Capability Header				
7:0	**Capability ID** Program to 05h, as required by the *PCI r3.0*.	RO	Yes	05h
15:8	**Next Capability Pointer** Program to 68h, to point to the **PCI Express Capability** structure.	RO	Yes	68h
MSI Control				
16	**MSI Enable** 0 = MSIs for the NT Port Link Interface are disabled 1 = MSIs for the NT Port Link Interface are enabled, and INT*x* Interrupt Messages and PEX_INTA# output assertion are disabled	RW	Yes	0
19:17	**Multiple Message Capable** 000b = NT Port Link Interface can request only one Vector 001b = NT Port Link Interface can request two Vectors 010b = NT Port Link Interface can request four Vectors All other encodings are ***reserved***.	RO	Yes	010b
22:20	**Multiple Message Enable** 000b = NT Port Link Interface is allocated one Vector, by default 001b = NT Port Link Interface is allocated two Vectors 010b = NT Port Link Interface is allocated four Vectors All other encodings are ***reserved***. ***Note:*** *This field should not be programmed with a value larger than that of field [19:17] (Multiple Message Capable). If the value of this field is larger than that of field [19:17], the Multiple Message Capable value takes effect.*	RW	Yes	000b
23	**MSI 64-Bit Address Capable** 0 = PEX 8649 is capable of generating MSI 32-bit addresses (**MSI Address** register, offset 4Ch, is the Message address) 1 = PEX 8649 is capable of generating MSI 64-bit addresses (**MSI Address** register, offset 4Ch, is the lower 32 bits of the Message address, and **MSI Upper Address** register, offset 50h, is the upper 32 bits of the Message address)	RO	Yes	1
24	**Per Vector Masking Capable** 0 = PEX 8649 does not have Per Vector Masking capability 1 = PEX 8649 has Per Vector Masking capability	RO	Yes	1
31:25	***Reserved***	RsvdP	No	0-0h

Register 16-18. 58h MSI Mask

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
	The interrupt sources in the NT Port Link Interface are grouped into two categories – Power Management/Link State events and NT-Link Doorbell-generated interrupts. The number of allocated MSI Vectors is determined by the **MSI Control** register *Multiple Message Capable* and *Multiple Message Enable* fields (offset 48h[19:17 and 22:20], respectively). When the number of MSI Vectors that can be requested is: • **Two** – Both interrupt categories generate their own MSI Vector • **One** – Both interrupt categories generate the same MSI Vector ***Note:*** *The offset for this register changes from 58h, to 54h, when the **MSI Control** register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.* *The bits in this register can be used to mask their respective **MSI Status** register bits (offset 5Ch).*				
0	**MSI Mask for Link State Events** MSI mask for Power Management event- or Link State event-generated interrupts.	Offset 48h[22:20]=001b	RW	Yes	0
	MSI Mask for Shared Interrupt Sources MSI mask for all interrupt sources when the **MSI Control** register *Multiple Message Enable* field indicates that the Host has allocated one or two Vectors.	Offset 48h[22:20]=000b	RW	Yes	0
2:1	***Reserved***		RsvdP	No	00b
3	**MSI Mask for NT-Link Doorbell-Generated Interrupts** Refer to NT Port registers located at offsets C5Ch through C68h.	Offset 48h[22:20]=001b	RW	Yes	0
	Reserved	Offset 48h[22:20]=000b	RsvdP	No	0
31:4	***Reserved***		RsvdP	No	0000_000h

Register 16-19. 5Ch MSI Status

<table>
<tr><th>Bit(s)</th><th colspan="2">Description</th><th>Type</th><th>Serial EEPROM and I^{2}C</th><th>Default</th></tr>
<tr><td colspan="6">The interrupt sources in the NT Port Link Interface are grouped into two categories – Power Management/Link State events and NT-Link Doorbell-generated interrupts.
The number of allocated MSI Vectors is determined by the <b>MSI Control</b> register <i>Multiple Message Capable</i> and <i>Multiple Message Enable</i> fields (offset 48h[19:17 and 22:20], respectively). When the number of MSI Vectors that can be requested is:
• <b>Two</b> – Both interrupt categories generate their own MSI Vector
• <b>One</b> – Both interrupt categories generate the same MSI Vector
<b><i>Note:</i></b> <i>The offset for this register changes from 5Ch, to 58h, when the <b>MSI Control</b> register MSI 64-Bit Address Capable bit (offset 48h[23]) is Cleared.</i>
<i>The bits in this register can be masked by their respective <b>MSI Mask</b> register bits (offset 58h).</i></td></tr>
<tr><td rowspan="2">0</td><td><b>MSI Pending Status for Link State Events</b>
MSI pending status for Power Management event- or Link State event-generated interrupts.</td><td>Offset 48h[22:20]=001b</td><td>RO</td><td>No</td><td>0</td></tr>
<tr><td><b>MSI Pending Status for Shared Interrupt Sources</b>
MSI pending status for all interrupt sources when the <b>MSI Control</b> register <i>Multiple Message Enable</i> field indicates that the Host has allocated one or two Vectors.</td><td>Offset 48h[22:20]=000b</td><td>RO</td><td>No</td><td>0</td></tr>
<tr><td>2:1</td><td colspan="2"><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>00b</td></tr>
<tr><td rowspan="2">3</td><td><b>MSI Pending Status for NT-Link Doorbell-Generated Interrupts</b>
Refer to NT Port registers located at offsets C5Ch through C68h.</td><td>Offset 48h[22:20]=001b</td><td>RO</td><td>No</td><td>0</td></tr>
<tr><td><b><i>Reserved</i></b></td><td>Offset 48h[22:20]=000b</td><td>RsvdP</td><td>No</td><td>0</td></tr>
<tr><td>31:4</td><td colspan="2"><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>0000_000h</td></tr>
</table>

16.8 NT Port Link Interface PCI Express Capability Registers (Offsets 68h – A0h)

The registers detailed in Section 13.10, “PCI Express Capability Registers (Offsets 68h – A0h),” are also applicable to the NT Port Link Interface, except as defined in Table 16-5 (register map; offsets 7Ch, 80h, 8Ch, and 90h are ***reserved***), and Register 16-20 through Register 16-25.

Table 16-5. NT Port Link Interface PCI Express Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
PCI Express Capability	Next Capability Pointer (A4h)	Capability ID (10h)	68h
Device Capability			6Ch
Device Status	***Not Supported/Reserved***	Device Control	70h
Link Capability			74h
Link Status	***Reserved***	Link Control	78h
Reserved			7Ch – 94h
Link Status 2	Link Control 2		98h
Reserved			9Ch – A0h

Register 16-20. 68h PCI Express Capability List and Capability

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
	PCI Express Capability List			
7:0	**Capability ID** Program to 10h, by default.	RO	Yes	10h
15:8	**Next Capability Pointer** Program to A4h, to point to the **Subsystem Capability** structure.	RO	Yes	A4h
	PCI Express Capability			
19:16	**Capability Version** The PEX 8649 NT Port Link Interface programs this field to 2h, as required by the *PCI Express Base r2.0*.	RO	Yes	2h
23:20	**Device/Port Type** Default = PCI Express endpoint device.	RO	No	0h
24	**Slot Implemented** ***Not valid for PCI Express endpoint devices***	RsvdP	No	0
29:25	**Interrupt Message Number** The serial EEPROM writes 00_000b, because the Base Message and MSI Messages are the same.	RO	Yes	00_000b
31:30	***Reserved***	RsvdP	No	00b

Register 16-21. 6Ch Device Capability

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
2:0	**Maximum Payload Size Supported** Maximum Payload Size Port limitations are as follows: • 2,048 bytes if the number of Ports is ≤ 6 • 1,024 bytes if the number of Ports is > 6 and ≤ 12 000b = NT Port Link Interface supports a 128-byte maximum payload 001b = NT Port Link Interface supports a 256-byte maximum payload 010b = NT Port Link Interface supports a 512-byte maximum payload 011b = NT Port Link Interface supports a 1,024-byte maximum payload 100b = NT Port Link Interface supports a 2,048-byte maximum payload No other encodings are supported.	HwInit	Yes	011b = > 6 and ≤ 12 Ports 100b = ≤ 6 Ports
4:3	**Phantom Functions Supported** ***Not supported***	RO	Yes	00b
5	**Extended Tag Field Supported** 0 = Maximum *Tag* field is 5 bits 1 = Maximum *Tag* field is 8 bits	RO	Yes	0
8:6	**Endpoint L0s Acceptable Latency** 111b = No Limit	RO	Yes	111b
11:9	**Endpoint L1 Acceptable Latency** 111b = No Limit	RO	Yes	111b
14:12	***Reserved***	RsvdP	No	000b
15	**Role-Based Error Reporting**	RO	Yes	1
17:16	***Reserved***	RsvdP	No	00b
25:18	**Captured Slot Power Limit Value** For the NT Port Link Interface, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [27:26] (*Captured Slot Power Limit Scale*).	RO	Yes	00h
27:26	**Captured Slot Power Limit Scale** For the NT Port Link Interface, the upper limit on power supplied by the slot is determined by multiplying the value in this field by the value in field [25:18] (*Captured Slot Power Limit Value*). 00b = 1.0 01b = 0.1 10b = 0.01 11b = 0.001	RO	Yes	00b
31:28	***Reserved***	RsvdP	No	0h

Register 16-22. 70h Device Status and Control

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
Device Control				
0	**Correctable Error Reporting Enable** 0 = Disables 1 = Enables the NT Port Link Interface to report Correctable errors to the System Host	RW	Yes	0
1	**Non-Fatal Error Reporting Enable** 0 = Disables 1 = Enables the NT Port Link Interface to report Non-Fatal errors to the System Host	RW	Yes	0
2	**Fatal Error Reporting Enable** 0 = Disables 1 = Enables the NT Port Link Interface to report Fatal errors to the System Host	RW	Yes	0
3	**Unsupported Request Reporting Enable** 0 = Disables 1 = Enables the NT Port Link Interface to report UR errors as Error Messages with a programmed uncorrectable error severity	RW	Yes	0
4	**Enable Relaxed Ordering** ***Not supported***	RsvdP	No	0
7:5	**Maximum Payload Size** The NT Port Link Interface power-on/reset value is 000b, to support a Maximum Payload Size of 128 bytes. Software can change this field to configure the NT Port Link Interface to support other Payload sizes; however, software cannot change this field to a value larger than that indicated by the **Device Capability** register *Maximum Payload Size Supported* field (offset 6Ch[2:0]), for the NT Port Virtual and Link Interfaces. (Requester and Completer domains must possess the same Maximum Payload Size.) 000b = NT Port Link Interface supports a 128-byte maximum payload 001b = NT Port Link Interface supports a 256-byte maximum payload 010b = NT Port Link Interface supports a 512-byte maximum payload 011b = NT Port Link Interface supports a 1,024-byte maximum payload 100b = NT Port Link Interface supports a 2,048-byte maximum payload No other encodings are supported. ***Note:*** *Software must halt all transactions through the NT Port before changing this field.*	RW	Yes	000b
8	**Extended Tag Field Enable** ***Not supported***	RsvdP	No	0
9	**Phantom Functions Enable** ***Not supported***	RsvdP	No	0
10	**AUX Power PM Enable** ***Not supported***	RsvdP	No	0
11	**Enable No Snoop** ***Not supported***	RsvdP	No	0
14:12	**Maximum Read Request Size** ***Not supported***	RsvdP	No	000b
15	***Reserved***	RsvdP	No	0

Register 16-22. 70h Device Status and Control *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	Device Status			
16	**Correctable Error Detected** 0 = NT Port Link Interface did not detect a Correctable error 1 = NT Port Link Interface detected a Correctable error, regardless of the bit 0 (*Correctable Error Reporting Enable*) state.	RW1C	Yes	0
17	**Non-Fatal Error Detected** 0 = NT Port Link Interface did not detect a Non-Fatal error 1 = NT Port Link Interface detected a Non-Fatal error, regardless of the bit 1 (*Non-Fatal Error Reporting Enable*) state	RW1C	Yes	0
18	**Fatal Error Detected** 0 = NT Port Link Interface did not detect a Fatal error 1 = NT Port Link Interface detected a Fatal error, regardless of the bit 2 (*Fatal Error Reporting Enable*) state	RW1C	Yes	0
19	**Unsupported Request Detected** 0 = NT Port Link Interface did not detect a UR 1 = NT Port Link Interface detected a UR, regardless of the bit 3 (*Unsupported Request Reporting Enable*) state	RW1C	Yes	0
20	**AUX Power Detected** ***Not supported***	RsvdP	No	0
21	**Transactions Pending** ***Not supported*** Because the PEX 8649 NT Port is a bridging device, it does not track Completion for the corresponding Non-Posted transactions. Therefore, the NT Port Link Interface does not implement this bit.	RsvdP	No	0
31:22	***Reserved***	RsvdP	No	0-0h

Register 16-23. 74h Link Capability

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
3:0	**Supported Link Speeds** Indicates the NT Port Link Interface's supported Link speed. 0001b = 2.5 GT/s Link speed is supported 0010b = 5.0 GT/s and 2.5 GT/s Link speeds are supported All other encodings are ***reserved***.	RO	Yes	0010b (STRAP_RESERVED17#=H) 0001b (STRAP_RESERVED17#=L)
9:4	**Maximum Link Width** The PEX 8649 maximum Link width is x16 = 01_0000b. Actual maximum Link width is Set by the STRAP_STN*x*_PORTCFG*x* balls. 00_0000b = ***Reserved*** 00_0001b = x1 00_0010b = x2 00_0100b = x4 00_1000b = x8 01_0000b = x16 All other encodings are ***not supported***.	ROS	No	Set by STRAP_STN*x*_PORTCFG*x* ball levels, or by serial EEPROM value for the **Port Configuration**-related registers (Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface, offsets 300h through 308h)
11:10	**Active State Power Management (ASPM) Support** Active State Link PM support. Indicates the level of ASPM supported by the Port. 01b = L0s Link PM state entry is supported 11b = L0s and L1 Link PM states are supported All other encodings are ***reserved***.	RO	Yes	11b

Register 16-23. 74h Link Capability *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
14:12	**L0s Exit Latency** Indicates the L0s Link PM state exit latency for the given PCI Express Link. Value depends upon the Port's **Synchronous Advertised N_FTS** or **Asynchronous Advertised N_FTS** register (Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface, offset B84h or B88h, respectively) *Port x Advertised N_FTS* field value, Link speed, and state of the Port's **Link Control** register *Common Clock Configuration* bit (offset 78h[6]). When the *Common Clock Configuration* bit is Set, the Synchronous Advertised N_FTS register value is used; otherwise, the Asynchronous Advertised N_FTS register value is used. Exit latency is calculated, as follows: • **2.5 GHz** – Multiply *Port x Advertised N_FTS* x 4 (4 symbol times in 1 N_FTS) x 4 ns (1 symbol time at 2.5 GT/s) • **5.0 GHz** – Multiply *Port x Advertised N_FTS* x 4 (4 symbol times in 1 N_FTS) x 2 ns (1 symbol time at 5.0 GT/s) 100b = NT Port Link Interface L0s Link PM state Exit Latency is 512 ns to less than 1 µs at 5.0 GT/s 101b = NT Port Link Interface L0s Link PM state Exit Latency is 1 µs to less than 2 µs at 2.5 GT/s All other encodings are ***reserved***.	RO	No	100b (5.0 GT/s) 101b (2.5 GT/s)
17:15	**L1 Exit Latency** Indicates the L1 Link PM state exit latency for the given PCI Express Link. Value depends upon the Link speed. 001b = NT Port Link Interface L1 Link PM state Exit Latency is 1 µs to less than 2 µs at 5.0 GT/s 010b = NT Port Link Interface L1 Link PM state Exit Latency is 2 µs to less than 4 µs at 2.5 GT/s All other encodings are ***reserved***.	RO	Yes	001b (5.0 GT/s) 010b (2.5 GT/s)
18	**Clock Power Management**	RO	Yes	0
23:19	***Reserved***	RsvdP	No	0-0h

Register 16-23. 74h Link Capability *(Cont.)*

<table>
<tr><th>Bit(s)</th><th>Description</th><th>Type</th><th>Serial EEPROM and I^2C</th><th>Default</th></tr>
<tr><td>31:24</td><td><b>NT Port Number</b>
The NT Port Number value is selected by the STRAP_NT_UPSTRM_PORTSEL[4, 2:0] Strapping balls. All other encodings are <b><i>reserved</i></b>.
<table>
<tr><th>Field Value</th><th>Strapping Ball Value</th><th>Port Number</th></tr>
<tr><td>00h</td><td>0000b (LLLL)</td><td>0</td></tr>
<tr><td>01h</td><td>0001b (LLLH)</td><td>1</td></tr>
<tr><td>02h</td><td>0010b (LLHL)</td><td>2</td></tr>
<tr><td>03h</td><td>0011b (LLHH)</td><td>3</td></tr>
<tr><td>08h</td><td>1000b (HLLL)</td><td>16</td></tr>
<tr><td>09h</td><td>1001b (HLLH)</td><td>17</td></tr>
<tr><td>0Ah</td><td>1010b (HLHL)</td><td>18</td></tr>
<tr><td>0Bh</td><td>1011b (HLHH)</td><td>19</td></tr>
<tr><td>0Ch</td><td>1100b (HHLL)</td><td>20</td></tr>
<tr><td>0Dh</td><td>1101b (HHLH)</td><td>21</td></tr>
<tr><td>0Eh</td><td>1110b (HHHL)</td><td>22</td></tr>
<tr><td>0Fh</td><td>1111b (HHHH)</td><td>23</td></tr>
</table></td><td>ROS</td><td>No</td><td>Set by STRAP_NT_UPSTRM_PORTSEL[4, 2:0] ball levels</td></tr>
</table>

Register 16-24. 78h Link Status and Control

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	Link Control			
1:0	**Active State Power Management (ASPM) Control** 00b = Disable[a] 01b = Enables only L0s Link PM state Entry 10b = Enables only L1 Link PM state Entry 11b = Enables both L0s and L1 Link PM state Entries	RW	Yes	00b
2	***Reserved***	RsvdP	No	0
3	**Read Request Return Parameter Control** Read Request Return Parameter "R" control. Read Completion Boundary (RCB).	RO	Yes	0
4	**Link Disable** ***Reserved*** for the NT Port Link Interface.	RsvdP	No	0
5	**Retrain Link** ***Reserved*** for the NT Port Link Interface. Always read as 0.	RsvdP	No	0
6	**Common Clock Configuration** 0 = NT Port Link Interface and the device at the other end of the Port's PCI Express Link use an asynchronous Reference Clock source 1 = NT Port Link Interface and the device at the other end of the Port's PCI Express Link use a common Reference Clock source (constant phase relationship)	RW	Yes	0
7	**Extended Sync** Setting this bit causes the NT Port Link Interface to transmit: • 4,096 FTS Ordered-Sets in the L0s Link PM state, • Followed by a single SKIP Ordered-Set prior to entering the L0 Link PM state, • Finally, transmission of 1,024 TS1 Ordered-Sets in the *Recovery* state.	RW	Yes	0
15:8	***Reserved***	RsvdP	No	00h

Register 16-24. 78h Link Status and Control *(Cont.)*

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
Link Status				
19:16	**Current Link Speed** Indicates the negotiated Link speed of the Port’s PCI Express Link. 0001b = 2.5 GT/s Link speed 0010b = 5.0 GT/s Link speed All other encodings are ***reserved***. The value in this field is undefined when the Link is not up.	RO	No	0001b
25:20	**Negotiated Link Width** Dependent upon the configuration of the physical Ports. Link width is determined by the negotiated value with the attached Lane/Port. If the Link is not up, the value of this field is undefined. 00_0000b = Link is down (default) 00_0001b = x1 00_0010b = x2 00_0100b = x4 00_1000b = x8 01_0000b = x16 All other encodings are ***not supported***.	RO	No	00_0000b
26	***Reserved***	RsvdP	No	0
27	**Link Training** ***Reserved*** for the NT Port Link Interface.	RsvdP	No	0
28	**Slot Clock Configuration** Set by the upstream Port or NT Port Link Interface, but not both. 0 = Indicates that the PEX 8649 uses an independent clock 1 = Indicates that the PEX 8649 uses the same physical Reference Clock that the platform provides on the connector	HwInit	Yes	0
31:29	***Reserved***	RsvdP	No	000b

a. The Port Receiver must be capable of entering the L0s Link PM state, regardless of whether the state is disabled.

Register 16-25. 98h Link Status and Control 2

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
	Link Control 2			
3:0	**Target Link Speed** 0001b = 2.5 GT/s Link speed is supported 0010b = 5.0 GT/s Link speed is supported All other encodings are ***reserved***.	RWS	Yes	0010b
4	**Enter Compliance**	RWS	Yes	0
5	**Hardware Autonomous Speed Disable** ***Reserved*** Initial transition to the highest supported common Link speed is not blocked by this bit.	RsvdP	No	0
6	**Selectable De-Emphasis** ***Reserved***	RsvdP	Yes	0
9:7	**Transmit Margin** Intended for debug and compliance testing only.	RWS	Yes	000b
10	**Enter Modified Compliance**	RWS	Yes	0
11	**Compliance SOS** 1 = Link Training and Status State Machine (LTSSM) must periodically send SKIP Ordered-Sets between sequences when sending the Compliance Pattern or Modified Compliance Pattern	RWS	Yes	0
12	**Compliance De-Emphasis** Sets the de-emphasis level in the *Polling.Compliance* state, if the entry occurred due to bit 4 (*Enter Compliance*) being Set.	RWS	Yes	0
15:13	***Reserved***	RsvdP	No	000b
	Link Status 2			
16	**Current De-Emphasis Level** Reflects the de-emphasis level. 0 = -6 dB (Link is operating at 5.0 GT/s) 1 = -3.5 dB	RO	No	0 (5.0 GT/s) 1 (2.5 GT/s)
31:17	***Reserved***	RsvdP	No	0-0h

16.9 NT Port Link Interface Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – C4h)

The registers detailed in Section 13.11, "Subsystem ID and Subsystem Vendor ID Capability Registers (Offsets A4h – FCh)," are also applicable to the NT Port, except as defined in Table 16-6 (register map) and Register 16-26.

Table 16-6. NT Port Link Interface Subsystem ID and Subsystem Vendor ID Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved	Next Capability Pointer (C8h)	SSID/SSVID Capability ID (0Dh)	A4h
Subsystem ID	Subsystem Vendor ID		A8h
Reserved			ACh – C4h

Register 16-26. A4h Subsystem Capability

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
7:0	**SSID/SSVID Capability ID** SSID/SSVID registers for the PCI-to-PCI bridge. Program to 0Dh, as required by the *PCI-to-PCI Bridge r1.2*.	RO	Yes	0Dh
15:8	**Next Capability Pointer** Program to C8h, to point to the **Vendor-Specific Capability 3** structure.	RO	Yes	C8h
31:16	***Reserved***	RsvdP	No	0000h

16.10 NT Port Link Interface Vendor-Specific Capability 3 Registers (Offsets C8h – FCh)

This section details the NT Port Link Interface Vendor-Specific Capability 3 registers. Table 16-7 defines the register map used by the NT Port Link Interface.

The Cursor Mechanism registers at offsets F8h and FCh provide a means for accessing PCI Express Extended Configuration Space registers (offsets 100h through FFFh) within the NT Port Link and Virtual Interfaces, when only standard PCI Configuration transactions (that do not support the *Extended Register Number* field within the Completion Request Header) are available.

Table 16-7. NT Port Link Interface Vendor-Specific Capability 3 Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16		15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Reserved	Vendor-Specific Capability 3	Next Capability Pointer (00h)	Capability ID 3 (09h)	C8h
Vendor-Specific Header 3 ***(Reserved)***				CCh
Reserved				D0h – E0h
NT Port Link Interface BAR0/1 Setup				E4h
NT Port Link Interface Memory BAR2 Setup				E8h
NT Port Link Interface Memory BAR2/3 Setup				ECh
NT Port Link Interface Memory BAR4 Setup				F0h
NT Port Link Interface Memory BAR4/5 Setup				F4h
Configuration Address Window		***Reserved***		F8h
Configuration Data Window				FCh

Register 16-27. C8h Vendor-Specific Capability 3

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
7:0	**Capability ID 3**	RO	Yes	09h
15:8	**Next Capability Pointer** 00h = This capability is the last capability in the Linked List	RO	Yes	00h
23:16	**Length** Number of bytes in this Capability structure.	RO	Yes	38h
31:24	***Reserved***	RsvdP	No	00h

Register 16-28. CCh Vendor-Specific Header 3

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
31:0	***Reserved***	RO	Yes	0380_0002h

Register 16-29. E4h NT Port Link Interface BAR0/1 Setup

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
1:0	**BAR0/1 Enable** 00b = Disables Link Interface **BAR0** and **BAR1** 01b = ***Reserved*** 10b = Enables Link Interface **BAR0** and disables **BAR1** (**BAR0** is a 32-bit BAR) 11b = Enables Link Interface **BAR0** and **BAR1** (**BAR0/1** is a 64-bit BAR)	RW	No	10b
2	**BAR0 Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	RW	No	0
31:3	***Reserved***	RsvdP	No	0-0h

Register 16-30. E8h NT Port Link Interface Memory BAR2 Setup

<table>
<tr><th>Bit(s)</th><th colspan="2">Description</th><th>Type</th><th>Serial EEPROM and I^2C</th><th>Default</th></tr>
<tr><td>0</td><td colspan="2"><b>Type Selector</b></td><td>RsvdP</td><td>No</td><td>0</td></tr>
<tr><td>2:1</td><td colspan="2"><b>BAR2 Type</b>
00b = <b>BAR2</b> is implemented as a 32-bit Memory BAR
10b = <b>BAR2/3</b> is implemented as a 64-bit Memory BAR
No other encodings are allowed.</td><td>RW</td><td>Yes</td><td>00b</td></tr>
<tr><td>3</td><td colspan="2"><b>Prefetchable</b>
0 = Non-Prefetchable
1 = Prefetchable</td><td>RW</td><td>Yes</td><td>0</td></tr>
<tr><td>19:4</td><td colspan="2"><b><i>Reserved</i></b></td><td>RsvdP</td><td>No</td><td>0_000h</td></tr>
<tr><td>30:20</td><td colspan="2"><b>BAR2 Size</b>
Specifies the Address Range size requested by <b>BAR2</b>.
0 = Corresponding <b>BAR2</b> bits are RO bits that always return 0, and Writes are ignored
1 = Corresponding <b>BAR2</b> bits are RW bits</td><td>RW</td><td>Yes</td><td>0-0h</td></tr>
<tr><td rowspan="2">31</td><td><b>BAR2 Enable</b>
0 = <b>BAR2</b> is disabled, all <b>BAR2</b> bits read 0
1 = <b>BAR2</b> is enabled</td><td>Field [2:1] (<i>BAR2 Type</i>) = 00b</td><td>RW</td><td>Yes</td><td>0</td></tr>
<tr><td><b>BAR2 Size</b>
Included with field [30:20] when this BAR is used as a 64-bit BAR.</td><td>Field [2:1] (<i>BAR2 Type</i>) = 10b</td><td>RW</td><td>Yes</td><td>0</td></tr>
</table>

Register 16-31. ECh NT Port Link Interface Memory BAR2/3 Setup

Bit(s)	Description		Type	Serial EEPROM and I^2C	Default
Note: *This register has RW privilege if **BAR2/3** is configured as a 64-bit BAR (**NT Port Link Interface Memory BAR2 Setup** register BAR2 Type field, offset E8h[2:1], is programmed to 10b).*					
0	**Type Selector**	Offset E8h[2:1]=00b	RsvdP	No	0
		Offset E8h[2:1]=10b	RW	Yes	0
2:1	**BAR3 Type** 00b = **BAR3** is implemented as a 32-bit Memory BAR No other encodings are allowed.	Offset E8h[2:1]=00b	RsvdP	No	00b
		Offset E8h[2:1]=10b	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***	Offset E8h[2:1]=00b	RsvdP	No	0_000h
	When **BAR2/3** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset E8h[2:1]=10b	RW	Yes	0_000h
30:20	**BAR3 Size** Specifies the Address Range size requested by **BAR3**. 0 = Corresponding **BAR3** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR3** bits are RW bits		RW	Yes	0-0h
31	**BAR3 Enable** **32-Bit BAR** 0 = **BAR3** is disabled 1 = **BAR3** is enabled as a 32-bit BAR	Offset E8h[2:1]=00b	RW	Yes	0
	64-Bit BAR 0 = **BAR2/3** is disabled, all **BAR2/3** bits read 0 1 = **BAR2/3** is enabled as a 64-bit BAR	Offset E8h[2:1]=10b	RW	Yes	0

Register 16-32. F0h NT Port Link Interface Memory BAR4 Setup

Bit(s)	Description		Type	Serial EEPROM and I^{2}C	Default
0	**Type Selector**		RsvdP	No	0
2:1	**BAR4 Type** 00b = **BAR4** is implemented as a 32-bit Memory BAR (**BAR4**) 10b = **BAR4/5** is implemented as a 64-bit Memory BAR (**BAR4/5**) No other encodings are allowed.		RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable		RW	Yes	0
19:4	***Reserved***		RsvdP	No	0_000h
30:20	**BAR4 Size** Specifies the Address Range size requested by **BAR4**. 0 = Corresponding **BAR4** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR4** bits are RW bits		RW	Yes	0-0h
31	**BAR4 Enable** 0 = **BAR4** is disabled, all **BAR4** bits read 0 1 = **BAR4** is enabled	Field [2:1] (*BAR4 Type*) = 00b	RW	Yes	0
	BAR4 Size Included with field [30:20] when this BAR is used as a 64-bit BAR.	Field [2:1] (*BAR4 Type*) = 10b	RW	Yes	0

Register 16-33. F4h NT Port Link Interface Memory BAR4/5 Setup

Bit(s)	Description		Type	Serial EEPROM and I^{2}C	Default
Note: *This register has RW privilege if **BAR4/5** is configured as a 64-bit BAR (**NT Port Link Interface Memory BAR4 Setup** register BAR4 Type field, offset F0h[2:1], is programmed to 10b).*					
0	**Type Selector**	Offset F0h[2:1]=00b	RsvdP	No	0
		Offset F0h[2:1]=10b	RW	Yes	0
2:1	**BAR5 Type** 00b = **BAR5** is implemented as a 32-bit Memory BAR No other encodings are allowed.	Offset F0h[2:1]=00b	RsvdP	No	00b
		Offset F0h[2:1]=10b	RW	Yes	00b
3	**Prefetchable** 0 = Non-Prefetchable 1 = Prefetchable	Offset F0h[2:1]=00b	RsvdP	No	0
		Offset F0h[2:1]=10b	RW	Yes	0
19:4	***Reserved***	Offset F0h[2:1]=00b	RsvdP	No	0_000h
	When **BAR4/5** are used as a 64-bit BAR, bits [31:0] (including bits [19:4]) are used as the upper 32 bits.	Offset F0h[2:1]=10b	RW	Yes	0_000h
30:20	**BAR5 Size** Specifies the Address Range size requested by **BAR5**. 0 = Corresponding **BAR5** bits are RO bits that always return 0, and Writes are ignored 1 = Corresponding **BAR5** bits are RW bits		RW	Yes	0-0h
31	**BAR5 Enable** **32-Bit BAR** 0 = **BAR5** is disabled 1 = **BAR5** is enabled as a 32-bit BAR	Offset F0h[2:1]=00b	RW	Yes	0
	64-Bit BAR 0 = **BAR4/5** is disabled, all **BAR4/5** bits read 0 1 = **BAR4/5** is enabled as a 64-bit BAR	Offset F0h[2:1]=10b	RW	Yes	0

Register 16-34. F8h Configuration Address Window (Device-Specific Cursor Mechanism)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
15:0	***Reserved***	RsvdP	No	0000h
25:16	**Register Offset**	RW	Yes	0-0h
30:26	***Reserved***	RsvdP	No	0-0h
31	**Interface Select** 0 = Access is to the NT Port Link Interface Type 0 Configuration Space register 1 = Access is to the NT Port Virtual Interface Type 0 Configuration Space register	RW	Yes	0

Register 16-35. FCh Configuration Data Window (Device-Specific Cursor Mechanism)

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
31:0	**Register Data** Software selects a register by writing into the NT Port Link Interface Configuration Address window, then reads from or writes to that register using this register.	RW	Yes	0000_0000h

16.11 NT Port Link Interface Device Serial Number Extended Capability Registers (Offsets 100h – 134h)

The registers detailed in Section 13.12, “Device Serial Number Extended Capability Registers (Offsets 100h – 134h),” are also applicable to the NT Port. Table 16-8 defines the register map used by all Ports.

Table 16-8. NT Port Link Interface Device Serial Number Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16		15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (FB4h)	Capability Version (1h)	PCI Express Extended Capability ID (0003h)	100h
Serial Number (Lower DW)			104h
Serial Number (Upper DW)			108h
Reserved			10Ch – 134h

16.12 NT Port Link Interface Power Budget Extended Capability Registers (Offsets 138h – 144h)

The registers detailed in Section 13.13, “Power Budget Extended Capability Registers (Offsets 138h – 144h),” are also applicable to the NT Port Link Interface. Table 16-9 defines the register map used by all upstream Ports.

Table 16-9. NT Port Link Interface Power Budget Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16		15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (148h)	Capability Version (1h)	PCI Express Extended Capability ID (0004h)	138h
Reserved		Data Select	13Ch
Power Budget Data			140h
Power Budget Capability			144h

16.13 NT Port Link Interface Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)

The registers detailed in Section 13.14, "Virtual Channel Extended Capability Registers (Offsets 148h – 1BCh)," are also applicable to the NT Port Link Interface, except as defined in Table 16-10 (register map), and Register 16-36 through Register 16-40.

Table 16-10. NT Port Link Interface Virtual Channel Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16		15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0		
Next Capability Offset (C34h)	Capability Version (1h)	PCI Express Extended Capability ID (0002h)		148h
Reserved			Port VC Capability 1	14Ch
Port VC Capability 2				150h
Port VC Status ***(Reserved)***		Port VC Control		154h
Reserved		VC0 Resource Capability		158h
VC0 Resource Control				15Ch
VC0 Resource Status		***Reserved***		160h
Reserved				164h – 1BCh

Register 16-36. 148h Virtual Channel Extended Capability Header

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
15:0	**PCI Express Extended Capability ID** Program to 0002h, as required by the *PCI Express Base r2.0*.	RO	No	0002h
19:16	**Capability Version** Program to 1h, as required by the *PCI Express Base r2.0*.	RO	No	1h
31:20	**Next Capability Offset** Next extended capability is the **Vendor-Specific Extended Capability 2** structure, offset C34h.	RO	No	C34h

Register 16-37. 14Ch Port VC Capability 1

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
0	**Extended VC Counter** 0 = NT Port Link Interface supports only one Virtual Channel (VC0) 1 = ***Reserved***	RO	No	0
3:1	***Reserved***	RsvdP	No	000b
4	**Low-Priority Extended VC Counter** For Strict Priority arbitration, indicates the number of extended VCs (those in addition to VC0) that belong to the Low-Priority Virtual Channel group for the NT Port Link Interface. 0 = For NT Port Link Interface, only VC0 belongs to the Low-Priority Virtual Channel group 1 = ***Reserved***, because the PEX 8649 supports only one VC	RO	No	0
7:5	***Reserved***	RsvdP	No	000b
9:8	**Reference Clock** ***Reserved***	RsvdP	No	00b
11:10	**Port Arbitration Table Entry Size**	RsvdP	No	00b
31:12	***Reserved***	RsvdP	No	0000_0h

Register 16-38. 158h VC0 Resource Capability

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
1:0	**Port Arbitration Capability** Bit 0 = 1 – Non-configurable Round-Robin (Hardware-Fixed) arbitration Bit 1 = 1 – Weighted Round-Robin (WRR) arbitration with 64 Phases	RO	No	00b
13:2	***Reserved***	RsvdP	No	0-0h
14	**Advanced Packet Switching**	RsvdP	No	0
15	**Reject Snoop Transactions** Not a PCI Express switch feature; therefore, this bit is Cleared.	RsvdP	No	0
22:16	**Maximum Time Slots** ***Not supported***	RsvdP	No	000_0000b
23	***Reserved***	RsvdP	No	0
31:24	**Port Arbitration Table Offset**	RsvdP	No	00h

Register 16-39. 15Ch VC0 Resource Control

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
0	**TC/VC Map** Defines Traffic Classes [7:0], respectively, and indicates which TCs are mapped into VC0. Traffic Class 0 (TC0) must be mapped to VC0. By default, Traffic Classes [7:1] are mapped to VC0.	RO	No	1
7:1		RW	Yes	7Fh
15:8	***Reserved***	RsvdP	No	00h
16	**Load Port Arbitration Table** Hardware writable and software readable.	RW	Yes	0
19:17	**Port Arbitration Select** Selects the Port Arbitration type for the NT Port Link Interface. Indicates the bit number in the **VC0 Resource Capability** register *Port Arbitration Capability* field (offset 158h[1:0]) that corresponds to the arbitration type. 0 = Round-Robin (Hardware-Fixed) arbitration scheme	RW	Yes	000b
23:20	***Reserved***	RsvdP	No	0h
24	**VC ID** Defines the NT Port Link Interface VC0 ID code. 0 = VC0 (default; VC0 is the only/default VC) 1 = ***Reserved***	RO	No	0
30:25	***Reserved***	RsvdP	No	0-0h
31	**VC Enable** 0 = Not allowed 1 = Enables the NT Port Link Interface VC0	RO	No	1

Register 16-40. 160h VC0 Resource Status

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
15:0	***Reserved***	RsvdP	No	0000h
16	**Port Arbitration Table Status** ***Not implemented***	RO	No	0
17	**VC0 Negotiation Pending** 0 = VC0 negotiation completed 1 = VC0 initialization is not complete for the NT Port Link Interface	RO	Yes	1
31:18	***Reserved***	RsvdP	No	0-0h

16.14 NT Port Link Interface Device-Specific Registers (Offsets 1C0h – C88h)

The registers detailed in Section 13.15, "Device-Specific Registers (Offsets 1C0h – DFCh)," and Section 13.19, "Device-Specific Registers (Offsets F30h – FB0h)" (for offsets 1C0h through C88h), are unique to the PEX 8649 and not referenced in the *PCI Express Base r2.0*. These registers are also applicable to the NT Port Link Interface, except as defined in Table 16-11 (register map; offsets 1D0h through 1D8h, 200h through 6FCh, 760h through B6Ch, and B80h through BFCh, are ***reserved***; offsets C34h through C88h are ***not reserved***) through Table 16-14, and Register 16-43 through Register 16-47.

Other NT Port Link Interface Device-Specific registers are detailed in Section 16.16, "NT Port Link Interface Device-Specific Registers (Offsets F30h – FB0h)."

***Note:** It is recommended that these registers not be changed from their default values.*

Table 16-11. NT Port Link Interface Device-Specific Register Map (Offsets 1C0h – C88h)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16		15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved			1C0h – 1D8h
NT Port Link Interface Device-Specific Registers – Captured Bus and Device Number (Offsets 1DCh – 1FCh)			1DCh … 1FCh
Reserved			200h – 6FCh
NT Port Link Interface Device-Specific Registers – Error Checking and Debug (Offsets 700h – 75Ch)			700h … 75Ch
Reserved			760h – B6Ch
Next Capability Offset 2 (000h)	1h	PCI Express Extended Capability ID 2 (000Bh)	B70h
Device-Specific Registers – Vendor-Specific Extended Capability 2 (Offsets B70h – B7Ch)			… B7Ch
Reserved			B80h – C30h
Next Capability Offset 4 (B70h)	1h	PCI Express Extended Capability ID 4 (000Bh)	C34h
NT Port Link Interface Device-Specific Registers – Vendor-Specific Extended Capability 4 (Offsets C34h – C88h)			… C88h

16.14.1 NT Port Link Interface Device-Specific Registers – Captured Bus and Device Number (Offsets 1DCh – 1FCh)

The registers detailed in Section 13.15.2, “Device-Specific Registers – Captured Bus and Device Numbers (Offsets 1DCh – 1FCh),” are also applicable to the NT Port Link Interface, except as defined in Table 16-12 (register map; offset 1E0h is not ***reserved***; offset 1E4h is ***reserved***), and Register 16-41 and Register 16-42.

Table 16-12. NT Port Link Interface Device-Specific Captured Bus and Device Number Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0	
Reserved	NT Captured Bus Number	1DCh
Reserved	NT Captured Device Number	1E0h
Reserved		1E4h – 1FCh

Register 16-41. 1DCh NT Captured Bus Number

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Captured Bus Number** NT Port Link Interface Endpoint Captured Bus Number register value. ***Note: Overwriting the Captured Bus Number value is not recommended.***	RWS	Yes	00h
31:8	***Reserved***	RsvdP	No	0000_00h

Register 16-42. 1E0h NT Captured Device Number

Bit(s)	Description	Type	Serial EEPROM and I²C	Default
7:0	**Captured Device Number** NT Port Link Interface Endpoint Captured Device Number register value. ***Note: Overwriting the Captured Device Number value is not recommended.***	RWS	Yes	00h
31:8	***Reserved***	RsvdP	No	0000_00h

16.14.2 NT Port Link Interface Device-Specific Registers – Error Checking and Debug (Offsets 700h – 75Ch)

The registers detailed in Section 13.15.10, “Device-Specific Registers – Error Checking and Debug (Offsets 700h – 75Ch),” are also applicable to the NT Port Link Interface, except as defined in Table 16-13 (register map; offsets 700h through 71Ch are ***reserved*** and/or ***Factory Test Only***) and Register 16-43.

Table 16-13. Device-Specific Error Checking and Debug Register Map (Offsets 700h – 75Ch)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved/Factory Test Only		700h – 704h
Reserved		708h – 71Ch
Reserved	ECC Error Check Disable	720h
Reserved		724h – 75Ch

Register 16-43. 720h ECC Error Check Disable

Bit(s)	Description	Type	Serial EEPROM and I^2C	Default
1:0	***Not used***	RWS	Yes	00b
2	**Software Force Error Enable** 1 = **Correctable Error Status** and **Uncorrectable Error Status** registers (offsets FC4h and FB8h, respectively) change from RW1CS to RW	RWS	Yes	0
3	**Software Force Non-Posted Request** Used to select software-forced errors to be associated with Posted or Non-Posted TLPs, because some errors are handled differently, depending upon the TLP type (Posted or Non-Posted). 0 = Handle software-forced errors as if the errors are associated with Posted TLPs 1 = Enables handling of errors associated with Posted TLPs as if those errors are associated with Non-Posted TLPs	RWS	Yes	0
4	***Reserved***	RsvdP	No	0
5	**Enable PEX_INTA# Ball for Device-Specific Error-Triggered Interrupt** 0 = Device-Specific Error Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA#) 1 = Device-Specific Error Interrupt Requests assert PEX_INTA# (and do not send an INT*x* Message)	RWS	Yes	0
6	**Enable PEX_INTA# Ball Interrupt for GPIO-Generated Interrupts** 0 = General-Purpose Input/Output (GPIO) Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA#) 1 = GPIO Interrupt Requests assert PEX_INTA# (and do not send an INT*x* Message)	RWS	Yes	0
7	**Enable PEX_INTA# Ball Interrupt for NT Link Doorbell-Generated Interrupts** 0 = NT Port Link Interface Doorbell Interrupt Requests send an INT*x* Message (and do not assert PEX_INTA#) 1 = NT Port Virtual Link Doorbell Interrupt Requests assert PEX_INTA# (and do not send an INT*x* Message)	RWS	Yes	0
31:8	***Reserved***	RsvdP	No	0000_00h

16.14.3 NT Port Link Interface Device-Specific Registers – Vendor-Specific Extended Capability 4 (Offsets C34h – C88h)

The registers detailed in Section 15.14.5, "NT Port Virtual Interface Device-Specific Registers – Vendor-Specific Extended Capability 4 (Offsets C34h – C88h)," are also applicable to the NT Port Link Interface, except as defined in Table 16-14 (register map), and Register 16-44 through Register 16-47.

Table 16-14. NT Port Link Interface Device-Specific, Vendor-Specific Extended Capability 4 Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16		15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset 4 (B70h)	Capability Version 4 (1h)	PCI Express Extended Capability ID 4 (000Bh)	C34h
Vendor-Specific Header 4			C38h
Memory BAR2 Address Translation Lower			C3Ch
Memory BAR3 Address Translation Upper			C40h
Memory BAR4 Address Translation Lower			C44h
Memory BAR5 Address Translation Upper			C48h
Reserved		Virtual Interface IRQ Set	C4Ch
Reserved		Virtual Interface IRQ Clear	C50h
Reserved		Virtual Interface IRQ Mask Set	C54h
Reserved		Virtual Interface IRQ Mask Clear	C58h
Reserved		Link Interface IRQ Set	C5Ch
Reserved		Link Interface IRQ Clear	C60h
Reserved		Link Interface IRQ Mask Set	C64h
Reserved		Link Interface IRQ Mask Clear	C68h
NT Port SCRATCH0			C6Ch
NT Port SCRATCH1			C70h
NT Port SCRATCH2			C74h
NT Port SCRATCH3			C78h
NT Port SCRATCH4			C7Ch
NT Port SCRATCH5			C80h
NT Port SCRATCH6			C84h
NT Port SCRATCH7			C88h

Register 16-44. C3Ch Memory BAR2 Address Translation Lower

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**NT Port Link-to-Virtual Interface BAR2 Base Translation Address** Base Translation address when **BAR2** is enabled (**NT Port Link Interface Memory BAR2 Setup** register *BAR2 Enable* bit, offset E8h[31], is Set).	RW	Yes	000h

Register 16-45. C40h Memory BAR3 Address Translation Upper

Bit(s)	Description		Type	Serial EEPROM and I^{2}C	Default
19:0	***Reserved***	Offset ECh[31]=0	RsvdP	No	0_0000h
	When **BAR2/3** are used as a 64-bit BAR, bits [31:0] (including bits [19:0]) are used as the upper 32 bits.	Offset ECh[31]=1	RW	Yes	0_0000h
31:20	**NT Port Link-to-Virtual Interface BAR3 Base Translation Address** Base Translation address when **BAR3** is enabled (**NT Port Link Interface Memory BAR2/3 Setup** register *BAR3 Enable* bit, offset ECh[31], is Set).		RW	Yes	000h

Register 16-46. C44h Memory BAR4 Address Translation Lower

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
19:0	***Reserved***	RsvdP	No	0_0000h
31:20	**NT Port Link-to-Virtual Interface BAR4 Base Translation Address** Base Translation address when **BAR4** is enabled (**NT Port Link Interface Memory BAR4 Setup** register *BAR4 Enable* bit, offset F0h[31], is Set).	RW	Yes	000h

Register 16-47. C48h Memory BAR5 Address Translation Upper

Bit(s)	Description		Type	Serial EEPROM and I^{2}C	Default
19:0	***Reserved***	Offset F4h[31]=0	RsvdP	No	0_0000h
	When **BAR4/5** are used as a 64-bit BAR, bits [31:0] (including bits [19:0]) are used as the upper 32 bits.	Offset F4h[31]=1	RW	Yes	0_0000h
31:20	**NT Port Link-to-Virtual Interface BAR5 Base Translation Address** Base Translation address when **BAR5** is enabled (**NT Port Link Interface Memory BAR4/5 Setup** register *BAR5 Enable* bit, offset F4h[31], is Set).		RW	Yes	000h

16.15 NT Bridging-Specific Registers (Offsets C8Ch – EFCh)

Table 16-15 defines the register map of the NT Port Link Interface NT Bridging-Specific registers.

Table 16-15. NT Port Link Interface NT Bridging-Specific Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved		C8Ch – DB0h
NT Bridging-Specific Registers – Requester ID Translation Lookup Table Entry (Offsets DB4h – DF0h)		DB4h … DF0h
Reserved		DF4h – EFCh

16.15.1 NT Bridging-Specific Registers – Requester ID Translation Lookup Table Entry (Offsets DB4h – DF0h)

This section describes the NT Port Link Interface NT Bridging-Specific Requester ID Translation Lookup Table (LUT) Entry registers. The NT Port uses these registers for Requester ID translation when it forwards:

- Memory Requests from the NT Port Link Interface to the NT Port Virtual Interface, –or–
- Completion TLPs from the NT Port Virtual Interface to the NT Port Link Interface

If the application needs to send traffic through the NT Port Link Interface, program the registers listed in this group with the corresponding Requester's Requester ID, then Set the *LUT Entry_n Enable* and *LUT Entry_m Enable* bits (bits 0 and 16, respectively) for each LUT entry, as needed.

Table 16-16 defines the register and address locations, as they relate to Register 16-48.

Table 16-16. NT Port Link Interface NT Bridging-Specific Requester ID Translation LUT Entry*_n_m* Register Locations

ADDR Location	Lookup Table Entry*_n_m*	ADDR Location	Lookup Table Entry*_n_m*
DB4h	0_1	DD4h	16_17
DB8h	2_3	DD8h	18_19
DBCh	4_5	DDCh	20_21
DC0h	6_7	DE0h	22_23
DC4h	8_9	DE4h	24_25
DC8h	10_11	DE8h	26_27
DCCh	12_13	DECh	28_29
DD0h	14_15	DF0h	30_31

Register 16-48. DB4h – DF0h NT Port Link Interface Requester ID Translation LUT Entry_*n_m* (where *n_m* = 0_1 through 30_31)

Bit(s)	Description		Type	Serial EEPROM and I^{2}C	Default
0	**LUT Entry_*n* Enable** 0 = Disables 1 = Enables		RW	Yes	0
1	**LUT Entry_*n* No Snoop Enable** If Set, the NT Port Clears the TLP *No Snoop* attribute bit for the Memory Request, then goes from the NT Port Link Interface to the NT Port Virtual Interface, and re-calculates the End-to-end Cyclic Redundancy Check (ECRC). If the original TLP has an ECRC error, the NT Port corrupts the re-calculated ECRC before transmitting to the other Host domain. The NT Port sets the *No Snoop* attribute bit when it forwards the Completion TLP from the NT Port Virtual Interface to the NT Port Link Interface if this bit is Set for the corresponding Requester ID entry. This ECRC rule applies to Completion TLPs as well. 0 = Disables 1 = Enables		RW	Yes	0
2	***Reserved***		RsvdP	No	0
7:3	**Requester ID on Link Side**	**Device Number** LUT Entry_*n* Requester Device Number.	RW	Yes	0000_0b
15:8		**Bus Number** LUT Entry_*n* Requester Bus Number.	RW	Yes	00h
16	**LUT Entry_*m* Enable** 0 = Disables 1 = Enables		RW	Yes	0
17	**LUT Entry_*m* No Snoop Enable** If Set, the NT Port Clears the TLP *No Snoop* attribute bit for the Memory Request, then goes from the NT Port Link Interface to the NT Port Virtual Interface, and re-calculates the ECRC. If the original TLP has an ECRC error, the NT Port corrupts the re-calculated ECRC before transmitting to the other Host domain. The NT Port sets the *No Snoop* attribute bit when it forwards the Completion TLP from the NT Port Virtual Interface to the NT Link Virtual Interface if this bit is Set for the corresponding Requester ID entry. This ECRC rule applies to Completion TLPs as well. 0 = Disables 1 = Enables		RW	Yes	0
18	***Reserved***		RsvdP	No	0
23:19	**Requester ID on Link Side**	**Device Number** LUT Entry_*m* Requester Device Number.	RW	Yes	0000_0b
31:24		**Bus Number** LUT Entry_*m* Requester Bus Number.	RW	Yes	00h

16.16 NT Port Link Interface Device-Specific Registers (Offsets F30h – FB0h)

The registers detailed in Section 13.19, “Device-Specific Registers (Offsets F30h – FB0h),” are unique to the PEX 8649 and not referenced in the *PCI Express Base r2.0*. These registers are also applicable to the NT Port Link Interface, except as defined in Table 16-17 (register map) through Table 16-19, and Register 16-49.

Other NT Port Link Interface Device-Specific registers are detailed in Section 16.14, “NT Port Link Interface Device-Specific Registers (Offsets 1C0h – C88h).”

Note: It is recommended that these registers not be changed from their default values.

Table 16-17. NT Port Link Interface Device-Specific Register Map (Offsets F30h – FB0h)

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved		F30h – F44h
NT Port Link Interface Device-Specific Registers – Ingress Control and Port Enable (Offsets F48h – F6Ch)		F48h … F6Ch
NT Port Link Interface Device-Specific Registers – Error Checking and Debug (Offsets F70h – FB0h)		F70h … FB0h

16.16.1 NT Port Link Interface Device-Specific Registers – Ingress Control and Port Enable (Offsets F48h – F6Ch)

The registers detailed in Section 13.19.2, “Device-Specific Registers – Ingress Control and Port Enable (Offsets F48h – F6Ch),” are also applicable to the NT Port Link Interface, except as defined in Table 16-18 (register map; offsets F48h and F60h are ***reserved***).

Table 16-18. NT Port Link Interface Device-Specific Ingress Control and Port Enable Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Reserved		F48h
Port Enable Status		F4Ch
Reserved	Negotiated Link Width for Ports 0, 1, 2, 3	F50h
Reserved		F54h
Negotiated Link Width for Ports 16, 17, 18, 19, 20, 21, 22, 23		F58h
Reserved		F5Ch – F6Ch

16.16.2 NT Port Link Interface Device-Specific Registers – Error Checking and Debug (Offsets F70h – FB0h)

The registers detailed in Section 13.19.3, "Device-Specific Registers – Error Checking and Debug (Offsets F70h – FB0h)," are also applicable to the NT Port Link Interface, except as defined in Table 16-19 (register map) and Register 16-49.

Other NT Port Link Interface Device-Specific Error Checking and Debug registers are detailed in Section 16.14.2, "NT Port Link Interface Device-Specific Registers – Error Checking and Debug (Offsets 700h – 75Ch)."

Table 16-19. NT Port Link Interface Device-Specific Error Checking and Debug Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Power Management Hot Plug User Configuration	F70h
Reserved	F74h – FA4h
ACK Transmission Latency Limit	FA8h
Bad TLP Counter	FACh
Bad DLLP Counter	FB0h

Register 16-49. F70h Power Management Hot Plug User Configuration

Bit(s)	Description	Type	Serial EEPROM and I^{2}C	Default
0	**L0s Entry Idle Counter** Traffic Idle time to meet, to enter the L0s Link PM state. 0 = Idle condition must last 1 µs 1 = Idle condition must last 4 µs	RWS	Yes	0
7:1	***Factory Test Only***	RWS	Yes	0-0h
8	**DLLP Timeout Link Retrain Disable** Disable Link retraining when no Data Link Layer Packets (DLLPs) are received for more than 256 µs. 0 = Enables Link retraining when no DLLPs are received for more than 256 µs (default) 1 = DLLP Timeout is disabled	RWS	Yes	0
9	***Factory Test Only***	RWS	Yes	0
10	**L0s Entry Disable** 0 = Enables entry into the L0s Link PM state on a Port when the L0s idle conditions are met 1 = Disables entry into the L0s Link PM state on a Port when the L0s idle conditions are met	RWS	Yes	0
31:11	***Reserved***	RsvdP	No	0-0h

16.17 NT Port Link Interface Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)

The registers detailed in Section 15.17, "NT Port Virtual Interface Advanced Error Reporting Extended Capability Registers (Offsets FB4h – FDCh)," are also applicable to the NT Port Link Interface. Table 16-20 defines the register map for the NT Port.

Table 16-20. NT Port Link Interface Advanced Error Reporting Extended Capability Register Map

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16		15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
Next Capability Offset (138h)	Capability Version (1h)	PCI Express Extended Capability ID (0001h)	FB4h
Uncorrectable Error Status			FB8h
Uncorrectable Error Mask			FBCh
Uncorrectable Error Severity			FC0h
Correctable Error Status			FC4h
Correctable Error Mask			FC8h
Advanced Error Capabilities and Control			FCCh
Header Log 0			FD0h
Header Log 1			FD4h
Header Log 2			FD8h
Header Log 3			FDCh

Chapter 17 Test and Debug

17.1 Introduction

This chapter describes the following test- and debug-related information:

- Physical Layer Loopback Operation
- User Test Pattern
- Pseudo-Random Bit Sequence
- Using the SerDes Quad x Diagnostic Data Registers
- Pseudo-Random and Bit-Pattern Generation
- PHY Testability Features
- JTAG Interface
- Port Good Status LEDs

17.2 Physical Layer Loopback Operation

17.2.1 Overview

Physical Layer (PHY) Loopback functions are used to test the SerDes in the PEX 8649, connections between devices, and SerDes of external devices, as well as various PEX 8649 and external digital logic. The PEX 8649 supports four types of Loopback operations, as described in Table 17-1. Additional information regarding each type is provided in the sections that follow.

Table 17-1. Loopback Operations

Operation	Description
Analog Loopback Master Mode	This mode depends upon an external device or passive connection (*such as* a cable) to loopback the transmitted data to the PEX 8649, without SKIP Ordered-Set clock compensation. If an external device is used, it must not include its Elastic buffer in the Slave Loopback data path, so that SKIP Ordered-Sets are not inserted. A device's re-transmitted Receive data must be sent back to the Master, synchronous to the Master's Transmit Reference Clock. *That is*, the Slave device re-serializes the Transmit data, using the recovered clock from the received data. In that mode, the PRBS generator and checker should be used to create and check the data pattern.
Digital Loopback Master Mode	This mode depends upon an external device to loopback the transmitted data that includes at least its Elastic buffer in the Loopback data path, allowing for reliable loopback testing, in case the two devices have asynchronous Reference Clock sources with Parts per Million (PPM) offsets. The Master's pattern generator inserts SKIP Ordered-Sets at regular intervals, and its received data checker can handle PPM offset clock compensation, by way of SKIP symbol addition or deletion. The PEX 8649 provides a User Test Pattern generator and checker that can be used for Digital loopback testing.
Analog Loopback Slave Mode	The PEX 8649 enters this mode when an external device transmits Training Sets with the *Loopback* Training Control Bit Set and the **Physical Layer Test** register *Analog Loopback Enable* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 228h[6]) is Set. Another way to unconditionally force the Slave into Analog loopback is described later in Section 17.2.4. While in this mode, the received data is looped back from the SerDes 10-bit Receive interface to the 10-bit Transmit interface. Internal to the SerDes, the serial-to-parallel and parallel-to-serial converters are included in the Loopback data path. The re-serialized data is transmitted back to the Master device synchronous to that Master's Reference Clock. This is because the recovered clock is fed back around to the Transmit Data interface and used as the Tx clock.
Digital Loopback Slave Mode	The PEX 8649 enters this mode when an external device transmits Training Sets with the *Loopback* Training Control Bit Set and the **Physical Layer Test** register *Analog Loopback Enable* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 228h[6]) is Cleared. This is the default Loopback mode for the LTSSM Slave *Loopback.Active* state. In this mode, the data is looped back at the 8-bit level, which includes the PEX 8649's Elastic buffer, 8b/10b decoder, and 8b/10b encoder in the Slave Loopback data path. Asynchronous clock compensation can occur in the Elastic buffer through SKIP symbol addition or deletion, depending upon clock PPM offsets and fill threshold decoding. The Master data pattern checker must be able to handle the presence of SKIP Ordered-Sets and variations in their contents.

17.2.2 Analog Loopback Master Mode

Analog Loopback Master mode is typically used for Analog Far-End testing (refer to Figure 17-1), with a shallow Loopback path Slave device, to determine overall Bit Error rates. However, it can also be used for passive external serial loopback with a cable. Looping back with a cable includes the internal circuitry, package connections to bond pads, package balls, board traces, and any connectors that might be in the test data path, as illustrated in Figure 17-2. A PRBS pattern is typically used for this mode, because it is appropriate for bit error rate testing. A User Test Pattern (UTP) is ***not*** recommended for this application – refer to Section 17.3 for details.

Figure 17-1. Analog Far-End Loopback

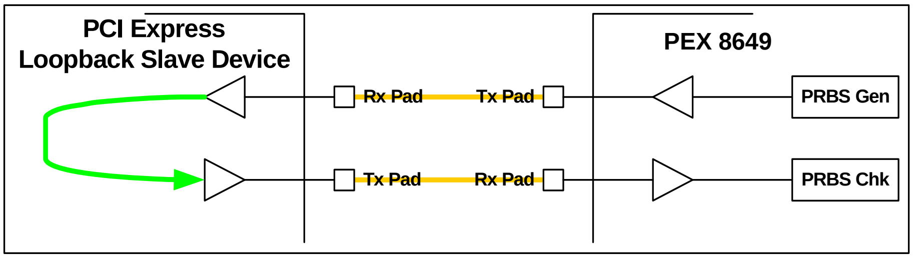
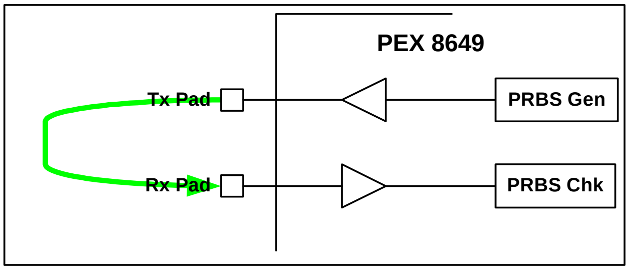


Figure 17-2. Cable Loopback



17.2.2.1 Initiating Far-End Analog Operations in PEX 8649 Master Devices

Note: *Initiating a Master Loopback operation on an upstream Port can cause a Deadlock condition to occur, unless an I^2C Slave interface is used to write and read Configuration Space register bits instead of writing them through upstream Port Configuration transactions. Therefore, it is recommended to restrict Analog Master loopback testing to downstream Ports when external devices are used.*

One way to test Master Analog loopback with passive cables is to have an upstream Port connected to a Root Complex, for Configuration Write/Read transactions that are used to Set and monitor the key device register bits. In that case, only downstream Ports would be test-capable, to avoid potential Deadlock conditions on the upstream Port. Alternatively, an I^2C Slave interface and Rapid Development Kit (RDK) software could be used to write or read the registers. This makes any Port testable. The user has the option of attaching one or more cables to the appropriate high-speed Tx and Rx differential pairs that belong to the Ports being tested.

Loopback cables can be attached before or after a standard power-up initialization sequence. If the cables are attached before power-up, use a serial EEPROM to program the **Physical Layer Port Command** register *Port x Loopback Command* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 230h[0, 4, 8, or 12]) for the Port being tested. The Port's *Port x Loopback Command* bit arms the Port to enter the Master *Loopback.Entry* state. When written from a serial EEPROM, the bit's assertion is present before the Ports begin Link training. In that case, the Ports directly transition to the LTSSM *Loopback* state from the LTSSM *Configuration* state. The LTSSM exits the *Polling* state and enters the *Configuration.LinkWidth.Start* state, then immediately transitions to the Master *Loopback.Entry* state.

At this point, users can sample the Port's **Physical Layer Port Command** register *Port x Ready as Loopback Master* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 230h[3, 7, 11, or 15]), to determine whether the bit is Set, which indicates that the Master has reached the LTSSM *Loopback.Active* state. At this time, the PRBS engine can be enabled, by Setting the **Physical Layer Test** register *SerDes Quad x PRBS Enable* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 228h[19:16]) associated with the SerDes assigned to the Port being tested.

The PRBS Receive data checker first synchronizes the de-serialized parallel data words from the returned pattern with a reference PRBS pattern generator. At this point, users should check the Lane synchronization status in the **PRBS Control/Status** register *PRBS Pattern Sync Status Device Lane x* bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 258h[15:0]). If there is no synchronization, there is likely a physical connection problem. Once synchronized, the PRBS checker looks for errors, on a continuous basis. Any errors detected are logged in one or more of the **SerDes Quad *x* Diagnostic Data** register RO bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets 238h through 244h, bits [30, 23:0]). The errors can be retrieved, by reading the appropriate bit.

If the *Port x Loopback Command* bits are not Set through the serial EEPROM, the Ports' Loopback Training Sets can be used to cause the Ports to linkup, by way of a Configuration cross-link track, resulting with the Ports being in L0 Link Power Management (PM) state. This linkup of a Port, in response to its own Training Sets, only works if the Port's **Physical Layer Additional Status/Control** register *Port x External Loopback Enable* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 254h[19:16]) is Set by serial EEPROM. Once the Port is in the L0 Link PM state, Configuration Space register programming can then be performed manually, to invoke a Master Loopback operation.

Once the Ports linkup, users can direct the Ports into an Analog Loopback Master condition, by writing the *Port x Loopback Command* bit(s), through the upstream Port and/or I^{2}C Slave interface. However, this is not sufficient to initiate the LTSSM transition from the L0 Link PM state, to the *Loopback* state. The Link must pass through a *Recovery* substate, before the *Port x Loopback Command* bits can be sampled and allow the LTSSM to pass through the *Recovery* state to the *Loopback* state. To cause the Port to enter the *Recovery* state, users must Set the Port's **Link Control** register *Retrain Link* bit (offset 78h[5]). At this point, users should monitor the Port's *Port x Ready as Loopback Master* bit(s), and when Set, the PRBS engine(s) can be enabled, as previously described.

If loopback cables are attached after the device powers up, then those Ports whose Lanes are floating unconnected did not detect Receivers. Therefore, those Ports are not trained up to the L0 Link PM state.

If the Port's *Port x Loopback Command* and *Port x External Loopback Enable* bit(s) for the downstream Ports to be tested are written ***before*** the cables are attached, then once cabled, there is Receiver detection, the Port(s) go through Link training, and then exit the LTSSM *Configuration* state and directly enter the *Loopback* state.

However, if the Port's *Port x Loopback Command* and *Port x External Loopback Enable* bit(s) are Set ***after*** the cables are attached, the Ports do not recognize their own Training Sets and will likely cycle back and forth between *Configuration* and *Detect*. Therefore, users must at least Set the *Port x External Loopback Enable* bit for the Ports being tested, by way of serial EEPROM, if the PEX 8649 is powered up before the cables are attached. Users can then program the Port's *Port x Loopback Command* bit(s). In addition to this, a forced retrain is also needed, to enter into the *Loopback* state through the *Recovery* state, as previously described.

17.2.3 Digital Loopback Master Mode

The only difference between Analog and Digital Loopback Master modes is that the external device is assumed to have at least an Elastic buffer in the Loopback data path. Because of this, SKIP Ordered-Sets must be included in the test data pattern, which precludes use of the PRBS engine.

Figure 17-3 illustrates a Far-End Digital Loopback Master connection and data path.

The PEX 8649 provides a User Test Pattern engine on a per-Lane basis, for Digital Far-End Loopback testing. The user pattern itself, however, is common to all Lanes where it is enabled. Details on the use of the User Test Pattern registers and controls are described later in Section 17.5.

What is important to note about the data path (not shown in Figure 17-3) is that the pattern generators and checkers in the PEX 8649 Digital Loopback Master have 8/10b encode, 10b/8b decode, and Elastic buffers included in the Tx/Rx path. The scramblers and de-scramblers are disabled. Therefore, the Digital Loopback Slave device must not scramble the returning data. The 10-bit data can be decoded to 8-bit, and encoded back to 10-bit as an option, and will not affect the UTP pattern checker in the PEX 8649, unless there is a coding error.

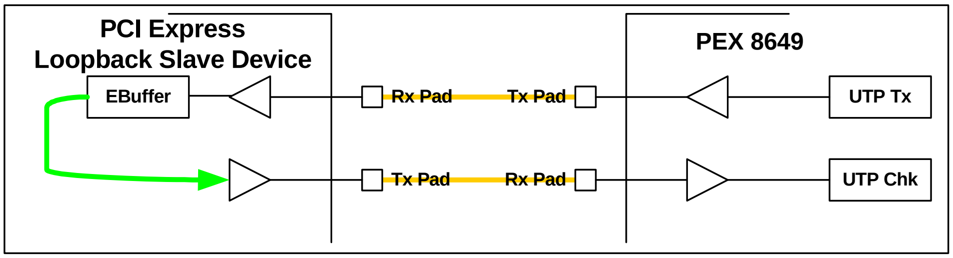
Digital Loopback Master mode is established by either programming method previously described in Section 17.2.2 for Analog Loopback Master mode. The Port’s **Physical Layer Port Command** register *Port x Loopback Command* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 230h[0, 4, 8, or 12]) can be Set with a serial EEPROM, causing Loopback to be entered directly from the LTSSM *Configuration* state. Otherwise, the Port’s *Port x Loopback Command* bit can be Set after linkup, and then the Port’s **Link Control** register *Retrain Link* bit (offset 78h[5]) can be used to move the Port to the *Loopback* state, through the LTSSM *Recovery* state.

Once Digital Loopback Master mode is established, Configuration Space register Writes are used to establish a User Test Pattern transmission, as well as error checking, which are described later in Section 17.3.

The UTP is multiplexed, unconditionally, onto the Transmit data path, upon Setting one or more of the **Physical Layer Test** register *SerDes Quad x User Test Pattern Enable* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 228h[31:28]).

Note: *It is important to verify that the LTSSM is in a Master Loopback.Active state, before writing 1 to the SerDes Quad x User Test Pattern Enable bits. Therefore, do not use the serial EEPROM to Set the SerDes Quad x User Test Pattern Enable bits. (Refer to Section 17.4 for details.)*

Figure 17-3. Digital Far-End Loopback



17.2.4 Analog Loopback Slave Mode

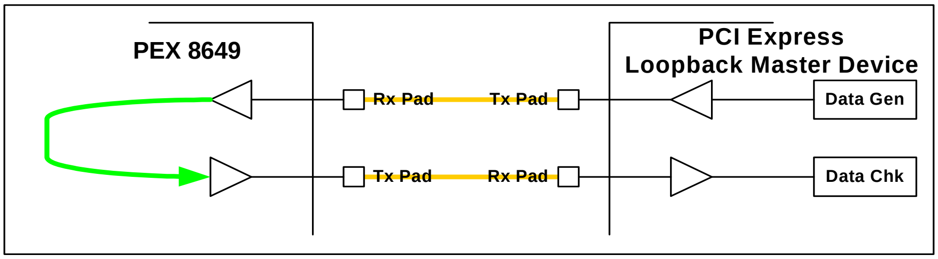
The PEX 8649 becomes an Analog Loopback Slave (as illustrated in Figure 17-4) if it receives Training Sets with the *Loopback* Training Control Bit Set while the **Physical Layer Test** register *Analog Loopback Enable* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 228h[6]) is Set. It is recommended that the *Analog Loopback Enable* bit be Set first, before bringing the PEX 8649 into an LTSSM Slave *Loopback.Active* state.

As previously described, Analog Loopback does not have only pure analog circuitry in the Slave's data path. While in this mode, the received data and recovered clock are looped back from the SerDes Parallel Receive Data interface to the Parallel Transmit Data interface. Internal to the SerDes, the serial-to-parallel and parallel-to-serial converters are included in the Loopback data path. The re-serialized data is transmitted back to the Master device, synchronous to that Master's Reference Clock.

The multiplexing control that enables Parallel data from the Receive path, directly back to the Transmit path, is held off from asserting until the Slave reaches the *Loopback.Active* state. Then, the Parallel Recovered data and clock are multiplexed back into the SerDes Parallel Transmit Data interface. That multiplexer remains effective until the PEX 8649 Loopback Slave exits the *Loopback.Active* state. There are alternate ways to transition out of the Slave *Loopback.Active* state:

- If the Loopback is operating at Gen 2 speeds (5.0 GT/s), receipt of four consecutive Electrical Idle Ordered-Sets (EIOS) causes a Loopback exit
- If the Link is operating at Gen 1 speeds (2.5 GT/s), then receipt of a single EIOS, or detection of Electrical Idle entry, causes an exit
- If the Slave device appears to be "stuck" in the *Loopback.Active* state, toggling of the Port's **Physical Layer Port Command** register *Port x Loopback Command* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 230h[0, 4, 8, or 12]), from 0 to 1 to 0, breaks the LTSSM out of Loopback Slave operation

Figure 17-4. Analog Loopback Slave Mode



Analog Loopback Slave mode is most suitable for a PRBS test pattern. However, because the PEX 8649 includes only the SerDes in the Loopback data path, and the Transmit data is clocked out at the recovered clock frequency, the Master can include SKIP Ordered-Sets in its data pattern, regardless of whether the system uses synchronous or asynchronous clocking, as long as it can tolerate the presence of SKIP Ordered-Sets in the data pattern. In this case, the Master sees its own SKIP Ordered-Sets returned to it, at the same intervals and positions in the data pattern.

If the Master device is not capable of bringing the PEX 8649 to a Slave *Loopback.Active* state (*such as*, a Bit Error Rate Tester (BERT) as the Master) through the LTSSM state transition arcs previously described, there is a way to unconditionally force the Slave into Analog Loopback Slave mode, through device Configuration Space register Writes to the appropriate bit states. The BERT Loopback Path Enable bits (**Physical Layer Test** register *SerDes Quad x Parallel Loopback Path Enable* bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 228h[27:24])) are first Set for all device Lanes associated with the Port being tested.

Next, the **Physical Layer Test** register *Analog Loopback Enable* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 228h[6]) is Set. The Lanes enabled by the BERT's *SerDes Quad x Parallel Loopback Path Enable* bits immediately go into an Analog Loopback path mode, ***regardless of the Slave's current LTSSM state***.

Concurrently Setting the *Analog Loopback Enable* and BERT's *SerDes Quad x Parallel Loopback Path Enable* bits, for all Lanes of the Port being tested, changes the Loopback data path, as described; however, that does not guarantee that the SerDes transmitters are powered on and operating at the correct speed. Other PHY Safety bits can be used to ensure that the SerDes are powered up and ready to be placed into Analog Loopback Slave mode. The **Port Control** register (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 234h) contains useful bits for controlling loopback operations:

- *Disable Port x* bits (bits [19:16])
- *Hold Port x Quiet* bits (bits [23:20])
- *Port x Test Pattern x Rate* bits (bits [27:24])

The Port's *Hold Port x Quiet* bit holds the Port in the *Detect.Quiet* state once it enters that state, and does not allow the LTSSM to advance. The Port's *Hold Port x Quiet* bits also keep the SerDes Transmitters and Receivers powered on, as long as the Port's *Disable Port x* bit is not Set. The Port's *Port x Test Pattern x Rate* bit, if Set, forces the Port's SerDes to shift their Link speed to Gen 2 (5.0 GT/s) **if** the Port's *Hold Port x Quiet* bit is also Set.

When forcing the PEX 8649 into Analog Loopback Slave mode with a BERT attached, the Port's LTSSM looks at whatever the BERT is transmitting on the attached Lanes. Because the BERT does not transmit Training Sets, the LTSSM detects Receivers, goes to the *Polling* state, times out, and then returns to the *Detect* state to try again. The LTSSM should remain in the *Detect.Quiet* state once it returns to that state. The Port's *Hold Port x Quiet* bit, therefore, should be Set, to hold the PEX 8649 in a stable LTSSM *Detect.Quiet* state, that keeps the SerDes powered on and prevents additional state transitions. If it is necessary for the BERT to test the SerDes at the Gen 2 rate, Set the Port's *Port x Test Pattern x Rate* bit before Setting the Port's *Hold Port x Quiet* bit.

To Set the necessary bits prior to BERT testing, for the Port being tested:

1. Use I^{2}C to Set the Port’s **Port Control** register *Hold Port x Quiet* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 234h[23:20]).
2. If Analog Loopback Slave mode must operate at the Gen 2 rate (5.0 GT/s), Set the Port’s **Port Control** register *Port x Test Pattern x Rate* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 234h[27:24]).
3. Set the BERT’s **Physical Layer Test** register *SerDes Quad x Parallel Loopback Path Enable* bit(s) (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 228h[27:24]).
4. Set the **Physical Layer Test** register *Analog Loopback Enable* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 228h[6]).

   The Slave device should now be in Analog Loopback Slave, properly powered, and at the correct Link speed for BERT testing.

17.2.5 Digital Loopback Slave Mode

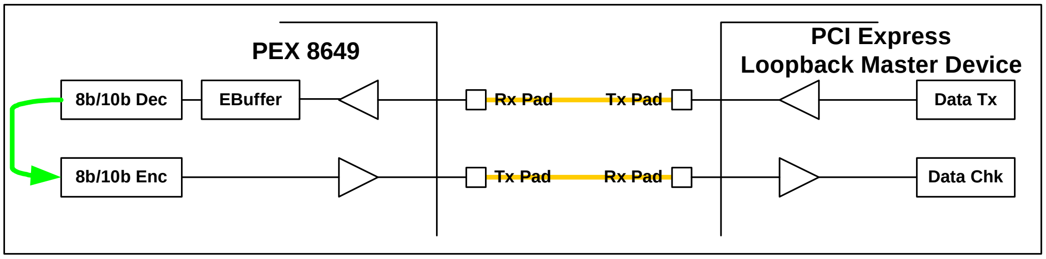
When a PEX 8649 Port is in the LTSSM Slave *Loopback.Active* state, it automatically becomes a Digital Loopback Slave, by default. The Port enters this state after it receives Training Sets with the *Loopback* Training Control Bit Set.

When a PEX 8649 Port is a Digital Loopback Slave, it includes the Elastic buffer, 8b/10b decoder, and 8b/10b encoder in the Loopback data path. The Loopback Master must provide the test data pattern and data pattern checker (*such as*, a PEX 8649 User Test Pattern). The Loopback Master must also transmit SKIP Ordered-Sets with the data pattern. Depending upon the PEX 8649 Reference Clock source's PPM offset, the PEX 8649 Digital Loopback Slave's Elastic buffers can compensate for the offset, by returning more or fewer SKIP symbols than the PEX 8649 received from the Master. Therefore, the Master's data pattern checker must make provisions for this when decoding for errors.

This mode is ***not*** suitable for a PRBS pattern as transmitted from the Master, because neither device can compensate for Reference Clock offset differences, should they exist.

Unlike Analog Loopback Slave mode (described in Section 17.2.4), there is no way to unconditionally force the Loopback path into Digital Loopback Slave mode, through the use of PHY-related register bits – the Slave must be brought into the mode by a Master-connected device, through standard LTSSM tracks.

Figure 17-5. Digital Loopback Slave Mode



17.3 User Test Pattern

The PEX 8649 provides a User Test Pattern (UTP) Transmit and Receive data checker, for Digital Far-End Loopback testing. (Refer to Figure 17-3.) After LTSSM Loopback Master mode is established, Configuration Writes are used to fill the Test Data Pattern registers. One or more **Physical Layer Test** register *SerDes Quad x User Test Pattern Enable* bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 228h[31:28]) are used to start the UTP transmission, on the Lanes assigned to each bit. The UTP logic assumes that there is asynchronous clocking between the PEX 8649 Loopback Master and the connected Slave device. Therefore, the expectation is that there is at least a clock-crossing boundary in the Slave device's Loopback data path (*such as* an Elastic buffer). SKIP Ordered-Sets are inserted into the user's test data pattern, at the nearest data pattern boundary according to the programmed SKIP interval. That interval is determined by the **SKIP Ordered-Set Interval** register *SKIP Ordered-Set Interval* field (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 234h[11:0]) value. The default interval is 1,180 symbol times.

The Test Pattern checker ignores SKIP Ordered-Sets returned by the Loopback Slave, because the quantity of SKIP symbols received can be different from the quantity transmitted. All other data is compared to the transmitted data, and errors are logged in the **SerDes Quad *x* Diagnostic Data** register (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets 238h through 244h).

The 16-byte UTP is loaded into the **Physical Layer User Test Pattern, Bytes *x* through *y*** registers (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets 210h through 21Ch). The pattern is common to all Lanes. Prior to transmission, the 8b/10b encoder converts the 16 bytes to 10-bit encoded data. Pattern bytes only go out as control symbols (k-bit set), if their corresponding **Physical Layer Command and Status** register *User Test Pattern Control/Data* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 220h[31:16]) is Set.

Caution: ***Use caution when Setting User Test Pattern Control/Data bits, because UTP logic does not check the validity of Control characters.***

The UTP Transmitter logic does not immediately transmit the UTP bytes upon being enabled – a fixed, 4-byte sync pattern (5243h) is continuously transmitted first. The sync word detection validates the physical Loopback wiring and connected device Loopback path, to qualify the UTP transmission's initiation. The sync DWord allows the Pattern Checking logic to determine the starting boundary of the received pattern byte sequence. Sync detection also enables Received Data error checking and logging. Unfortunately, there are no sync-acquired status bits in the Physical Layer registers, like there are for PRBS; therefore, it is not possible to verify that the sync pattern has been detected. However, a single UTP Error Count is logged if the sync pattern is not detected within 256 ns from the initial transmission of the sync DWord. Therefore, a single Error Count may, or may not, indicate the absence of received sync data (*for example*, a good sync could have been followed by a single bit error).

Notes: *There are no explicit Control bits for deliberately injecting UTP errors into the transmission, to test the error checking ability. However, one way of testing the ability is to write a test pattern byte to a different value after the transmission has started. That usually causes a temporary unequal boundary condition, which will log an error. While not guaranteed to inject an error, this method is useful for testing error checking ability.*

A UTP is not recommended for Master mode far-end cable testing, especially when initiated by way of serial EEPROM from a power-up sequence. If a UTP is enabled and looped back before Link training begins, the symbol framers will not have seen any COM symbols, and the true 10-bit symbol boundaries are unknown. The framer requires three COMs in a row, in the same bit position, to achieve symbol lock. Neither the sync pattern, nor the user pattern, would be detected in this case, and the test is certain to fail.

In addition to the 16-byte pattern registers, the UTP is enabled on a per-Lane basis, by Setting the **Physical Layer Test** register *SerDes Quad x User Test Pattern Enable* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 228h[31:28]), for the SerDes associated with the Port being tested.

Note: *The UTP is unconditionally multiplexed onto the Transmit data path, upon setting the SerDes Quad x User Test Pattern Enable bits. Therefore, it is necessary to verify that the LTSSM is in an LTSSM Master Loopback.Active state* ***before*** *writing those Enable bits to a value of 1.* ***Do not use a serial EEPROM to Set the SerDes Quad x User Test Pattern Enable bits.***

UTP testing results can be monitored in one of the **SerDes Quad *x* Diagnostic Data** registers (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets 238h through 244h). Each register can be used to examine the Error Count in the *UTP/PRBS Error Counter* field [23:16], and expected/actual data of the first failing byte (fields [7:0 and 15:8], respectively). The *Status* bits are on a per-Lane basis associated with a SerDes quad. **The important field in these registers is field [25:24] (*SerDes Diagnostic Data Select*).** When the Lane code for the quad is written to that field, the UTP status for that Lane appears in the *Status* fields. Bit 30 of the register (*PRBS Counter/-UTP Counter*) is a pattern type indicator, and is Cleared when UTP is enabled for a Lane.

Notes: *Use of the* ***SerDes Quad x Diagnostic Data*** *registers is explained in Section 17.5.*

The UTP and PRBS Enables are mutually exclusive, and must not be Set concurrently. *If both Enables are simultaneously Set, the resulting operation is undefined. The UTP/PRBS Error Counter field continues to count, until it saturates at 255. To clear the Counter and allow it to begin logging errors again, write all zeros (0) to that field. Alternatively, the Counter status is Cleared if the SerDes Quad x User Test Pattern Enable bit for that Lane is Cleared, and then Set again.*

17.4 Pseudo-Random Bit Sequence

A Pseudo-Random Bit Sequence (PRBS) generator and checker are useful as a diagnostic/debugging tool, and for measuring short- or long-term bit error rates in PCI Express systems. The PEX 8649 also uses a specially enabled power-up self-test that runs after reset, as a wafer sort test for use on automated test equipment. PRBS pattern generators and checkers reside within the SerDes_rclk_blk modules, because they transmit and receive 10- or 20-bit data directly to/from the SerDes quads. Locating them in the modules helps ensure tight timing and short trace length on SerDes Tx and Rx parallel data.

The PEX 8649 PRBS logic is enabled by one or more of the **Physical Layer Test** register *SerDes Quad x PRBS Enable* bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 228h[19:16]), for the SerDes associated with the Port being tested. Prior to enabling PRBS, an externally connected PCI Express device must be in an LTSSM Slave *Loopback.Active* state. Furthermore, the reference clocking between the two devices must be synchronous. (*That is*, the returning PRBS pattern must have its transmission clock source synchronous to the PEX 8649 Reference Clock.) The PEX 8649 PRBS pattern generator does not insert any SKIP Ordered-Sets, and, if the Slave device inserts SKIP Ordered-Sets into the returning pattern, they cannot be ignored by the PRBS checker (it causes an error). Alternatively, the PRBS pattern can be used to test an external cable Loopback, after the correct LTSSM Master *Loopback.Active* state is reached, as described in Section 17.2.2.

After a PEX 8649 Lane’s PRBS engine is enabled, the PRBS engine immediately begins to transmit the PRBS pattern on that Lane. No 8b/10b encoding is performed. The PRBS pattern generator produces 10- or 20-bit symbols on every Clock cycle, depending upon the current Link speed. The symbols are written directly into the SerDes Tx data Port, for immediate transmission.

The PRBS Receive Data Checking logic first synchronizes the de-serialized 10- or 20-bit Parallel Data symbols from the SerDes Rx data Port, using a reference PRBS pattern generator. After pattern synchronization is achieved, the Receive data checker begins comparing the Rx data symbols on a continuous basis, to discover any mismatch between a symbol’s expected and received values.

Note: *Error checking cannot begin until synchronization is achieved; therefore, it is important to monitor the pattern synchronization status, before checking the error status. Synchronization status is available in the* ***PRBS Control/Status*** *register PRBS Pattern Sync Status Device Lane x bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 258h[15:0]).* ***This status should always be checked.*** *If there is no synchronization, there is likely a physical connection problem. Any errors detected are logged in one or more of the* ***SerDes Quad x Diagnostic Data*** *registers (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets 238h through 244h). Use of these registers is explained in Section 17.5.*

PRBS testing results can be monitored in one of the **SerDes Quad *x* Diagnostic Data** registers (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets 238h through 244h). Each register can be used to examine the Error Count in the *UTP/PRBS Error Counter* field [23:16], and expected/actual data of the first failing byte (fields [7:0 and 15:8], respectively). The *Status* bits are on a per-Lane basis associated with a SerDes quad. **The important field in these registers is field [25:24] (*SerDes Diagnostic Data Select*).** When the Lane code for the quad is written to that field, the PRBS status for that Lane appears in the *Status* fields. Bit 30 of the register (*PRBS Counter/-UTP Counter*) is a pattern type indicator, and is Set when PRBS is enabled for a Lane.

Notes: *Use of the **SerDes Quad x Diagnostic Data** registers is explained in Section 17.5.*

The UTP and PRBS Enables are mutually exclusive, and must not be Set concurrently. *If both Enables are simultaneously Set, the resulting operation is undefined. The UTP/PRBS Error Counter field continues to count, until it saturates at 255. To Clear the Counter and allow it to begin logging errors again, write all zeros (0) to that field. Alternatively, the Counter status is Cleared if the SerDes Quad x User Test Pattern Enable bit for that Lane is Cleared, and then Set again.*

The PRBS Error Count does not necessarily represent a true Bit Error rate. The PRBS checker detects one or more mismatched bits in each examined symbol, on a symbol-per-core-clock basis. Therefore, the Error Counter advances one count for every symbol mismatch, regardless of how many bits are in error for that failing symbol.

17.5 Using the SerDes Quad *x* Diagnostic Data Registers

Each SerDes quad has its own Diagnostic Data register, per Station. The **SerDes Quad *x* Diagnostic Data** register (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets 238h through 244h) contents reflect the performance of the SerDes selected by the registers' *SerDes Diagnostic Data Select* field [25:24].

When field [25:24] is Cleared, the information in that Diagnostic Data register is for the first SerDes in each SerDes quad. When field [25:24] is programmed to 01b, the information in that Diagnostic Data register is for the second SerDes in each SerDes quad, as illustrated in Table 17-2. Following this pattern, a value of 10b indicates the third SerDes in each SerDes quad, and a value of 11b indicates the fourth SerDes in each SerDes quad.

Table 17-2. SerDes Register Contents When *SerDes Diagnostic Data Select* Field = 01b (Base mode – Ports 0, 16, and 20, except if any of these Ports is a Legacy NT Port, then the registers for that Station exist in the NT Port Virtual Interface; Virtual Switch mode – Ports 0, 16, and 20, accessible through the Management Port)

Register Offset	Register	SerDes		
		Port 0	Port 16	Port 20
238h	**SerDes Quad 0 Diagnostic Data**	1	33	17
23Ch	**SerDes Quad 1 Diagnostic Data**	5	37	21
240h	**SerDes Quad 2 Diagnostic Data**	9	41	25
244h	**SerDes Quad 3 Diagnostic Data**	13	45	29

17.6 Pseudo-Random and Bit-Pattern Generation

Each SerDes quad has an associated PRBS generator and checker. The PRBS generator is based upon a 7-bit **Linear Feedback Shift** register (**LFSR**), which can generate up to (2^7 - 1) unique patterns. The PRBS logic is assigned to a SerDes in the quad, by manipulating the appropriate **SerDes Quad *x* Diagnostic Data** register *SerDes Diagnostic Data Select* bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets 238h through 244h, field [25:24]). The PRBS bit stream is used for Analog Far-End Loopback testing.

The PEX 8649 also provides a method of creating a repeating programmable bit pattern. Each of the four 32-bit **Physical Layer User Test Pattern, Bytes *x* through *y*** registers (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets 210h through 21Ch) are loaded with a 32-bit data pattern. After a Port is established as a Loopback Master, Set the appropriate **Physical Layer Test** register *SerDes Quad x User Test Pattern Enable* bit(s) (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 228h[31:28]), for the SerDes associated with that Port. The PEX 8649 proceeds to transmit the data pattern on all Lanes, starting with Byte 0 of the **Physical Layer User Test Pattern, Bytes 0 through 3** register and continuing, in sequence, through Byte 3 of the **Physical Layer User Test Pattern, Bytes 12 through 15** register. SKIP Ordered-Sets are inserted at the proper intervals, which makes this method appropriate for Digital Far-End Loopback testing. The received pattern is compared to the transmitted pattern. Any errors are logged and can be retrieved, by reading the appropriate **SerDes Quad *x* Diagnostic Data** register RO bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets 238h through 244h, bits [30, 23:0]).

To produce a pseudo-clock bitstream in Analog Loopback mode, Set the registers as follows:

1. In the Slave device, enable Analog Loopback by Setting the **Physical Layer Test** register *Analog Loopback Enable* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 228h[6]).

2. In the PEX 8649 Loopback Master device, Set the Port's **Physical Layer Port Command** register *Port x Loopback Command* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 230h[0, 4, 8, or 12]).

3. Check whether loopback is successful, by reading the Port's **Physical Layer Port Command** register *Port x Ready as Loopback Master* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 230h[3, 7, 11, or 15]) in the same Nibble that was Set in step 2. The Nibble value is 9h if Loopback was successful.

4. Set the **Physical Layer Test** register *SerDes Quad x PRBS Enable* bit (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 228h[19:16]) for the SerDes used by the Port selected in step 2.

5. Check the **PRBS Control/Status** register *PRBS Pattern Sync Status Device Lane x* bits (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset 258h[15:0]). A bit returning a value of 1 indicates that the looped-back PRBS pattern is detected at the Master's Receiver.

6. Exit Loopback mode, by Clearing the following bits:
   a. *SerDes Quad x PRBS Enable* bit, for the SerDes (selected in step 4) used by the Port selected in step 2.
   b. *Port x Loopback Command* bit, for the Port selected in step 2.

   Clearing these bits causes both sides of the Link to exit their LTSSM *Loopback* states, and return to the L0 Link PM state.

17.7 PHY Testability Features

The PEX 8649 includes several Configuration bits to ease PHY testability. Features include:

- Full support of the standard and modified compliance patterns
- Register controllability of the common block and Lane-specific inputs of the SerDes

Table 17-3 describes the Configuration bits.

Table 17-3. Configuration Bits to Ease PHY Testability

Register Bit(s)[a]	Description
SerDes x Mask Electrical Idle Detect **Physical Layer Electrical Idle Detect Mask** register (offset 204h[15:0])	When any one of these bits is Set, the Electrical Idle condition flag of the corresponding Lane does not assert, regardless of the actual presence of Electrical Idle.
SerDes x Mask Receiver Not Detected **Physical Layer Receiver Not Detected Mask** register (offset 204h[31:16])	When any one of these bits is Set, the PHY functions as if a Receiver was detected on the corresponding Lane, regardless of the actual presence of a Receiver.
Test Pattern x **Physical Layer User Test Pattern, Bytes *x* through *y*** registers (offsets 210h through 21Ch)	A 16-byte test pattern can be written to these four registers. When UTP transmission is enabled, Byte 0 of register offset 210h is transmitted first and Byte 3 (Byte 15 of the UTP) of register offset 21Ch is transmitted last. (Refer to Section 17.2.3 for further details.) Every byte of the UTP can be a Control or Data character. Illegal Control characters can be specified.
Port x Scrambler Disable Command **Physical Layer Port Command** register (offset 230h[1, 5, 9, or 13])	Unconditionally disables the data scramblers on the Lanes of the corresponding Port, and causes the Training Control Bit to be Set in transmitted Training Sets. There is one bit for each Port in the associated Station.
Disable Port x **Port Control** register (offset 234h[19:16])	LTSSM remains in the *Detect.Quiet* state on the corresponding PEX 8649 Port if it is currently in, or returns to, that state. When Set, unconditionally disables the corresponding Port. This is different from the LTSSM *Disabled* state, in that the Port does not attempt to enter this state. If the Port is idle, it ceases attempting to detect a Receiver. If the Port is up, it immediately returns to the *Detect.Quiet* state and remains there. No Electrical Idle Ordered-Set (EIOS) is sent, which could force any connected device to the *Recovery* state, and then to the LTSSM *Detect* state. The Port remains disabled until its *Disable Port x* bit is Cleared. While the Port is disabled, Receiver termination is disabled and the SerDes that belong to the disabled Port are placed into the L1 Link PM state.
Hold Port x Quiet **Port Control** register (offset 234h[23:20])	When Set, the Link Training and Status State Machine (LTSSM) remains in the *Detect.Quiet* state if it is currently in, or returns to, that state. Once in the *Detect.Quiet* state, Receiver termination is enabled and the Transmitters are placed into the L0 Link PM state. This Port can now transmit test patterns (PRBS or UTP), with or without an attached device and without being in the *Loopback.Active* state.
Port x Test Pattern x Rate **Port Control** register (offset 234h[27:24])	The corresponding Port transmits the selected test pattern (PRBS or UTP) at 5.0 GT/s, if the Port's *Hold Port x Quiet* bit is also Set (manual rate selection is enabled only when the *Hold Port x Quiet* bit is Set).

Table 17-3. Configuration Bits to Ease PHY Testability *(Cont.)*

Register Bit(s)[a]	Description
Port x Bypass UTP Alignment Pattern **Port Control** register (offset 234h[31:28])	When Cleared, the UTP Transmitter continuously transmits the alignment pattern until any UTP checker in the corresponding SerDes quad indicates that it has received the alignment pattern. The UTP Transmitter will then transmit one sync pattern, followed by the programmed UTP. When Set, the programmed UTP will be preceded by one alignment pattern and one sync pattern.
Port x Receiver Error Counter **Port Receiver Error Counter** register (offset 248h[31:0])	Contains four 8-bit fields that, when read, return the number of Receiver errors detected by the corresponding Port. The Error Counter saturates at 255. The Counter is Cleared with any Write to the corresponding byte in this register; otherwise, this register is RO.
Port x Internal PIPE Interface PhyStatus Signal **Physical Layer Additional Status/Control** register (offset 254h[7:4])	Internal PHY Interface for the PCI Express standard (PIPE), for the Physical Layer Status (PhyStatus) signal. Returns the state of the PIPE interface PhyStatus signals, for the corresponding Port. If any of the PhyStatus signals that are mapped to a particular Port are asserted, then the corresponding Port's bit is Set. This is useful for manually changing the Link speed when the *Hold Port x Quiet* bit is Set. When software is used to change the Link speed, it should poll PhyStatus for assertion, then de-assertion. After PhyStatus has de-asserted, the speed change is complete and test pattern transmission can begin.
x1 Only for Station x **x1 Port Configuration** register (offset 304h[23:16, 3:0])	Forces the corresponding Port to linkup with a x1 negotiated Link width, regardless of the quantity of Lanes connected to the Port.
x2 Only for Station x **x2 Port Configuration** register (offset 308h[23:16])	Forces the corresponding Port to linkup with a x2 negotiated Link width, regardless of the quantity of Lanes connected to the Port. Fields exist for each Station, except Station 0.

a. *All registers listed in this table are located, as follows:*

***Register offsets 204h through 254h** – Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port.*

***Register offsets 304h and 308h** – Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port.*

17.8 JTAG Interface

The PEX 8649 provides a Joint Test Action Group (JTAG) Boundary Scan interface, which is used to debug board connectivity for each ball.

17.8.1 *IEEE 1149.1* and *IEEE 1149.6* Test Access Port

The *IEEE Standard 1149.1* Test Access Port (TAP), commonly called the *JTAG Debug Port*, is an architectural standard described in the *IEEE Standard 1149.1-1990*. The *IEEE Standard 1149.6-2003* defines extensions to *1149.1* to support PCI Express SerDes testing. These standards describe methods for accessing internal device facilities, using a four- or five-signal interface.

The JTAG Debug Port, originally designed to support scan-based board testing, is enhanced to support the attachment of debug tools. The enhancements, which comply with the *IEEE Standard 1149.1-1994 Specifications for Vendor-Specific Extensions*, are compatible with standard JTAG hardware for boundary-scan system testing.

- **JTAG Signals** – JTAG Debug Port implements the four required JTAG signals – JTAG_TCK, JTAG_TDI, JTAG_TDO, JTAG_TMS – and optional JTAG_TRST# signal
- **Clock Requirements** – JTAG_TCK signal frequency ranges from 0 to 15 MHz
- **JTAG Reset Requirements** – Refer to Section 17.8.4

17.8.2 JTAG Instructions

The JTAG Debug Port provides the *IEEE Standard 1149.1-1990* BYPASS, EXTEST, SAMPLE, PRELOAD, CLAMP, and IDCODE instructions. *IEEE Standard 1149.6-2003* EXTEST_PULSE and EXTEST_TRAIN instructions are also supported. Table 17-4 lists the JTAG instructions, along with their input codes.

The PEX 8649 returns the JTAG IDCODE values listed in Table 17-5.

Table 17-4. JTAG Instructions

Instruction	Input Code	Comments
BYPASS	3FFF_FFFFh	*IEEE Standard 1149.1-1990*
EXTEST	3FFF_FFE8h	
SAMPLE	3FFF_FFF8h	
PRELOAD	3FFF_FFF8h	
EXTEST_PULSE	3FFB_FFE8h	*IEEE Standard 1149.6-2003*
EXTEST_TRAIN	3FE9_FFE8h	
CLAMP	3FFF_FFEFh	*IEEE Standard 1149.1-1990*
IDCODE	3FFF_FFFEh	

Table 17-5. JTAG IDCODE Values

Units	Version	Part Number	PLX Manufacturer Identity	Least Significant Bit
Bits	0000b	1000_0110_0100_1001b	001_1100_1101b	1
Hex	0h	8649h	1CDh	1h
Decimal	0	34377	461	1

17.8.3 JTAG Boundary Scan

Boundary Scan Description Language (BSDL), IEEE Standard 1149.1-1994, is a supplement to the *IEEE Standard 1149.1-1990* and *IEEE Standard 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*. BSDL, a subset of the *IEEE 1076-1993 Standard VHSIC Hardware Description Language (VHDL)*, allows a rigorous description of testability features in components which comply with the standard. This standard is used by automated test pattern generation tools for package interconnect tests and Electronic Design Automation (EDA) tools for synthesized test logic and verification. BSDL supports robust extensions that can be used for internal test generation and to write software for hardware debug and diagnostics.

The primary components of BSDL include the logical Port description, physical ball map, instruction set, and **Boundary** register description.

The logical Port description assigns symbolic names to the device’s signal balls. Each ball includes a logical type of *in*, *out*, *in out*, *buffer*, or *linkage* that defines the logical direction of signal flow.

The physical ball map correlates the device’s logical Ports to the physical balls of a specific package. A BSDL description can include several physical ball maps, and maps are provided with a unique name.

Instruction set statements describe the bit patterns that must be shifted into the **Instruction** register to place the device in the various test modes defined by the standard. Instruction set statements also support descriptions of instructions that are unique to the PEX 8649.

The **Boundary** register description lists each cell or shift stage of the **Boundary** register. Each cell has a unique number, the cell numbered 0 is the closest to the Test Data Out (JTAG_TDO) ball and the cell with the highest number is closest to the Test Data In (JTAG_TDI) ball. Each cell includes additional information, including:

- Cell type
- Logical Port associated with the cell
- Logical function of the cell
- Safe value
- Control cell number
- Disable value
- Result value

17.8.4 JTAG Reset Input – JTAG_TRST#

The JTAG_TRST# input is the asynchronous JTAG logic reset. When JTAG_TRST# is Set Low, it causes the PEX 8649’s JTAG TAP Controller to initialize. In addition, when the JTAG TAP Controller is initialized, it selects the PEX 8649 standard logic path (core-to-I/O). It is recommended to take the following into consideration when implementing the asynchronous JTAG logic reset on a board:

- If JTAG functionality is required, consider one of the following:
  – JTAG_TRST# Input signal to use a Low-to-High transition once during PEX 8649 boot-up, along with the system PEX_PERST# and/or VS*x*_PERST# signal
  – Hold the JTAG_TMS ball High while clocking the JTAG_TCK ball five times
- If JTAG functionality is not required, the JTAG_TRST# signal must be directly connected to VSS, to hold the JTAG TAP Controller inactive
- If the PEX 8649’s JTAG TAP Controller is not intended to be used by the design, it is recommended that a 1.5KΩ pull-down resistor be connected to the JTAG_TRST# ball, to hold the JTAG TAP Controller in the *Test-Logic-Reset* state, which enables standard logic operation

17.9 Port Good Status LEDs

The PEX 8649 provides Port Good outputs, PEX_PORT_GOOD*x*#, that can directly drive external common anode LED modules, to provide visual indication that the PHY for each Port's Link is trained to at least x1 width. These signals can:

- Default to the PORT_GOOD output function (when the STRAP_TESTMODE[3:0] inputs are asserted to 1011b or 1101b), –or–
- Be programmed as a general-purpose I/O, to assume the PORT_GOOD function

Software can determine:

- Which Lanes have completed PHY linkup, by performing a Memory Read of the **Station *x* Lane Status** register *Lane x Up Status* bits (Base mode – Port 0, except if Port 0 is a Legacy NT Port, then this register exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, accessible through the Management Port, offsets 330h and 338h).
- Whether the Link for each Port has trained, by reading either the Port's **Link Status** register *Data Link Layer Link Active* bit (offset 78h[29]), or **VC0 Resource Status** register *VC0 Negotiation Pending* bit (offset 160h[17]). If the Port's *Data Link Layer Link Active* bit is Set, or *VC0 Negotiation Pending* bit is Cleared, the Link has completed Flow Control (FC) initialization.

  The **Link Status** register can be read by either a PCI Express Configuration Request or Memory Read. The **VC0 Resource Status** register can be read by either a PCI Express Enhanced Configuration access or Memory Read.
- The negotiated Link width of each Port, by reading the Port's **Link Status** register *Negotiated Link Width* field (offset 78h[25:20]). This register can be read by either a Configuration Request or Memory Read.

Table 17-6 describes the LED On/Off patterns when connected to the PEX_PORT_GOOD*x*# signals.

Table 17-6. PEX_PORT_GOOD*x*# LED On/Off Patterns, by State

State	LED Pattern
Link is down	Off
Link is up, 5.0 GT/s, all Lanes are up	On
Link is up, 5.0 GT/s, reduced Lanes are up	Blinking, 0.5 seconds On, 0.5 seconds Off
Link is up, 2.5 GT/s, all Lanes are up	Blinking, 1.5 seconds On, 0.5 seconds Off
Link is up, 2.5 GT/s, reduced Lanes are up	Blinking, 0.5 seconds On, 1.5 seconds Off

Chapter 18 Electrical Specifications

18.1 Introduction

This chapter provides the PEX 8649 electrical specifications.

18.2 Power-Up/Power-Down Sequence

The PEX 8649 does not have power sequencing requirements. The power rails can be powered up and powered down, in any sequence.

18.3 Absolute Maximum Ratings

Warning: ***Maximum limits indicate the temperatures and voltages above which permanent damage can occur. Proper operation at these conditions is not guaranteed, and continuous operation of the PEX 8649 at these limits is not recommended.***

Table 18-1. Absolute Maximum Rating (All Voltages Referenced to VSS System Ground)

Item	Symbol	Absolute Maximum Rating	Units
I/O Interface Supply Voltage	VDD25	-0.5 to +3.6	V
Phase-Locked Loop (PLL) Supply Voltage	VDD25A	-0.5 to +3.6	V
Core (Logic) Supply Voltage	VDD10	-0.3 to +1.5	V
SerDes Analog Supply Voltage	VDD10A	-0.3 to +1.5	V
Input Voltage (2.5V Interface)	V_I	-0.3 to +3.6	V
Operating Ambient Temperature (Commercial)	T_A	0 to +70	°C
Operating Ambient Temperature (Extended)	T_A	-5 to +85	°C
Storage Temperature	T_{STG}	-65 to +150	°C

18.4 Power Characteristics

Table 18-2. Operating Condition Power Supply Rails

Symbol	Parameter	Min	Typ	Max	Units
VDD10	Digital Core Supply {1.0V ±5%}	0.95	1.0	1.05	V
VDD10A	Analog SerDes Supply {1.0V ±5%}	0.95	1.0	1.05	V
VDD25	I/O Supply {2.5V ±10%}	2.25	2.50	2.75	V
VDD25A	Phase-Locked Loop (PLL) Supply {2.5V ±10%}	2.25	2.50	2.75	V

18.5 Power Consumption Estimates

Table 18-3 lists the PEX 8649 power consumption estimates.

Table 18-3. Power Consumption Estimates

Lanes	Ports	Digital (VDD10)		SerDes Analog (VDD10A)		PLL and I/O (VDD25A/VDD25)		Total	
		Typ	Max	Typ	Max	Typ	Max	Typ[a]	Max[b c]
		(Watts)							
48	12	5.25	9.61	1.31	3.54	0.18	0.25	6.74	13.39
		(Amps)							
		5.25	9.15	1.31	3.37	0.07	0.09	6.63	12.61

a. *Typical power based upon 35% traffic, idle Lanes in active L0s Power Management (PM) state, typical power rails (1.0V/2.50V).*

b. *Maximum power based upon 85% traffic, idle Lanes in active L0s Link PM state, maximum power rails (1.05V/2.75V).*

c. *Maximum power is at 110°C Junction temperature and Fast/Fast (FF) process corner silicon.*

18.6 I/O Interface Signal Groupings

Table 18-4. Signal Group PCI Express Analog Interface

Signal Group	Signal Type	Signals	Notes
(a)	PCI Express Output (Transmit)	PEX_PETn*x*, PEX_PETp*x*	Refer to Table 18-6 and Table 18-7
(b)	PCI Express Input (Receive)	PEX_PERn*x*, PEX_PERp*x*	Refer to Table 18-6 and Table 18-8
(c)	PCI Express Differential Clock Input	PEX_REFCLKn, PEX_REFCLKp	Refer to Table 18-6 and Table 18-9
(d)	SerDes External Resistor	REXT_A[11:8, 1:0], REXT_B[11:8, 1:0]	1.43KΩ ±1%, and refer to Table 18-6

Table 18-5. Signal Group Digital Interface

Signal Group	Signal Type	Signals	Note
(e)	Digital Input[a]	STRAP_RESERVED16	Refer to Table 18-6
(f)	Digital Input with Internal Pull-up Resistor	PEX_PERST#, STRAP_FAST_BRINGUP#, STRAP_G1_COMPATIBLE#, STRAP_I2C_CFG_EN#, STRAP_NT_P2P_EN#, STRAP_PLL_BYPASS#, STRAP_PROBE_MODE#, STRAP_RESERVED17#, STRAP_SERDES_MODE_EN#, STRAP_SMBUS_EN#	
(g)	Digital Input with Internal Pull-down Resistor	JTAG_TCK, JTAG_TDI, JTAG_TMS, JTAG_TRST#, STRAP_DEBUG_SEL[1:0], STRAP_NT_UPSTRM_PORTSEL[4, 2:1], STRAP_STN0_PORTCFG0, STRAP_STN4_PORTCFG[1:0], STRAP_STN5_PORTCFG[1:0], STRAP_TESTMODE[3:0], STRAP_UPSTRM_PORTSEL[3:0]	
(h)	Digital Tri-State Output (8 mA)	EE_DI, FATAL_ERR#, JTAG_TDO, PEX_NT_RESET#, VS*x*_FATAL_ERR#	
(i)	Bidirectional with Internal Pull-up Resistor (8 mA Drive)	EE_CS#, EE_DO, EE_SK, GPIO[31:24], HP_ATNLED_*x*#, HP_BUTTON_*x*#, HP_CLKEN_*x*#, HP_MRL_*x*#, HP_PERST_*x*#, HP_PRSNT_*x*#, HP_PWRFLT_*x*#, HP_PWRLED_*x*#, I2C_ADDR[2:0], PEX_PORT_GOOD*x*#, SHPC_INT#, SPARE2, STRAP_NT_ENABLE#, VS*x*_PERST#	
(j)	Bidirectional with Internal Pull-down Resistor (8 mA Drive)	HP_PWREN_*x*, HP_PWR_GOOD_*x*, STRAP_NT_UPSTRM_PORTSEL0, STRAP_STN0_PORTCFG1, STRAP_VS_MODE[1:0]	
(k)	Bidirectional (Open Drain) Schmitt Trigger Input	I2C_SCL0, I2C_SCL1, I2C_SDA0, I2C_SDA1, PEX_INTA#, VS*x*_PEX_INTA#	

[a] *Signals of this type must be tied High to VDD25 or Low to VSS (GND). This particular signal, however, must be tied directly to VSS (GND).*

Table 18-6. Analog and Digital Interfaces (All Signal Groups) – DC Electrical Characteristics

Symbol	Signal Group	Parameter	Min	Typ	Max	Unit	Conditions
I_{OL}	(h) (i) (k)	Output Low Current	13	22	32	mA	V_{OLmax} = 0.7V
I_{OH}	(h) (i)	Output High Current	8	16	27	mA	V_{OHmin} = 1.7V
V_{IL}	(e) (f) (g) (i) (k)	Input Low Voltage	-0.3		0.7	V	
V_{IH}	(e) (f) (g) (i) (k)	Input High Voltage	1.7		2.8	V	Refer to Note 1.
V_T	(e) (g) (i)	Threshold Point	0.97	1.05	1.14	V	
C_{PIN}	(a) (b) (c) (d) (e) (f) (g) (h) (i) (j) (k)	Ball Capacitance			5	pF	
$I_{LEAKAGE}$	(h)	Tri-State Leakage			±10	µA	
	(e) (f)	Input Leakage			±10	µA	
	(f) (i)	Pull-Up Leakage	-22.6		-47.5	µA	
	(g) (j)	Pull-Down Leakage	22.6		47.5	µA	
R_{PU}	(f) (i)	Pull-Up Impedance	74K	111K	178K	Ω	
R_{PD}	(g) (j)	Pull-Down Impedance	62K	99K	179K	Ω	
V_T	(k)	Schmitt Trigger Rising Threshold	1.2	1.3	1.4	V	
		Schmitt Trigger Falling Threshold	0.84	0.93	1.01	V	
V_{HYS}	(k)	Input Hysteresis	360	370	390	mV	

Note:

1. *The specified maximum V_{IH} is for recommended operating conditions. Because these I/O buffers are 3.3V tolerant, a maximum V_{IH} of 3.6V can safely be applied to these signal balls.*

Table 18-7. 2.5 and 5.0 GT/s PCI Express Transmitter (Signal Group a) – AC and DC Characteristics

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	ps	The specified UI is equivalent to a tolerance of ±300 ppm. UI does not account for variations caused by Spread-Spectrum Clock (SSC). Refer to Note 1.
$V_{\text{TX-DIFF-PP}}$	Differential Peak-to-Peak Output Voltage	0.8 (min) 1.2 (max)	0.8 (min) 1.2 (max)	V	Measured with compliance test load. $V_{\text{TX-DIFF-PP}} = 2\ x\ \lvert V_{\text{TX-D+}} - V_{\text{TX-D-}} \rvert$
$V_{\text{TX-DIFF-PP-LOW}}$	Low Power Differential Peak-to-Peak Output Voltage	0.4 (min) 1.2 (max)	0.4 (min) 1.2 (max)	V	Measured with compliance test load. $V_{\text{TX-DIFF-PP-LOW}} = 2\ x\ \lvert V_{\text{TX-D+}} - V_{\text{TX-D-}} \rvert$ Must be implemented with no de-emphasis.
$V_{\text{TX-DE-RATIO-3.5dB}}$	Tx De-Emphasis Level Ratio	3.0 (min) 4.0 (max)	3.0 (min) 4.0 (max)	dB	Ratio of the $V_{\text{TX-DIFF-PP}}$ of the 2nd and following bits after a transition, divided by the $V_{\text{TX-DIFF-PP}}$ of the 1st bit after a transition. Refer to Note 2.
$V_{\text{TX-DE-RATIO-6dB}}$	Tx De-Emphasis Level Ratio	N/A	5.5 (min) 6.5 (max)	dB	Ratio of the $V_{\text{TX-DIFF-PP}}$ of the 2nd and following bits after a transition, divided by the $V_{\text{TX-DIFF-PP}}$ of the 1st bit after a transition. Refer to Note 2.
$T_{\text{MIN-PULSE}}$	Instantaneous Pulse Width (including all jitter sources)	Not specified	0.9 (min)	UI	Measured relative to rising/falling pulse. Refer to Note 3.
$T_{\text{TX-EYE}}$	Minimum Tx Eye Width	0.75 (min)	0.75 (min)	UI	Does not include SSC nor REFCLK jitter. Includes Rj at 10^{-12}. Refer to Notes 3 and 4.
$T_{\text{TX-EYE-MEDIAN-to-MAX-JITTER}}$	Maximum Time between the Jitter Median and Maximum Deviation from the Median	0.125 (max)	Not specified	UI	Measured differentially at zero crossing points, after applying the 2.5 GT/s Clock Recovery function. Refer to Note 3.
$T_{\text{TX-HF-DJ-DD}}$	Tx Deterministic Jitter > 1.5 MHz	Not specified	0.15 (max)	UI	Deterministic jitter only. Refer to Note 3.
$T_{\text{TX-LF-RMS}}$	Tx RMS Jitter < 1.5 MHz	Not specified	3.0	ps RMS	Total energy measured over a 10-kHz to 1.5-MHz range.
$T_{\text{TX-RISE-FALL}}$	Tx Rise and Fall Time	0.125 (min)	0.15 (min)	UI	Measured differentially from 20 to 80% of swing. Refer to Note 3.
$T_{\text{RF-MISMATCH}}$	Tx Rise/Fall Mismatch	Not specified	0.1 (max)	UI	Measured from 20 to 80% differentially. Refer to Note 3.
$BW_{\text{TX-PLL}}$	Maximum Tx PLL Bandwidth	22 (max)	16 (max)	MHz	Second Order PLL Jitter Transfer Bounding function. Refer to Note 5.

Table 18-7. 2.5 and 5.0 GT/s PCI Express Transmitter (Signal Group a) – AC and DC Characteristics *(Cont.)*

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$BW_{TX-PLL-LO-3DB}$	Minimum Tx PLL Bandwidth for 3-dB Peaking	1.5 (min)	8 (min)	MHz	Second Order PLL Jitter Transfer Bounding function. Refer to Notes 5 and 7.
$BW_{TX-PLL-LO-1DB}$	Minimum Tx PLL Bandwidth for 1-dB Peaking	Not specified	5 (min)	MHz	
$PKG_{TX-PLL1}$	TX PLL Peaking with 8-MHz Minimum Bandwidth	Not specified	3.0 (max)	dB	
$PKG_{TX-PLL2}$	TX PLL peaking with 5-MHz Minimum Bandwidth	Not specified	1.0 (max)	dB	Refer to Note 7.
$RL_{TX-DIFF}$	TX Differential Return Loss (Package + Silicon)	10 (min)	10 (min) for 0.05 to 1.25 GHz 8 (min) for 1.25 to 2.5 GHz	dB	
RL_{TX-CM}	TX Common Mode Return Loss (Package + Silicon)	6 (min)	6 (min)	dB	S_{11} parameter. 2.5 GT/s – Measured over 0.05- to 1.25-GHz range. 5.0 GT/s – Measured over 0.05- to 2.5-GHz range.
$Z_{TX-DIFF-DC}$	DC Differential Tx Impedance	80 (min) 120 (max)	120 (max)	Ω	Tx DC Differential mode low impedance. Parameter is captured for 5.0 GHz by $RL_{TX-DIFF}$.
$V_{TX-CM-AC-PP}$	Tx AC Common Mode Voltage (5.0 GT/s)	Not specified	100 (max)	mVPP	Refer to Note 6.
$V_{TX-CM-AC-P}$	Tx AC Common Mode Voltage (2.5 GT/s)	20 (max)	Not specified	mVPP	Refer to Note 6.
$I_{TX-SHORT}$	Tx Short Circuit Current Limit	90 (max)	90 (max)	mA	Total current the Transmitter can provide when shorted to its Ground.
$V_{TX-DC-CM}$	Tx DC Common Mode Voltage	0 (min) 3.6 (max)	0 (min) 3.6 (max)	V	Allowed DC common mode voltage, under any conditions.
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute Delta of DC Common Mode Voltage during L0 Link PM state and Electrical Idle	0 (min) 100 (max)	0 (min) 100 (max)	mV	$\lvert V_{TX-CM-DC}$ [during L0] - $V_{TX-CM-Idle-DC}$ [during Electrical Idle]$\rvert \leq 100$ mV $V_{TX-CM-DC} = DC_{(avg)}$ of $\lvert V_{TX-D+} + V_{TX-D-}\rvert / 2$ [L0] $V_{TX-CM-Idle-DC} = DC_{(avg)}$ of $\lvert V_{TX-D+} + V_{TX-D-}\rvert / 2$ [Electrical Idle]

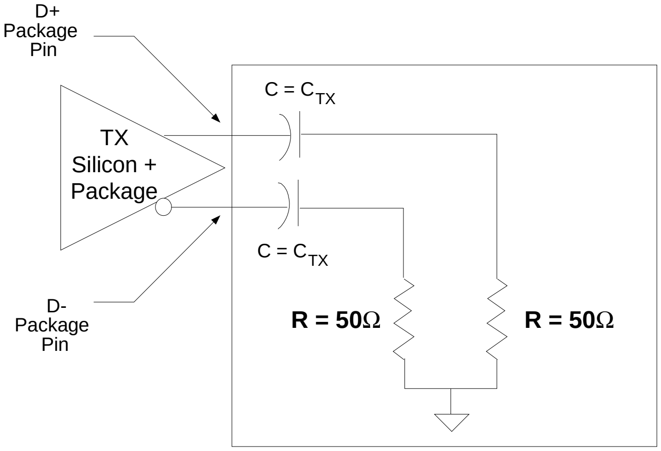
Table 18-7. 2.5 and 5.0 GT/s PCI Express Transmitter (Signal Group a) – AC and DC Characteristics *(Cont.)*

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$V_{\text{TX-CM-DC-LINE-DELTA}}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0 (min) 25 (max)	0 (min) 25 (max)	mV	$\lvert V_{\text{TX-CM-DC-D+}} - V_{\text{TX-CM-DC-D-}} \rvert \le 25$ mV $V_{\text{TX-CM-DC-D+}} = DC_{(avg)}$ of $\lvert V_{\text{TX-D+}} \rvert$ $V_{\text{TX-CM-DC-D-}} = DC_{(avg)}$ of $\lvert V_{\text{TX-D-}} \rvert$
$V_{\text{TX-IDLE-DIFF-AC-p}}$	Electrical Idle Differential Peak Output Voltage	0 (min) 20 (max)	0 (min) 20 (max)	mV	$V_{\text{TX-IDLE-DIFFp}} = \lvert V_{\text{TX-Idle-D+}} - V_{\text{TX-Idle-D-}} \rvert \le 20$ mV Voltage must be high-pass filtered, to remove any DC component.
$V_{\text{TX-IDLE-DIFF-DC}}$	DC Electrical Idle Differential Peak Output Voltage	Not specified	0 (min) 5 (max)	mV	$V_{\text{TX-IDLE-DIFF-DC}} = \lvert V_{\text{TX-Idle-D+}} - V_{\text{TX-Idle-D-}} \rvert \le 5$ mV Voltage must be high-pass filtered, to remove any AC component.
$V_{\text{TX-RCV-DETECT}}$	Amount of Voltage Change Allowed during Receiver Detection	600 (max)	600 (max)	mV	Total amount of voltage change that a Transmitter can apply, to sense whether a low-impedance Receiver is present.
$T_{\text{TX-IDLE-MIN}}$	Minimum Time Spent in Electrical Idle	20 (min)	20 (min)	ns	Minimum time a Transmitter must be in Electrical Idle. Used by the Receiver to start looking for an Electrical Idle Exit after successfully receiving an Electrical Idle Ordered-Set (EIOS).
$T_{\text{TX-IDLE-SET-TO-IDLE}}$	Maximum Time to Transition to a Valid Electrical Idle after Sending an Electrical Idle Ordered-Set	8 (max)	8 (max)	ns	After sending the required EIOS, the Transmitter must meet all Electrical Idle specifications within this time. This is measured from the end of the last UI of the last EIOS to the Tx in Electrical Idle.
$T_{\text{TX-IDLE-TO-DIFF-DATA}}$	Maximum Time to Transition to Valid Differential Signaling after Leaving Electrical Idle	8 (max)	8 (max)	ns	Maximum time to transition to valid differential signaling, after leaving Electrical Idle. This is considered a de-bounce time to the Tx.
$T_{\text{CROSSLINK}}$	Cross-Link Random Timeout	1.0 (max)	1.0 (max)	ms	Random timeout that helps resolve potential conflicts in the cross-link configuration.
$L_{\text{TX-SKEW}}$	Lane-to-Lane Output Skew	500 ps + 2 UI (max)	500 ps + 4 UI (max)	ps	Static skew between any two Lanes within a single Transmitter.
C_{TX}	AC-Coupling Capacitor	75 (min) 200 (max)	75 (min) 200 (max)	nF	All Transmitters shall be AC-coupled. The AC coupling is required either within the media, or within the transmitting component itself.

Notes:

1. *SSC permits a +0, -5,000 ppm modulation of the clock frequency, at a modulation rate not to exceed 33 kHz.*
2. *Specified at the measurement point into a timing and voltage compliance test load, as illustrated in Figure 18-1.*

Figure 18-1. Compliance Test/Measurement Load



3. *Measurements at 5.0 GT/s require an oscilloscope with a bandwidth of ≥12.5 GHz, or equivalent, while measurements made at 2.5 GT/s require a scope with at least 6.2 GHz bandwidth. Measurements at 5.0 GT/s must de-convolve effects of the compliance test board, to yield an effective measurement at the Tx balls. 2.5 GT/s can be measured within 200 mils of the Tx device's balls; however, de-convolution is recommended. At least 10^6 UI of data must be acquired.*
4. *Transmitter jitter is measured by driving the Tx under test with a low jitter "ideal" clock and connecting the device under test (DUT) to a reference load.*
5. *The Tx PLL bandwidth must lie between the minimum and maximum ranges listed in Table 18-7. PLL peaking must lie below the values listed in Table 18-7.*

   The PLL bandwidth extends from zero (0) up to the value(s) specified in Table 18-7.
6. *Measurement is made over at least 10^6 UI.*
7. *A single combination of PLL bandwidth and peaking is specified for 2.5 GT/s implementations. For 5.0 GT/s, two 20 combinations of PLL bandwidth and peaking are specified to permit designers to make a tradeoff between the two parameters. If the PLL's minimum bandwidth is ≥8 MHz, then up to 3.0 dB of peaking is permitted. If the PLL's minimum bandwidth is relaxed to ≥5.0 MHz, then a tighter peaking value of 1.0 dB must be met. In both cases, the maximum PLL bandwidth is 16 MHz.*

Table 18-8. 2.5 and 5.0 GT/s PCI Express Receiver (Signal Group b) – AC and DC Characteristics

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
UI	Unit Interval	399.88 (min) 400.12 (max)	199.94 (min) 200.06 (max)	ps	UI does not account for variations caused by SSC.
$V_{RX-DIFF-PP-CC}$	Differential Rx Peak-to-Peak Voltage for Common REFCLK Rx Architecture	0.175 (min) 1.2 (max)	0.120 (min) 1.2 (max)	V	$V_{RX-DIFF-PP} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$
T_{RX-EYE}	Receiver Eye Time Opening	0.40 (min)	N/A	UI	Minimum eye time at Rx pins to yield a 10^{-12} Bit Error Rate. Receiver eye margins are defined into a 2 x 50Ω reference load.
$T_{RX-TJ-CC}$	Maximum Rx Inherent Timing Error	N/A	0.40 (max)	UI	Maximum Rx inherent total timing error for common REFCLK Rx architecture. Refer to Note 1.
$T_{RX-DJ-DD-CC}$	Maximum Rx Inherent Deterministic Timing Error	N/A	0.30 (max)	UI	Maximum Rx inherent deterministic timing error for common REFCLK Rx architecture. Refer to Note 1.
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time Delta between the Median and Deviation from the Median	0.3 (max)	Not specified	UI	
$T_{RX-MIN-PULSE}$	Minimum Width Pulse at Rx	Not specified	0.6 (min)	UI	Measured to account for worst Tj at 10^{-12} Bit Error Rate.
$V_{RX-MAX-MIN-RATIO}$	Minimum/ Maximum Pulse Voltage on Consecutive UI	Not specified	5 (max)	Ratio	Rx eye must simultaneously meet V_{RX-EYE} limits.
$BW_{RX-PLL-HI}$	Maximum Rx PLL Bandwidth	22 (max)	16 (max)	MHz	Second Order PLL Jitter Transfer Bounding function. Refer to Note 2.
$BW_{RX-PLL-LO-3DB}$	Minimum Rx PLL Bandwidth for 3-dB Peaking	1.5 min	8 (min)	MHz	
$BW_{RX-PLL-LO-1DB}$	Minimum Rx PLL Bandwidth for 1-dB Peaking	Not specified	5 (min)	MHz	
$PKG_{RX-PLL1}$	Rx PLL Peaking with 8-MHz Minimum Bandwidth	Not specified	3.0	dB	
$PKG_{RX-PLL2}$	Rx PLL Peaking with 5-MHz Minimum Bandwidth	Not specified	1.0	dB	

Table 18-8. 2.5 and 5.0 GT/s PCI Express Receiver (Signal Group b) – AC and DC Characteristics *(Cont.)*

Symbol	Parameter	2.5 GT/s	5.0 GT/s	Units	Comments
$RL_{\text{RX-DIFF}}$	Rx Differential Return Loss (Package + Silicon)	10 (min)	10 (min) for 0.05 to 1.25 GHz 8 (min) for 1.25 to 2.5 GHz	dB	Refer to Note 3.
$RL_{\text{RX-CM}}$	Common Mode Return Loss	6 (min)	6 (min)	dB	Refer to Note 3.
$Z_{\text{RX-DC}}$	Rx DC Single-Ended Impedance	40 (min) 60 (max)	40 (min) 60 (max)	Ω	Required Rx D+ and D- DC impedance (50Ω ±20% tolerance). Refer to Note 4.
$Z_{\text{RX-DIFF-DC}}$	DC Differential Rx Impedance	80 (min) 120 (max)	Not specified	Ω	Rx DC Differential mode impedance. Parameter is captured for 5.0 GHz by $RL_{\text{RX-DIFF}}$. Refer to Note 4.
$V_{\text{RX-CM-AC-P}}$	Rx AC Common Mode Voltage	150 (max)	150 (max)	mVP	Measured at Rx pins, into a pair of 50Ω terminations into Ground. Refer to Note 5.
$Z_{\text{RX-HIGH-IMP-DC-POS}}$	DC Input Common Mode Input Impedance for Voltage >0 during Reset or Power-Down	50K (min)	50K (min)	Ω	Rx DC common mode impedance with the Rx terminations not powered, measured over the range 0 to 200 mV (with respect to Ground). Refer to Note 6.
$Z_{\text{RX-HIGH-IMP-DC-NEG}}$	DC Input Common Mode Input Impedance for Voltage <0 during Reset or Power-Down	1.0K (min)	1.0K (min)	Ω	Rx DC common mode impedance with the Rx terminations not powered, measured over the range -150 to 0 mV (with respect to Ground). Refer to Note 6.
$V_{\text{RX-IDLE-DET-DIFFp-p}}$	Electrical Idle Detect Threshold	65 (min) 175 (max)	65 (min) 175 (max)	mV	$V_{\text{RX-IDLE-DET-DIFFp-p}} = 2 \text{ x } \lvert V_{\text{RX-D+}} - V_{\text{RX-D-}} \rvert$ Measured at the Receiver's package pins.
$T_{\text{RX-IDLE-DET-DIFF-ENTERTIME}}$	Unexpected Electrical Idle Enter Idle Detect Threshold Integration Time	10 (max)	10 (max)	ms	An un-expected Electrical Idle ($V_{\text{RX-DIFFp-p}} < V_{\text{RX-IDLE-DET-DIFFp-p}}$) must be recognized no longer than $T_{\text{RX-IDLE-DET-DIFF-ENTERTIME}}$ to signal an unexpected idle condition.
$L_{\text{RX-SKEW}}$	Total Lane-to-Lane Skew	20 (max)	8 (max)	ns	Across all Lanes on a Port. Includes variation in the length of a SKIP Ordered-Set at the Rx, as well as any delay differences arising from the interconnect itself. Refer to Note 7.

Notes:

1. *The four inherent timing error parameters are defined for the convenience of Rx designers, and they are measured during Receiver tolerancing.*
2. *Two combinations of PLL bandwidth and peaking are specified at 5.0 GT/s, to permit designers to make trade-offs between the two parameters. If the PLL's minimum bandwidth is ≥8 MHz, then up to 3.0 dB of peaking is permitted. If the PLL's minimum bandwidth is relaxed to ≥5.0 MHz, then a tighter peaking value of 1.0 dB must be met.*

   A PLL bandwidth extends from zero up to the value(s) defined as the minimum or maximum in Table 18-8. For 2.5 GT/s, a single PLL bandwidth and peaking value of 1.5 to 22 MHz and 3.0 dB are defined.
3. *Measurements must be made for both common mode and differential return loss. In both cases, the DUT must be powered up and DC-isolated, and its D+/D- inputs must be in the low-Z state.*
4. *The Rx DC single-ended impedance must be present when the Receiver terminations are first enabled, to ensure that the Receiver Detect occurs properly. Compensation of this impedance can start immediately, and the Rx single-ended impedance (constrained by* $RL_{RX\text{-}CM}$ *to* $50\Omega \pm 20\%$*) must be within the specified range by the time Detect is entered.*
5. *Common mode peak voltage is defined by the expression:*

   max{|(Vd+ - Vd-) - V-CMDC|}
6. $Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}NEG}$ *and* $Z_{RX\text{-}HIGH\text{-}IMP\text{-}DC\text{-}POS}$ *are defined, respectively, for negative and positive voltages at the input of the Receiver. Transmitter designers must comprehend the large difference between >0 and <0 Rx impedances when designing Receiver detect circuits.*
7. *The* $L_{RX\text{-}SKEW}$ *parameter exists to handle repeaters that re-generate REFCLK and introduce differing numbers of skips on different Lanes.*

Table 18-9. PCI Express Differential Clock (Signal Group c) – AC and DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
F_{REFCLK}	Reference Clock Frequency		100		MHz	1
$T_{REFCLK-HF-RMS}$	High frequency jitter -> 1.5 MHz to Nyquist RMS jitter after applying filter functions, per the *PCI Express Base r2.0*			3.1	ps RMS	
$T_{REFCLK-LF-RMS}$	Low frequency jitter – 10 kHz to 1.5 MHz jitter after applying filter functions, per the *PCI Express Base r2.0*			3.0	ps RMS	
$T_{REFCLK-SSC-RES}$	SSC residual after applying filter functions, per the *PCI Express Base r2.0*			75	ps	
V_{SW}	Differential Voltage Swing (0-to-peak)	125	200	800	mV	
	Differential Voltage Swing (peak-to-peak)	250	400	1,600	mV	
T_R/T_F	Clock Input Rise/Fall Time	0.6		4.0	V/ns	2
DC_{REFCLK}	Input Clock Duty Cycle	45	50	55	%	
R_{TERM}	Input Parallel Termination (Single-ended)		50		Ω	
	Input Parallel Termination (Differential)		100		Ω	
PPM	Reference Clock Tolerance	-300		+300	ppm	

Notes:

1. *PEX_REFCLKn/p must be AC-coupled. Use a 0.01 to 0.1 µF capacitor.*
2. *Specified at 20 to 80% points at the package balls.*

18.7 Transmit Drive Characteristics

The Drive Current and Transmit Equalization functions are programmable, to allow for optimization of different backplane lengths and materials.

The Transmit Drive Level is programmable (5-bit, per SerDes/Lane), to provide differential swing within the range listed in Table 18-10. The **SerDes Drive Level *x*** registers (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets B8Ch through B94h) provide access to all 48 Lanes for Drive Level programmability.

The Transmitter also incorporates programmable (5-bit, per SerDes/Lane) de-emphasis, to provide equalization to compensate for FR4 channel effects within the range listed in Table 18-10. The **Post-Cursor Emphasis Level *x*** registers (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets B98h through BA0h) provide access to all 48 Lanes for de-emphasis programmability.

The Transmit_Drive_Level[4:0] and Post-Cursor_Emphasis_Level[4:0] bits are used together to program the differential swing, as well as the dB loss for optimum Tx drive across the intended backplane.

Table 18-10 lists all possible combinations of Tx DRV_LVL[4:0] and POST_CURSOR[4:0], to achieve minimum 800 mV transition amplitude and the resulting de-emphasis (in decibels, dB). Of these, only certain combinations yield the specified 3 to 4 dB or 5.5 to 6.5 dB de-emphasis, per the *PCI Express Base r2.0* (**highlighted in bold**). All combinations are listed, however, to provide maximum flexibility for fine-tuning the Tx drive characteristics to a specific backplane.

Table 18-10. Tx Programmable Drive and De-Emphasis Levels

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
01h	11h	820	789	0.34	
	12h	849	818	0.33	
	13h	876	845	0.31	
02h	10h	799	742	0.65	
	11h	830	773	0.61	
	12h	858	802	0.58	
	13h	884	829	0.56	
03h	10h	809	727	0.93	
	11h	839	758	0.88	
	12h	867	787	0.84	
	13h	893	814	0.80	
04h	10h	818	712	1.22	
	11h	848	743	1.15	
	12h	876	772	1.09	
	13h	901	799	1.04	

Table 18-10. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
05h	0Fh	797	664	1.59	
	10h	828	697	1.50	
	11h	857	728	1.41	
	12h	884	758	1.34	
	13h	909	785	1.27	
	1Fh	796	663	1.59	
06h	0Fh	806	649	1.88	
	10h	837	682	1.77	
	11h	866	714	1.68	
	12h	892	743	1.59	
	13h	916	770	1.51	
	1Fh	806	649	1.88	
07h	0Fh	816	635	2.18	
	10h	846	668	2.05	
	11h	874	700	1.94	
	12h	900	729	1.83	
	13h	924	756	1.74	
	1Fh	816	635	2.18	
08h	0Fh	825	620	2.48	
	10h	855	654	2.33	
	11h	883	685	2.20	
	12h	908	715	2.08	
	13h	931	742	1.98	
	1Fh	825	620	2.47	
09h	0Eh	802	571	2.95	
	0Fh	834	607	2.77	
	10h	863	640	2.60	
	11h	891	671	2.46	
	12h	916	701	2.33	
	13h	938	728	2.21	
	1Eh	802	571	2.96	
	1Fh	834	606	2.77	

Table 18-10. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
0Ah	0Eh	811	557	3.27	
	0Fh	843	593	3.06	
	10h	872	626	2.88	
	11h	899	658	2.71	
	12h	923	687	2.57	
	13h	945	714	2.43	
	1Eh	811	557	**3.27**	
	1Fh	843	593	**3.06**	
0Bh	0Eh	821	543	**3.58**	
	0Fh	851	579	**3.35**	
	10h	880	612	**3.15**	
	11h	906	644	2.97	
	12h	930	673	2.81	
	13h	951	700	2.66	
	1Eh	820	543	**3.58**	
	1Fh	851	579	**3.35**	
0Ch	0Dh	797	492	4.19	
	0Eh	829	530	**3.89**	
	0Fh	860	566	**3.64**	
	10h	888	599	**3.42**	
	11h	914	630	**3.22**	
	12h	937	660	**3.05**	
	13h	958	687	2.89	
	1Dh	797	492	4.19	
	1Eh	829	530	**3.89**	
	1Fh	860	565	**3.64**	
0Dh	0Dh	806	479	4.52	
	0Eh	838	517	4.20	
	0Fh	868	552	**3.93**	
	10h	896	586	**3.69**	-3.5 dB default for PEX 8649
	11h	921	617	**3.48**	
	12h	944	646	**3.29**	
	13h	964	673	**3.11**	
	1Dh	806	479	4.52	
	1Eh	838	516	4.20	
	1Fh	868	552	**3.93**	

Table 18-10. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
0Eh	0Dh	815	466	4.86	
	0Eh	847	503	4.51	
	0Fh	876	539	4.22	
	10h	903	572	**3.96**	
	11h	928	604	**3.73**	
	12h	950	633	**3.53**	
	13h	970	660	**3.34**	
	1Dh	815	466	4.86	
	1Eh	846	503	4.52	
	1Fh	876	539	4.22	
0Fh	0Dh	824	453	5.20	
	0Eh	855	490	4.83	
	0Fh	884	526	4.51	
	10h	911	559	4.23	
	11h	935	591	**3.98**	
	12h	957	620	**3.76**	
	13h	975	647	**3.56**	
	1Dh	823	453	5.20	
	1Eh	855	490	4.83	
	1Fh	884	526	4.51	
10h	0Ch	799	399	**6.02**	
	0Dh	832	439	**5.55**	
	0Eh	863	477	5.15	
	0Fh	892	513	4.81	
	10h	918	546	4.51	
	11h	942	578	4.25	
	12h	963	607	4.01	
	13h	981	634	3.79	
	1Ch	799	399	**6.02**	
	1Dh	832	439	**5.55**	
	1Eh	863	477	5.15	
	1Fh	892	513	4.81	

Table 18-10. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
11h	0Ch	808	387	**6.40**	
	0Dh	841	427	**5.89**	
	0Eh	871	464	5.46	
	0Fh	899	500	5.10	
	10h	925	533	4.78	
	11h	948	565	4.50	
	12h	969	594	4.24	
	13h	986	621	4.02	
	1Ch	808	387	**6.40**	
	1Dh	840	427	**5.89**	
	1Eh	871	464	5.46	
	1Fh	899	500	5.10	
12h	0Ch	816	374	6.77	
	0Dh	849	414	**6.23**	
	0Eh	879	452	**5.78**	
	0Fh	906	487	5.39	
	10h	932	521	5.05	
	11h	954	552	4.75	
	12h	974	582	4.48	
	13h	991	609	4.24	
	1Ch	816	374	6.78	
	1Dh	849	414	6.23	
	1Eh	879	452	5.78	
	1Fh	906	487	5.39	
13h	0Ch	825	362	7.16	
	0Dh	857	402	6.58	
	0Eh	886	439	6.09	
	0Fh	913	475	5.68	
	10h	938	509	5.32	
	11h	960	540	5.00	
	12h	980	569	4.72	
	13h	996	596	4.46	
	1Bh	795	326	7.76	
	1Ch	825	362	7.16	
	1Dh	856	402	6.58	
	1Eh	886	439	**6.09**	
	1Fh	913	475	**5.68**	

Table 18-10. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
14h	0Bh	799	308	8.29	
	0Ch	833	350	7.54	
	0Dh	864	389	6.93	
	0Eh	893	427	**6.41**	
	0Fh	920	463	**5.97**	
	10h	944	496	**5.59**	
	11h	966	528	5.25	
	12h	985	557	4.95	
	13h	1,001	584	4.68	
	1Bh	804	313	8.19	
	1Ch	833	349	7.54	
	1Dh	864	389	6.93	
	1Eh	893	427	**6.41**	
	1Fh	920	463	**5.97**	
15h	0Bh	808	296	8.73	
	0Ch	841	337	7.93	
	0Dh	872	377	7.28	
	0Eh	901	415	6.73	-6 dB default for PEX 8649
	0Fh	927	451	**6.26**	
	10h	950	484	**5.86**	
	11h	972	516	**5.50**	
	12h	990	545	5.19	
	13h	1,006	572	4.90	
	1Bh	812	301	8.62	
	1Ch	841	337	7.93	
	1Dh	872	377	7.28	
	1Eh	900	415	6.73	
	1Fh	927	451	**6.62**	

Table 18-10. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
16h	0Bh	816	284	9.18	
	0Ch	849	326	8.32	
	0Dh	879	365	7.63	
	0Eh	907	403	7.05	
	0Fh	933	439	6.56	
	10h	956	472	**6.13**	
	11h	977	504	**5.76**	
	12h	995	533	5.42	
	13h	1,010	560	5.12	
	1Bh	820	289	9.05	
	1Ch	849	325	8.33	
	1Dh	879	365	7.63	
	1Eh	907	403	7.05	
	1Fh	933	439	6.56	
17h	0Bh	824	272	9.63	
	0Ch	856	314	8.72	
	0Dh	886	354	7.98	
	0Eh	914	391	7.37	
	0Fh	939	427	6.85	
	10h	962	460	**6.40**	
	11h	982	492	**6.01**	
	12h	999	521	**5.65**	
	13h	1,014	548	5.34	
	1Bh	828	277	9.50	
	1Ch	856	314	8.72	
	1Dh	886	353	7.99	
	1Eh	914	391	7.37	
	1Fh	939	427	6.85	

Table 18-10. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
18h	0Ah	798	216	11.35	
	0Bh	832	260	10.10	
	0Ch	864	302	9.13	
	0Dh	893	342	8.35	
	0Eh	921	380	7.70	
	0Fh	945	415	7.15	
	10h	968	449	6.68	
	11h	987	480	**6.26**	
	12h	1,004	509	**5.89**	
	13h	1,018	537	**5.56**	
	1Ah	802	222	11.16	
	1Bh	836	266	9.96	
	1Ch	864	302	9.13	
	1Dh	893	342	8.35	
	1Eh	921	379	7.70	
	1Fh	945	415	7.15	
19h	0Ah	806	204	11.91	
	0Bh	840	249	10.57	
	0Ch	871	290	9.54	
	0Dh	900	330	8.71	
	0Eh	927	368	8.02	
	0Fh	951	404	7.45	
	10h	973	437	6.95	
	11h	992	469	6.51	
	12h	1,008	498	**6.12**	
	13h	1,021	525	**5.78**	
	1Ah	810	210	11.71	
	1Bh	844	254	10.42	
	1Ch	871	290	9.54	
	1Dh	900	330	8.71	
	1Eh	927	368	8.03	
	1Fh	951	404	7.45	

Table 18-10. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
1Ah	0Ah	814	193	12.49	
	0Bh	847	237	11.05	
	0Ch	878	279	9.95	
	0Dh	907	319	9.08	
	0Eh	933	357	8.35	
	0Fh	957	392	7.74	
	10h	978	426	7.22	
	11h	996	457	6.76	
	12h	1,012	487	**6.36**	
	13h	1,025	514	**6.00**	
	1Ah	818	199	12.28	
	1Bh	851	243	10.89	
	1Ch	878	279	9.96	
	1Dh	907	319	9.08	
	1Eh	933	357	8.35	
	1Fh	957	392	7.74	
1Bh	0Ah	821	182	13.09	
	0Bh	854	226	11.55	
	0Ch	885	268	10.38	
	0Dh	913	308	9.45	
	0Eh	939	346	8.68	
	0Fh	962	381	8.04	
	10h	983	415	7.50	
	11h	1,000	446	7.01	
	12h	1,016	475	6.59	
	13h	1,028	503	**6.22**	
	1Ah	826	188	12.86	
	1Bh	858	232	11.38	
	1Ch	885	268	10.38	
	1Dh	913	308	9.45	
	1Eh	939	345	8.69	
	1Fh	962	381	8.04	

Table 18-10. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
1Ch	0Ah	829	171	13.71	
	0Bh	861	215	12.06	
	0Ch	892	257	10.81	
	0Dh	919	297	9.82	
	0Eh	945	334	9.02	
	0Fh	967	370	8.35	
	10h	987	404	7.77	
	11h	1,004	435	7.27	
	12h	1,019	464	6.83	
	13h	1,031	491	**6.44**	
	19h	799	131	15.71	
	1Ah	833	177	13.46	
	1Bh	865	221	11.87	
	1Ch	891	257	10.81	
	1Dh	919	297	9.83	
	1Eh	944	334	9.02	
	1Fh	967	370	8.35	
1Dh	09h	802	114	16.95	
	0Ah	836	160	14.36	
	0Bh	868	204	12.58	
	0Ch	898	246	11.25	
	0Dh	925	286	10.20	
	0Eh	950	324	9.36	
	0Fh	972	359	8.65	
	10h	992	393	8.05	
	11h	1,008	424	7.52	
	12h	1,022	454	7.06	
	13h	1,034	481	6.65	
	19h	806	120	16.55	
	1Ah	841	166	14.09	
	1Bh	872	210	12.38	
	1Ch	898	246	11.25	
	1Dh	925	286	10.21	
	1Eh	950	323	9.36	
	1Fh	972	359	8.65	

Table 18-10. Tx Programmable Drive and De-Emphasis Levels *(Cont.)*

POST_CURSOR [4:0]	DRV_LVL [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	De-Emphasis (dB)	Notes
1Eh	09h	809	103	17.90	
	0Ah	843	149	15.04	
	0Bh	875	193	13.11	
	0Ch	904	235	11.69	
	0Dh	931	275	10.59	
	0Eh	955	313	9.69	
	0Fh	977	349	8.95	
	10h	996	382	8.32	
	11h	1,012	413	7.77	
	12h	1,025	443	7.29	
	13h	1,037	470	6.87	
	19h	814	109	17.44	
	1Ah	848	155	14.74	
	1Bh	879	199	12.90	
	1Ch	904	235	11.70	
	1Dh	931	275	10.59	
	1Eh	955	313	9.70	
	1Fh	977	348	8.95	
1Fh	09h	817	93	18.91	
	0Ah	850	139	15.75	
	0Bh	881	183	13.66	
	0Ch	910	225	12.15	
	0Dh	936	265	10.98	
	0Eh	960	302	10.04	
	0Fh	981	338	9.26	
	10h	999	371	8.60	
	11h	1,015	403	8.03	
	12h	1,028	432	7.53	
	13h	1,039	459	7.09	
	19h	821	99	18.40	
	1Ah	854	145	15.43	
	1Bh	885	188	13.44	
	1Ch	910	225	12.15	
	1Dh	936	264	10.98	
	1Eh	960	302	10.04	
	1Fh	981	338	9.26	

18.7.1 Default Transmit Settings

Table 18-11 lists the default values of the Transmit Drive and Post-Cursor De-Emphasis levels (**SerDes Drive Level *x*** and **Post-Cursor Emphasis Level *x*** registers (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets B8Ch, B90h, and B94h, and offsets B98h, B9Ch, and BA0h, respectively)).

Table 18-11. Default Transmit Settings

Mode (dB)	Link Speed (GT/s)	DRV_LVL [4:0]	POST_CURSOR [4:0]	Transition Amplitude (mV)	Non-Transition Amplitude (mV)	Equalization[a] (dB)
-3.5	2.5	10h	0Dh	896	586	-3.69
-3.5	5.0	10h	0Dh	896	586	-3.69
-6	5.0	0Eh	15h	901	415	-6.73[b]

[a] *dB Equalization formula:*

```
20 x log[(Drive Level - De-Emphasis) / (Drive Level + De-Emphasis)]
```

[b] *The -6 dB setting is slightly larger than the maximum -6.5 dB specification, to better compensate for FR4 loss characteristics across a typical backplane application.*

18.8 Receive Characteristics

The Receiver circuit includes programmable equalization, to further compensate for the low-pass FR4 loss characteristics of the channel.

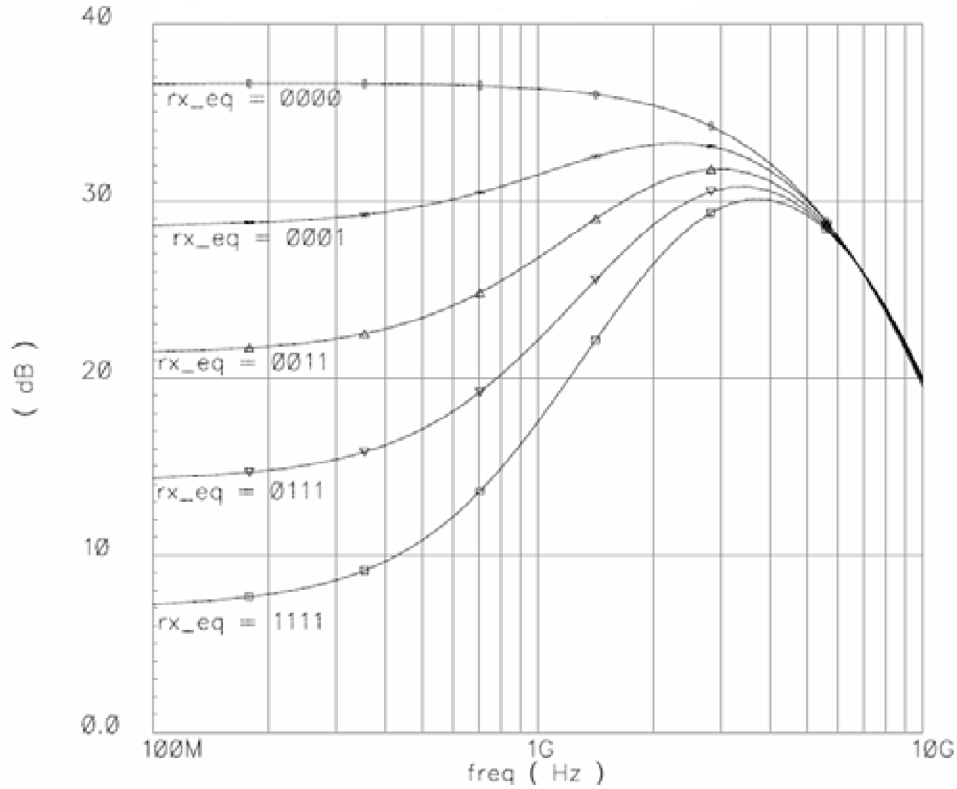
18.8.1 Receive Equalization

Table 18-12 lists the programmable bits used for controlling the Receiver circuit’s electrical characteristics, to mitigate the effects of signal loss and distortion across the PCB channel. The **Receiver Equalization Level *x*** registers (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offsets BA4h and BA8h) provide access to all 48 Lanes for Rx Equalization programmability. Figure 18-2 illustrates the Rx Equalization frequency characteristics.

Table 18-12. Receiver Equalization Settings

Rx Equalization[3:0]	Equalization
0h (default)	Off
1h	Minimum
2h to 3h	Low
4h to 6h	Low to Medium
7h to 9h	Medium
Ah to Dh	High to Medium
Eh to Fh	Maximum

Figure 18-2. Rx Equalization Frequency Characteristics



18.8.2 Receiver Electrical Idle

The Receiver circuit contains a signal detect circuit that is used to detect signal idling at the input. The threshold to detect the idle level is programmable, using the **Signal Detect Level** register (Base mode – Port 0, 16, or 20, except if any of these Ports is a Legacy NT Port, then the register for that Station exists in the NT Port Virtual Interface; Virtual Switch mode – Port 0, 16, or 20, accessible through the Management Port, offset BACh). A value of 00b provides the lowest signal voltage level detection threshold.

Chapter 19 Thermal and Mechanical Specifications

19.1 Thermal Characteristics

The PEX 8649 does not include a heat sink. The information described in this section is based upon sample thermal performance when a heat sink is used with the PEX 8649, and is provided for reference only.

19.1.1 Sample Thermal Data

The sample thermal data varies, with respect to Commercial and Extended temperature.

19.1.1.1 Sample Thermal Data – Commercial Temperature

Table 19-1 lists sample thermal data for the PEX 8649 at Commercial temperature, at Gen 2 (5.0 GT/s).

Table 19-1. Sample Thermal Data (27 x 27 mm^2 FCBGA Package with Heat Spreader, Commercial Temperature)[a]

Maximum Power (Watts)[b]	Heat Sink (Yes/No)	Air Flow (m/s)	Θ_{JA} (°C/W) JEDEC 8-Layer Board (109.22 x 167.64 mm^2)	Θ_{JC} (°C/W)	Θ_{JB} (°C/W)	Comments
13.39	Yes	2	2.60	0.30	5.90	Heat sink from Alpha W30-20W 30 x 30 x 15 mm^3. Thermal tape of 0.5 W/m/K conductivity T405 from Coumarics as TIM1.
			2.60			Heat sink from Alpha N30-20B 30 x 30 x 15 mm^3. Thermal tape of 0.5 W/m/K conductivity T405 from Coumarics as TIM1.
			2.40			Heat sink from Alpha W30-25W 30 x 30 x 15 mm^3. Thermal tape of 0.5 W/m/K conductivity T405 from Coumarics as TIM1.
			2.30			Heat sink from Alpha N30-25B 30 x 30 x 15 mm^3. Thermal tape of 0.5 W/m/K conductivity T405 from Coumarics as TIM1.

a. *The Maximum Operating Junction Temperature is 110°C.*
The Maximum Junction Temperature for Reliability is 125°C.

b. *The maximum power value listed assumes the conditions listed in Chapter 18, "Electrical Specifications," at Gen 2 (5.0 GT/s).*

19.1.1.2 Sample Thermal Data – Extended Temperature

Table 19-2 lists sample thermal data for the PEX 8649 at Extended temperature, at Gen 2 (5.0 GT/s).

Table 19-2. Sample Thermal Data (27 x 27 mm^2 FCBGA Package with Heat Spreader, Extended Temperature)[a]

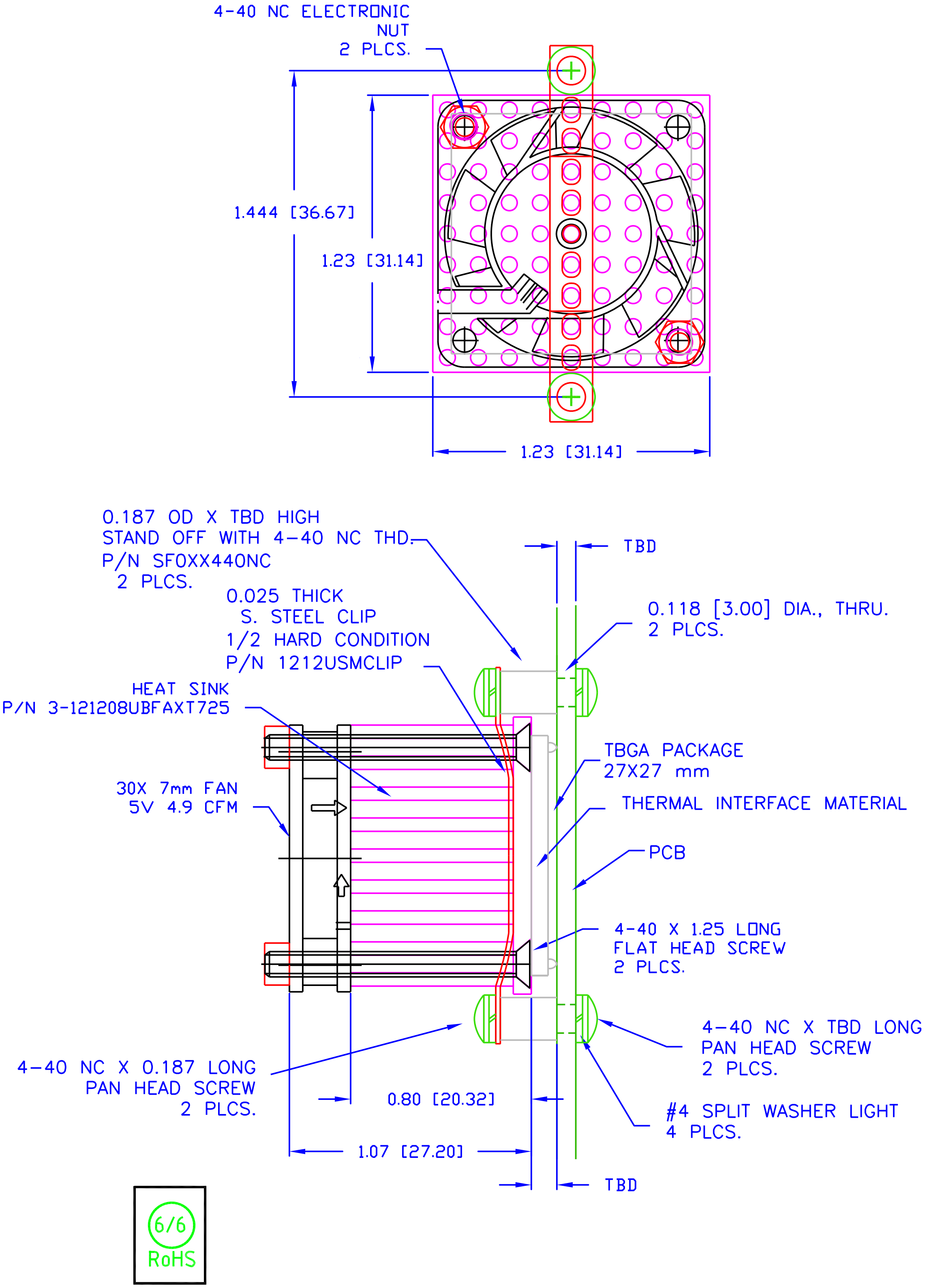
Maximum Power (Watts)[b]	Heat Sink (Yes/No)	Θ_{JA} (°C/W)		Θ_{JC} (°C/W)	Θ_{JB} (°C/W)	Comments
		Fan is On	At -5°C, with Fan Off[c]			
13.39	Yes	1.5	15	0.3	5.9	Refer to Figure 19-1.

[a] *The Maximum Operating Junction Temperature is 110°C.*
The Maximum Junction Temperature for Reliability is 125°C.

[b] *The maximum power value listed assumes the conditions listed in Chapter 18, "Electrical Specifications," at Gen 2 (5.0 GT/s).*

[c] ***Powering on at ambient temperature of -5°C** – Initially turn Off the fan on the heat sink when powering on the system at -5°C. The system must be warmed up for 10 seconds prior to turning On the fan.*

Figure 19-1. Extended Temperature Thermal Solution



19.2 General Package Specifications

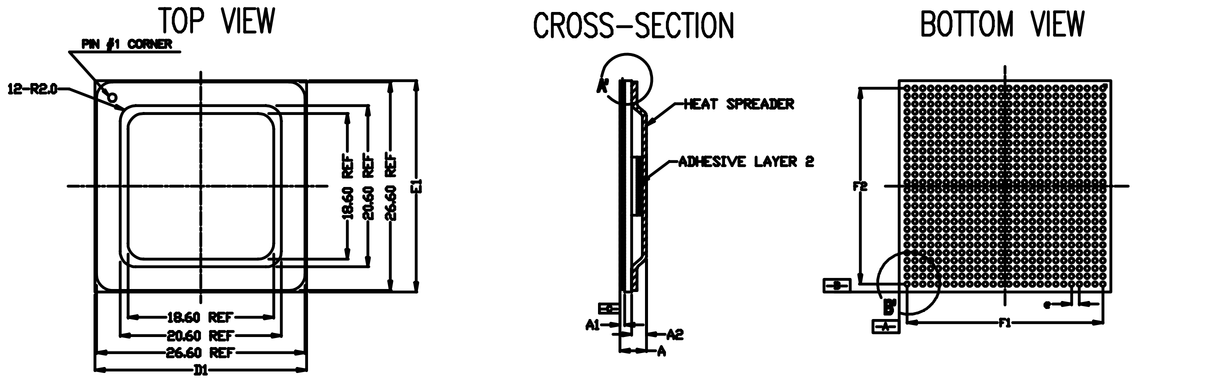
Table 19-3 lists general package specifications. For a more complete list, refer to Figure 19-2.

Table 19-3. General Package Specifications

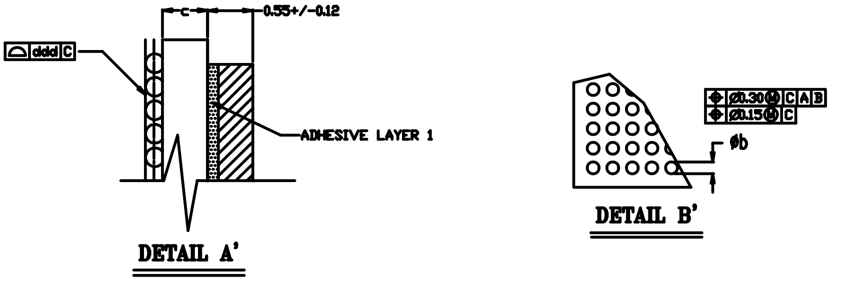
Parameter	Specification
Package Type	Flip-Chip Ball Grid Array (FCBGA) with Heat Spreader
Number of Balls	676
Package Dimensions	27 x 27 mm^2 (approximately 2.28 ±0.20-mm high)
Ball Matrix Pattern	26 x 26
Ball Pitch	1.0 mm
Ball Diameter	0.60 ±0.1 mm
Ball Spacing	0.40 mm

19.3 Mechanical Dimensions

Figure 19-2. Mechanical Dimensions (27 x 27 mm^2 FCBGA Package with Heat Spreader)



Symbol	UNITS IN MILLIMETER		
	MIN	NOM	MAX
c	0.48	0.58	0.68
A	2.08	2.28	2.48
A1	0.40	0.50	0.60
A2	1.08	1.20	1.32
Øb	0.50	0.60	0.70
D1	26.80	27.00	27.20
E1	26.80	27.00	27.20
F1	—	25.00	—
F2	—	25.00	—
e	—	1.00	—
ddd	—	—	0.20



BALL NAMES (BOTTOM VIEW)

A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
B26	B25	B24	B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
C26	C25	C24	C23	C22	C21	C20	C19	C18	C17	C16	C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1
D26	D25	D24	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
E26	E25	E24	E23	E22	E21	E20	E19	E18	E17	E16	E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1
F26	F25	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1
G26	G25	G24	G23	G22	G21	G20	G19	G18	G17	G16	G15	G14	G13	G12	G11	G10	G9	G8	G7	G6	G5	G4	G3	G2	G1
H26	H25	H24	H23	H22	H21	H20	H19	H18	H17	H16	H15	H14	H13	H12	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1
J26	J25	J24	J23	J22	J21	J20	J19	J18	J17	J16	J15	J14	J13	J12	J11	J10	J9	J8	J7	J6	J5	J4	J3	J2	J1
K26	K25	K24	K23	K22	K21	K20	K19	K18	K17	K16	K15	K14	K13	K12	K11	K10	K9	K8	K7	K6	K5	K4	K3	K2	K1
L26	L25	L24	L23	L22	L21	L20	L19	L18	L17	L16	L15	L14	L13	L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1
M26	M25	M24	M23	M22	M21	M20	M19	M18	M17	M16	M15	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1
N26	N25	N24	N23	N22	N21	N20	N19	N18	N17	N16	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1
P26	P25	P24	P23	P22	P21	P20	P19	P18	P17	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1
R26	R25	R24	R23	R22	R21	R20	R19	R18	R17	R16	R15	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
T26	T25	T24	T23	T22	T21	T20	T19	T18	T17	T16	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1
U26	U25	U24	U23	U22	U21	U20	U19	U18	U17	U16	U15	U14	U13	U12	U11	U10	U9	U8	U7	U6	U5	U4	U3	U2	U1
V26	V25	V24	V23	V22	V21	V20	V19	V18	V17	V16	V15	V14	V13	V12	V11	V10	V9	V8	V7	V6	V5	V4	V3	V2	V1
W26	W25	W24	W23	W22	W21	W20	W19	W18	W17	W16	W15	W14	W13	W12	W11	W10	W9	W8	W7	W6	W5	W4	W3	22	W1
Y26	Y25	Y24	Y23	Y22	Y21	Y20	Y19	Y18	Y17	Y16	Y15	Y14	Y13	Y12	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
AA26	AA25	AA24	AA23	AA22	AA21	AA20	AA19	AA18	AA17	AA16	AA15	AA14	AA13	AA12	AA11	AA10	AA9	AA8	AA7	AA6	AA5	AA4	AA3	AA2	AA1
AB26	AB25	AB24	AB23	AB22	AB21	AB20	AB19	AB18	AB17	AB16	AB15	AB14	AB13	AB12	AB11	AB10	AB9	AB8	AB7	AB6	AB5	AB4	AB3	AB2	AB1
AC26	AC25	AC24	AC23	AC22	AC21	AC20	AC19	AC18	AC17	AC16	AC15	AC14	AC13	AC12	AC11	AC10	AC9	AC8	AC7	AC6	AC5	AC4	AC3	AC2	AC1
AD26	AD25	AD24	AD23	AD22	AD21	AD20	AD19	AD18	AD17	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1
AE26	AE25	AE24	AE23	AE22	AE21	AE20	AE19	AE18	AE17	AE16	AE15	AE14	AE13	AE12	AE11	AE10	AE9	AE8	AE7	AE6	AE5	AE4	AE3	AE2	AE1
AF26	AF25	AF24	AF23	AF22	AF21	AF20	AF19	AF18	AF17	AF16	AF15	AF14	AF13	AF12	AF11	AF10	AF9	AF8	AF7	AF6	AF5	AF4	AF3	AF2	AF1

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Appendix A General Information

A.1 Product Ordering Information

Contact your local PLX Sales Representative for ordering information.

Table A-1. Product Ordering Information

Part Numbers	Description
PEX8649-AA50RBC F	PEX 8649 48-Lane, 12-Port PCI Express Gen 2 Multi-Root Switch (5.0 GT/s) Switch, 676-ball FCBGA Enhanced Noise Immunity 27 x 27 mm^2 package; RoHS
where	PEX – PCI Express Product Family 8649 – Part Number AA – Silicon Revision 50 – Signaling Rate (5.0 GT/s) R – Enhanced Noise Immunity B – Flip-Chip Ball Grid Array C – Commercial Temperature F – Lead-free 2nd Level Interconnect (2LI) Solder bump First Level Interconnect (FLI) contains lead per RoHS exemption for Flip-Chip
PEX 8649-16U16D BB RDK	PEX 8649 Base Board Rapid Development Kit with x16 Edge Connector
x1 Adapter	PCI Express x16 to x1 Adapter
x4 Adapter	PCI Express x16 to x4 Adapter
x8 Adapter	PCI Express x16 to x8 Adapter

A.2 United States and International Representatives and Distributors

PLX Technology, Inc., representatives and distributors are listed at www.plxtech.com.

A.3 Technical Support

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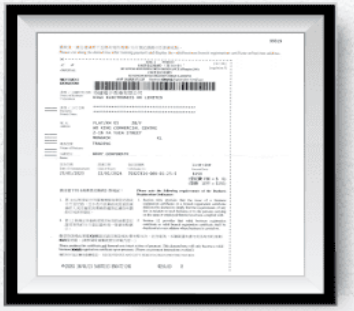

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