T8F49C2X Datasheet

DiGi Electronics Part Number	T8F49C2X-DG
Manufacturer	Efinix, Inc.
Manufacturer Product Number	T8F49C2X
Description	IC FPGA TRION T8 33 I/O 49FBGA
Detailed Description	Trion® Field Programmable Gate Array (FPGA) IC 33 125829 7384 49-VFBGA

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Manufacturer Product Number:	Manufacturer:
T8F49C2X	Efinix, Inc.
Series:	Product Status:
Trion®	Active
DiGi-Electronics Programmable:	Number of Logic Elements/Cells:
Not Verified	7384
Total RAM Bits:	Number of I/O:
125829	33
Voltage - Supply:	Mounting Type:
1.05V ~ 1.15V	Surface Mount
Operating Temperature:	Package / Case:
0°C ~ 85°C (TJ)	49-VFBGA
Supplier Device Package:	Base Product Number:
49-FBGA (3x3)	T8F49

Environmental & Export classification

RoHS Status:	Moisture Sensitivity Level (MSL):
ROHS3 Compliant	3 (168 Hours)

Trion® Packaging User Guide

UG-TRION-PKG-v4.5
April 2022
www.efinixinc.com

Contents

Introduction

Efinix offers Trion® FPGAs in packages that are designed for the device's maximum number of user I/O pins. This document describes Trion® FPGA pin and package specifications as well as solder reflow guidelines.

Learn more: Refer to the following documents for more information:
FPGA pinout specification
FPGA data sheet for pin definitions

Available Package Options

Table 1: Available Packages

Package	Dimensions (mm x mm)	Pitch (mm)
T4/T8 FPGAs		
49-ball FBGA(1)	3 x 3	0.4
81-ball FBGA	5 x 5	0.5
T20 FPGAs		
80-ball WLCSP	4.5 x 3.6	0.4
T8/T20 FPGAs		
144-pin QFP	20 x 20	0.5
T13/T20 FPGAs		
169-ball FBGA	9 x 9	0.65
256-ball FBGA	13 x 13	0.8
T20/T35 FPGAs		
324-ball FBGA	12 x 12	0.65
400-ball FBGA	16 x 16	0.8
T55/T85/T120 FPGAs		
324-ball FBGA	12 x 12	0.65
484-ball FBGA	18 x 18	0.80
576-ball FBGA	16 x 16	0.65

Refer to the FPGA data sheet for information on the number of GPIO and other resources in each FPGA/package combination.

(1) This package does not have dedicated JTAG pins (TDI, TDO, TCK, TMS).

Device Pinout File

Efinix provides pinout files for Trion® FPGAs. For each device/package combination, these files contain the pin name, I/O bank number for each pin, configuration function, and pin location.

Download: Download the pinout files from the Documentation page in the Support section of the Efinix® web site (www.efinixinc.com/support)

Pinout Description

The following tables describe the pinouts for power, ground, configuration, and interfaces.

Table 2: General Pinouts

Function	Group	Direction	Description
VCC	Power	–	Core power supply.
VCCIO*xx* VCCIO*xx_yy_zz*	Power	–	I/O pin power supply. Power for I/O banks that are shorted together. *xx*, *yy*, and *zz* are the bank locations.
VCCA_*xx* VCCA_PLL	Power	–	PLL analog power supply. *xx* indicates the location.
VCCIO	Power	–	I/O pin power supply.
VCCA_PLL	Power	–	PLL analog power supply.
VCCA_*xx*	Power	–	PLL analog power supply. *xx* indicates location: TL: Top left, TR: Top right, BR: bottom right
VCCA_*xx*	Power	–	PLL analog power supply. *xx* indicates the location.
VCCIO*xx*	Power	–	I/O pin power supply. *xx* indicates the bank location: 1A: Bank 1A, 3E: Bank 3E 4A: Bank 4A (only for 3.3 V) , 4B: Bank 4B (only for 3.3 V)
VCCIO*xx*	Power	–	I/O pin power supply. *xx* indicates the bank location.
VCCIO*xx_yy_zz*	Power	–	Power for I/O banks that are shorted together. *xx*, *yy*, and *zz* are the bank locations. For example: VCCIO1B_1C shorts banks 1B and 1C VCCIO3C_TR_BR shorts banks 3C, TR, and BR
GND	Ground	–	Ground.
GNDA_PLL	Ground	–	(T4/T8) PLL ground pin.
GNDA_PLL	Ground	–	PLL ground pin.
CLK*n*	Alternate	Input	Global clock network input. *n* is the number. The number of inputs is package dependent.
CTRL*n*	Alternate	Input	Global network input used for high fanout and global reset. *n* is the number. The number of inputs is package dependent.
PLLIN	Alternate	Input	PLL reference clock.
PLLIN	Alternate	Input	(T4) PLL reference clock.
PLLIN	Alternate	Input	(T8) PLL reference clock resource. There are 5 PLL reference clock resource assignments (depending on the package). Assign the reference clock resource based on the PLL you are using.
PLLIN	Alternate	Input	(T13/T20) PLL reference clock resource. There are 5 PLL reference clock resource assignments. Assign the reference clock resource based on the PLL you are using.
PLLIN	Alternate	Input	(T35) PLL reference clock resource. There are 7 PLL reference clock resource assignments. Assign the reference clock resource based on the PLL you are using.

Function	Group	Direction	Description
PLLIN	Alternate	Input	(T55/T85/T120) PLL reference clock resource. There are 7 (BGA324) or 8 (BGA484 and BGA576) PLL reference clock resource assignments. Assign the reference clock resource based on the PLL you are using.
MREFCLK	Alternate	Input	MIPI PLL reference clock source.
GPIO*x_n*	GPIO	I/O	General-purpose I/O for user function. User I/O pins are single-ended. *x*: Indicates the bank (L or R) *n*: Indicates the GPIO number.
GPIO*x_n_yyy* GPIO*x_n_yyy_zzz* GPIO*x_zzzn*	GPIO Multi-Function	I/O	Multi-function, general-purpose I/O. These pins are single ended. If these pins are not used for their alternate function, you can use them as user I/O pins. *x*: (T4) Indicates the bank; left (L) or right (R). *x*: (T13/T20) Indicates the bank; left (L), right (R), or bottom (B). *n*: Indicates the GPIO number. *yyy, yyy_zzz*: Indicates the alternate function. *zzzn*: Indicates LVDS TX or RX and number.
TXN*n*, TXP*n*	LVDS	I/O	LVDS transmitter (TX). *n*: Indicates the number.
RXN*n*, RXP*n*	LVDS	I/O	LVDS receiver (RX). *n*: Indicates the number.
CLKN*n*, CLKP*n*	LVDS	I/O	Dedicated LVDS receiver clock input. *n*: Indicates the number.
RXN*n*_EXTFB*n* RXP*n*_EXTFB*n*	LVDS	I/O	LVDS PLL external feedback. *n*: Indicates the number.
REF_RES	–	–	REF_RES is a reference resistor to generate constant current for LVDS TX. Connect a 12 kΩ resistor with a tolerance of ±1% to the REF_RES pin with respect to ground. If none of the pins in a bank are used for LVDS, leave this pin floating.

Table 3: Dedicated Configuration Pins

These pins cannot be used as general-purpose I/O after configuration.

Pins	Direction	Description	Use External Weak Pull-Up
CDONE	Bidirectional	Configuration done status pin. CDONE is an open drain output; connect it to an external pull-up resistor to VCCIO. When CDONE = 1, configuration is complete. If you hold CDONE low, the device will not enter user mode.	✓
CRESET_N	Input	Initiates FPGA re-configuration (active low). Pulse CRESET_N low for a duration of t_{creset_N} before asserting CRESET_N from low to high to initiate FPGA re-configuration. This pin does not perform a system reset.	✓
TCK	Input	JTAG test clock input (TCK). The rising edge loads signals applied at the TAP input pins (TMS and TDI). The falling edge clocks out signals through the TAP TDO pin.	✓
TMS	Input	JTAG test mode select input (TMS). The I/O sequence on this input controls the test logic operation . The signal value typically changes on the falling edge of TCK. TMS has an internal weak pull-up; when it is not driven by an external source, the test logic perceives a logic 1.	Recommended
TDI	Input	JTAG test data input (TDI). Data applied at this serial input is fed into the instruction register or into a test data register depending on the sequence previously applied at TMS. Typically, the signal applied at TDI changes state following the falling edge of TCK while the registers shift in the value received on the rising edge. Like TMS, TDI has an internal weak pull-up; when it is not driven from an external source, the test logic perceives a logic 1.	Recommended
TDO	Output	JTAG test data output (TDO). This serial output from the test logic is fed from the instruction register or from a test data register depending on the sequence previously applied at TMS. During shifting, data applied at TDI appears at TDO after a number of cycles of TCK determined by the length of the register included in the serial path. The signal driven through TDO changes state following the falling edge of TCK. When data is not being shifted through the device, TDO is set to an inactive drive state (e.g., high-impedance).	✓

Note: All dedicated configuration pins have Schmitt Trigger buffer. See Table 5Table 6Table 6Table 6 for the Schmitt Trigger buffer specifications.

Table 4: Dual-Purpose Configuration Pins

In user mode (after configuration), you can use these dual-purpose pins as general I/O.

Pins	Direction	Description	Use External Weak Pull-Up
CBUS[2:0]	Input	Configuration bus width select. CBUS has an internal weak pull-up. However, Efinix recommends that you use an external pull-up accordingly. See *Selecting the Configuration Mode* in **AN 006: Configuring Trion FPGAs**	✓(2)
CBSEL[1:0]	Input	Optional multi-image selection input (if external multi-image configuration mode is enabled).	✓(3)
CCK	I/O	Passive SPI input configuration clock or active SPI output configuration clock (active low). Includes an internal weak pull-up.	Optional(4)
CDI*n*	I/O	*n* is a number from 0 to 31 depending on the SPI configuration. 0: Passive serial data input or active serial output. 1: Passive serial data output or active serial input. *n*: Parallel I/O. In multi-bit daisy chain connection, the CDI*n* (31:0) connects to the data bus in parallel.	Optional(4)
CSI	Input	Chip select. 0: The FPGA is not selected or enabled and will not be configured. 1: Selects the FPGA for configuration (SPI and JTAG configuration).	✓
CSO	Output	Chip select output. Selects the next device for cascading configuration.	N/A
NSTATUS	Output	T8 BGA49 and T8 BGA81: Status (active low). Indicates a configuration error. When the FPGA drives this pin low, it indicates an ID mismatch. T8 QFP144: Status (active low). Indicates a configuration error. When the FPGA drives this pin low, it indicates an ID mismatch, the bitstream CRC check has failed, or remote update has failed.	N/A
SS_N	Input	SPI slave select (active low). Includes an internal weak pull-up resistor to VCCIO during configuration. During configuration, the logic level samples on this pin determine the configuration mode. This pin is an input when sampled at the start of configuration (SS is low); an output in active SPI flash configuration mode. The FPGA senses the value of SS_N when it comes out of reset (pulse CRESET_N low to high). 0: Passive mode 1: Active mode	Optional(4)
TEST_N	Input	Active-low test mode enable signal. Set to 1 to disable test mode. During configuration, rely on the external weak pull-up or drive this pin high.	✓

(2) Optional for x1 mode.
(3) Not applicable to single-image or remote update.
(4) Optional if external load pull-up is not required.

Pins	Direction	Description	Use External Weak Pull-Up
RESERVED_OUT	Output	Reserved pin during user configuration. This pin drives high during user configuration. BGA49 and BGA81 packages only.	N/A

Table 5: MIPI Pinouts (Dedicated)

n Indicates the number. *L* indicates the lane

Function	Group	Direction	Description
VCC25A_MIPI0 VCC25A_MIPI1	Power	–	MIPI 2.5 V analog power supply.
VCC12A_MIPI0_TX VCC12A_MIPI1_TX	Power	–	MIPI 1.2 V TX analog power supply.
VCC12A_MIPI0_RX VCC12A_MIPI1_RX	Power	–	MIPI 1.2 V RX analog power supply.
GNDA_MIPI	Ground	–	Ground for MIPI analog power supply.
MIPI*n*_TXDP*L* MIPI*n*_TXDN*L*	MIPI	I/O	MIPI differential transmit data lane.
MIPI*n*_RXDP*L* MIPI*n*_RXDN*L*	MIPI	I/O	MIPI differential receive data lane.
MREFCLK	Clock	Input	MIPI PLL reference clock source.

Table 6: DDR Pinouts (Dedicated)

n indicates the number.

Function	Direction	Description
VCCIO_DDR	–	DDR power supply.
DDR_A[*n*]	Output	Address signals to the memories.
DDR_BA[*n*]	Output	Bank signals to the memories.
DDR_CAS_N	Output	Active-low column address strobe signal to the memories.
DDR_CKE	Output	Active-high clock enable signals to the memories.
DDR_CK DDR_CK_N	Output	Differential clock output pins to the memories.
DDR_CS_N	Output	Active-low chip select signals to the memories.
DDR_DQ[*n*]	I/O	Data bus to/from the memories.
DDR_DM[*n*]	Output	Active-high data-mask signals to the memories.
DDR_DQS_N[*n*]	I/O	Differential data strobes to/from the memories.
DDR_DQS[*n*]	I/O	Differential data strobes to/from the memories.
DDR_ODT	Output	ODT signal to the memories.
DDR_RAS_N	Output	Active-low row address strobe signal to the memories.
DDR_RST_N	Output	Active-low reset signals to the memories.
DDR_WE_N	Output	Active-low write enable strobe signal to the memories.
DDR_VREF	I/O	Reference voltage.
DDR_ZQ	I/O	ZQ calibration pin.

49-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 1: 49-Ball FBGA Pinout Diagram

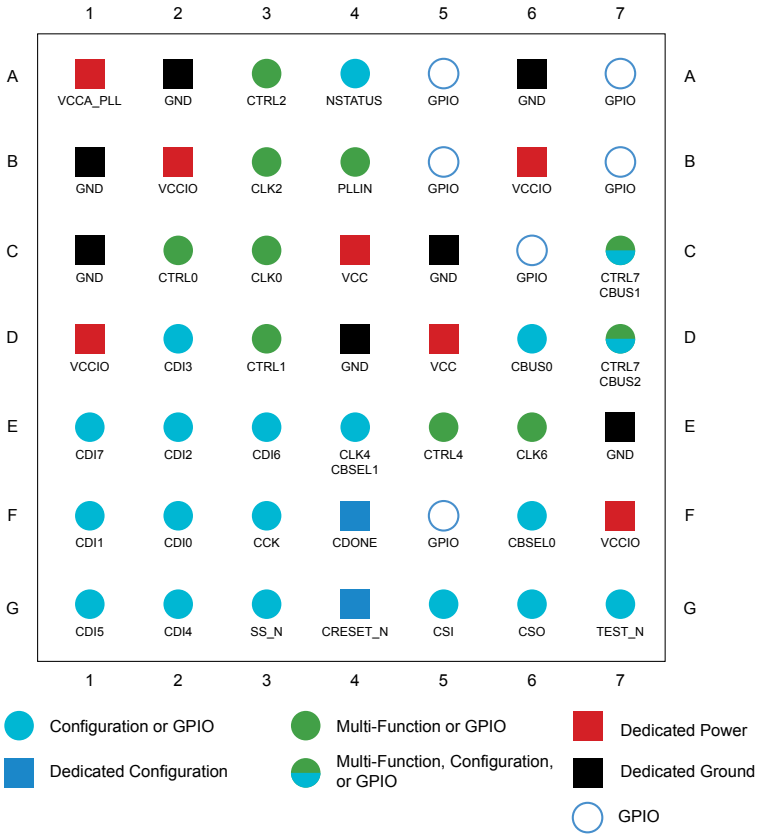


Figure 2: 49-Ball FBGA I/O Bank Diagram

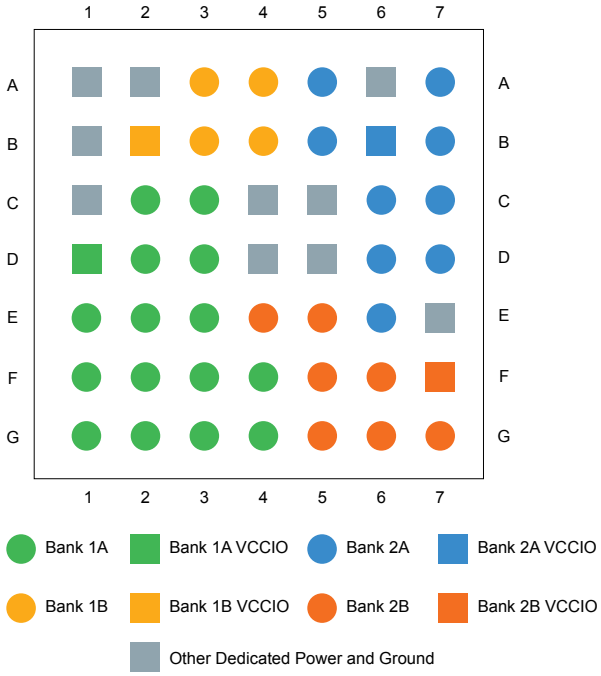


Figure 3: 49-Ball FPGA Package Marking

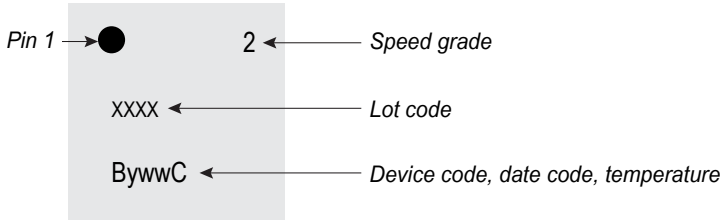
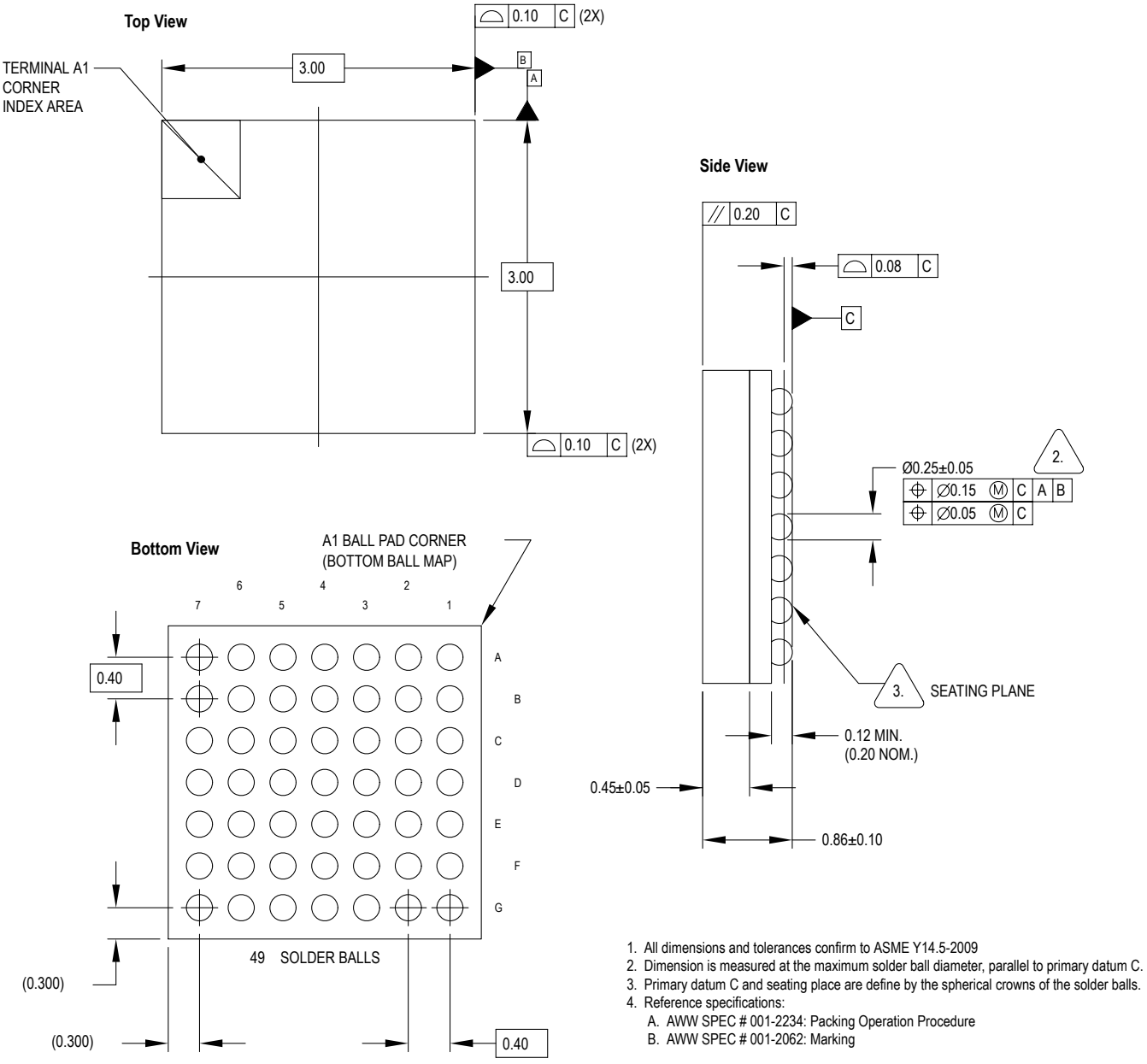


Figure 4: 49-Ball FBGA Package Outline



1. All dimensions and tolerances confirm to ASME Y14.5-2009
2. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
3. Primary datum C and seating place are define by the spherical crowns of the solder balls.
4. Reference specifications:
   A. AWW SPEC # 001-2234: Packing Operation Procedure
   B. AWW SPEC # 001-2062: Marking

80-Ball WLCSP Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 5: 80-Ball WLCSP Pinout Diagram

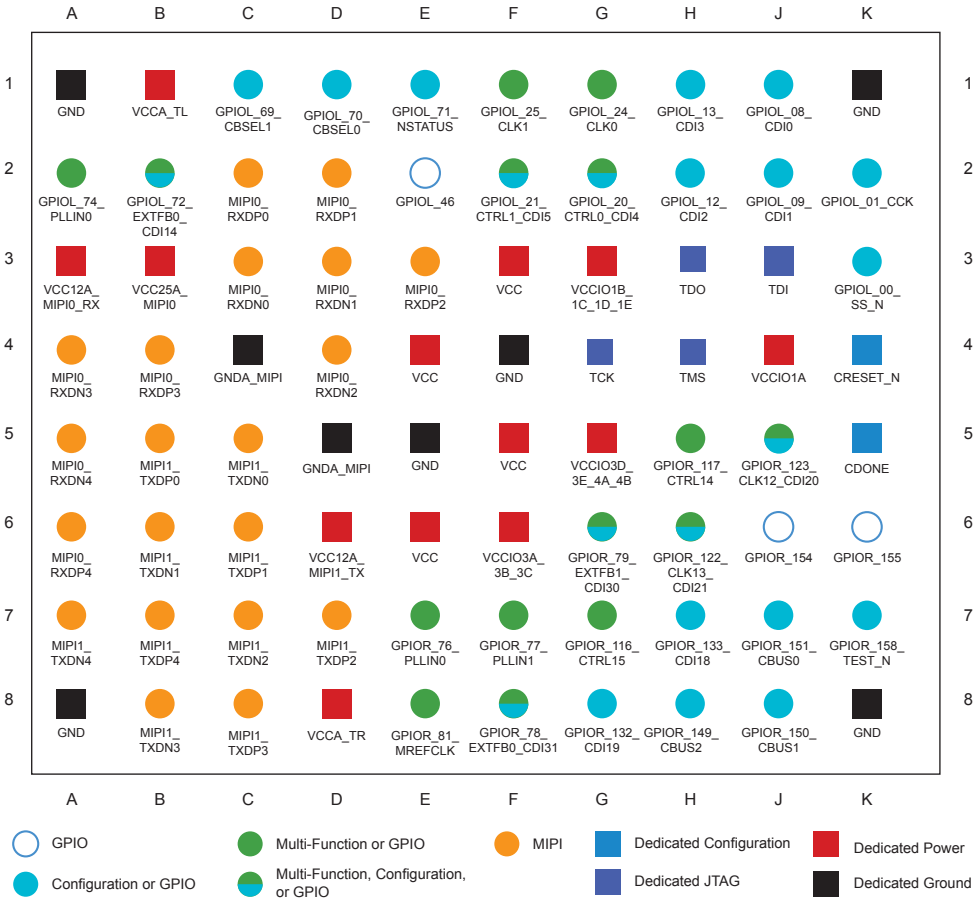


Figure 6: 80-Ball WLCSP I/O Bank Diagram

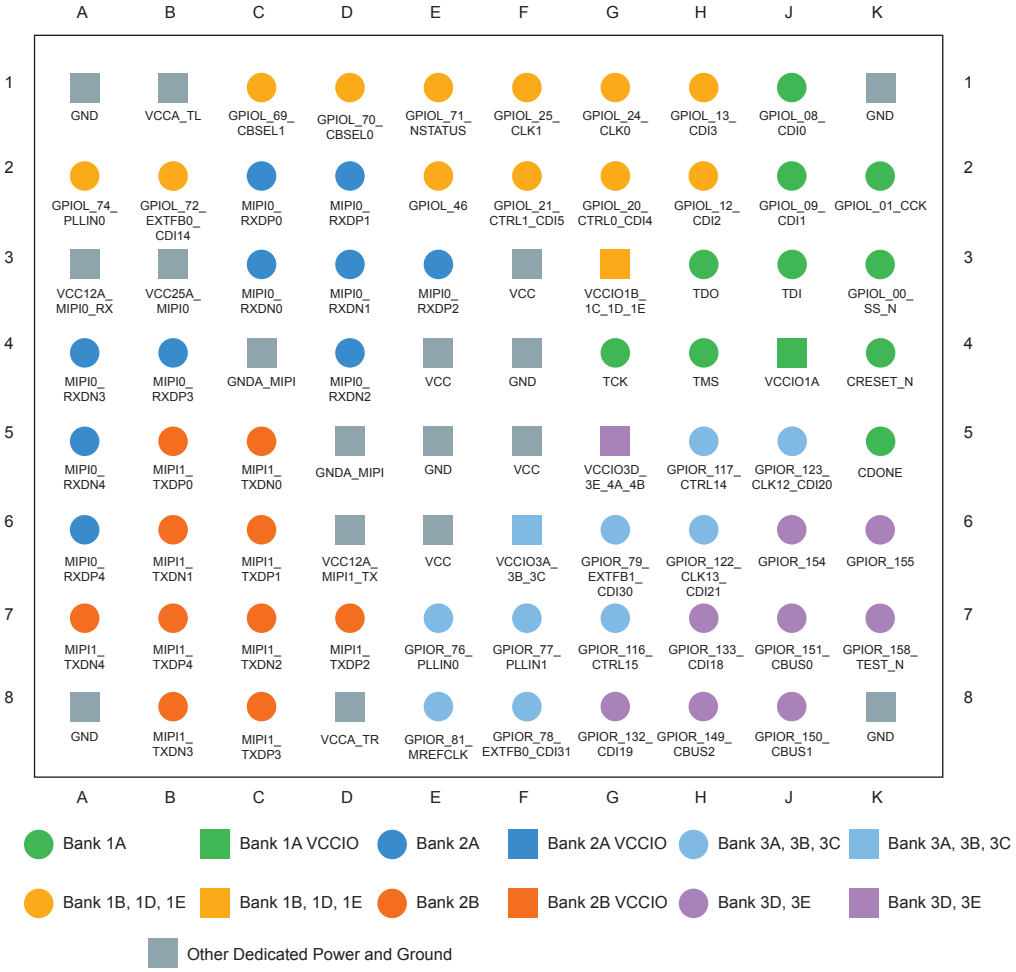


Figure 7: 80-Ball WLCSP Package Marking

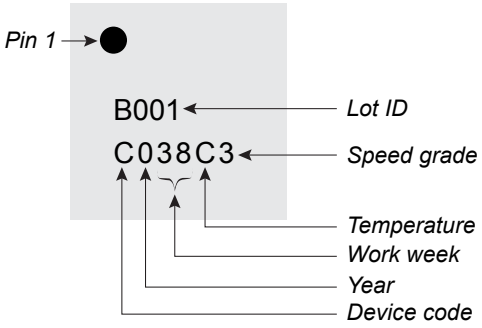
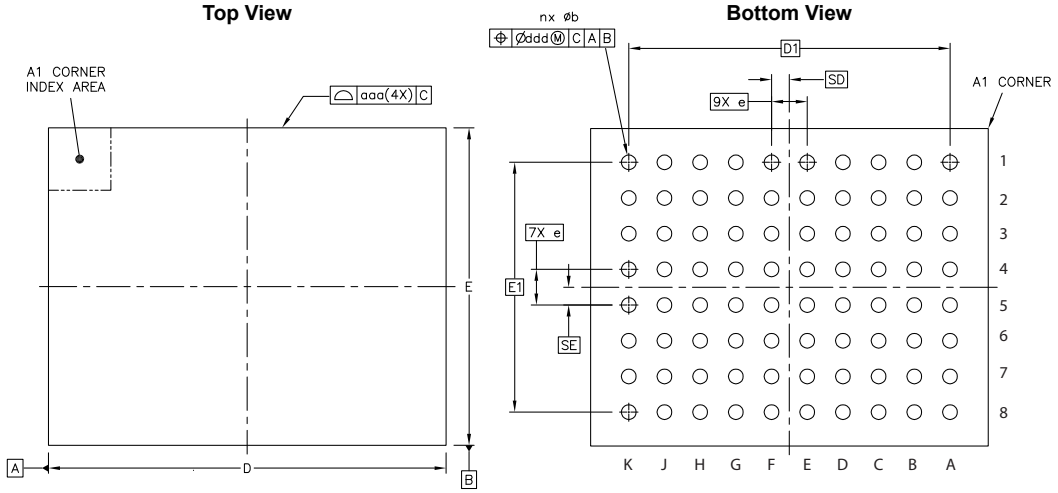
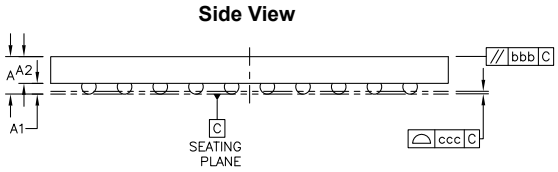


Figure 8: 80-Ball WLCSP Package Outline



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.4	0.455	0.51
STAND OFF		A1	0.125	---	0.185
WAFER THICKNESS		A2	0.275	0.3	0.325
FILM THICKNESS		A3	---	---	---
BODY SIZE	Y	D	4.4567		
	X	E	3.5569		
BALL/BUMP PITCH	Y	SD	0.2		BSC
	X	SE	0.2		BSC
EDGE BALL CENTER TO CENTER	Y	D1	3.6		BSC
	X	E1	2.8		BSC
PITCH		e	0.4		BSC
BALL DIAMETER (SIZE)			0.2		
BALL/BUMP WIDTH		b	0.19	---	0.25
BALL/BUMP COUNT		n	80		
PACKAGE EDGE TOLERANCE		aaa	0.03		
WAFER FLATNESS		bbb	0.06		
COPLANARITY		ccc	0.03		
BALL/BUMP OFFSET (PACKAGE)		ddd	0.015		



81-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 9: 81-Ball FBGA Pinout Diagram

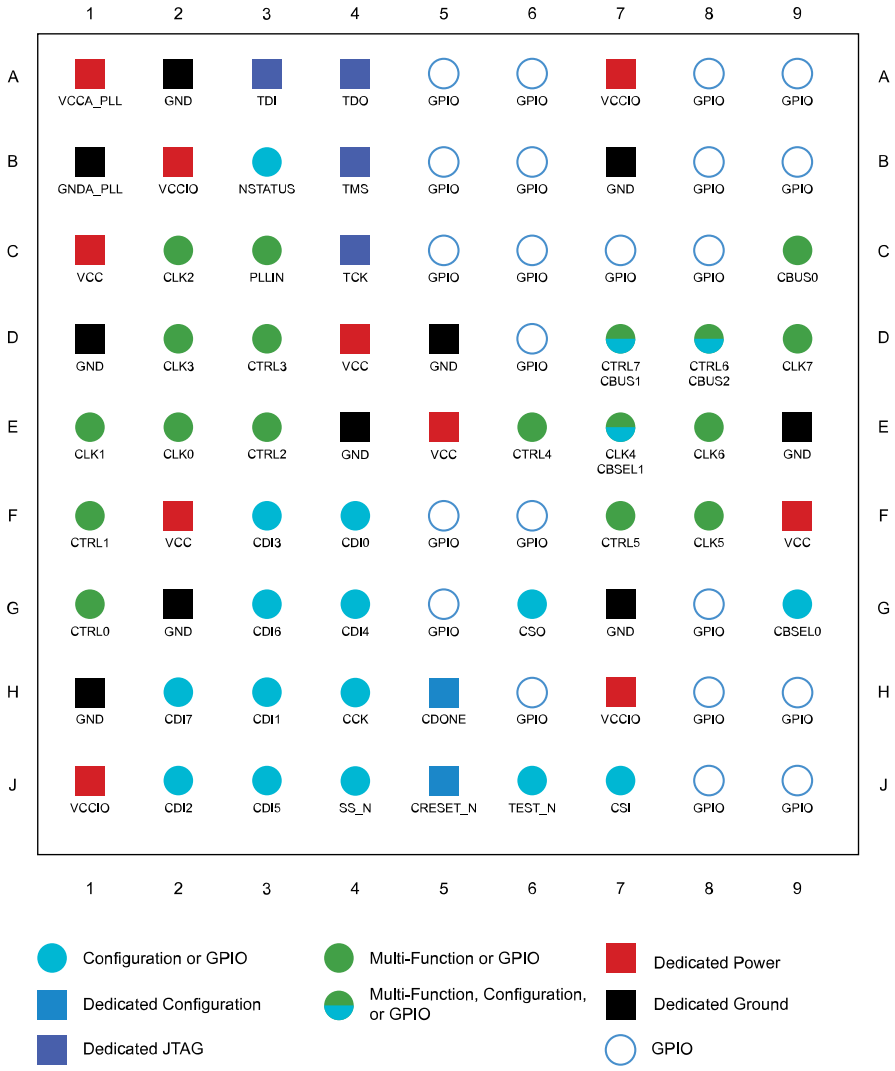


Figure 10: 81-Ball FBGA I/O Bank Diagram

Figure 11: 81-Ball FPGA Package Marking

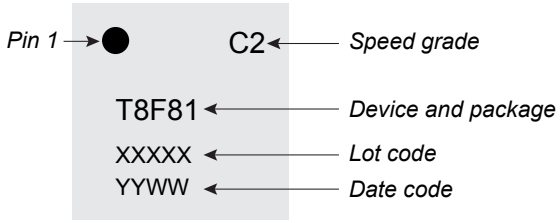
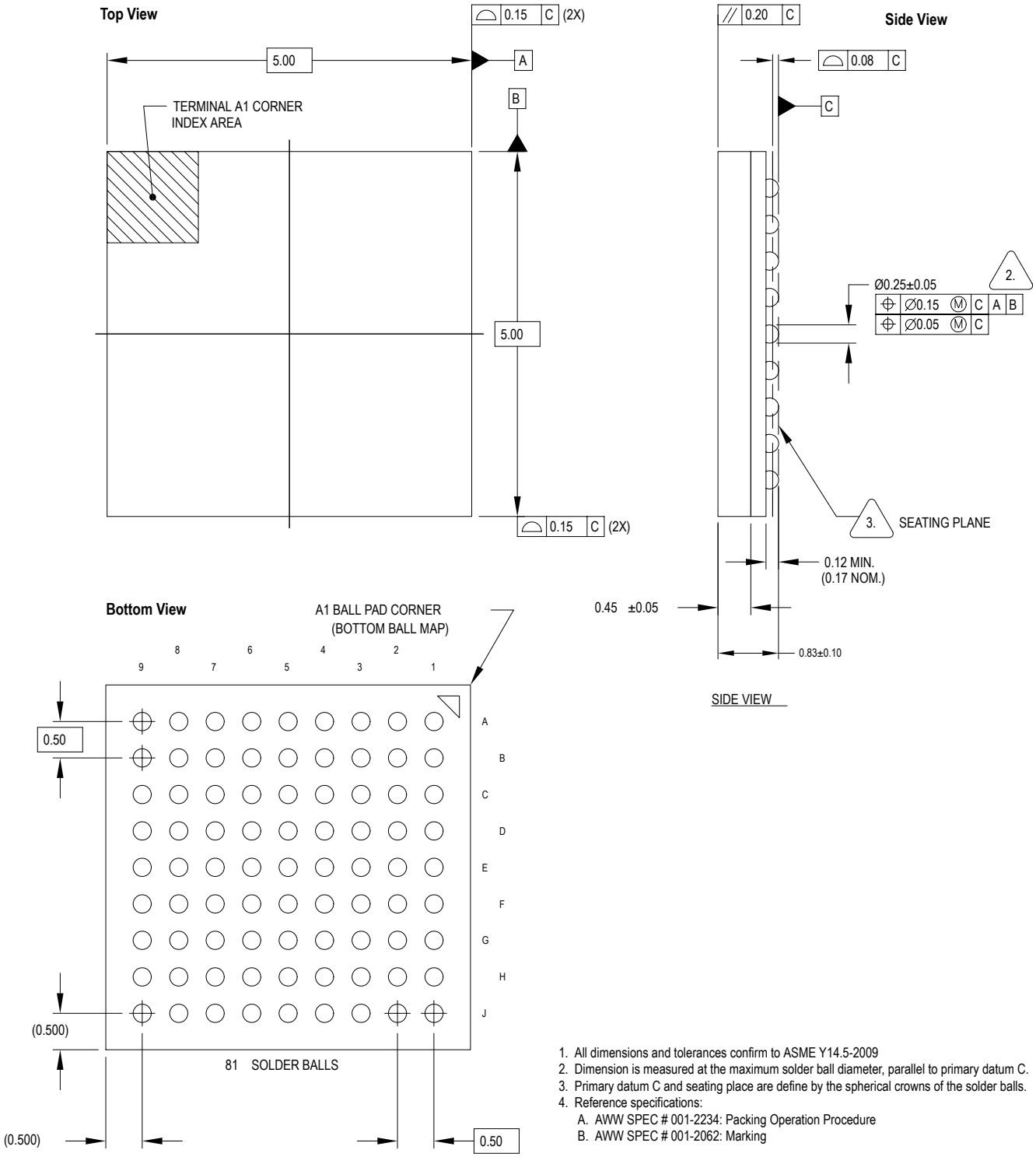


Figure 12: 81-Ball FBGA Package Outline



1. All dimensions and tolerances confirm to ASME Y14.5-2009
2. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
3. Primary datum C and seating place are define by the spherical crowns of the solder balls.
4. Reference specifications:
   A. AWW SPEC # 001-2234: Packing Operation Procedure
   B. AWW SPEC # 001-2062: Marking

144-Lead LQFP Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package.

Figure 13: 144-Lead LQFP Pinout Diagram

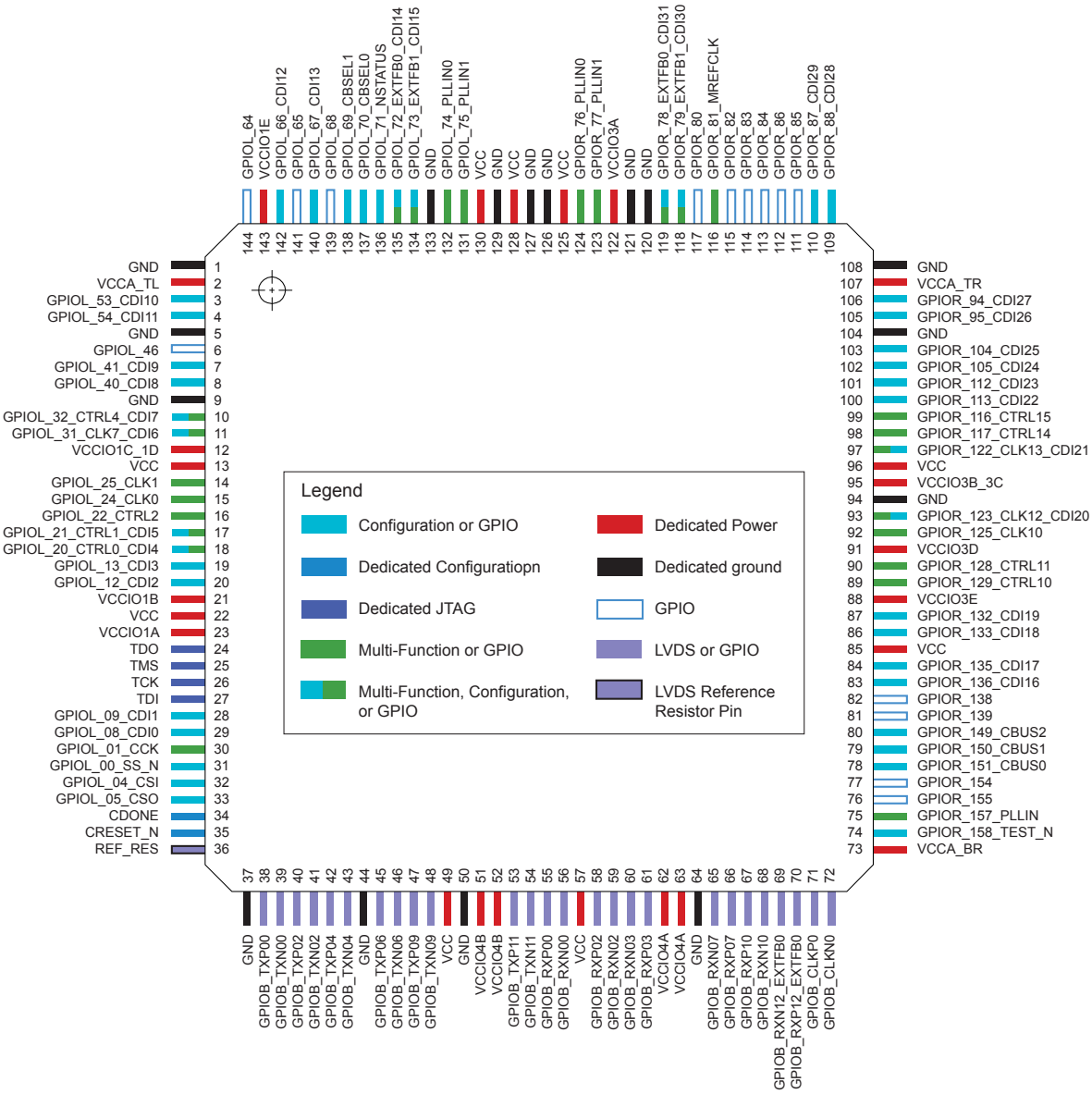


Figure 14: 144-Lead LQFP I/O Bank Diagram

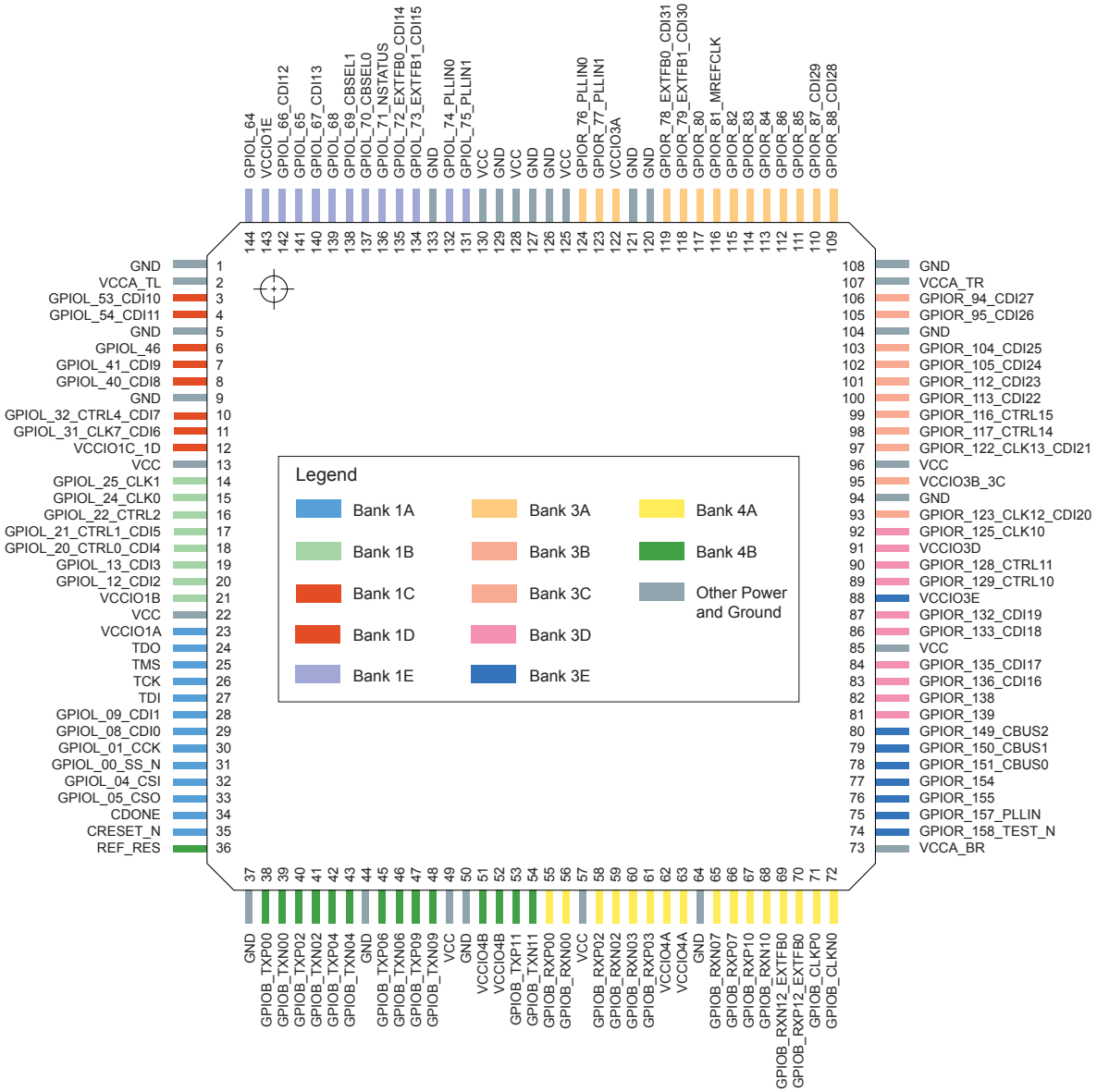


Figure 15: 144-Lead LQFP FPGA Package Marking

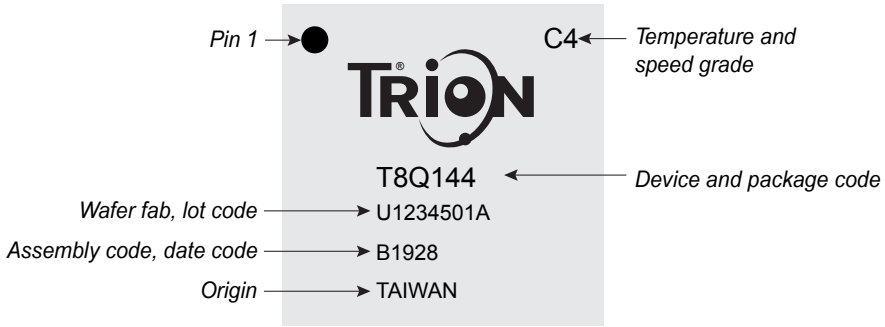
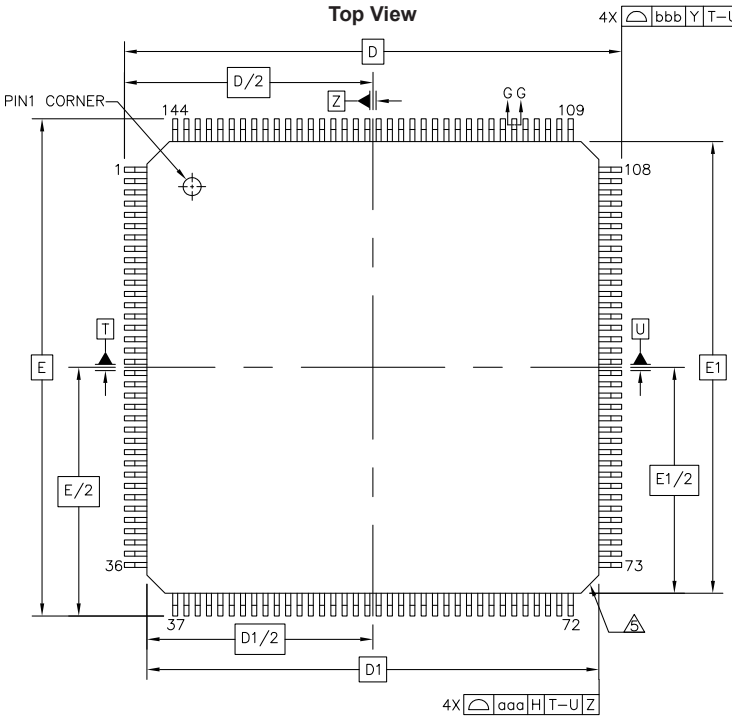
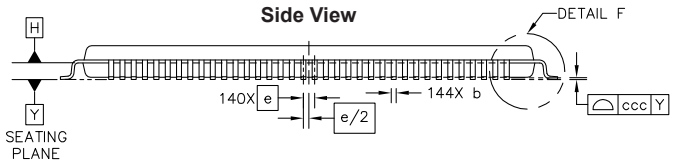
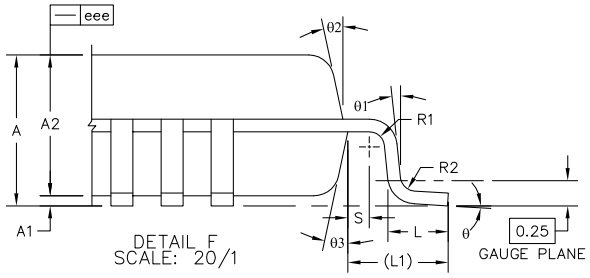


Figure 16: 144-Lead LQFP FBGA Package Outline





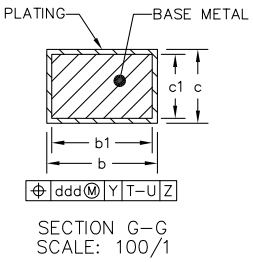


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.17	0.22	0.27
LEAD WIDTH		b1	0.17	0.2	0.23
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
	X	D	22 BSC		
	Y	E	22 BSC		
BODY SIZE	X	D1	20 BSC		
	Y	E1	20 BSC		
LEAD PITCH		e	0.5 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.1		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.08		
MOLD FLATNESS		eee	0.05		

NOTES

1. DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
2. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLDPROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
4. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUMb DIMENSION BY MORE THAN 0.08 mm. DAM BAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm.

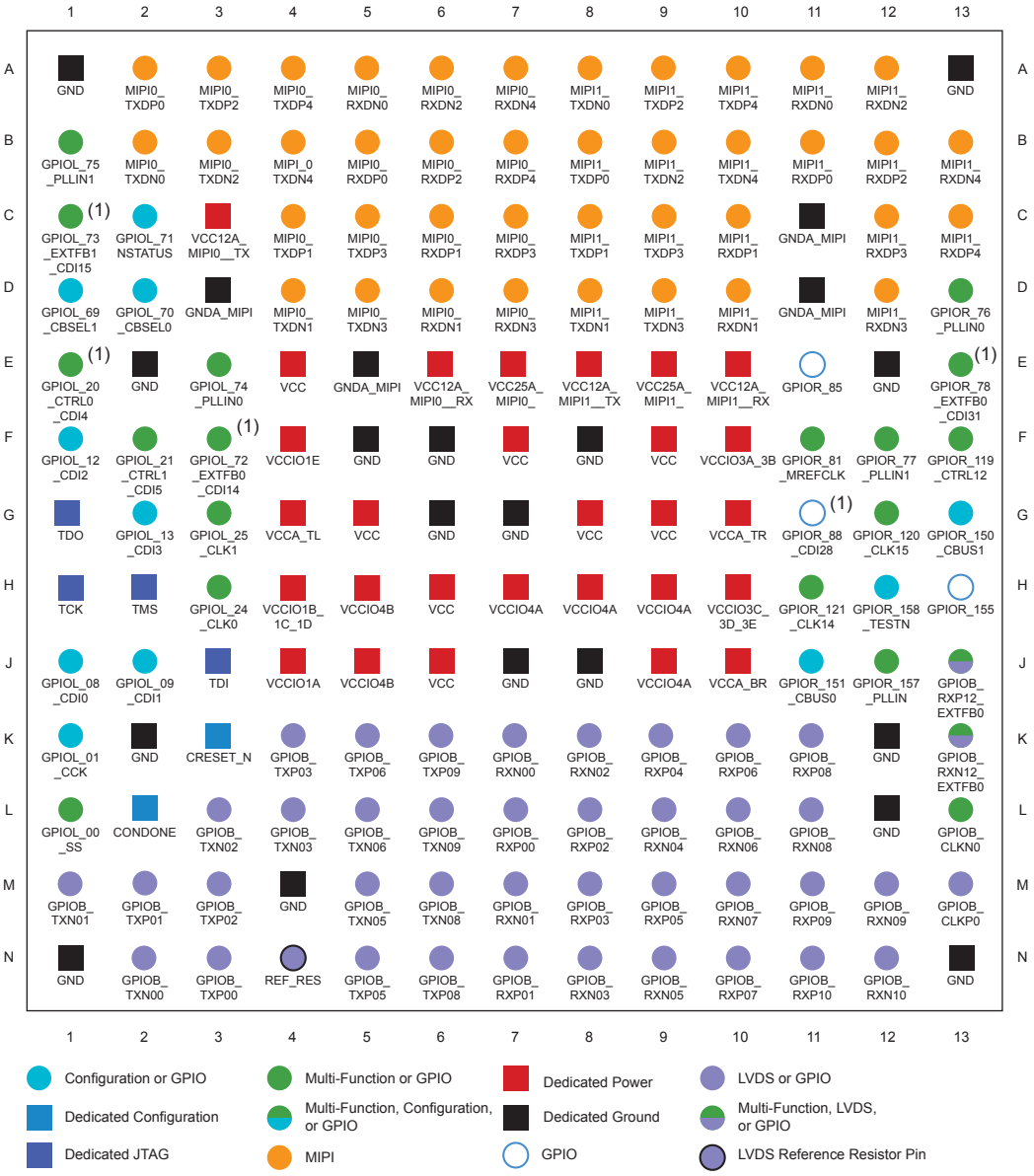
5 EXACT SHAPE OF EACH CORNER IS OPTIONAL.



169-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 17: 169-Ball FBGA Pinout Diagram



Note (1) In this package, this pin is not used for configuration functions.

Figure 18: 169-Ball FBGA I/O Bank Diagram

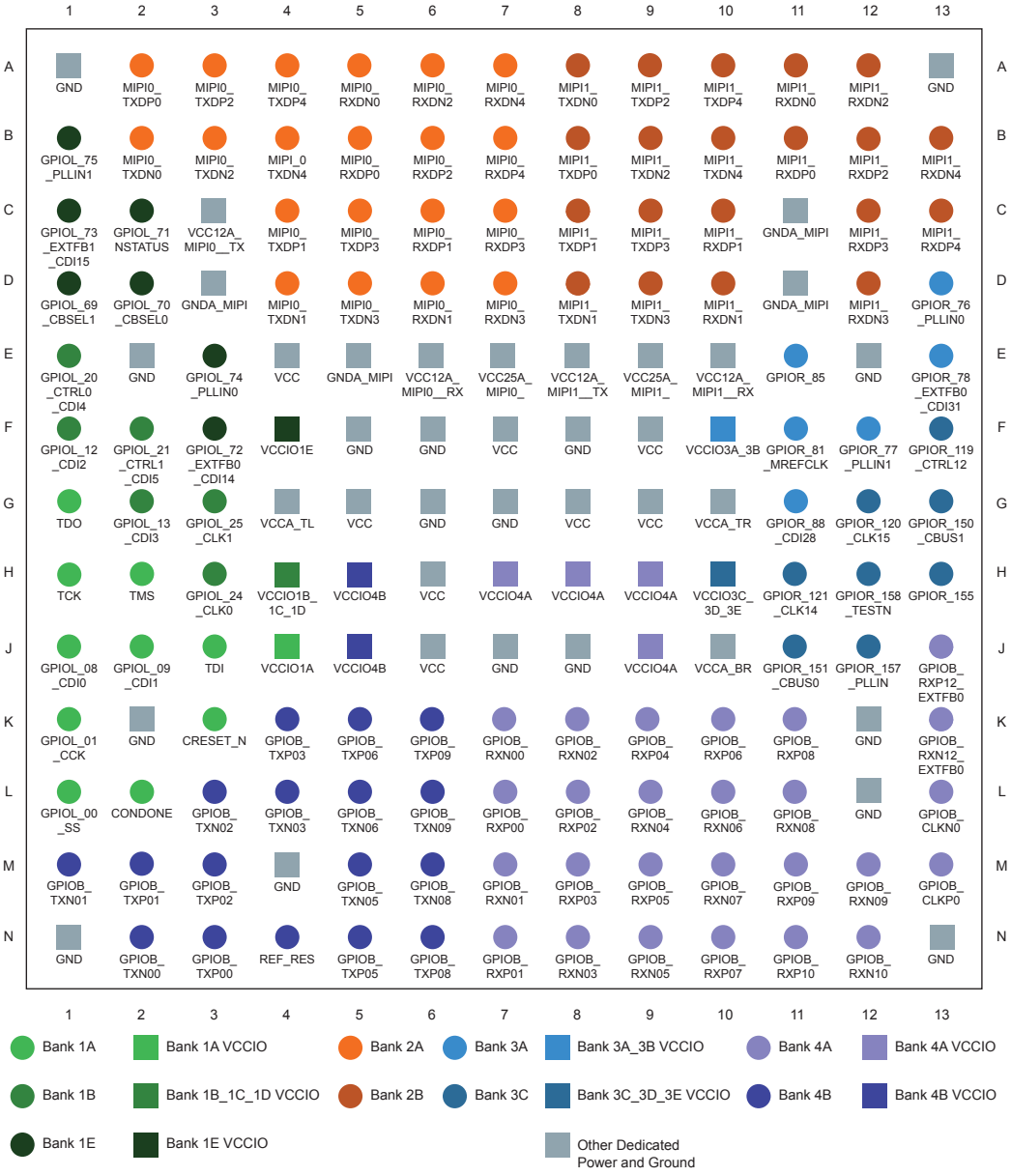


Figure 19: 169-Ball FPGA Package Marking

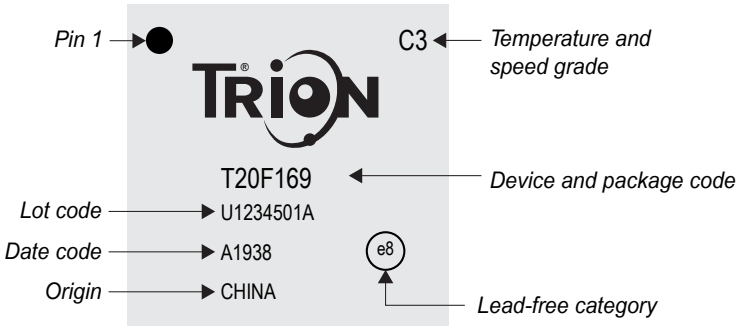
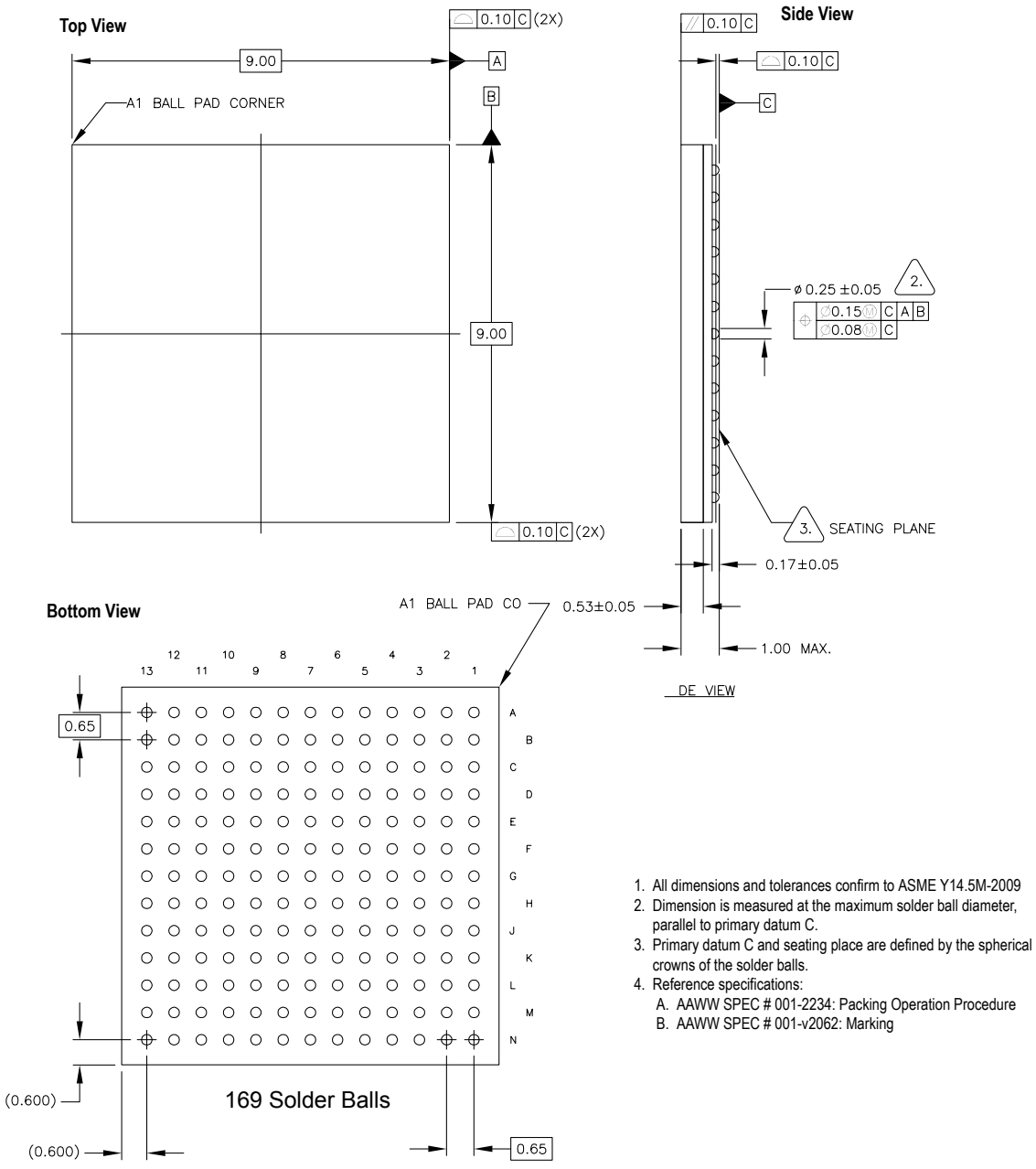


Figure 20: 169-Ball FBGA Package Outline



1. All dimensions and tolerances confirm to ASME Y14.5M-2009
2. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
3. Primary datum C and seating place are defined by the spherical crowns of the solder balls.
4. Reference specifications:
   A. AAWW SPEC # 001-2234: Packing Operation Procedure
   B. AAWW SPEC # 001-v2062: Marking

256-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 21: 256-Ball FBGA Pinout Diagram

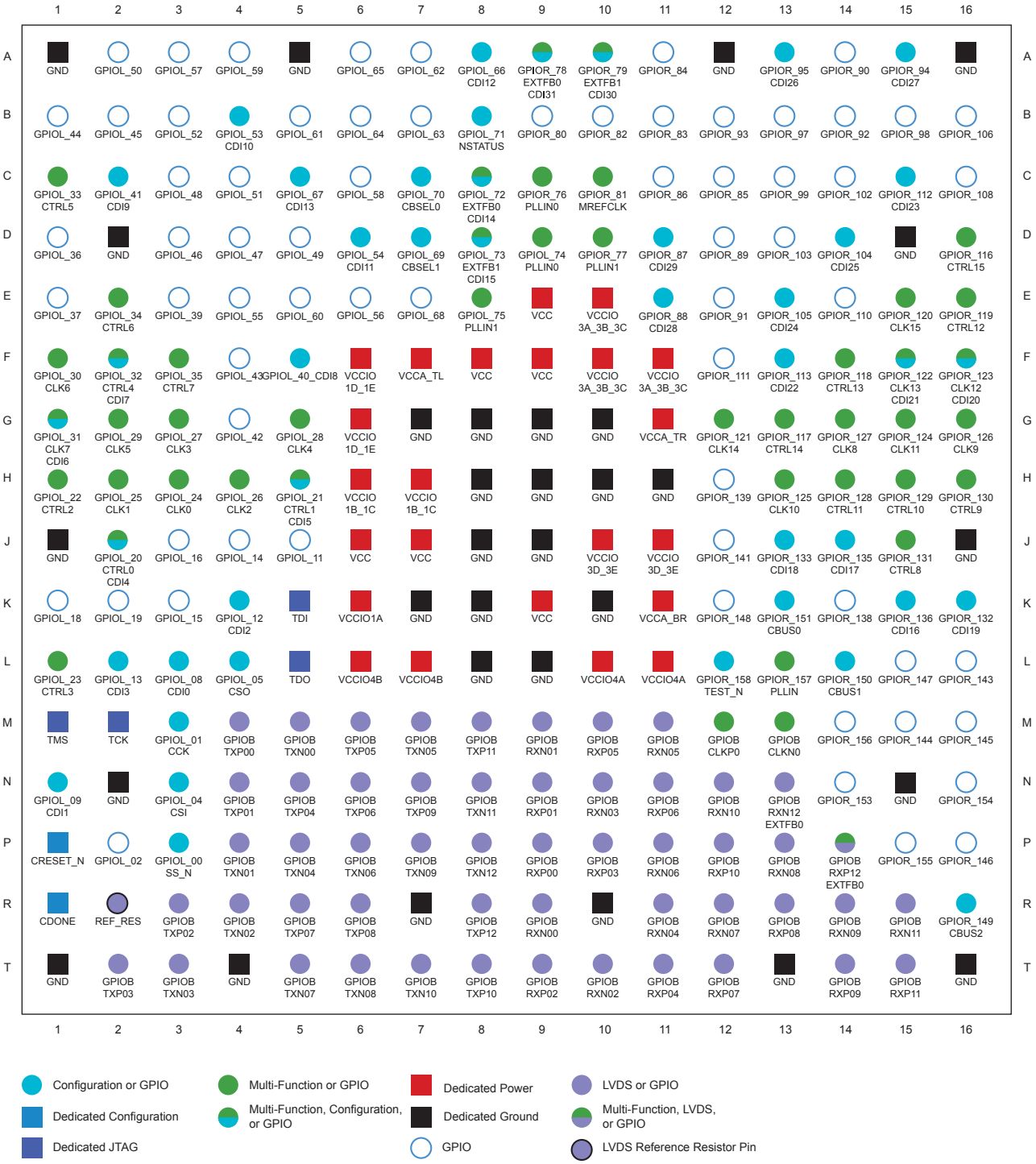


Figure 22: 256-Ball FBGA I/O Bank Diagram

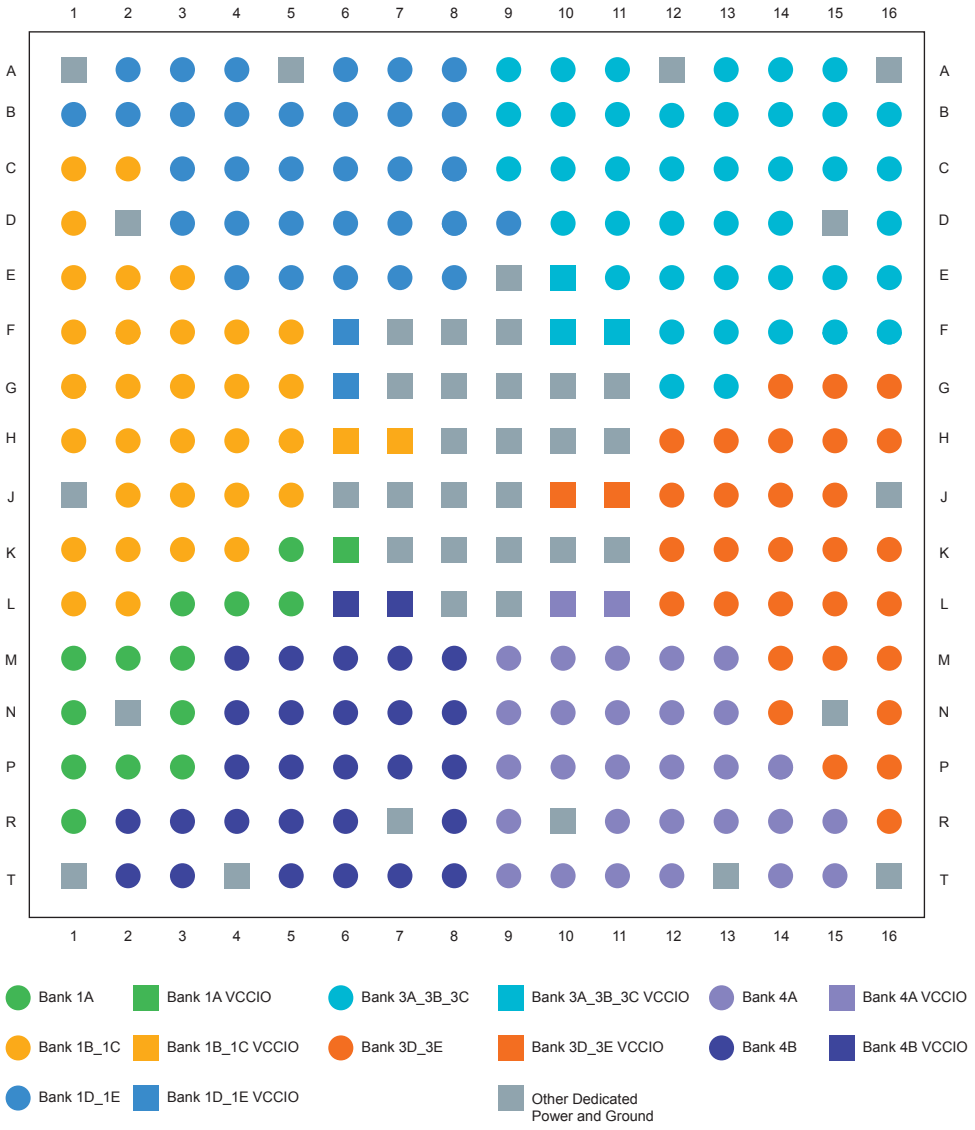


Figure 23: 256-Ball FPGA Package Marking

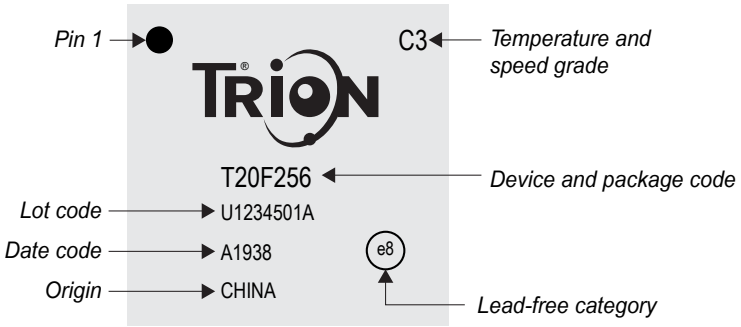
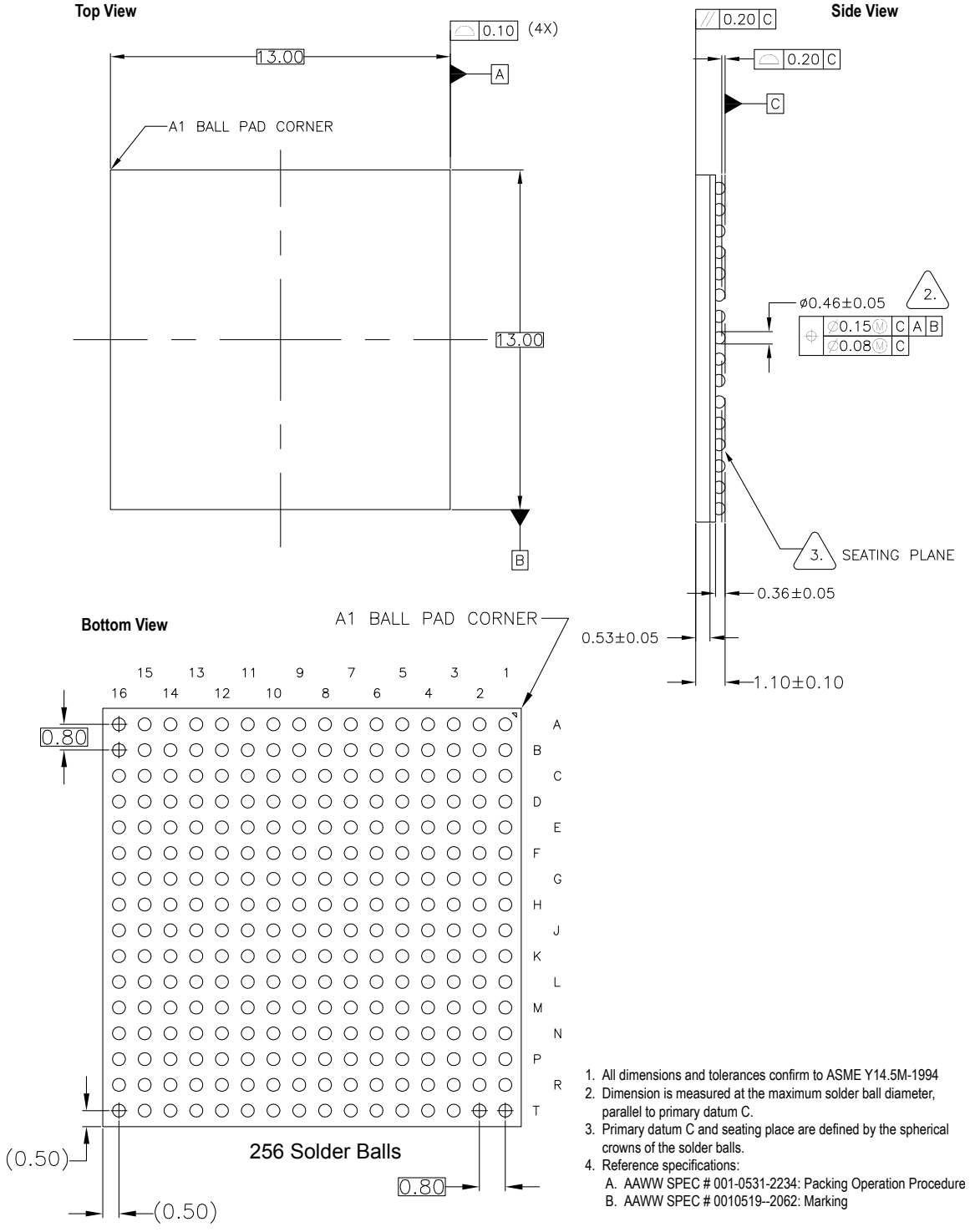


Figure 24: 256-Ball FBGA Package Outline



1. All dimensions and tolerances confirm to ASME Y14.5M-1994
2. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
3. Primary datum C and seating place are defined by the spherical crowns of the solder balls.
4. Reference specifications:
   A. AAWW SPEC # 001-0531-2234: Packing Operation Procedure
   B. AAWW SPEC # 0010519--2062: Marking

324-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. This is a flip chip package.

Note: Some pin names and I/O banks differ between T20/T35 and T55/T85/T120 FPGAs; however, you can still migrate between FPGAs in this package.

T20 and T35 FPGAs: Pinout and I/O Banks

Figure 25: 324-Ball FBGA Pinout Diagram (T20 and T35)

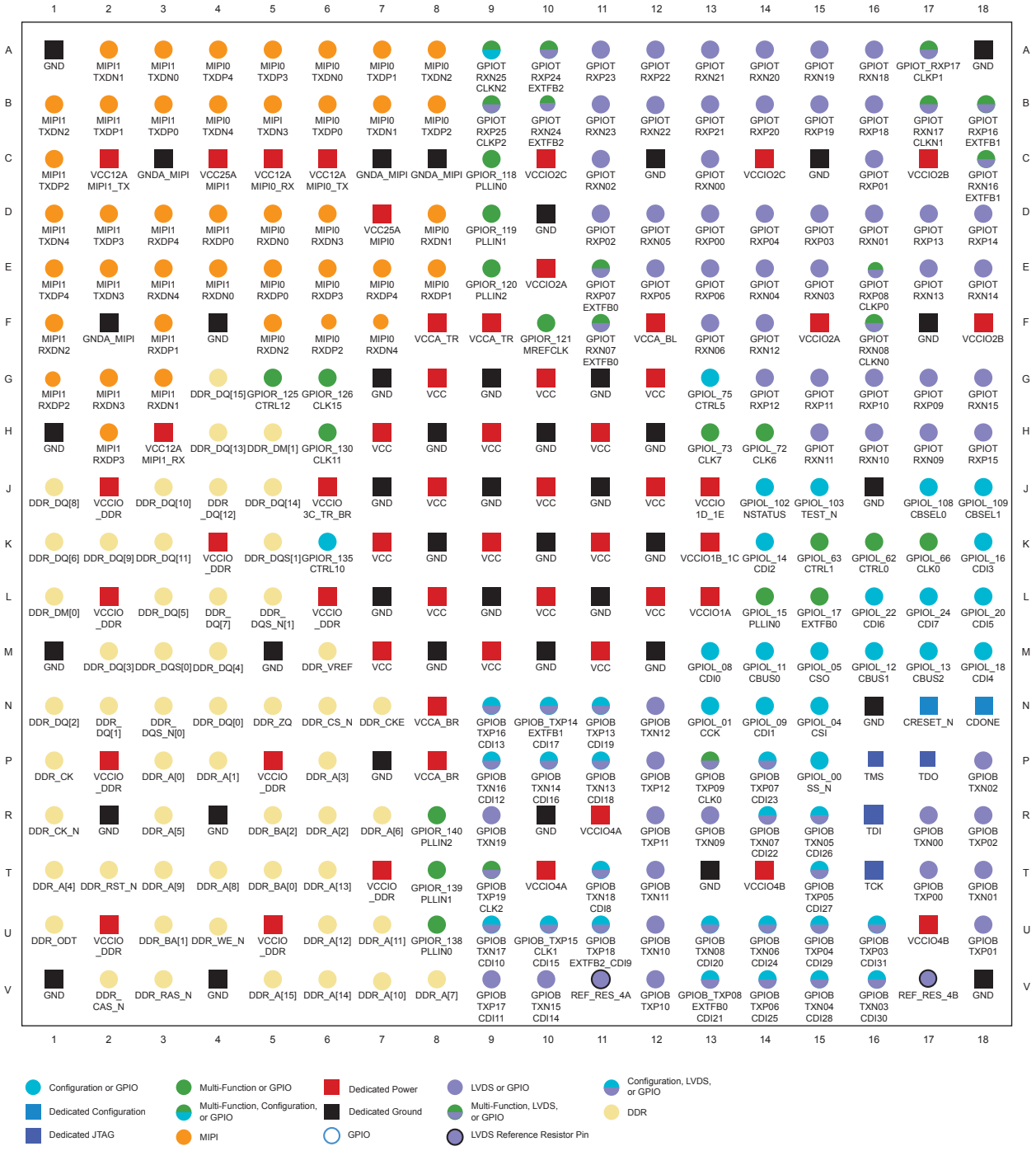
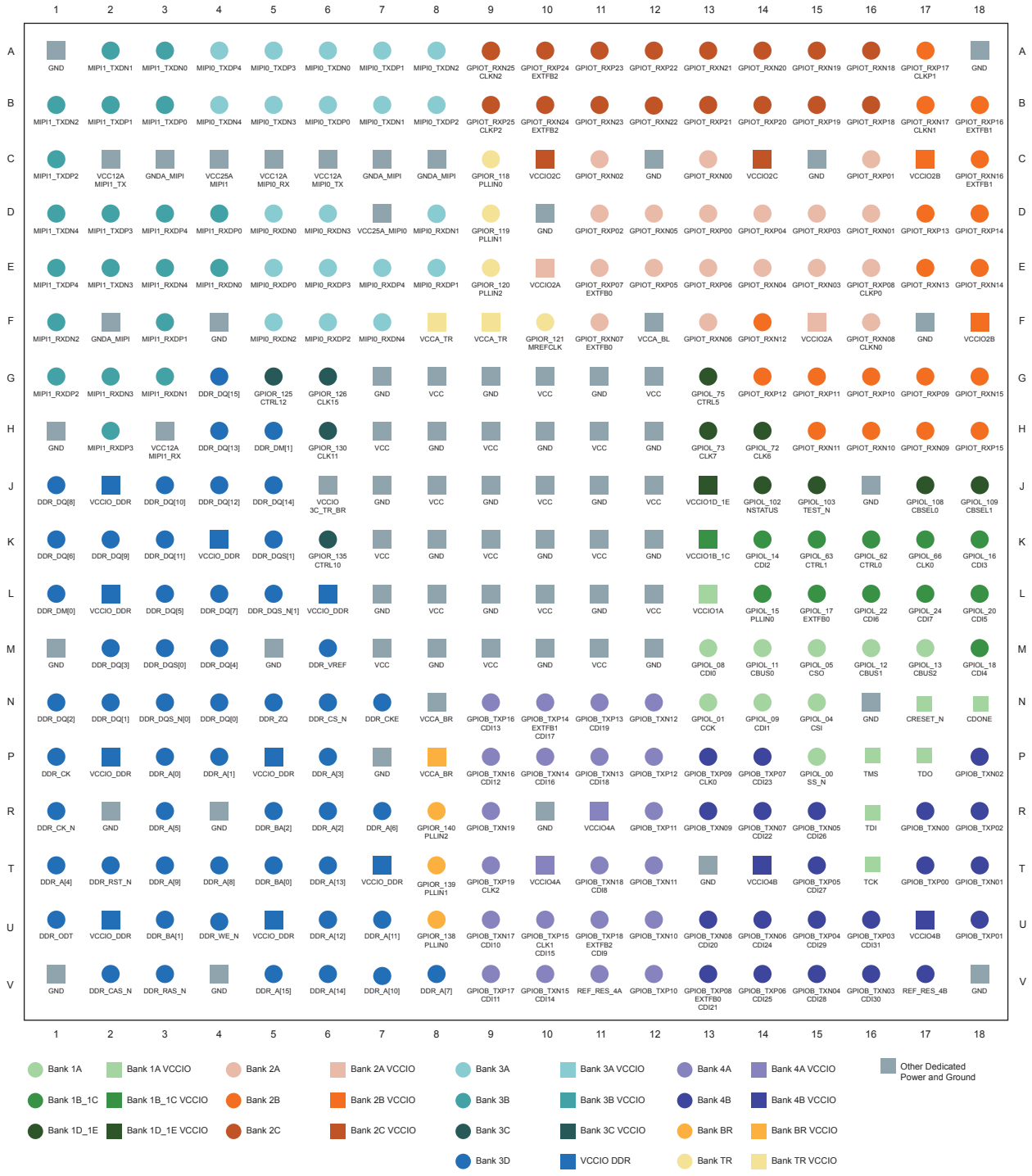


Figure 26: 324-Ball FBGA I/O Bank Diagram (T20 and T35)



T55, T85, and T120 FPGAs: Pinout and I/O Banks

Figure 27: 324-Ball FBGA Pinout Diagram (T55, T85, and T120)

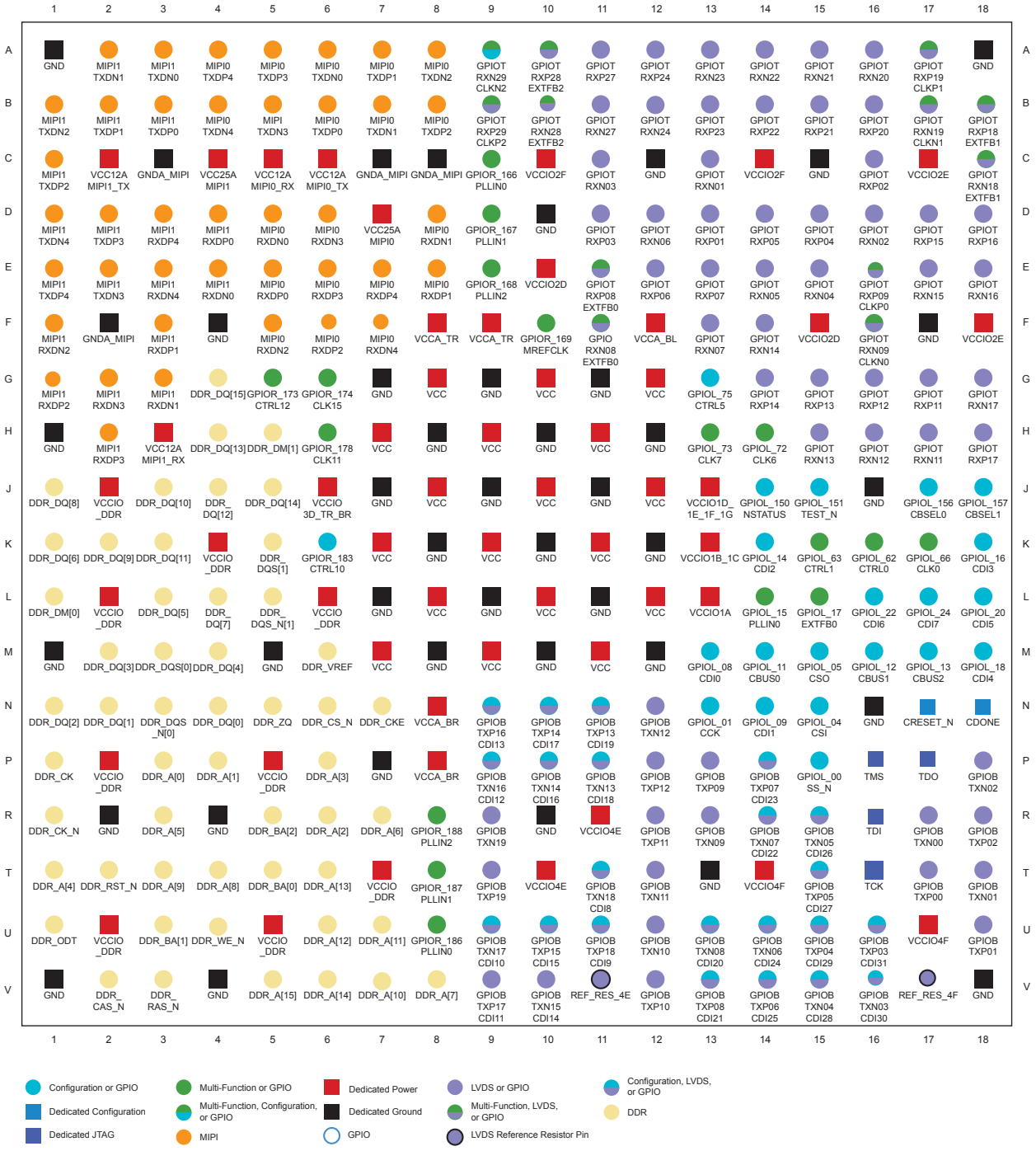
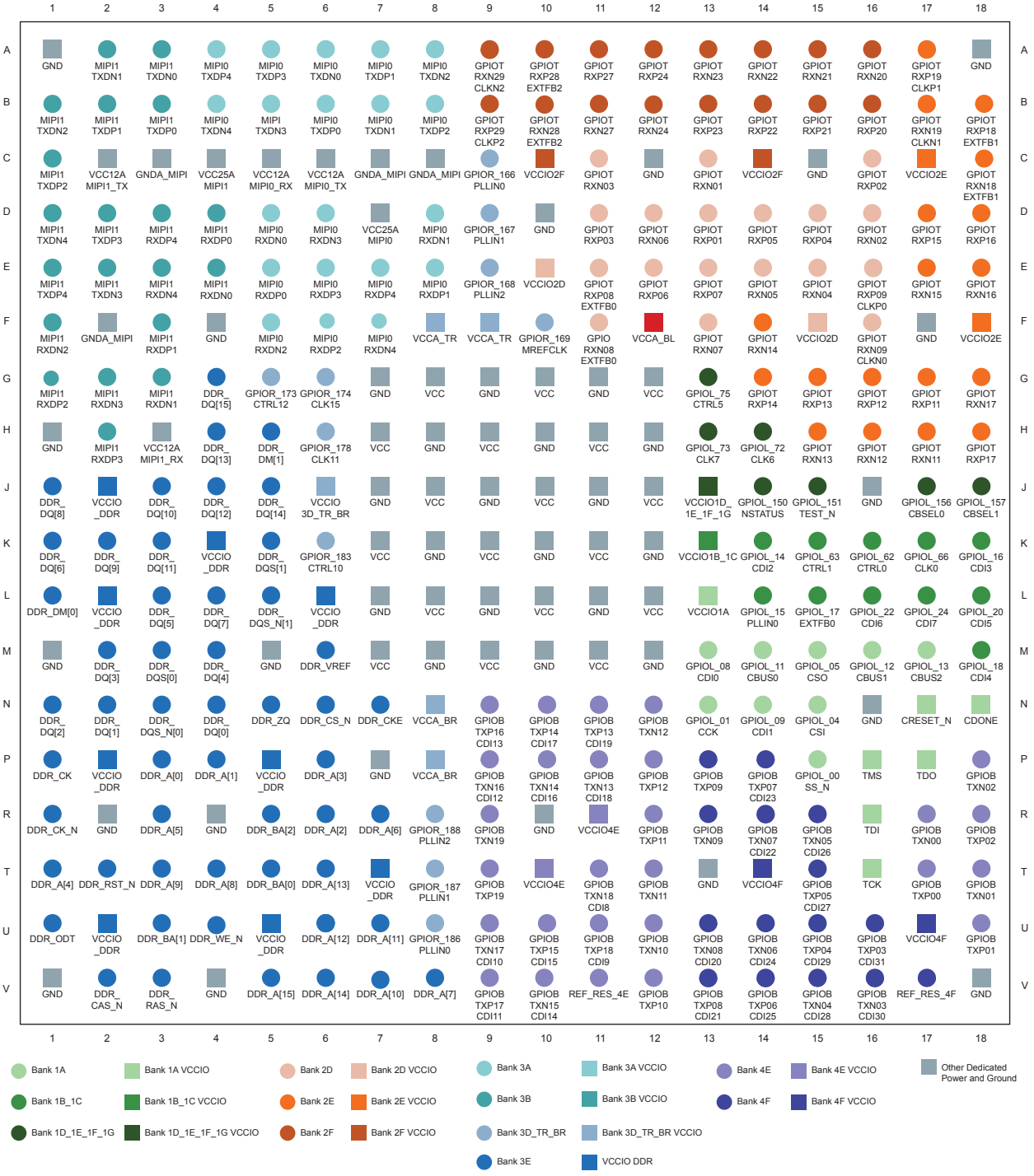


Figure 28: 324-Ball FBGA I/O Bank Diagram (T55, T85, and T120)



Package Outline and Marking (All FPGAs in this Package)

Figure 29: 324-Ball FBGA Package Outline

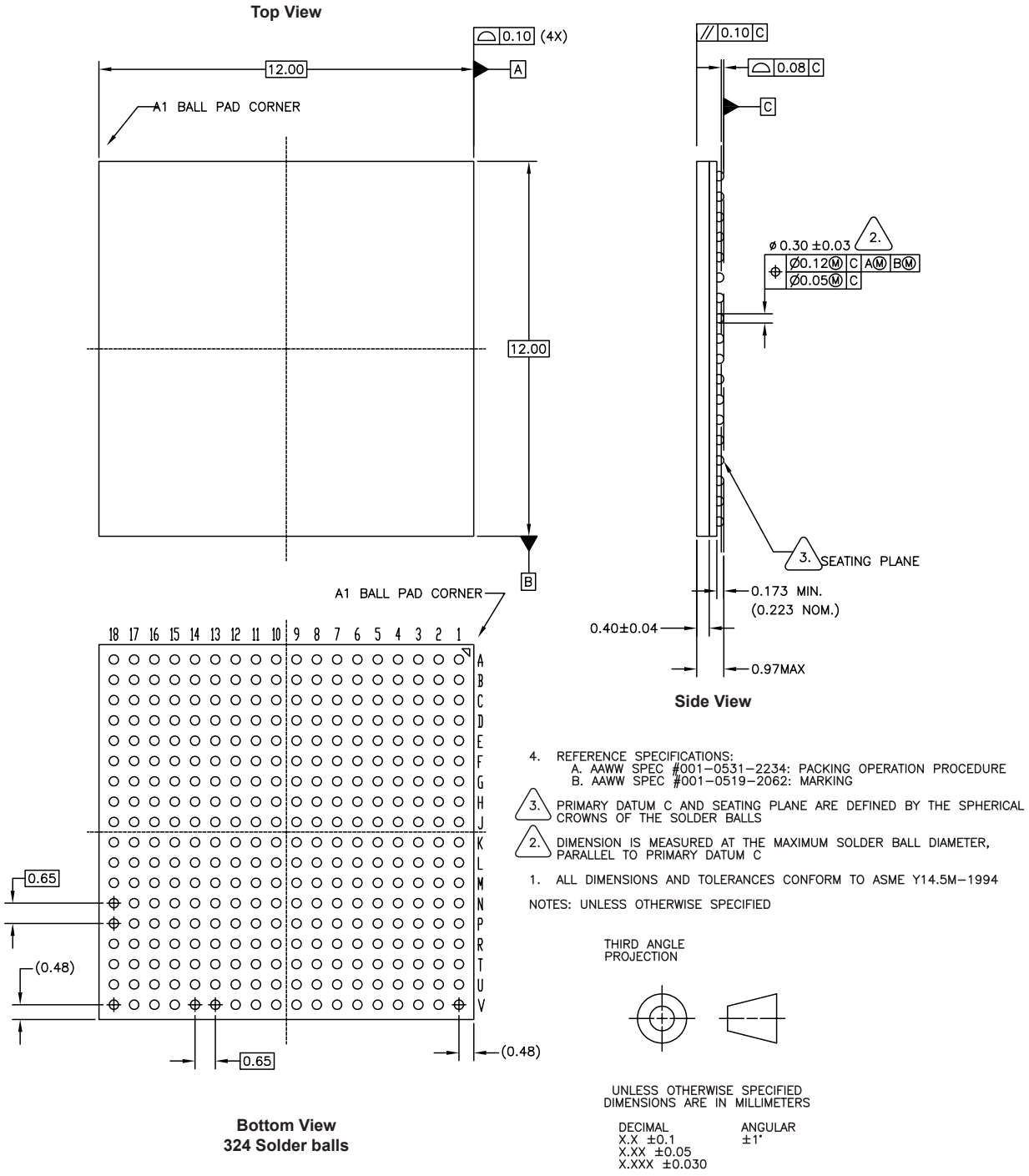
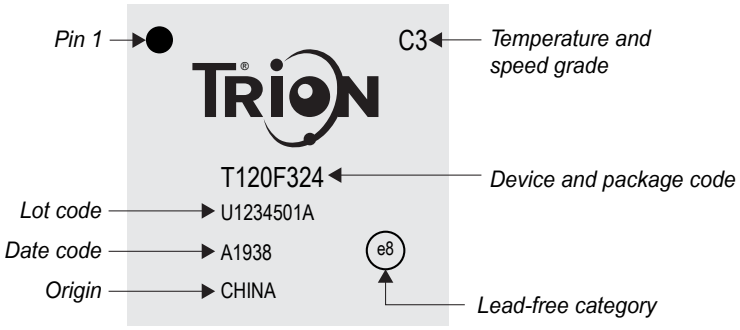


Figure 30: 324-Ball FPGA Package Marking



400-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. This is a flip chip package. FPGAs in this package are pin compatible.

Figure 31: 400-Ball FBGA Pinout Diagram

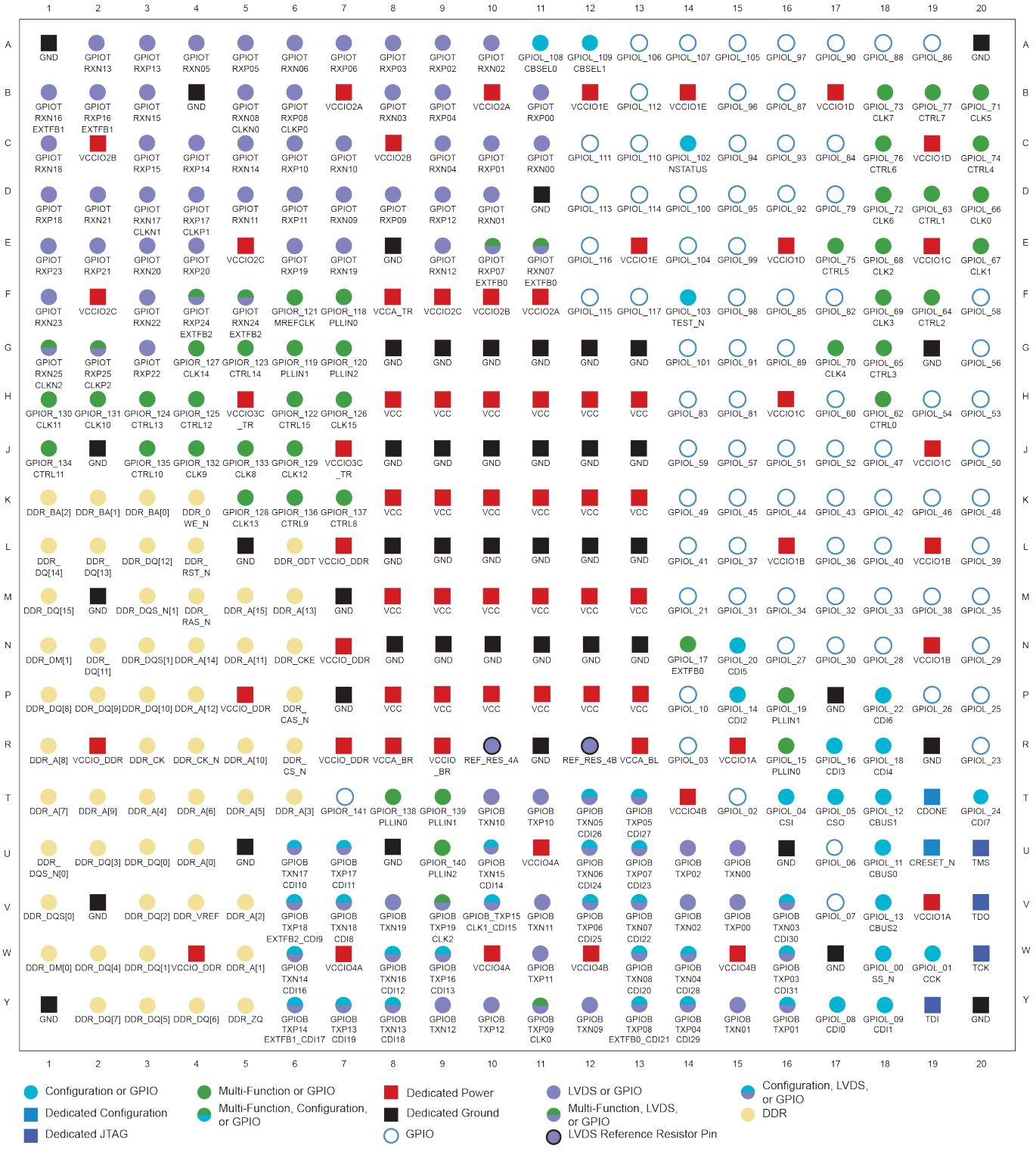


Figure 32: 400-Ball FBGA I/O Bank Diagram

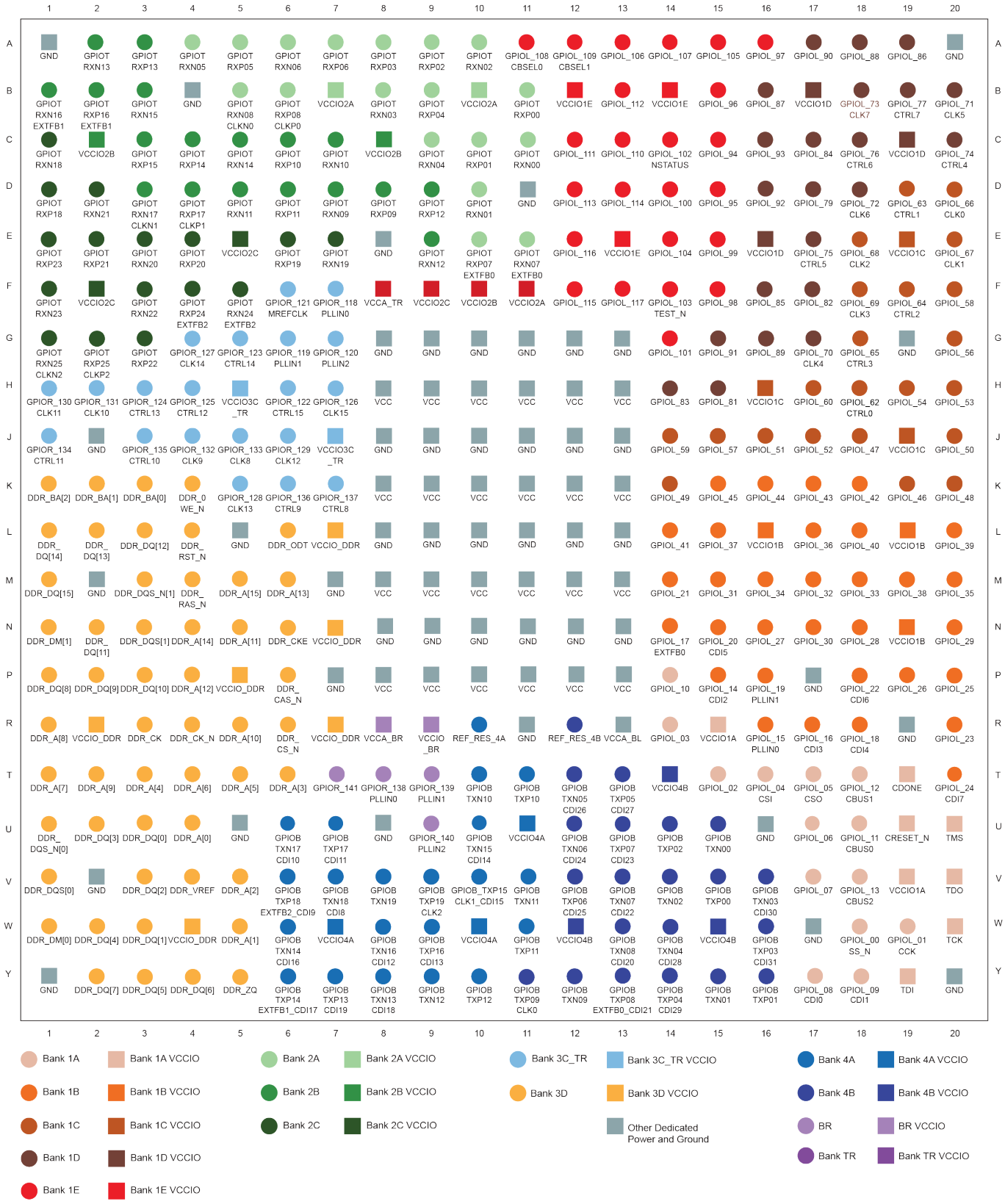


Figure 33: 400-Ball FBGA Package Outline

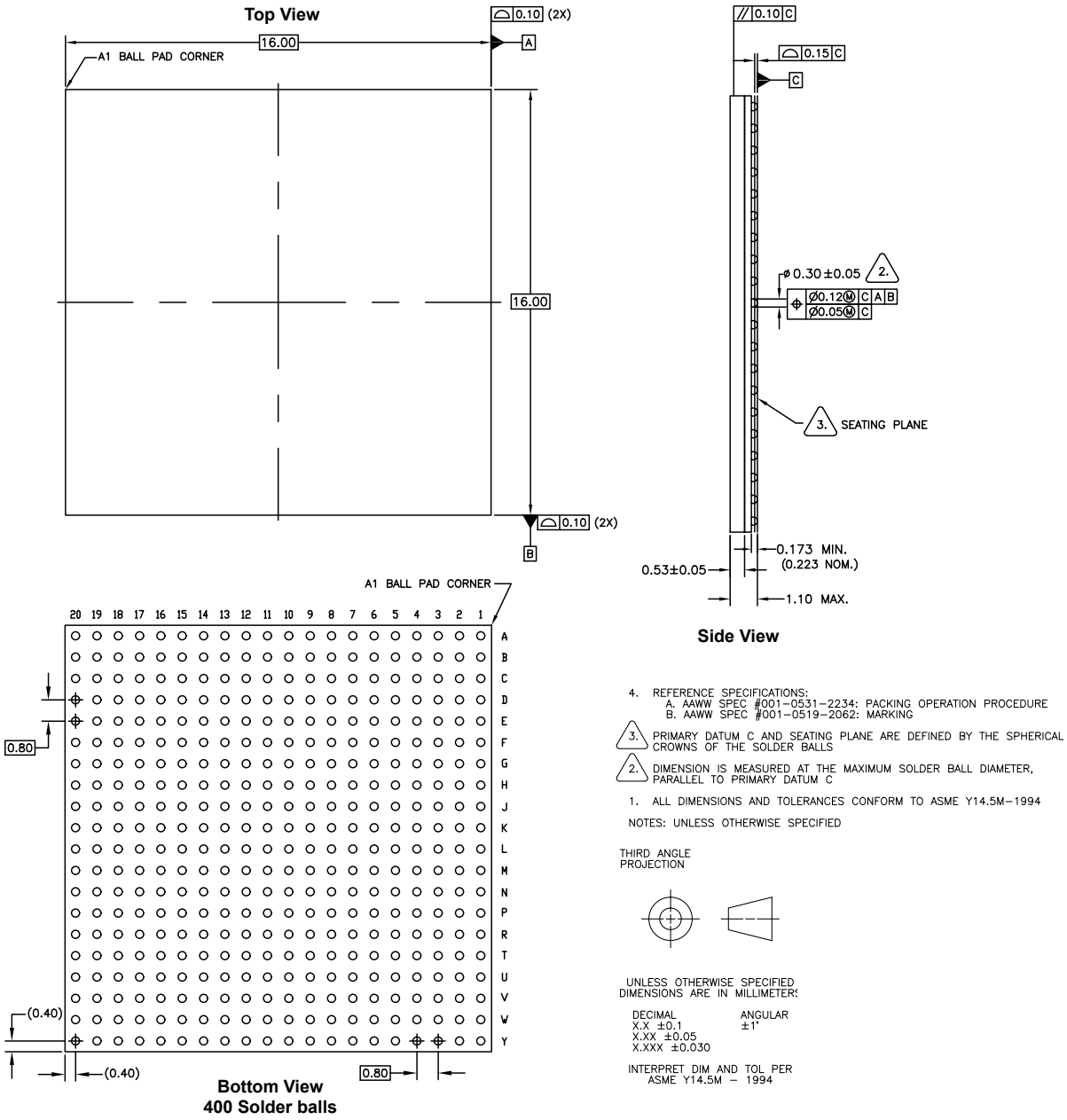
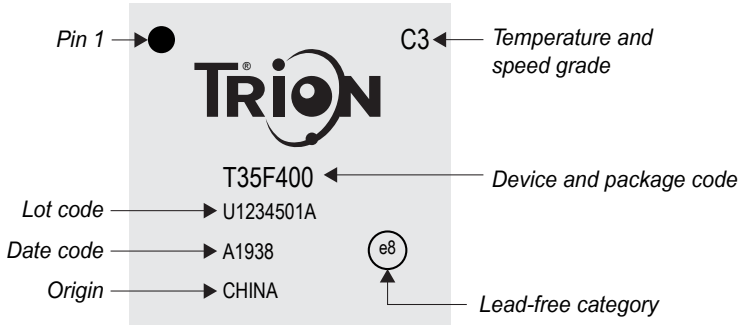


Figure 34: 400-Ball FPGA Package Marking



484-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. FPGAs in this package are pin compatible.

Figure 35: 484-Ball FBGA Pinout Diagram

Figure 36: 484-Ball FBGA I/O Bank Diagram

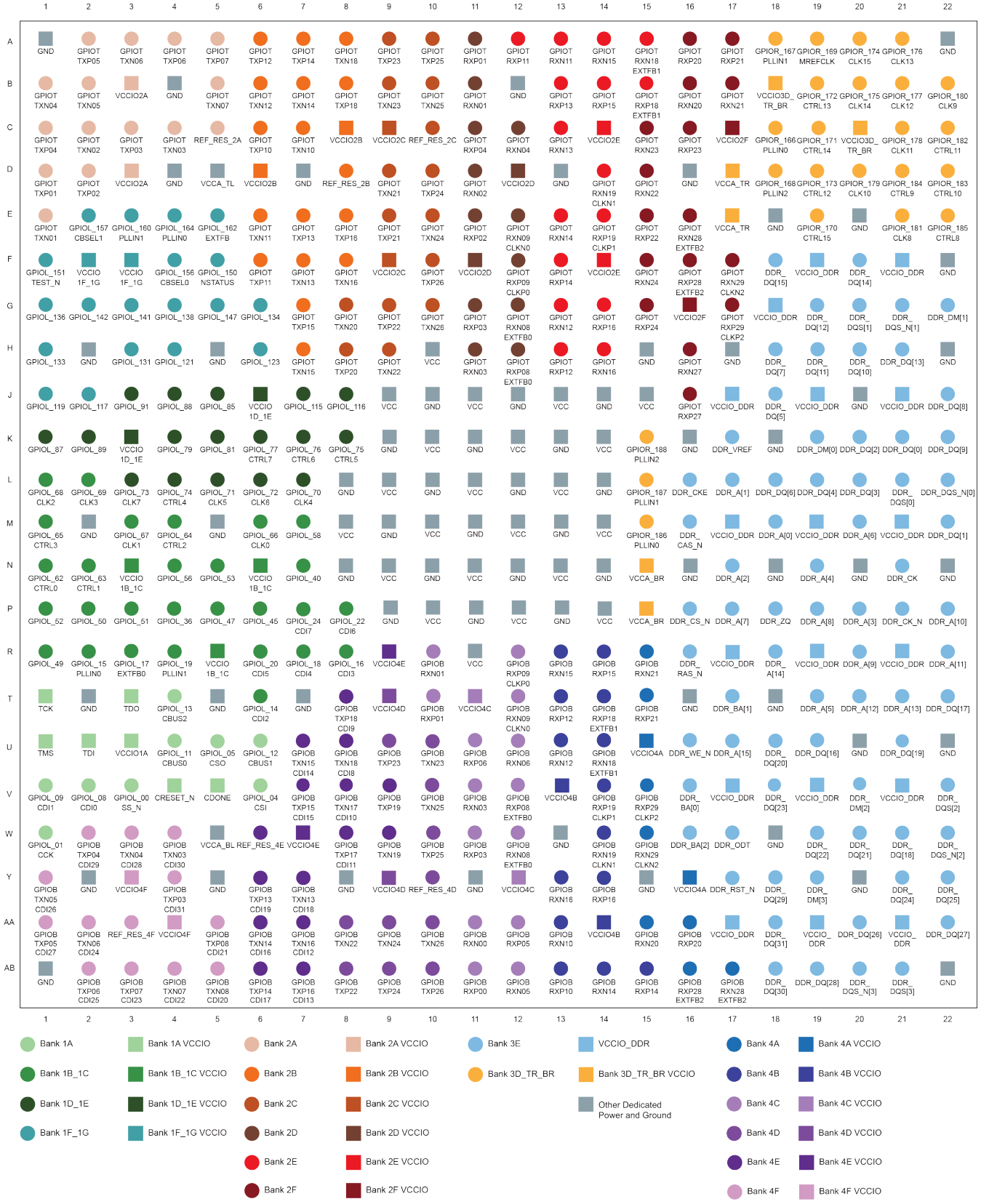


Figure 37: 484-Ball FBGA Package Outline

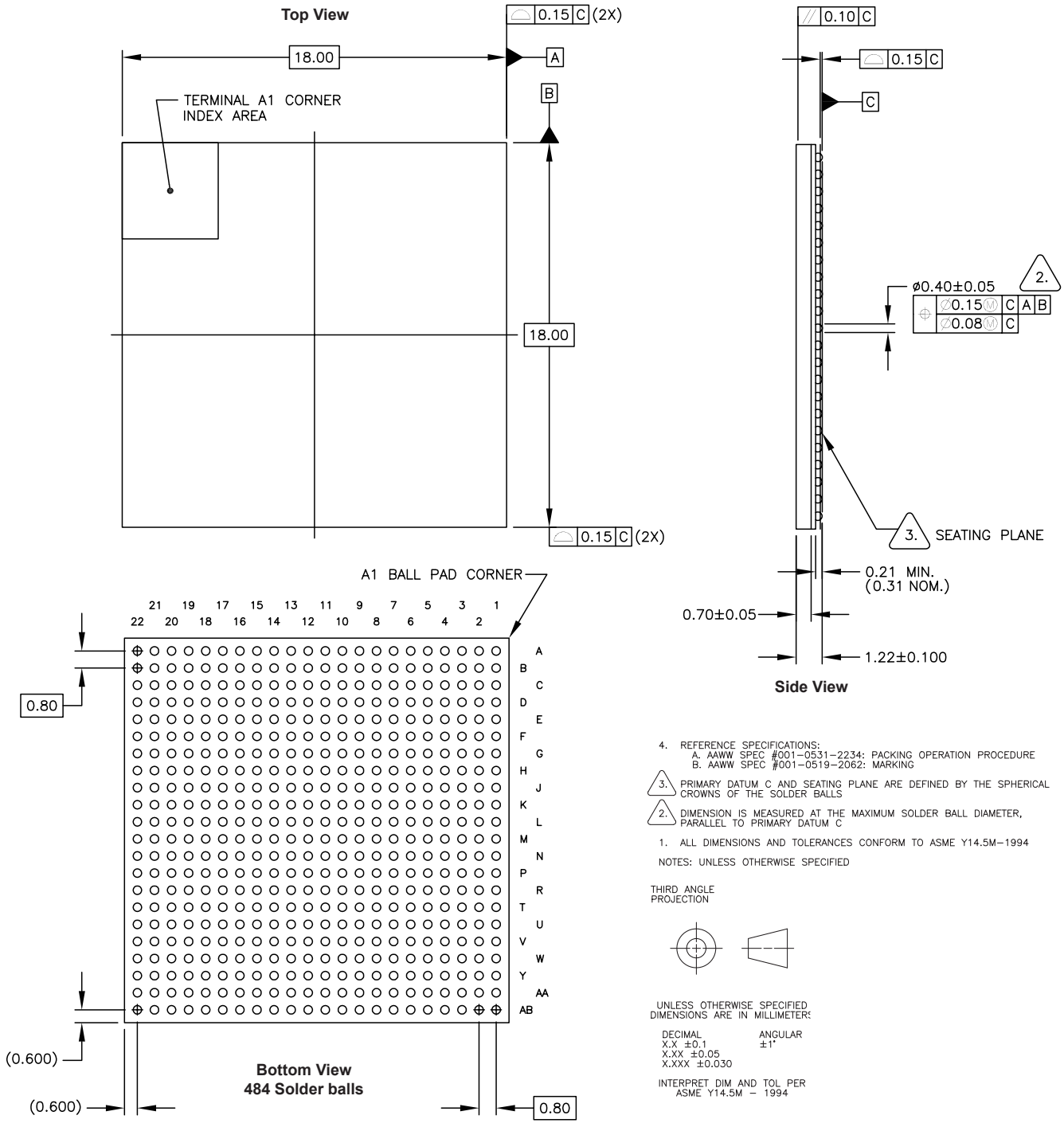
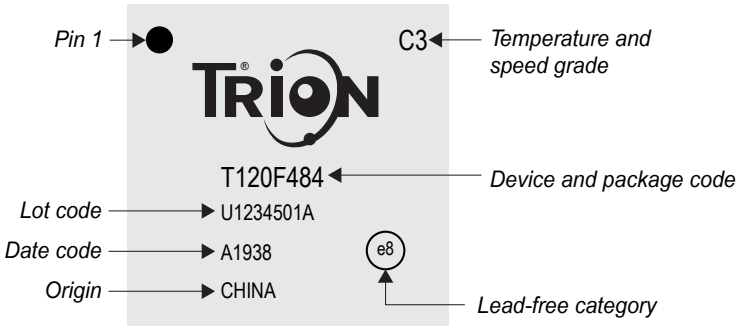


Figure 38: 484-Ball FPGA Package Marking



576-Ball FBGA Package Specifications

The following figures show the pin, I/O bank locations, package top-side marking, and outlines for this package. This is a flip chip package. FPGAs in this package are pin compatible.

Figure 39: 576-Ball FBGA Pinout Diagram

Figure 40: 576-Ball FBGA I/O Bank Diagram

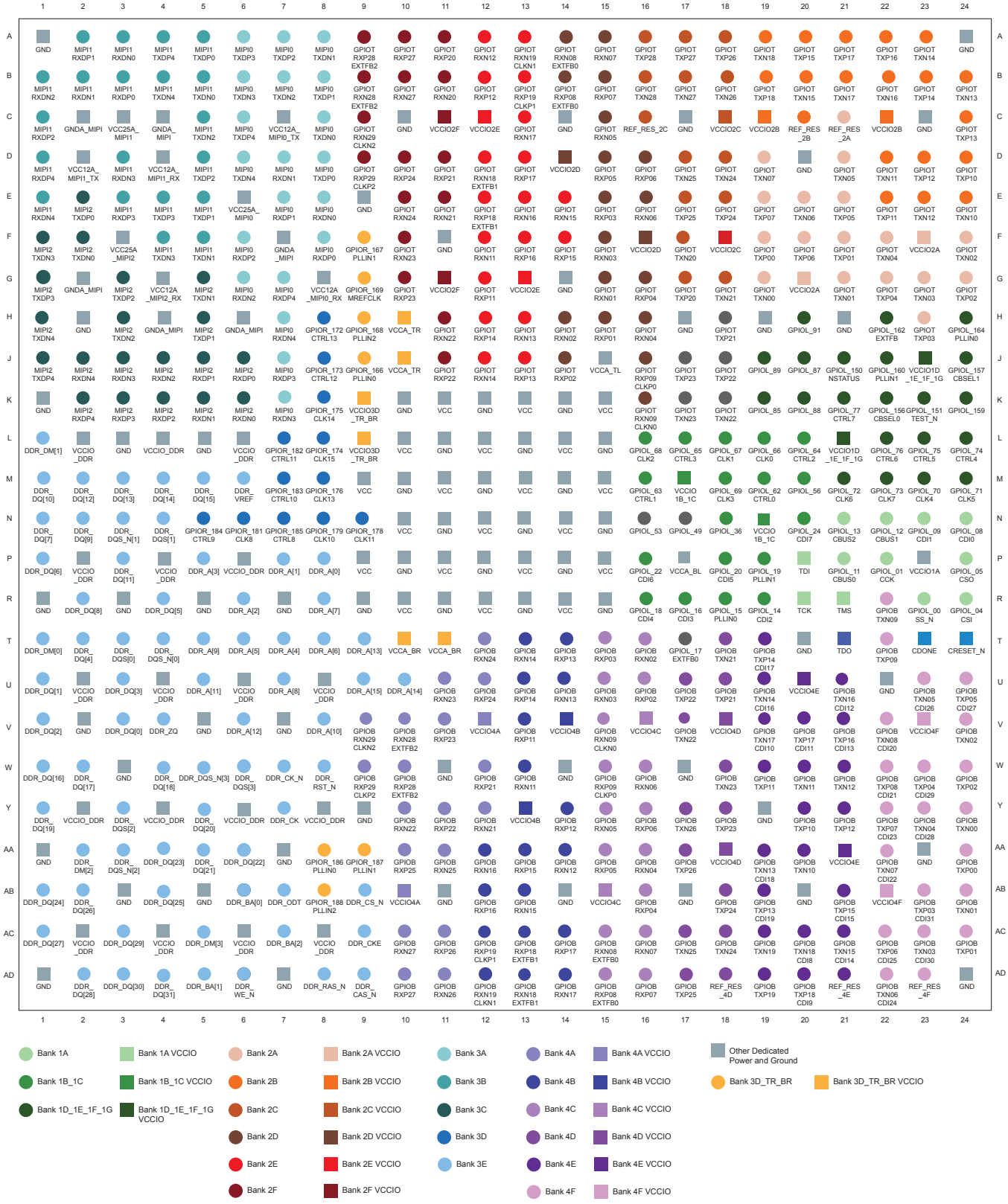


Figure 41: 576-Ball FBGA Package Outline

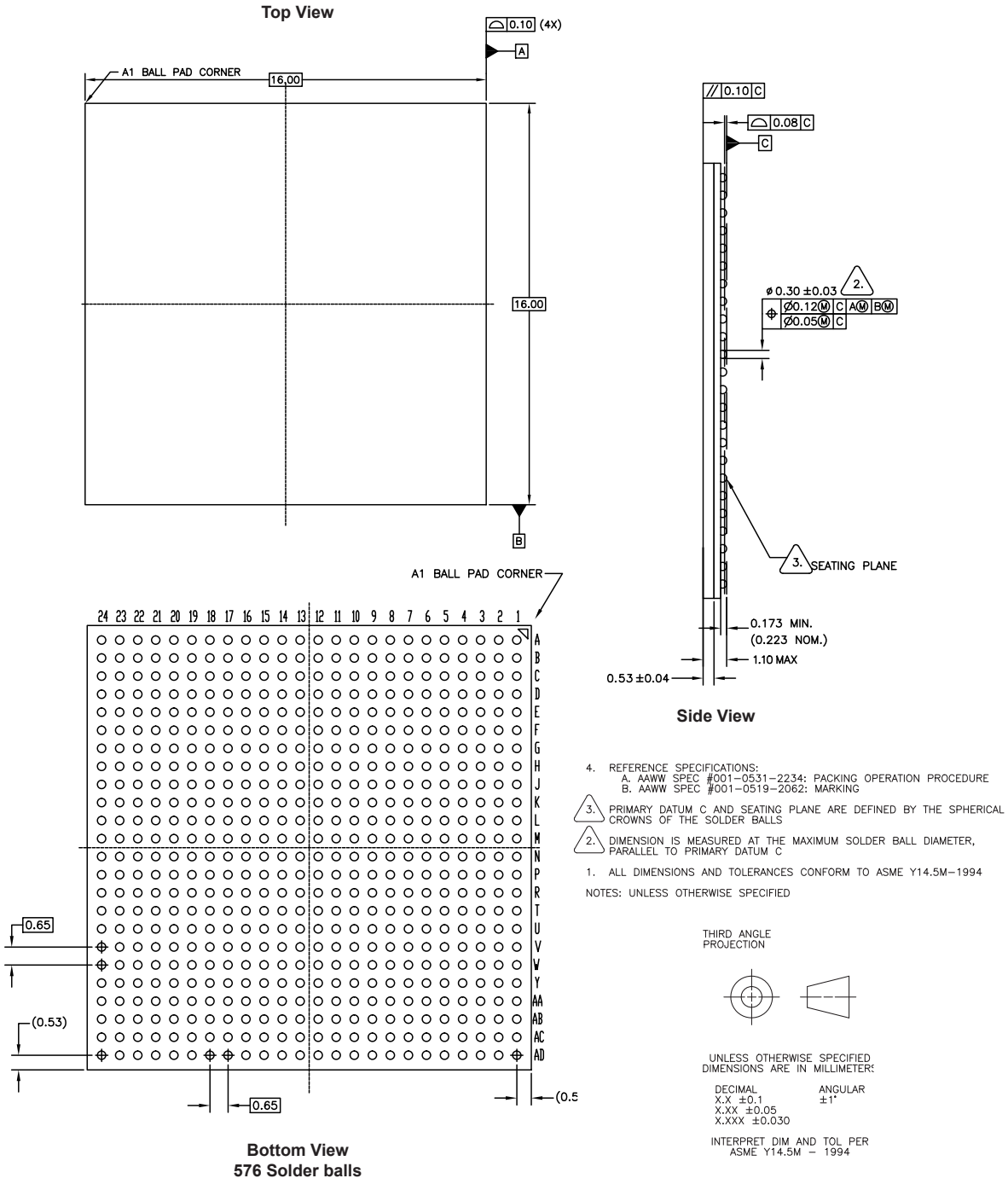
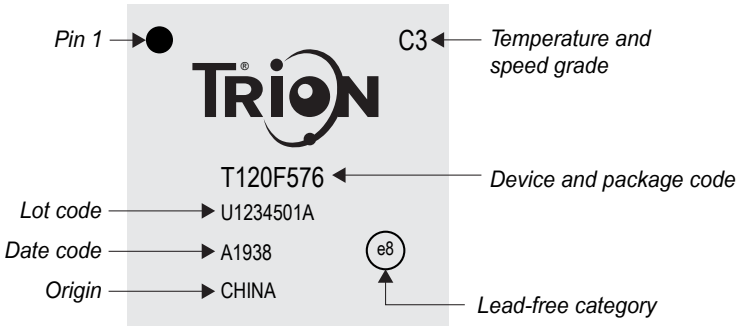


Figure 42: 576-Ball FPGA Package Marking



Solder Reflow Guidelines for Surface-Mount Devices

This section provides general guidelines for solder reflow process for Efinix® surface-mount FPGAs. The data used in this document is based on IPC/JEDEC (Association Connecting Electronics Industries/JEDEC Solid State Technology Association) standards. Each printed circuit board (PCB) has its own profile, which depends upon the reflow equipment used and the board design. You must characterize each PCB to find the profile that is reliable.

Reflow

During solder reflow, follow these guidelines:

- Use caution when profiling to ensure that the maximum temperature difference between components is less than 10 °C.
- For best results, perform forced convection reflow with nitrogen.

Inspection

Follow these inspection guidelines:

- **Pre-reflow**—Use visual inspection to verify solder paste dispense location and quantity.
- **Pick and place**—Use machine vision as necessary to ensure proper component placement.
- **Post reflow**—Use electrical testing to verify solder joint formation.

BGA Reballing

Efinix does not recommend BGA reballing. Reballed BGA packages void the original Efinix® specifications.

Peak Reflow Temperatures

Table 7: Peak Reflow Temperature (Tp) by Package

Package	Number of Leads/Balls	Moisture Sensitivity Level	Peak Reflow Temperature (+0/-5 °C)
FBGA	49	3	260
WLCSP	80	1	260
FBGA	81	3	260
FBGA	169	3	260
FBGA	256	3	260
FBGA	324	3	260
FBGA	400	3	260
FBGA	484	3	260
FBGA	576	3	260
LQFP	144	3	260

Note: These packages are "green" and RoHS compliant.

Reflow Profile for SMT Packages

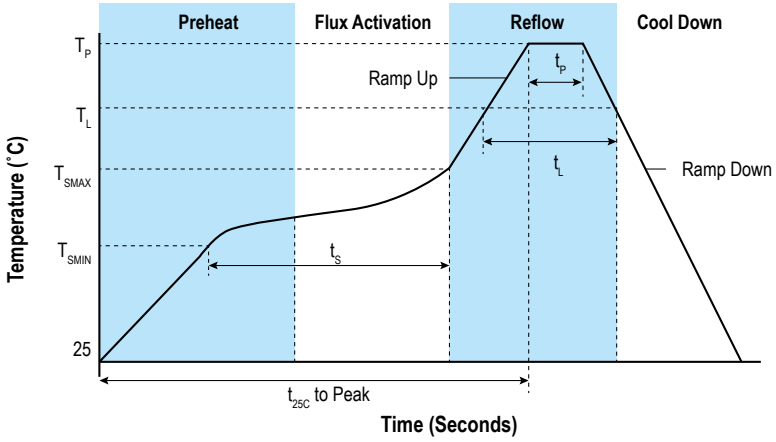
The reflow process usually includes four phases:

1. **Preheat Phase—**The preheat phase brings the assembly from 25 °C to T_S. During this phase, the solvent evaporates from the solder paste. The preheat temperature ramp rate should be less than 2 °C/second to avoid solder balling defects such as solder ball spattering and bridging.
   - **Solder Ball Spattering—**Spattering, the most common solder balling defect, is caused by solvents evaporating explosively. To eliminate spattering, use a slower temperature rise in the preheat phase.
   - **Bridging—**Bridging is usually caused by inaccurate or splashy screen printing, and can often occur with fine pitch components. It can also be caused by solder paste slumping during a rapid temperature rise in the preheat phase.
2. **Flux Activation Phase—**As the temperature rises slowly, it reaches a point at which the flux completely wets the surfaces to be soldered.
3. **Reflow Phase—**The temperature rises to a level sufficient to reflow the solder. The flux wicks surface oxides and contaminants away from the melted solder, resulting in a clean solder joint.
4. **Cool Down Phase—**Ramp down the temperature as fast as possible to control grain size; however, do not exceed 6 °C/second.

Table 8: Peak Reflow Temperature (T_P) Parameters

Parameter	Description	Specification (Lead and Halogen Free Packages)
Ramp up	Average ramp-up rate (T_{SMAX} to T_P)	3 °C/second maximum
T_{SMIN}	Preheat peak minimum temperature	150 °C
T_{SMAX}	Preheat peak maximum temperature	200 °C
t_s	Time between T_{SMIN} and T_{SMAX}	60 - 120 seconds
T_L	Solder melting point	217 °C
t_L	Time maintained above T_L	60 - 150 seconds
t_P	Time within 5 °C of peak temperature	30 seconds
Ramp down	Ramp-down rate	6 °C/second maximum
t_{25C} to T_p	Time from 25 °C to peak temperature	8 minutes maximum

Figure 43: Thermal Reflow Profile



Thermal Resistance

Thermal management is an important consideration when designing your system. Efinix® device data sheets describe the maximum allowable junction temperature so you can assess your system's thermal characteristics. To ensure that the device and package do not exceed the junction temperature requirements, you should always complete a thermal analysis of your specific design.

The data shown in this section is relative and actual values depend on a variety of factors such as die size, paddle size, airflow, power applied, printed circuit board design, proximity of other devices, and user applications. Because of this, Efinix FPGAs do not come with preset thermal solutions.

Table 9: Device/Package Thermal Resistance

Device	Package	Dimensions (mm)	Θ_{JA}/W Still Air	Θ_{JA} (200 LFM)/W	Θ_{JA} (500 LFM)/W	Θ_{JB}/W	Θ_{JC}/W
T4, T8	FBGA49	3 x 3	90.446	84.782	81.797	56.464	46.431
	FBGA81	5 x 5	80.476	75.363	72.797	55.352	32.583
T8, T20	LQFP144	20 x 20	42.82	37.68	35.50	31.12	10.51
T13, T20	FBGA169	9 x 9	38.25	33.33	31.60	23.64	12.39
	FBGA256	13 x 13	24.24	20.52	17.59	31.57	11.85
T20	WLCSP80	4.5 x 3.5	44.94	39.35	37.54	18.91	0.12
T20, T35	FBGA324	12 x 12	20.69	17.89	16.89	10.12	2.59
	FBGA400	16 x 16	18.70	16.95	15.92	12.45	11.10
T55, T85,T120	FBGA324	12 x 12	16.9	14.4	13.5	8.04	2.01
	FBGA484	18 x 18	15.85	12.83	11.99	6.10	4.10
	FBGA576	16 x 16	15.376	13.648	12.568	6.601	1.712

Where:

- Θ_{JA} is the junction-to-ambient thermal resistance

- Θ_{JB} is the junction-to-board thermal resistance
- Θ_{JC} is the junction-to-case thermal resistance

PCB Guidelines for BGA Packages

Solder Mask Defined Guidelines

Efinix provides solder mask defined (SMD) diameter information. Use this data when creating your board layout so that the board pads match the landing pads.

Figure 44: SMD Pad Specification

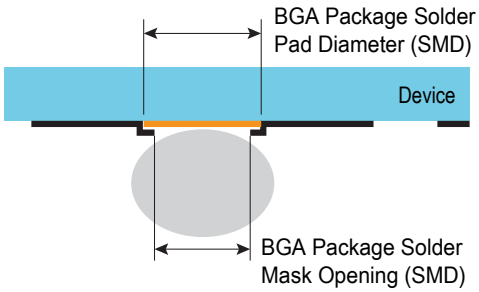


Table 10: PCB Solder Pad Recommendations

Package	Pitch (mm)	BGA Package Solder Mask Opening (mm)	Optimum PCB (SMD) Opening (mm)
FBGA49	0.40	0.275	0.200
WLCSP80	0.4	N/A	0.2
FBGA81	0.50	0.325	0.245
FBGA169	0.65	0.350	0.250
FBGA256	0.80	0.500	0.370
FBGA324 (T20, T35)	0.65	0.335	0.275
FBGA324 (T55, T85, T120)	0.65	0.380	0.275
FBGA400	0.80	0.380	0.275
FBGA484	0.80	0.450	0.350
FBGA576	0.65	0.380	0.275

Non-Solder-Mask Defined Guidelines

Non-solder-mask defined (NSMD) pad designs perform better than solder mask defined pads due to lower stresses in the solder near the top of pad. Additionally, they provide a better "grip" area around the pad edge. For best reliability, the Generic Requirements for Surface Mount Design and Land Pattern Standard (IPC-7351A) recommends a NSMD pad with a diameter that is slightly smaller than the solder ball. This size allows you to use a trace between pads while meeting clearance requirements.

Figure 45: Routing Traces between Pads on the Top Layer

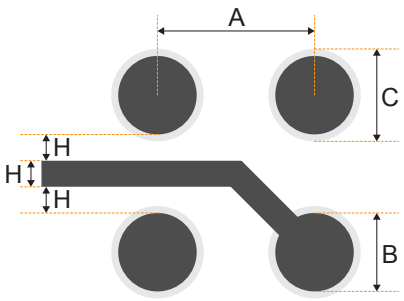


Table 11: Routing Measurements

Measurement	Description	Ball Count							Unit
		F49	F81	W80	F169	F324, F576	F484	F256	
A	Ball pitch.	0.4	0.5	0.4	0.65	0.65	0.8	0.8	mm
	Ball ϕ.	0.25	0.25	0.25	0.25	0.3	0.4	0.46	mm
B	Width of the solder landing pad ϕ.	0.25	0.25	0.25	0.25	0.3	0.4	0.46	mm
C	Width of the solder mask opening ϕ.	0.35	0.35	0.35	0.35	0.4	0.5	0.56	mm
H (min.)	Minimum space between the trace and the landing pad.	(5)	0.08	(5)	0.1	0.1	0.1	0.1	mm

(5) The via is under the pad, no traces between landing pads.

Guidelines for Vias

You use vias to drop routing down to lower layers. This type of via, called an "offset via," is very robust. The solder mask completely covers the via, which prevents short circuits during paste application, allows for paste overprinting, and prevents etch entrapment.

PCB fabricators use a laser drill for these size vias. Confirm that your fabricator can maintain the tight tolerances required to ensure adequate clearances between vias and pads.

Figure 46: Via Dimensions

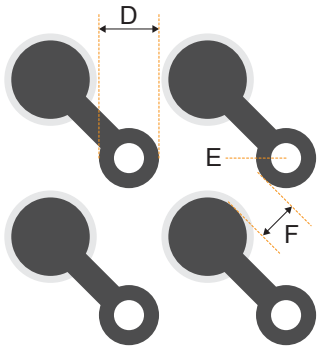


Table 12: Via Measurements

Measurement	Description	Ball Count							Unit
		F49	F81	W80	F169	F324, F576	F484	F256	
D	Via capture pad width.	0.25	0.25	0.25	0.4	0.4	0.5	0.5	mm
E	Finished via ϕ.	0.127[6]	0.127[6]	0.127	0.2	0.2	0.25	0.25	mm
F (min.)	Space between the landing pad and via.	[7]	0.072	[7]	0.122	0.122	0.115	0.085	mm

[6] Laser via.
[7] The via is under the pad, no traces between landing pads.

Routing Guidelines

You can route a trace between two solder pads, which allows you to route the outer two rows of solder pads on the top layer. If you use all of the top-layer routing tracks to route the first and second rows, the inner rows of solder pads must connect to another routing layer with vias for routing outside of the BGA area.

You can use this method to route all of the inner solder pads. Because there is only enough space to route one trace between vias, you need an additional routing layer for every inner row of solder pads after the fourth row.

Figure 47: BGA Trace Routing for Top and Second Layers

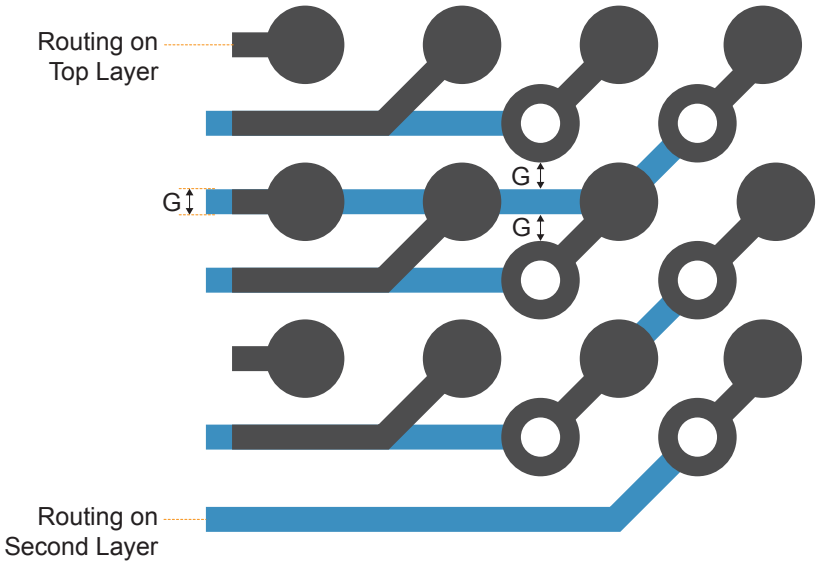


Table 13: Routing Measurements

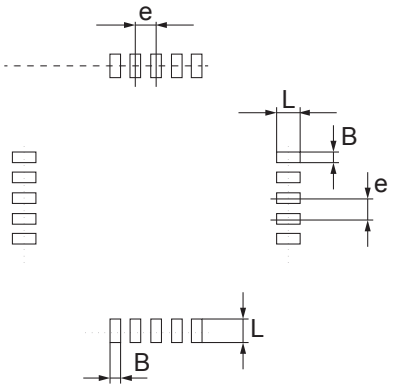
Measurement	Description	Ball Count							Unit
		F49	F81	W80	F169	F324, F576	F484	F256	
G (min.)	Minimum space required between via trace and spacing.	0.1	0.1	0.1	0.1	0.1	0.1	0.1	mm

PCB Guidelines for QFP Packages

PCB Solder Pad (LQFP Packages)

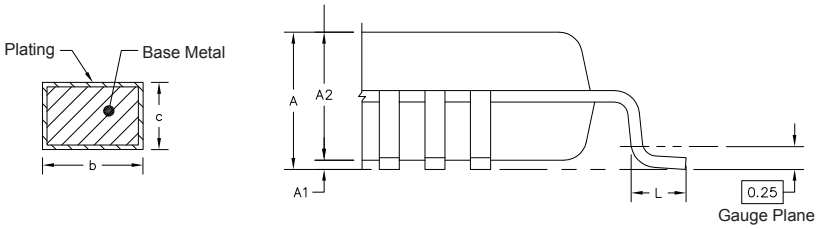
Efinix provides LQFP lead dimension information. Use this data when creating your board layout so that the board pads match the landing pads.

Figure 48: Recommended PCB Landing Pad Guideline



Package	L	B	e
LQFP 144-pin	1.35 mm	0.29 mm	0.5 BSC

Figure 49: LQFP Lead Dimensions



	Symbol	Min	Nom	Max
Total thickness	A	-	-	1.6
Stand-off	A1	0.05	-	0.15
Mold thickness	A2	1.35	1.4	1.45
Lead width	b	0.17	0.22	0.27
L/F thickness	c	0.09	-	0.2
	L	0.45	0.6	0.75

Green Packaging

Efinix FPGAs use packaging solutions that are safer for the environment. These packages are lead (Pb) free and are RoHS compliant. Efinix refers to these products as "green" packaging.

Tape and Reel Packaging

Efinix offers BGA and WLCSP devices in tape and reel packaging.

Table 14: Tape and Reel Packaging

Package	Carrier Width (mm)	Cover Width (mm)	Pitch (mm)	Reel Size (in)	Maximum Quantity per Reel
FBGA49	12	9.3	8	13	5,000
FBGA81	12	9.3	8	13	5,000
WLCSP80	12	9.5	8	13	2,500

Figure 50: Pin 1 Location (BGA49 and BGA81 Packages)

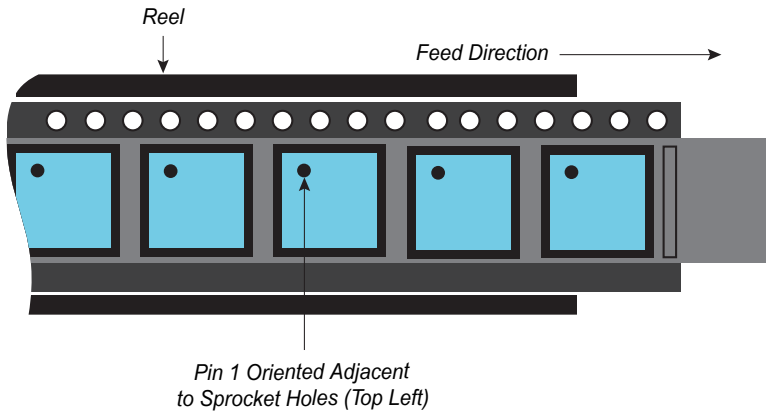
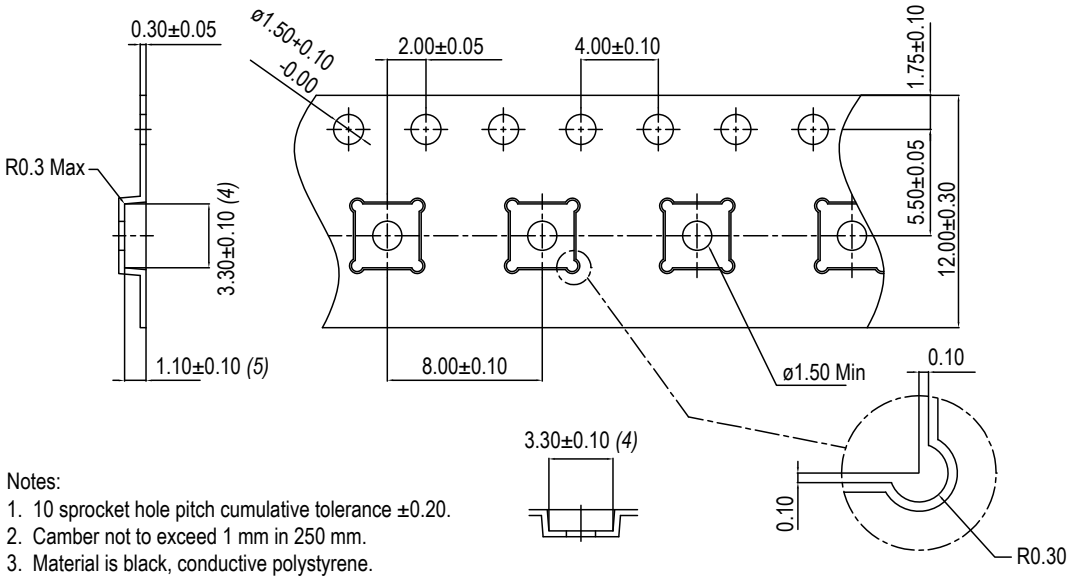


Figure 51: Tape Outline (BGA49 and BGA81 Packages)



Notes:
1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Camber not to exceed 1 mm in 250 mm.
3. Material is black, conductive polystyrene.
4. Measured on a plane 0.3 mm above the bottom of the pocket.
5. Measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
7. Pocket center and pocket hole center must be the same position.

Figure 52: Pin 1 Location (WLCSP80 Packages)

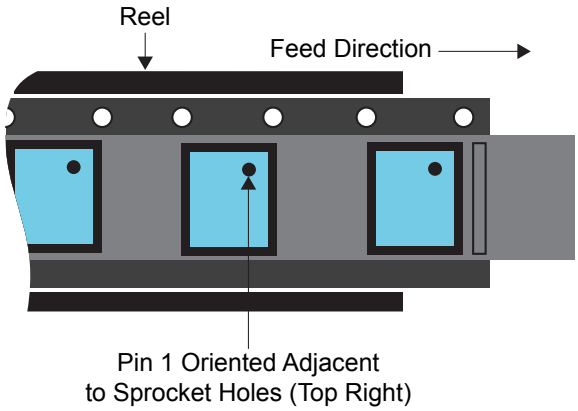
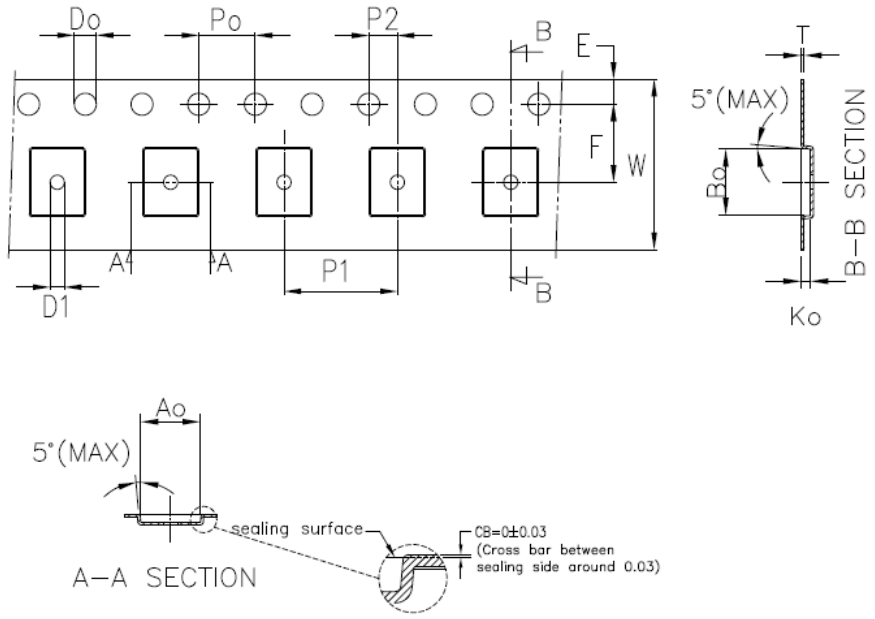


Figure 53: Tape Outline (WLCSP80 Packages)



Unit: mm

Symbol	Ao	Bo	Ko	Po	P1	P2	T
Spec	3.76±0.05	4.66±0.05	0.66±0.05	4.00±0.10	8.00±0.10	2.00±0.05	0.25±0.03
Symbol	E	F	Do	D1	W	10Po	
Spec	1.75±0.10	5.50±0.05	$1.50^{+0.10}_{-0}$	1.00±0.05	12.0±0.30	40.0±0.20	

Notice:

1. 10 Sprocket hole pitch cumulative tolerance is ±0.20mm.
2. Carrier camber shall be not more than 1mm per 250mm.
3. Ao & Bo measured on a place in the middle of corner radii.
4. Ko measured from a place on the inside bottom of the pocket to top surface of carrier.
5. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
6. Surface resistivity ≥ $1.0*10^{5}$ & ≤$1.0*10^{8}$ ohm/sq.

Tray Packaging

Efinix offers BGA and LQFP devices in tray packaging.

Table 15: Tray Packaging

Package	Quantity per Tray	Tray Matrix	Tray Stack	Minimum Quantity per Stack
FBGA256	119	7 x 17	10 + 1	1,190
FBGA169	260	10 x 26	10 + 1	2,600
LQFP144	60	12 x 5	10 + 1	600
FBGA324	168	21 x 8	10 + 1	1,680
FBGA400	84	14 x 6	10 + 1	840
FBGA484	84	14 x 6	10 + 1	840
FBGA576	84	14 x 6	10 + 1	840

Revision History

Table 16: Revision History

Date	Version	Description
April 2022	4.5	Corrected typo for pin A9 in BGA400 package pinout and I/O banks. (DOC-784)
March 2022	4.4	Corrected typos for pins G6 and H15 in BGA400 package pinout and I/O banks. (DOC-756) Noted that BGA324, BGA400, and BGA576 are flip-chip packages. (DOC-756)
March 2022	4.3	Removed thermal pad from LQFP144 Recommended PCB Landing Pad Guideline; this package does not have a thermal pad. (DOC-751)
February 2022	4.2	Fixed typo in LQFP144 package pinout and I/O banks. Pin 31 was incorrectly marked as 34.
February 2022	4.1	Added recommended PCB landing pad guideline for LQFP packages. Corrected color coding for VCCIO4A in the BGA169 I/O bank diagram. (DOC-719) Correct the F (min.) via measurement for the BGA484 and BGA256 packages. (DOC-710)
December 2021	4.0	Fix incorrect pin names for T55/T85/T120 FPGAs in the BGA324 package. (DOC-671)
November 2021	3.9	Fixed incorrect color coding for I/O banks VCCIO_1F_1G in the BGA484 package. (DOC-639)
November 2021	3.8	Corrected symbols for pins L19 and R15 for the 400 BGA package. (DOC-564)
August 2021	3.7	Corrected pin numbering for the WLCSP80 package. (DOC-504) Corrected pitch for F576 in the PCB Solder Pad Recommendations table. (DOC-504) Updated PCB solder pad recommendations (DOC-504) Corrected pin A9 for F256 package pinout. (DOC-493)
July 2021	3.6	Rotated package outline, pinout, and I/O banks figures for the WLCSP80 to make it easier to identify pin 1.
June 2021	3.5	Added thermal resistance data for WLCSP80 package. (DOC-439) Added tape and reel information for WLCSP80. (DOC-439) Added peak reflow temperature for WLCSP80. Corrected typos in BGA256 pinout and fixed mislabeled banks in BGA256 I/O banks. (DOC-452)
December 2020	3.4	Added WLCSP80 package information.
August 2020	3.3	Updated routing measurements and via measurements.
July 2020	3.2	Corrected the BGA169 pinout.
July 2020	3.1	Updated solder ball co-planarity limit from 0.1 to 0.15. Updated 81-ball FPGA package marking.
May 2020	3.0	Added guidelines for traces, pads, and vias for PCB design. Added BGA400 package information. Updated side view BGA576 package dimensions.

Date	Version	Description
February 2020	2.1	Fixed typos in BGA576 pinout and I/O bank diagrams.
January 2020	2.0	Added BGA324, BGA484, and BGA576 package information.
October 2019	1.6	Added LQFP144 package information.
August 2019	1.5	Updated BGA169 and BGA256 package marking.
June 2019	1.4	Added 169 ball FBGA package information.
February 2019	1.3	Added Thermal resistance, solder pad dimensions, and peak reflow data for the 256 BGA package. Aded information on tray packaging. Clarified PLL ground pin in the 81 ball BGA diagram and pinout. Updated 256 ball FBGA package marking.
November 2018	1.2	Added 256 ball FBGA package information.
August 2018	1.1	Updated BGA81 pin figure.
July 2018	1.0	Initial release.

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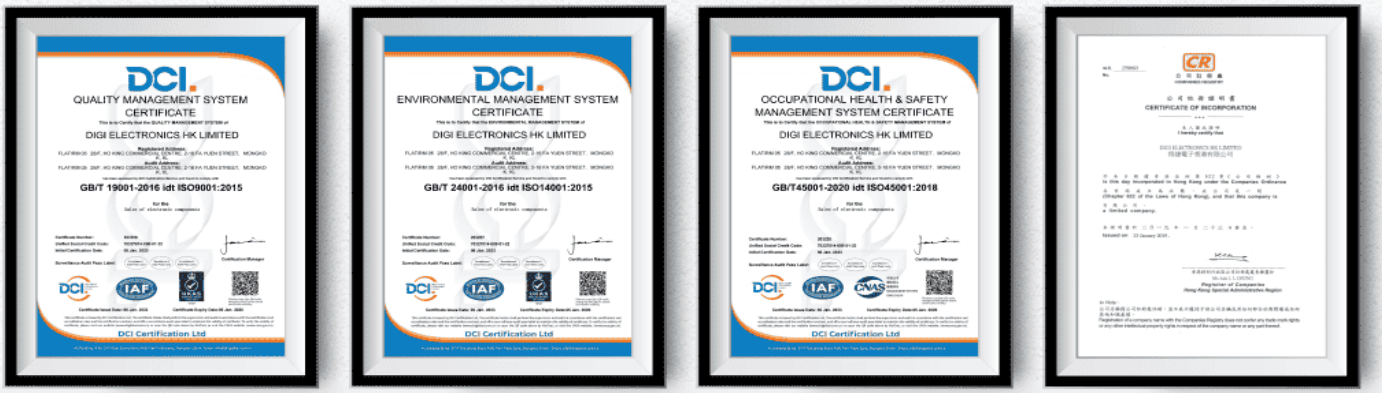

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